An Industrial Internship Report

submitted by

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22BEC0554

in partial fulfillment for the award of the degree of

B.TECH

in

ELECTRONICS AND COMMUNICATIONS ENGINEERING

VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Acknowledgment

I would like to express my sincere gratitude to Maven Silicon for providing me with the opportunity to undertake this VLSI Design internship. I am immensely grateful to my mentors and the entire team for their invaluable guidance, support, and encouragement throughout the project on AHB2APB Bridge Design. Their expertise and insights have been instrumental in enhancing my understanding of VLSI design and digital circuit verification.

I would also like to extend my heartfelt thanks to the faculty and staff at my institution for their continuous support and encouragement, which motivated me to pursue this internship and apply my academic knowledge to real-world applications.

This internship experience has been profoundly enriching, allowing me to develop both technical and professional skills that I am confident will contribute to my future career in Electronics and Communications Engineering.

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CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. **Sanskar Verma (22BEC0554)** *has successfully completed VLSI Design Internship Program from* **05-June-2024** *to* **13-July-2024**

During the internship program with us, he/she worked on **AHB2APB Bridge Design** *project.*

Date: 02/08/2024
Place: Bengaluru

MSUID: MS/V-DI/2024-25/538

MAVEN SILICON SOFTECH PVT. LTD. BANGALORE

SIVAKUMAR P R
FOUNDER & CEO, MAVEN SILICON

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1. Introduction / Background

1.1 Course Objectives

The internship primarily focused on providing a solid foundation in VLSI design, specifically through the creation and verification of an AHB to APB bridge. Detailed objectives included:

1. **Understanding AHB and APB Interfaces**:
    - *Advanced High-performance Bus (AHB)*: Introduced as a high-bandwidth bus used to connect the high-speed components of a system-on-chip (SoC).
    - *Advanced Peripheral Bus (APB)*: A simpler, low-power bus designed to connect slower peripherals.
    - Objective: Learn the characteristics of each bus, their architecture, data transfer mechanisms, and integration within VLSI design.
2. **Mastering Verilog Coding for Digital Design**:
    - Learn to write Verilog code for register-transfer level (RTL) design, including synthesizable and testable code.
    - Objective: Develop efficient, optimized Verilog code and understand key coding constructs like procedural blocks, blocking/non-blocking assignments, and testbench generation.
3. **Digital Circuit Design**:
    - Explore fundamental digital circuit components like adders, multiplexers, flip-flops, and latches. The goal was to develop the ability to design, simulate, and analyse these components.

4. **Skill Development in Synthesis and Verification**:

    - Understand the synthesis process (translating Verilog code to gate-level implementation) and develop testbenches for effective verification.
    - Objective: Familiarize with design tools and verify that each part of the circuit operates correctly within the intended design specifications.

1.2 Expected Outcomes:

The internship set clear goals aimed at equipping interns with valuable skills and knowledge in VLSI design, particularly in areas that align with industry standards and real-world applications.

1. Comprehensive Knowledge of AHB and APB Buses:

    - Interns were expected to gain a deep understanding of the AHB and APB buses, focusing on their roles in high-speed and low-power data transfers, respectively. Through practical application, they explored how these buses are integrated within an SoC and studied the critical role of the AHB to APB bridge in ensuring efficient communication between performance-critical and power-sensitive components.

2. Proficiency in Efficient Verilog Coding:

    - Mastering Verilog coding was a fundamental outcome, with emphasis on developing efficient, synthesizable code for digital circuits. Interns practiced optimizing code for readability, resource efficiency, and performance, learning best practices in modular design and testing. This proficiency in Verilog prepared them for creating complex digital systems within constrained environments.

3. Practical Skills in Simulation, Synthesis, and Debugging:

   - By engaging in hands-on simulation and synthesis, interns built practical skills essential for large-scale VLSI projects. They used simulation tools to verify design functionality and synthesis tools to translate RTL code into gate-level models, gaining insight into the entire design flow. Debugging techniques, such as waveform analysis and logging, were also a focus, equipping interns with problem-solving tools needed in professional environments.

4. Real-World Project Experience:

   - Completing the AHB to APB bridge project offered interns valuable real-world experience. This project required the application of theoretical knowledge in a practical setting, reinforcing the importance of synthesis and verification processes. Through this experience, interns gained a holistic understanding of how to design, implement, and troubleshoot a functional digital component within a larger VLSI system.

This set of outcomes positioned interns to confidently approach complex VLSI design challenges, armed with both technical skills and practical experience.

1.3 Target Domain:

The primary focus of this course was on **VLSI (Very Large-Scale Integration)**, specifically within **Digital Electronics**. VLSI is essential for designing modern digital systems, such as microcontrollers, processors, and communication devices, used across various domains like telecommunications, computing, automotive, and consumer electronics.

1.4 Course Syllabus: AHB to APB Bridge Design and VLSI

Introduction to VLSI & SoC Design

- Topics Covered:
  - Electronic System
  - Smartphone - SoC Architecture
  - SoC Design
  - ASIC vs. FPGA
- Knowledge Check: Introduction to VLSI

2. ASIC Design Flow

- Topics Covered:
  - ASIC Design Flow - Part 1: Specification
  - ASIC Design Flow - Part 2: Architecture to RTL Design
  - ASIC Design Flow - Part 3: Verification to Gate Level Simulation
  - ASIC Design Flow - Part 4: DFT to STA
  - ASIC Design Flow - Part 5: Layout to GDS-II and AMS Flow

3. Verilog HDL

- Sections:
  - Verilog HDL Reference Material (PDF)
  - Introduction to Verilog HDL (Videos)
  - Data Types (Videos)
  - Verilog Operators (Videos)
  - Advanced Verilog for Verification (Videos)
  - Assignments
  - Structured Procedures (Videos)
  - Synthesis Coding Style (Videos)
  - Finite State Machine (Videos)

- Verilog Labs:
    - Lab Instructions and Manual
    - EDA Tools Installation and User Guide
    - Solutions to Labs 1-6

4. Digital Electronics and Logic Design
    - Topics Covered:
        - Number Systems and Codes
        - Logic Circuits
        - Combinational Circuits
        - Sequential Circuits
        - Finite State Machines (FSM)
    - Assignments and Knowledge Checks:
        - Assignments and Online Exercises for each topic

5. AHB to APB Bridge Design
    - Topics Covered:
        - AHB2APB Bridge Design - Project Specification (Documents and Videos)
        - AHB to APB Bridge Design Test (Online Exercise)

1.5 Registration Procedure:

1. Visit the Official Website
    - Navigate to Maven Silicon's official website to explore the VLSI Design Internship program. Detailed information about the course, instructors, and learning objectives can be found there.

2. Program Details

    - Review the course curriculum, duration, and other pertinent details to ensure the program aligns with your learning objectives. This includes understanding the specific topics covered, the practical sessions offered, and the expected outcomes.

3. Contact for Enrollment

    - To enroll in the program, reach out to the administration as directed on the course page. Contact information is provided for inquiries about enrollment, course fees, and any prerequisites.

4. Complete Admission Formalities

    - Follow the provided instructions to complete the admission process. This typically includes filling out an application form, providing identification, and submitting any required documents as part of the registration.

5. Access Course Materials

    - Once registered, you will receive access to the e-learning platform. This includes course materials, schedules, and additional resources required to participate fully in the internship program.

2.Assessments Conducted

2.1 Details about Internal and External Assessments

The *AHB to APB Bridge Design and VLSI* course is structured to provide a balanced mix of theoretical knowledge and hands-on practical experience. Assessments are conducted regularly to reinforce learning, test comprehension, and ensure that practical skills are effectively developed. Below is an overview of the types of assessments conducted throughout the course:

1. **Weekly Theoretical Quizzes**
    - These quizzes evaluate students' understanding of core topics covered each week, including foundational concepts in digital design, Verilog syntax, and VLSI component functionalities. Topics for the quizzes include Number Systems, Verilog Basics, Digital Logic Design, and more.
2. **Practical Assignments**
    - Weekly assignments require students to apply their knowledge to real-world scenarios. For example, after learning Verilog HDL, students may be tasked with writing Verilog code for logic gates, designing a multiplexer, or creating testbenches for digital circuits. These hands-on assignments are essential for building coding and debugging skills.
3. **Verilog Labs**
    - The course includes multiple Verilog labs where students implement complex logic circuits and testbenches using industry-standard tools. Lab assignments focus on combinational and sequential circuits, finite state machines, and synthesizable Verilog code, testing students on both implementation and troubleshooting

skills.

4. **AHB to APB Bridge Project Mid-term Evaluation**

    - This internal assessment occurs halfway through the AHB to APB Bridge project, ensuring students understand interface protocols and are progressing with their project development. Feedback is provided to guide improvements as needed.

5. **Final Project Evaluation**

    - This comprehensive assessment evaluates the completed AHB to APB Bridge project, covering code synthesis, testbench verification, and project documentation. This serves as both an internal and external assessment, assessing students on functionality, code optimization, and overall project quality.

6. **Online Knowledge Checks**

    - Embedded throughout the course, these online exercises reinforce understanding of key concepts in modules such as Introduction to VLSI, FSM, and Verilog HDL. They serve as checkpoints to confirm comprehension before advancing to more complex topics.

3.Digital Diary / Week-by-Week Course Module Descriptions

The course is structured into weekly modules that progressively build students' understanding and skills in VLSI design, Verilog HDL, and AHB to APB bridge design. Below is a week-by-week breakdown:

3.1 Week 1: Introduction to VLSI & SoC Design

- **Topics Covered**: Basics of VLSI, System on Chip (SoC) architecture, and differences between ASIC and FPGA.
- **Activities**: Video lectures on electronic systems, smartphone SoC architecture, and SoC design provide foundational knowledge. An online knowledge check reinforces this introduction.
- **Assessment**: Online quiz testing understanding of introductory VLSI concepts.

3.2 Week 2: ASIC Design Flow

- **Topics Covered**: The stages of ASIC design, from specification to layout.
- **Activities**: Video lectures on ASIC design flow cover stages including specification, architecture, verification, DFT to STA, and layout.
- **Assessment**: Practical assignments require students to summarize each stage of the design flow.

3.3 Week 3: Verilog HDL Basics:

- **Topics Covered**: Introduction to Verilog HDL, data types, operators, and verification techniques.
- **Activities**: Videos, PDFs, and lab manuals guide students in writing Verilog code, covering procedural blocks, data manipulation, and coding styles.
- **Assessment**: Assignments and structured lab exercises on Verilog coding basics.

3.4 Week 4: Digital Electronics and Logic Design

- **Topics Covered**: Number systems, logic circuits, combinational circuits, sequential circuits, and finite state machines (FSM).
- **Activities**: Video lectures on each topic with assignments covering circuit implementation in Verilog. An online exercise on FSM reinforces understanding.
- **Assessment**: Weekly quizzes and lab activities on designing digital circuits.

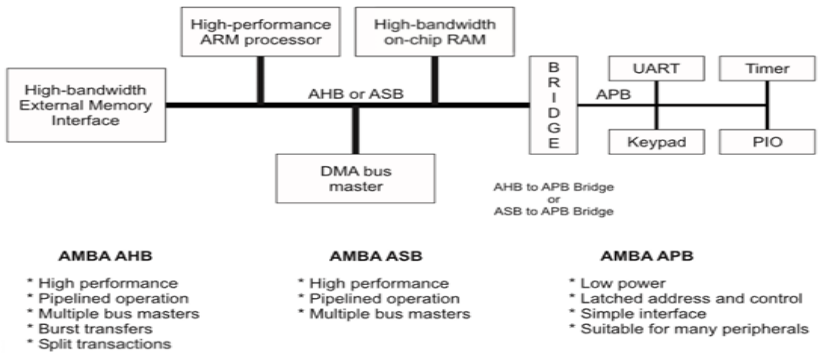
3.5 Week 5: Advanced Verilog and Verification Techniques

- **Topics Covered**: Synthesis coding styles, structured procedures, finite state machines, and testbenches.
- **Activities**: Video lectures and practical assignments on writing efficient, synthesizable Verilog code and creating testbenches.
- **Assessment**: Assignments and labs focused on creating testbenches for digital logic circuits.

3.6 Week 6: Verilog HDL Labs and EDA Tools

- **Topics Covered**: Practical lab sessions on implementing combinational and sequential circuits, FSMs, and more using Verilog.
- **Activities**: Video solutions for each lab and EDA tools user guides. Students complete labs 1-6, implementing digital circuits in Verilog and debugging as needed.
- **Assessment**: Lab solutions are evaluated for correct implementation and testing of digital circuits.

3.7 Week 7: Introduction to AHB to APB Bridge Design



- **Topics Covered**: AMBA protocols, AHB to APB bridge architecture, and signal flow.
- **Activities**: Videos and documentation introduce the project. Students begin work on the AHB to APB bridge design, focusing on protocol and component interactions.
- **Assessment**: Mid-term evaluation of the project to assess understanding and progress.

3.8 Week 8: AHB Master Interface

- **Topics Covered**: In-depth learning on AHB master interface, including RTL coding and signal understanding.
- **Activities**: Video lectures and tasks on writing RTL code for the master interface, with emphasis on testbench development.
- **Assessment**: Assignment to develop and verify the master interface using Verilog.

3.9 Week 9: AHB Slave Interface and APB Controller

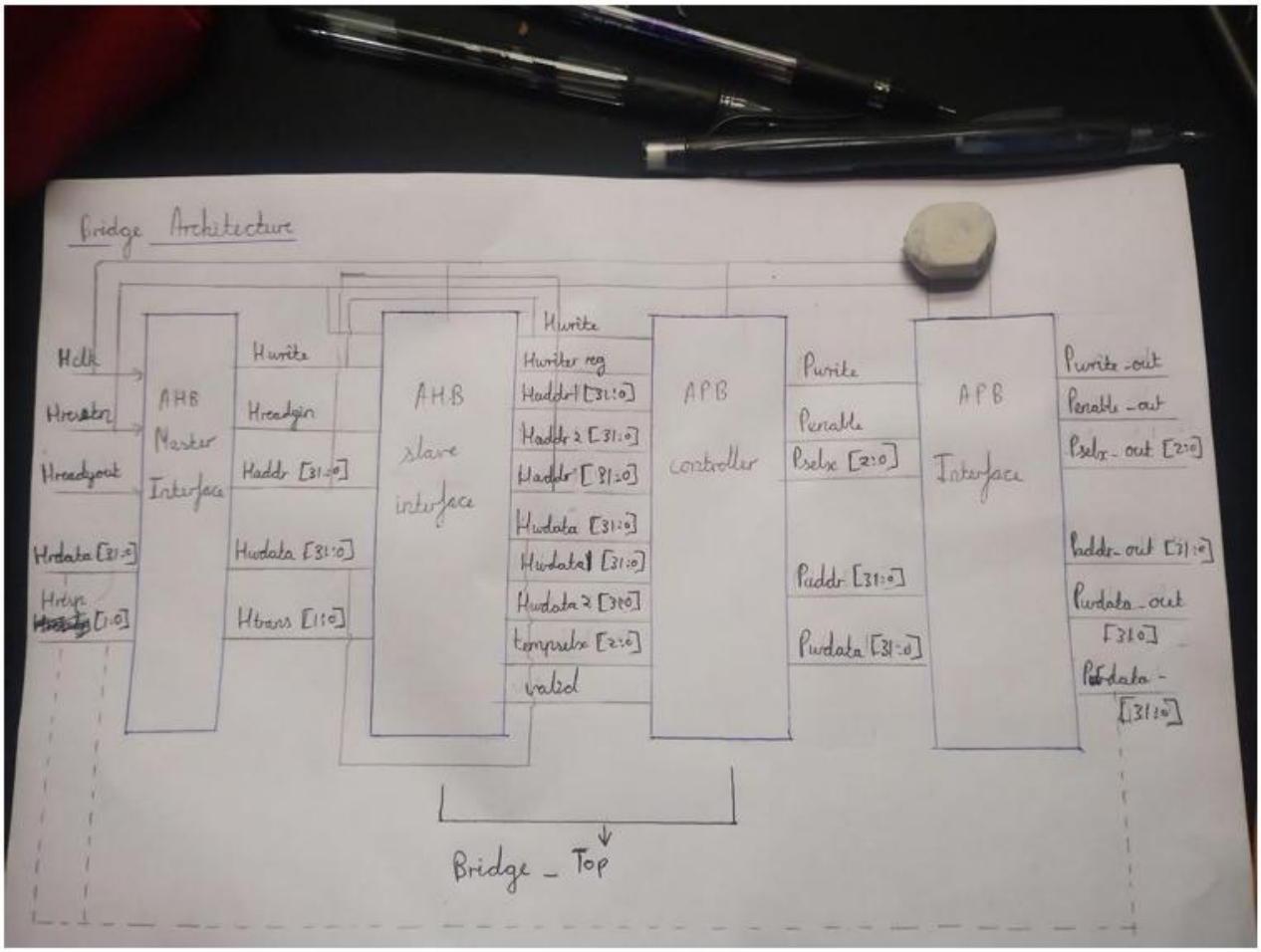
- **Topics Covered**: AHB slave interface and APB controller implementation.
- **Activities**: Video lectures and lab work on coding the slave interface and APB controller in Verilog, along with testbench verification.
- **Assessment**: Evaluation based on successful coding and testing of the slave interface.

3.10 Week 10: APB Interface and Finalizing the AHB to APB Bridge Project

- **Topics Covered**: Completion of APB interface and integration of all bridge components.
- **Activities**: Final coding and verification of the AHB to APB bridge, including creating a comprehensive testbench to verify the entire system.
- **Assessment**: Final project evaluation based on functionality, code efficiency, and testbench verification.

3.11 Weeks 11-12: Project Review and Preparation for Final Test

- **Activities**: Doubt-solving sessions, group discussions, and final project review.
- **Assessment**: Final project submission, group discussions, and test preparation assessments to reinforce concepts.



4 Software and Tools Observed

4.1 Software Used

During the *AHB to APB Bridge Design* course, Quartus Prime and Model-Sim were the primary tools utilized for designing, simulating, and verifying digital circuits and systems. These industry-standard tools provided students with practical experience in digital design, synthesis, and simulation, essential skills in VLSI design.

1. Quartus Prime

- Quartus Prime is an integrated design tool that supports FPGA design, including synthesis, analysis, and compilation of digital logic. In this course, students used Quartus Prime to write Verilog code, synthesize RTL (Register Transfer Level) designs, and verify gate-level implementations.

- Key features in Quartus Prime, such as logic synthesis, timing analysis, and RTL viewer, enabled students to observe logical structures and optimize code for synthesis. The tool's RTL-to-gate-level conversion ensured that Verilog code was accurately transformed into a gate-level netlist that adhered to timing and area constraints.

2. Model-Sim

- Model-Sim was employed as the primary simulation environment to verify Verilog designs. Its powerful simulation and debugging capabilities allowed students to create testbenches, visualize waveforms, and check circuit timing and functionality.

- Testbench development in Model-Sim enabled students to simulate data transfers, verify signal interactions, and ensure that the AHB and APB protocols behaved as expected. By examining

waveforms and signal transitions, students gained a deep understanding of data flow and signal timing.

4.2 Key Signals in AHB and APB Protocols

The AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) protocols within the AMBA (Advanced Microcontroller Bus Architecture) specification play distinct roles in data flow, direction, and timing. Understanding these signals was essential for implementing the AHB to APB bridge.

- ### AHB Signals

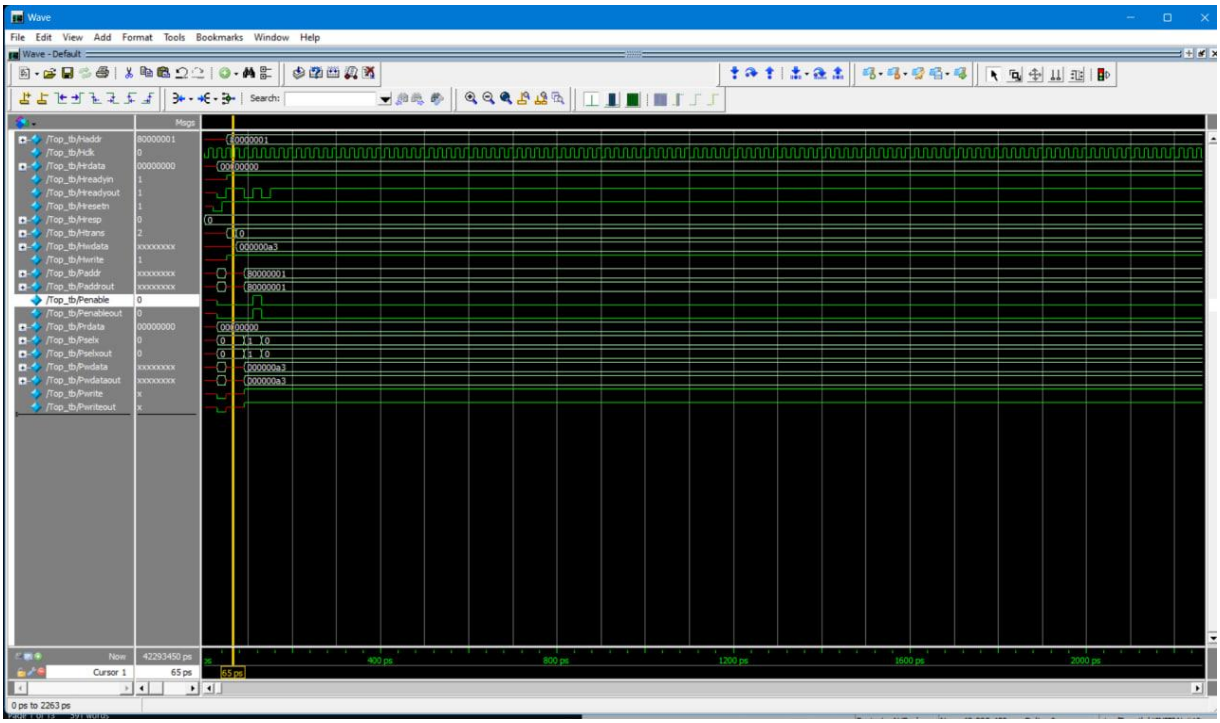
    - *HCLK*: Main clock signal that times all bus transfers, with transitions based on the rising edge of HCLK.
    - *HRESETn*: Active-low reset signal for system and bus resets, ensuring consistency across the system.
    - *HADDR[31:0]*: 32-bit address bus specifying the target address of each transaction.
    - *HTRANS[1:0]*: Indicates transfer type, including NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY, for controlled transaction flow.
    - *HWRITE*: Signals write (HIGH) or read (LOW) operations.
    - *HSIZE[2:0]*: Determines data transfer size, supporting up to 1024-bit data handling.
    - *HREADY*: Indicates transfer completion; HIGH signifies completion, and LOW extends transfer duration.
    - *HRESP[1:0]*: Provides transfer response status, like OKAY or ERROR, to indicate transaction health.

- ### APB Signals

    - *PCLK*: Governs all transfer timing, with transitions on the rising edge of PCLK.

- *PRESETn*: Active-low reset synchronized with the system reset for cohesive control.
- *PADDR[31:0]*: 32-bit address bus driven by the peripheral bus bridge for specific peripherals.
- *PENABLE*: Manages timing, marking the second cycle of each APB transfer.
- *PWRITE*: Sets transfer direction, HIGH for write, LOW for read.
- *PRDATA[31:0]* and *PWDATA[31:0]*: Buses for data transfer during read and write cycle.

SINGLE WRITE:



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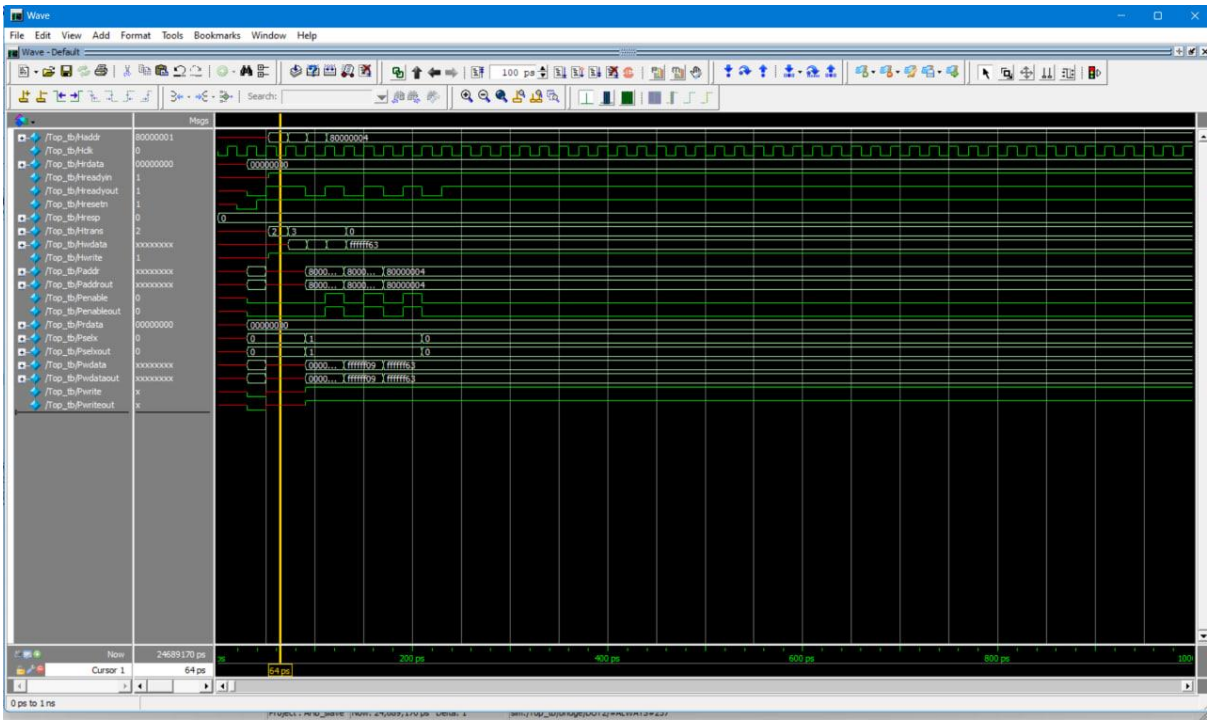
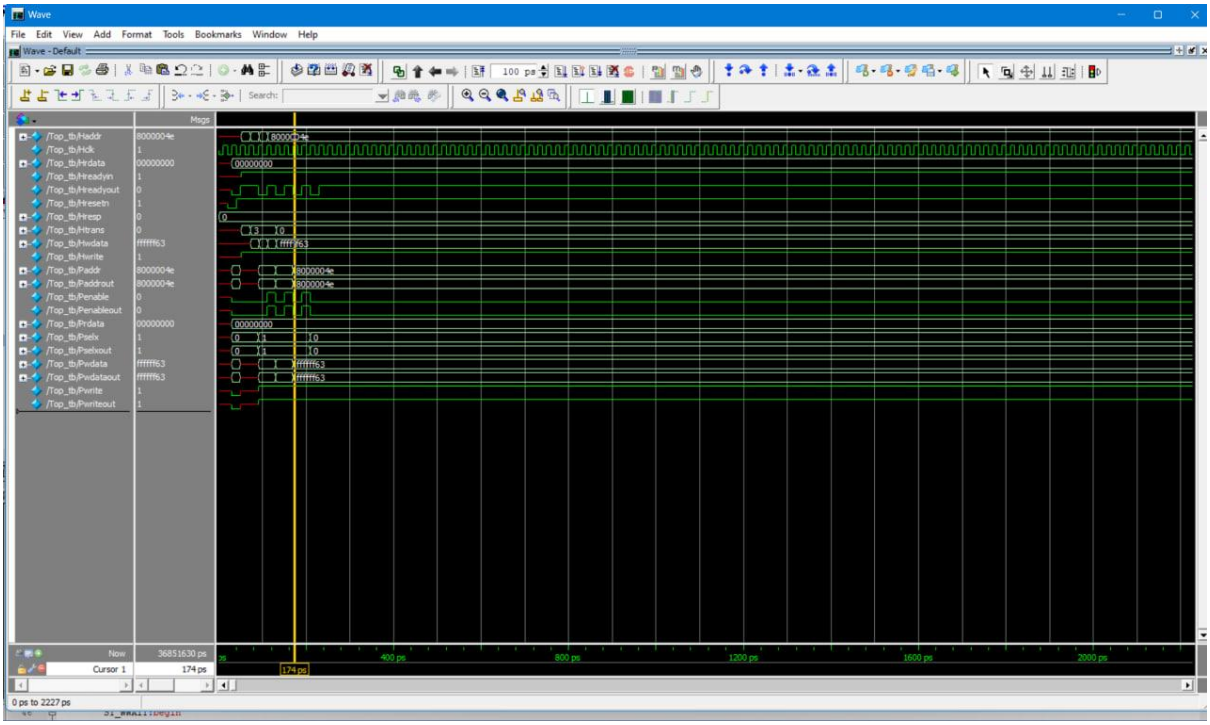
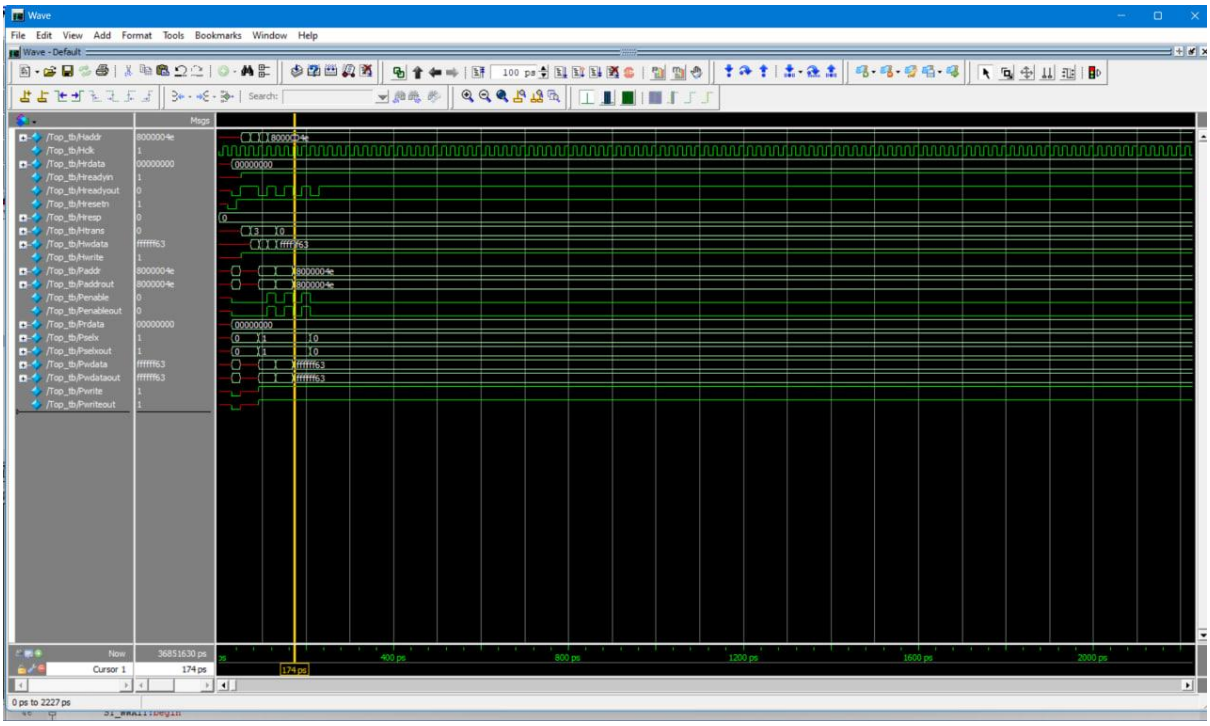


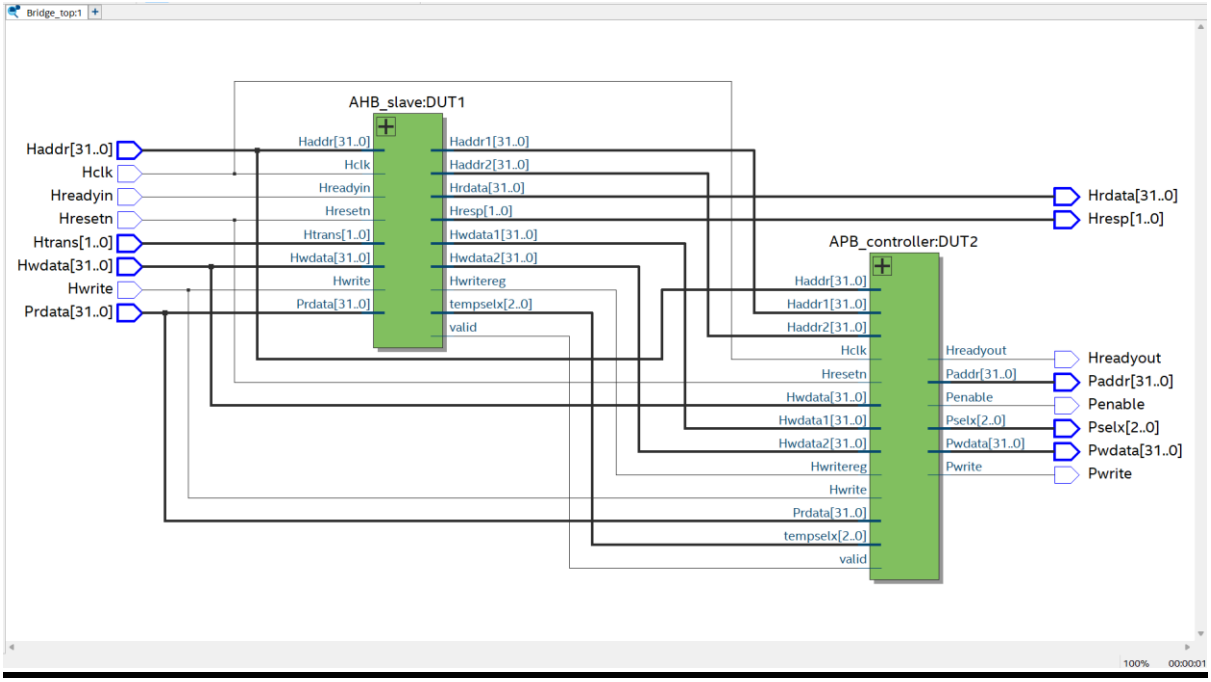
WRAP WRITE



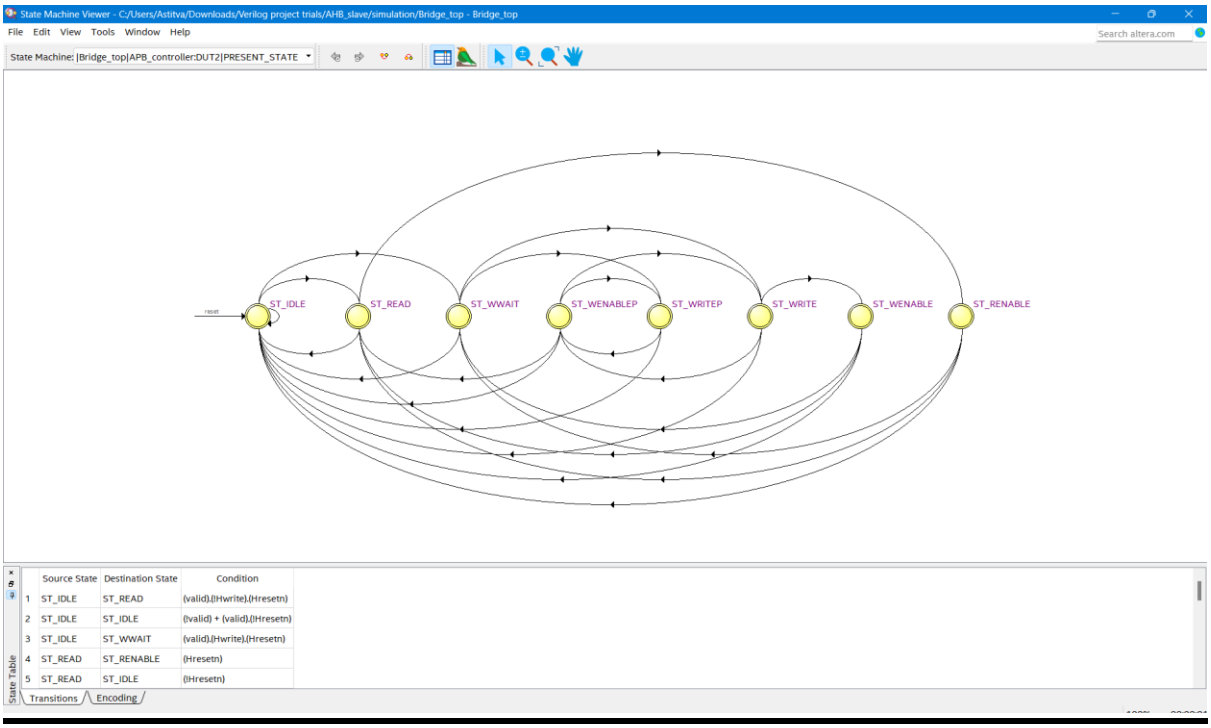
SINGLE READ



SYNTHESIS



STATE DIAGRAM



4.3 Hardware Observed (Simulated)

While the course primarily used simulation environments, several hardware concepts were observed to understand their digital representations in the AHB to APB bridge design. Simulated components helped students learn how actual hardware would behave within VLSI systems.

1. ## AHB and APB Interface Modules

   - The bridge connected high-speed AHB interfaces with lower-power APB peripherals. Students observed data movement between AHB and APB modules, mimicking real hardware connections within an SoC.

2. ## Digital Logic Components

- Core components like adders, multiplexers, latches, and flip-flops were implemented in Verilog and simulated in Model-Sim. These components are fundamental in complex digital systems, and understanding their interactions was critical for bridge design.

3. State Machines

- The AHB to APB bridge used state machines to control data and synchronization signals. Through Model-Sim, students tracked state transitions, ensuring the bridge responded correctly to different transfer requests.

4. **Memory Models (Simulated)**

- Although physical memory was not directly manipulated, SRAM and DRAM models were simulated to understand timing constraints and memory hierarchy, highlighting the role of memory in efficient data handling within digital systems.

5 Summary

The *AHB to APB Bridge Design Internship* by Maven Silicon offered a comprehensive experience in VLSI design, with an emphasis on practical digital design using Verilog HDL. This summary highlights skill enhancements achieved and suggestions for improvement.

5.1 Skill Enhancement

1. Foundational Knowledge in VLSI and SoC Design

- Students began with an introduction to VLSI, SoC architecture, and distinctions between ASIC and FPGA. Topics like ASIC design flow and AMBA bus architecture provided insight into large-scale integrated circuit design, laying the groundwork for hands-on activities.

2. Verilog HDL Programming and Digital Circuit Design

- A significant portion of the internship was dedicated to Verilog HDL, covering data types, procedural blocks, and testbench creation. Practical labs using Quartus Prime and Model-Sim reinforced these skills, allowing students to implement various digital components, including multiplexers and state machines.

3. Protocol Design with AHB and APB Buses

- The AHB to APB bridge project, a capstone exercise, focused on protocol-based design. Students gained in-depth knowledge of AHB and APB signal structures, timing, and transfer mechanisms, essential skills in SoC protocol integration.

4. Simulation, Synthesis, and Verification

- Using Model-Sim for simulation and Quartus Prime for synthesis, students verified design functionality and analyzed waveforms to ensure data flow integrity. Testbench development helped validate designs across operational scenarios, preparing students for complex VLSI systems.

5.2 Comments for Improvement

1. ### Enhanced Lab Access and Practical Hardware Exposure

   - More access to physical labs, including FPGA-based testing, would bridge simulation and real-world hardware constraints, deepening students' understanding of timing and signal integrity.

2. ### Additional Debugging Workshops

   - Dedicated workshops on advanced debugging techniques could improve problem-solving skills, covering topics like timing violations and multi-cycle path debugging.

3. ### **In-Depth Coverage of Memory and State Machines**

   - Practical modules on memory design or integrating memory models with the bridge would enhance understanding.
     Further exploration of state machine optimization could benefit FSM applications in various contexts.

4. ## Extended Project Duration

    - A longer project period would allow more time for iterative testing, synthesis, and code optimization, focusing on efficiency and power management.

5. ## More Interactive Doubt-Solving Sessions

    - Increasing the frequency of interactive sessions, with peer discussions and real-time Q&A, would improve collaboration and problem-solving, essential skills in VLSI design teams.

6 Conclusion

Throughout this internship, we gained comprehensive insights into the digital design of VLSI, from foundational concepts to the practical implementation of an AHB to APB bridge.

Here’s a concise summary of our journey and key learnings:
1. Introduction to VLSI and Digital Design: - We understood the importance of VLSI in modern electronics and explored digital number systems, complements, weighted and non weighted codes.

2. Basic Logic Design: - Learned De Morgan’s laws, converting expressions between SOP and POS, and implemented circuits using NAND/NOR gates. - Studied Boolean algebra, consensus theorem, and Karnaugh maps for logic simplification.

3. Combinational Circuits: - Explored contamination and propagation delays in adders and subtractors. - Studied multiplexers and demultiplexers, recognizing the multiplexer as a universal logic element.

4. Sequential Logic Circuits: - Examined RS latches, D latches, RS flip-flops, and D flip-flops, including setup and hold times. - Learned about Mealy and Moore state machines and implemented sequence detectors, vending machines, and odd parity detectors. - Understood different types of hazards in digital circuits.

5. Memory Design: - Compared SRAM and DRAM, understanding their applications and characteristics.

6. Verilog for Digital Design: - Wrote testbenches in Verilog, used various operators, and identified synthesizable and non-synthesizable commands. - Explored assignments, delays, blocking and non-blocking assignments, and case statements. - Learned to avoid unwanted latches and write efficient task-based testbenches.

7. Project: AHB to APB Bridge Design: - Under Sathya Priya ma’am's

guidance, we learned the significance and modelling of the AHB to APB bridge. - Modelled AHB, understood its combinational logic, and learned about the APB state machine. - Modelled the bridge in RTL, verified it with testbenches, synthesized the module, and integrated it with an AHB master and APB interface for complete system verification. This internship provided a deep understanding of VLSI digital design, from fundamental concepts to practical applications, equipping us with essential skills in Verilog coding, circuit design, and verification for advanced challenges in VLSI and digital electronics.