Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
First Semester 2021-22
General Lab Instructions

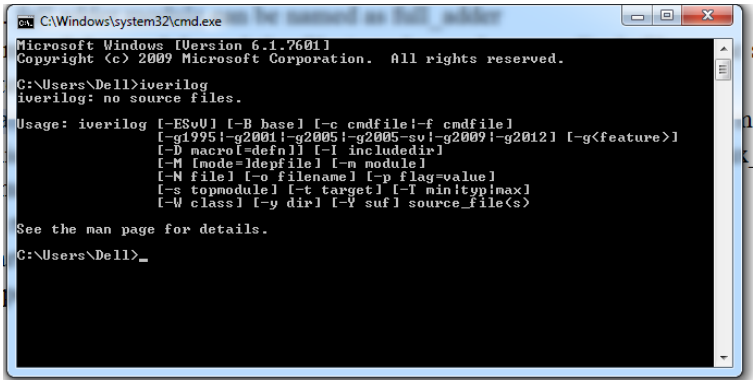
Installation of the software: The lab. shall be conducted in online mode. Therefore, the students are required to install required software before the lab. session. These software, are available for free and can be downloaded by anyone without any restrictions. The file size is less than 100 MB and might take only a few minutes to install. Students can download the relevant software as per their OS from here http://iverilog.icarus.com/home. While installing, the installer will ask you if *gtkwave* is to be installed or not please accept it. You will need this for viewing the waveforms generated after the simulation. It is also recommended to install *NotePad++* as the text editor, it helps in syntax highlighting, thereby making things look much better than an ordinary text editor. Other text editors like *vim* can also be used.

1. Once installed make sure that *iverilog* is properly added to the path.
2. You can add it on your own if not done automatically during installation.
3. In *Control panel -> Advanced System Settings -> Environment Variables*
4. Here in the *System Variables* choose *path* and edit it.
5. Click *New* and add two paths *C:\iverilog\bin* for iverilog
6. Click *New* and add two paths *C:\iverilog\gtkwave\bin* for gtkwave
7. Save the changes. Sometimes you may have to restart the system.
8. Check if *iverilog* is properly added to the path using the following process.

Process to Verify the installation

1. To run *icarus verilog* you need to go to the command prompt.
Start → Run → cmd

2. Type *iverilog* and press enter you should see the following screen if the installation is done properly.



My First Verilog Program

You can run the conventional "Hello World!" program to familiarize yourself with the process of executing program using *iverilog*.

```
module hello;
  initial
    begin
      $display("Hello World");
      $finish ;
    end
endmodule
```

Write this program in a text editor and save it as *hello.v.*

The command used to compile Verilog codes is (*filename* is *hello* here)

iverilog –o filename.vvp filename.v

The results of this compile are placed into the file "hello", because the "-o" flag tells the compiler where to place the compiled result. If there are syntax errors, you will find them after compilation. In case of no errors, proceed to see the output using

vvp filename.vvp

The "iverilog" and "vvp" commands are the most important commands available to users of Icarus Verilog. The "iverilog" command is the compiler, and the "vvp" command is the simulation runtime engine. What sort of output the compiler actually creates is controlled by command line switches, but normally it produces output in the default vvp format, which is in turn executed by the vvp program.

Good Practices Recommended for this Lab.

1. Create folder with the name *Comp_Arch* and use it as a working directory for all the works you will be doing as a part of this lab.
2. You will have to use the codes which you write in any lab some time later. This concept is called Hierarchy which you may think like building a library of your own. This also imposes that condition that one should be update with the lab.
3. The name of the modules, signals should be relevant to their functionality or else properly explained using comment lines.
4. A good coder is the one who knows what exactly will be the output of his/her code. Never rely on the trial and error method to make things work, inspect and assess each line carefully to properly architect your code.
5. Though the constructs of HDL resemble conventional programming languages, remember they are Hardware Description Languages. Therefore, try to come up with the equivalent hardware before you start deigning. This is not just fun but

will improve your analytical and design capabilities. The pleasure of applying the concepts learnt in your favorite course digital design will give you immense pleasure.

Most Common Mistakes in Verilog

1. All keywords should be in ***lower case***.
2. Upper case and lower case are distinct in verilog, it is ***case sensitive***.
3. Make sure that the ***wires*** are properly declared before usage.
4. Unwanted spaces will put you in trouble. For example, ***endmodule*** doesn't have any space in between.
5. Module declaration is a statement terminate it with a ***semicolon***.
6. Module name can't start with a number and can't have a special character in it.
7. The output 'x' indicates that the signal is still unknown and being evaluated.
8. In combinational circuits 'z' in the output means the signals are not connected properly.
9. The LHS of a procedural block has to be of the type *reg*.

A Few Lines Needed in iverilog:

1. While using *icarus Verilog*, make sure that the following lines of code are added in every *test bench*. The *.vcd* file generated goes as an input to a wave form viewer

```
initial
    begin
        $dumpfile("filename.vcd");
        $dumpvars;
    end
```

2. If you want to instantiate any module in any other module then the first line in the new module should have *`include "modulename.v"* ex. the full_adder.v which calls half_adder module which is in file half_adder.v then the full_adder.v should have the line *`include "half_adder.v"* in it. This is exclusive to *icarus verilog* only.

******The End******