MINI PROJECT

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CODE:

Latch:

```
module latch(input clock,reset,input [3:0] in,output reg [3:0]q);

//behavioural logic of d flipflop

always @(posedge clock)

  begin

    if(reset)

          q <= 1'b0;

        else

          q <= in;

     end

endmodule
```

Decoder:

```
module decoder (input en,input [1:0]in,output reg [3:0]
y);
//behavioural logic of decoder
always @(*)
 begin
 if (en == 1'b1)
  begin
  case(in)
        2'b00 : y = 4'd1;
        2'b01 : y = 4'd2;
        2'b10 : y = 4'd4;
        2'b11 : y = 4'd8;
  default : y = 4'd0;
  endcase
  end
  else
  y = 4'b0000;
  end
```

```
endmodule
```

Mux:

```
module mux(input [3:0]in,input [1:0]sel,output out);
// Mux 4to1  using data flow
assign out =in[sel];
endmodule
```

Top Module:

```
module top (input clk,output data, output [3:0]y);
 wire out;
 wire [1:0]sel;
 wire [3:0]t;
 mux MUX(in,sel,out);
 decoder DECODER(out,sel,t);
 latch LATCH(clk,reset,t,y);
 c_counter_binary_0
CONTER(.CLK(clk),.SCLR(reset),.Q(sel) );
```

```
 // input wire CLK
  // input wire SCLR
  // output wire [1 : 0] if
  ila_1 ILA(.clk(clk),.probe0(data),.probe1(y));
  // input wire clk
 // input wire [0:0]  probe0
// input wire [3:0]  probe1
vio_0 VIO (.clk(clk),.probe_out0(reset),.probe_out1(in));
  // input wire clk
 // output wire [0 : 0] probe_out0
// output wire [3 : 0] probe_out1
 assign data = out;
endmodule
```

Constraints:

```
set_property PACKAGE_PIN H17 [get_ports {y[3]}]
set_property PACKAGE_PIN K15 [get_ports {y[2]}]
set_property PACKAGE_PIN J13 [get_ports {y[1]}]
```

set_property PACKAGE_PIN N14 [get_ports {y[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports clk]

#set_property IOSTANDARD LVCMOS33 [get_ports reset]

#set_property IOSTANDARD LVCMOS33 [get_ports {in[3]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {in[2]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {in[1]}]

#set_property IOSTANDARD LVCMOS33 [get_ports {in[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {y[3]}]

set_property IOSTANDARD LVCMOS33 [get_ports {y[2]}]

set_property IOSTANDARD LVCMOS33 [get_ports {y[1]}]

set_property IOSTANDARD LVCMOS33 [get_ports {y[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports data]

set_property PACKAGE_PIN V17 [get_ports data]

#set_property PACKAGE_PIN J15 [get_ports {in[3]}]

#set_property PACKAGE_PIN L16 [get_ports {in[2]}]

#set_property PACKAGE_PIN M13 [get_ports {in[1]}]

#set_property PACKAGE_PIN R15 [get_ports {in[0]}]

#set_property PACKAGE_PIN T18 [get_ports reset]

set_property PACKAGE_PIN U18 [get_ports clk]

Synthesis: