CBCS SCHEME

USN | 1 | BT | 21 | CS | 096 |

21CS34

Third Semester B.E. Degree Examination, June/July 2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw and explain the connection between processor and memory with the respective registers. **(10 Marks)**

b. Assuming that the reference computer is Ultra SPARCIO workstation with 300 MHz Ultra SPARC – IIi processor. A company has to purchase 500 new computers, hence ordered testing of a new computer with SPEC 2000. Following observations were made:

Programs	Runtime on reference computer	Runtime on new computer
1	50 minutes	5 minutes
2	75 minutes	4 minutes
3	60 minutes	6 minutes
4	30 minutes	3 minutes

The company's system manager will place the orders for purchasing new computers only if the overall SPEC rating is at least 12. After the said test, will the system manager place order for the purchase of new computers? **(10 Marks)**

OR

2 a. Explain Big Endian and Little Endian methods of byte addressing. **(05 Marks)**

b. Explain the following:
(i) Three address instructions (ii) Two address instructions
(iii) One address instructions (iv) Zero address instructions **(08 Marks)**

c. What is an addressing mode? Registers R_1 and R_2 of a computer contain the decimal values 1400 and 5000. What is the effective address of the source operand in each of the following instructions?
(i) Load 20(R_1), R_5 (ii) Move # 3000, R_5 (iii) Store 30(R_1, R_2), R_5
(iv) Add (R_2)+, R_5 (v) Subtract –(R_1), R_5 **(07 Marks)**

Module-2

3 a. With neat diagram, explain interrupt operation. **(06 Marks)**

b. What is DMA? Showing the possible register configurations in DMA interface. Explain DMA. **(07 Marks)**

c. With neat timing diagram, explain synchronous input transfer. **(07 Marks)**

OR

4 a. Explain how interrupt requests from several IO devices can be communicated to a processor through a single INTR line. **(08 Marks)**

b. With a neat block diagram, explain how a keyboard is connected to a processor. **(08 Marks)**

c. Compare serial and parallel interface. **(04 Marks)**

Module-3

5 a. Explain the working of static RAM cell. (06 Marks)
b. With neat diagram explain the working of 16 Megabits DRAM chip configured as 2M × 8. (08 Marks)
c. With neat diagram, explain the memory hierarchy with respect to speed, size and cost. (06 Marks)

OR

6 a. Explain different types of ROMs. (06 Marks)
b. With neat diagram, explain the internal structure of ROM cell. (06 Marks)
c. With neat diagram, explain how virtual memory address translation takes place. (08 Marks)

Module-4

7 a. With neat diagram, explain 4-bit carry look ahead adder. (07 Marks)
b. Design a logic circuit to perform addition/subtraction of two 4 bit numbers X and Y. (06 Marks)
c. Perform multiplication for +14 and –6 using Booth's algorithm. (07 Marks)

OR

8 a. List out the actions needed to execute the instruction Add (R3), R1. Write the sequence of control steps needed for the execution of the same. Also explain. (10 Marks)
b. With neat block diagram, explain Hardwired Control Unit. (10 Marks)

Module-5

9 a. Explain Flynn's classification of computers. (06 Marks)
b. With neat diagram, explain attached array processor. (06 Marks)
c. Explain how the following expression is evaluated in pipelined mode:
$A_i * B_i + C_i$ for i = 1, 2, …. 7 (08 Marks)

OR

10 a. With neat diagram, explain SIMD array processor organization. (06 Marks)
b. With neat flow diagram, explain four-segment CPU pipeline. (10 Marks)
c. Write the sequence of operations for the following Do loop.

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Do 20 I = 1, 100
20 C[I] = B[I] + A[I]
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(04 Marks)

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