	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	DEBUG_ALU_OUT[*]	CLK1	16.677	16.791	Rise	CLK1
1	DEBUG_ALU_OUT[0]	CLK1	15.957	15.797	Rise	CLK1
2	DEBUG_ALU_OUT[1]	CLK1	13.032	12.974	Rise	CLK1
3	DEBUG_ALU_OUT[2]	CLK1	12.937	12.926	Rise	CLK1
4	DEBUG_ALU_OUT[3]	CLK1	14.149	14.162	Rise	CLK1
5	DEBUG_ALU_OUT[4]	CLK1	13.852	13.785	Rise	CLK1
6	DEBUG_ALU_OUT[5]	CLK1	16.677	16.791	Rise	CLK1
7	DEBUG_ALU_OUT[6]	CLK1	14.569	14.524	Rise	CLK1
8	DEBUG_ALU_OUT[7]	CLK1	14.339	14.257	Rise	CLK1
9	DEBUG_ALU_OUT[8]	CLK1	15.708	15.814	Rise	CLK1
10	DEBUG_ALU_OUT[9]	CLK1	14.649	14.577	Rise	CLK1
11	DEBUG_ALU_OUT[10]	CLK1	14.241	14.241	Rise	CLK1
12	DEBUG_ALU_OUT[11]	CLK1	14.098	14.019	Rise	CLK1
13	DEBUG_ALU_OUT[12]	CLK1	15.959	16.030	Rise	CLK1
14	DEBUG_ALU_OUT[13]	CLK1	14.926	14.824	Rise	CLK1
15	DEBUG_ALU_OUT[14]	CLK1	14.650	14.615	Rise	CLK1
16	DEBUG_ALU_OUT[15]	CLK1	14.698	14.634	Rise	CLK1
17	DEBUG_ALU_OUT[16]	CLK1	14.930	14.889	Rise	CLK1
18	DEBUG_ALU_OUT[17]	CLK1	14.753	14.697	Rise	CLK1
19	DEBUG_ALU_OUT[18]	CLK1	14.588	14.553	Rise	CLK1
20	DEBUG_ALU_OUT[19]	CLK1	15.691	15.726	Rise	CLK1
21	DEBUG_ALU_OUT[20]	CLK1	14.809	14.812	Rise	CLK1
22	DEBUG_ALU_OUT[21]	CLK1	15.155	15.059	Rise	CLK1
23	DEBUG_ALU_OUT[22]	CLK1	15.199	15.207	Rise	CLK1
24	DEBUG_ALU_OUT[23]	CLK1	15.623	15.545	Rise	CLK1
25	DEBUG_ALU_OUT[24]	CLK1	14.763	14.761	Rise	CLK1
26	DEBUG_ALU_OUT[25]	CLK1	15.422	15.361	Rise	CLK1
27	DEBUG_ALU_OUT[26]	CLK1	15.445	15.412	Rise	CLK1
28	DEBUG_ALU_OUT[27]	CLK1	15.462	15.399	Rise	CLK1
29	DEBUG_ALU_OUT[28]	CLK1	15.166	15.125	Rise	CLK1
30	DEBUG_ALU_OUT[29]	CLK1	15.156	15.102	Rise	CLK1
31	DEBUG_ALU_OUT[30]	CLK1	16.095	16.157	Rise	CLK1
32	DEBUG_ALU_OUT[31]	CLK1	16.266	16.212	Rise	CLK1
2	DEBUG_REG_T0[*]	CLK1	8.064	8.211	Rise	CLK1
1	DEBUG_REG_T0[0]	CLK1	6.818	6.812	Rise	CLK1
2	DEBUG_REG_T0[1]	CLK1	6.949	6.935	Rise	CLK1
3	DEBUG_REG_T0[2]	CLK1	7.509	7.576	Rise	CLK1
4	DEBUG_REG_T0[3]	CLK1	6.562	6.597	Rise	CLK1
5	DEBUG_REG_T0[4]	CLK1	6.501	6.500	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
6	DEBUG_REG_T0[5]	CLK1	6.806	6.838	Rise	CLK1
7	DEBUG_REG_T0[6]	CLK1	6.507	6.509	Rise	CLK1
8	DEBUG_REG_T0[7]	CLK1	6.855	6.882	Rise	CLK1
9	DEBUG_REG_T0[8]	CLK1	6.503	6.513	Rise	CLK1
10	DEBUG_REG_T0[9]	CLK1	6.504	6.482	Rise	CLK1
11	DEBUG_REG_T0[10]	CLK1	7.791	7.779	Rise	CLK1
12	DEBUG_REG_T0[11]	CLK1	6.720	6.701	Rise	CLK1
13	DEBUG_REG_T0[12]	CLK1	7.045	7.024	Rise	CLK1
14	DEBUG_REG_T0[13]	CLK1	7.114	7.116	Rise	CLK1
15	DEBUG_REG_T0[14]	CLK1	6.871	6.865	Rise	CLK1
16	DEBUG_REG_T0[15]	CLK1	6.585	6.604	Rise	CLK1
17	DEBUG_REG_T0[16]	CLK1	7.166	7.152	Rise	CLK1
18	DEBUG_REG_T0[17]	CLK1	6.647	6.682	Rise	CLK1
19	DEBUG_REG_T0[18]	CLK1	6.868	6.841	Rise	CLK1
20	DEBUG_REG_T0[19]	CLK1	6.459	6.496	Rise	CLK1
21	DEBUG_REG_T0[20]	CLK1	6.585	6.590	Rise	CLK1
22	DEBUG_REG_T0[21]	CLK1	6.252	6.330	Rise	CLK1
23	DEBUG_REG_T0[22]	CLK1	6.351	6.355	Rise	CLK1
24	DEBUG_REG_T0[23]	CLK1	6.966	6.985	Rise	CLK1
25	DEBUG_REG_T0[24]	CLK1	7.234	7.287	Rise	CLK1
26	DEBUG_REG_T0[25]	CLK1	8.064	8.211	Rise	CLK1
27	DEBUG_REG_T0[26]	CLK1	6.735	6.714	Rise	CLK1
28	DEBUG_REG_T0[27]	CLK1	7.130	7.100	Rise	CLK1
29	DEBUG_REG_T0[28]	CLK1	6.970	7.012	Rise	CLK1
30	DEBUG_REG_T0[29]	CLK1	6.760	6.771	Rise	CLK1
31	DEBUG_REG_T0[30]	CLK1	7.596	7.586	Rise	CLK1
32	DEBUG_REG_T0[31]	CLK1	6.711	6.732	Rise	CLK1
3	DEBUG_WB_DATA[*]	CLK1	10.872	11.056	Rise	CLK1
1	DEBUG_WB_DATA[0]	CLK1	10.584	10.862	Rise	CLK1
2	DEBUG_WB_DATA[1]	CLK1	8.602	8.664	Rise	CLK1
3	DEBUG_WB_DATA[2]	CLK1	8.981	9.125	Rise	CLK1
4	DEBUG_WB_DATA[3]	CLK1	9.017	9.027	Rise	CLK1
5	DEBUG_WB_DATA[4]	CLK1	8.917	8.870	Rise	CLK1
6	DEBUG_WB_DATA[5]	CLK1	8.324	8.451	Rise	CLK1
7	DEBUG_WB_DATA[6]	CLK1	8.142	8.012	Rise	CLK1
8	DEBUG_WB_DATA[7]	CLK1	8.995	8.971	Rise	CLK1
9	DEBUG_WB_DATA[8]	CLK1	9.394	9.340	Rise	CLK1
10	DEBUG_WB_DATA[9]	CLK1	9.122	9.172	Rise	CLK1
11	DEBUG_WB_DATA[10]	CLK1	9.269	9.357	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
12	DEBUG_WB_DATA[11]	CLK1	8.401	8.448	Rise	CLK1
13	DEBUG_WB_DATA[12]	CLK1	8.123	8.089	Rise	CLK1
14	DEBUG_WB_DATA[13]	CLK1	8.669	8.624	Rise	CLK1
15	DEBUG_WB_DATA[14]	CLK1	8.387	8.325	Rise	CLK1
16	DEBUG_WB_DATA[15]	CLK1	8.365	8.383	Rise	CLK1
17	DEBUG_WB_DATA[16]	CLK1	8.539	8.482	Rise	CLK1
18	DEBUG_WB_DATA[17]	CLK1	8.815	8.756	Rise	CLK1
19	DEBUG_WB_DATA[18]	CLK1	9.467	9.518	Rise	CLK1
20	DEBUG_WB_DATA[19]	CLK1	9.193	9.266	Rise	CLK1
21	DEBUG_WB_DATA[20]	CLK1	8.776	8.801	Rise	CLK1
22	DEBUG_WB_DATA[21]	CLK1	9.196	9.093	Rise	CLK1
23	DEBUG_WB_DATA[22]	CLK1	8.479	8.561	Rise	CLK1
24	DEBUG_WB_DATA[23]	CLK1	8.673	8.676	Rise	CLK1
25	DEBUG_WB_DATA[24]	CLK1	8.864	8.928	Rise	CLK1
26	DEBUG_WB_DATA[25]	CLK1	8.627	8.627	Rise	CLK1
27	DEBUG_WB_DATA[26]	CLK1	9.418	9.392	Rise	CLK1
28	DEBUG_WB_DATA[27]	CLK1	8.556	8.604	Rise	CLK1
29	DEBUG_WB_DATA[28]	CLK1	9.807	9.843	Rise	CLK1
30	DEBUG_WB_DATA[29]	CLK1	8.948	9.018	Rise	CLK1
31	DEBUG_WB_DATA[30]	CLK1	10.872	11.056	Rise	CLK1
32	DEBUG_WB_DATA[31]	CLK1	8.920	8.946	Rise	CLK1
4	INSTR_debug[*]	CLK1	9.079	9.141	Rise	CLK1
1	INSTR_debug[0]	CLK1	6.272	6.323	Rise	CLK1
2	INSTR_debug[1]	CLK1	5.999	5.972	Rise	CLK1
3	INSTR_debug[2]	CLK1	5.765	5.743	Rise	CLK1
4	INSTR_debug[3]	CLK1	6.265	6.282	Rise	CLK1
5	INSTR_debug[4]	CLK1	6.643	6.657	Rise	CLK1
6	INSTR_debug[5]	CLK1	6.452	6.423	Rise	CLK1
7	INSTR_debug[6]	CLK1	6.149	6.129	Rise	CLK1
8	INSTR_debug[7]	CLK1	6.398	6.416	Rise	CLK1
9	INSTR_debug[8]	CLK1	6.151	6.121	Rise	CLK1
10	INSTR_debug[9]	CLK1	6.772	6.772	Rise	CLK1
11	INSTR_debug[10]	CLK1	6.793	6.780	Rise	CLK1
12	INSTR_debug[11]	CLK1	5.995	5.980	Rise	CLK1
13	INSTR_debug[12]	CLK1	7.310	7.317	Rise	CLK1
14	INSTR_debug[13]	CLK1	6.184	6.145	Rise	CLK1
15	INSTR_debug[14]	CLK1	6.419	6.367	Rise	CLK1
16	INSTR_debug[15]	CLK1	9.079	9.141	Rise	CLK1
17	INSTR_debug[16]	CLK1	7.164	7.106	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
18	INSTR_debug[17]	CLK1	7.411	7.450	Rise	CLK1
19	INSTR_debug[18]	CLK1	6.842	6.883	Rise	CLK1
20	INSTR_debug[19]	CLK1	7.717	7.773	Rise	CLK1
21	INSTR_debug[20]	CLK1	7.915	7.996	Rise	CLK1
22	INSTR_debug[21]	CLK1	8.327	8.455	Rise	CLK1
23	INSTR_debug[22]	CLK1	6.441	6.505	Rise	CLK1
24	INSTR_debug[23]	CLK1	8.558	8.754	Rise	CLK1
25	INSTR_debug[24]	CLK1	6.514	6.518	Rise	CLK1
26	INSTR_debug[25]	CLK1	6.536	6.512	Rise	CLK1
27	INSTR_debug[26]	CLK1	5.763	5.753	Rise	CLK1
28	INSTR_debug[27]	CLK1	6.232	6.215	Rise	CLK1
29	INSTR_debug[28]	CLK1	6.589	6.579	Rise	CLK1
30	INSTR_debug[29]	CLK1	7.558	7.699	Rise	CLK1
31	INSTR_debug[30]	CLK1	6.587	6.624	Rise	CLK1
32	INSTR_debug[31]	CLK1	6.011	5.985	Rise	CLK1
5	PC_out[*]	CLK1	7.889	7.942	Rise	CLK1
1	PC_out[0]	CLK1	6.831	6.857	Rise	CLK1
2	PC_out[1]	CLK1	6.644	6.680	Rise	CLK1
3	PC_out[2]	CLK1	6.494	6.475	Rise	CLK1
4	PC_out[3]	CLK1	6.494	6.443	Rise	CLK1
5	PC_out[4]	CLK1	6.239	6.231	Rise	CLK1
6	PC_out[5]	CLK1	6.260	6.252	Rise	CLK1
7	PC_out[6]	CLK1	6.211	6.177	Rise	CLK1
8	PC_out[7]	CLK1	6.383	6.391	Rise	CLK1
9	PC_out[8]	CLK1	7.751	7.864	Rise	CLK1
10	PC_out[9]	CLK1	7.252	7.225	Rise	CLK1
11	PC_out[10]	CLK1	6.623	6.551	Rise	CLK1
12	PC_out[11]	CLK1	7.105	7.139	Rise	CLK1
13	PC_out[12]	CLK1	6.277	6.277	Rise	CLK1
14	PC_out[13]	CLK1	7.889	7.942	Rise	CLK1
15	PC_out[14]	CLK1	5.811	5.805	Rise	CLK1
16	PC_out[15]	CLK1	6.318	6.303	Rise	CLK1
17	PC_out[16]	CLK1	6.589	6.511	Rise	CLK1
18	PC_out[17]	CLK1	6.154	6.130	Rise	CLK1
19	PC_out[18]	CLK1	6.041	6.027	Rise	CLK1
20	PC_out[19]	CLK1	6.414	6.387	Rise	CLK1
21	PC_out[20]	CLK1	6.482	6.430	Rise	CLK1
22	PC_out[21]	CLK1	6.590	6.548	Rise	CLK1
23	PC_out[22]	CLK1	5.953	5.974	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
24	PC_out[23]	CLK1	6.170	6.144	Rise	CLK1
25	PC_out[24]	CLK1	6.341	6.298	Rise	CLK1
26	PC_out[25]	CLK1	6.223	6.224	Rise	CLK1
27	PC_out[26]	CLK1	6.367	6.305	Rise	CLK1
28	PC_out[27]	CLK1	6.648	6.637	Rise	CLK1
29	PC_out[28]	CLK1	7.474	7.630	Rise	CLK1
30	PC_out[29]	CLK1	6.250	6.235	Rise	CLK1
31	PC_out[30]	CLK1	6.249	6.217	Rise	CLK1
32	PC_out[31]	CLK1	6.267	6.238	Rise	CLK1