	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	DEBUG_ALU_OUT[*]	CLK1	7.020	6.954	Rise	CLK1
1	DEBUG_ALU_OUT[0]	CLK1	7.208	7.156	Rise	CLK1
2	DEBUG_ALU_OUT[1]	CLK1	7.459	7.491	Rise	CLK1
3	DEBUG_ALU_OUT[2]	CLK1	7.020	6.954	Rise	CLK1
4	DEBUG_ALU_OUT[3]	CLK1	8.060	8.207	Rise	CLK1
5	DEBUG_ALU_OUT[4]	CLK1	8.123	8.007	Rise	CLK1
6	DEBUG_ALU_OUT[5]	CLK1	9.824	10.026	Rise	CLK1
7	DEBUG_ALU_OUT[6]	CLK1	8.226	8.239	Rise	CLK1
8	DEBUG_ALU_OUT[7]	CLK1	8.303	8.264	Rise	CLK1
9	DEBUG_ALU_OUT[8]	CLK1	8.997	9.057	Rise	CLK1
10	DEBUG_ALU_OUT[9]	CLK1	7.755	7.689	Rise	CLK1
11	DEBUG_ALU_OUT[10]	CLK1	7.427	7.383	Rise	CLK1
12	DEBUG_ALU_OUT[11]	CLK1	7.189	7.122	Rise	CLK1
13	DEBUG_ALU_OUT[12]	CLK1	8.394	8.538	Rise	CLK1
14	DEBUG_ALU_OUT[13]	CLK1	7.605	7.526	Rise	CLK1
15	DEBUG_ALU_OUT[14]	CLK1	7.627	7.548	Rise	CLK1
16	DEBUG_ALU_OUT[15]	CLK1	7.785	7.713	Rise	CLK1
17	DEBUG_ALU_OUT[16]	CLK1	7.924	7.871	Rise	CLK1
18	DEBUG_ALU_OUT[17]	CLK1	7.329	7.273	Rise	CLK1
19	DEBUG_ALU_OUT[18]	CLK1	7.518	7.460	Rise	CLK1
20	DEBUG_ALU_OUT[19]	CLK1	8.065	8.100	Rise	CLK1
21	DEBUG_ALU_OUT[20]	CLK1	7.331	7.395	Rise	CLK1
22	DEBUG_ALU_OUT[21]	CLK1	7.834	7.731	Rise	CLK1
23	DEBUG_ALU_OUT[22]	CLK1	7.462	7.494	Rise	CLK1
24	DEBUG_ALU_OUT[23]	CLK1	7.967	8.032	Rise	CLK1
25	DEBUG_ALU_OUT[24]	CLK1	8.077	8.008	Rise	CLK1
26	DEBUG_ALU_OUT[25]	CLK1	8.368	8.310	Rise	CLK1
27	DEBUG_ALU_OUT[26]	CLK1	8.463	8.390	Rise	CLK1
28	DEBUG_ALU_OUT[27]	CLK1	8.239	8.123	Rise	CLK1
29	DEBUG_ALU_OUT[28]	CLK1	7.261	7.280	Rise	CLK1
30	DEBUG_ALU_OUT[29]	CLK1	7.207	7.257	Rise	CLK1
31	DEBUG_ALU_OUT[30]	CLK1	7.581	7.688	Rise	CLK1
32	DEBUG_ALU_OUT[31]	CLK1	7.872	7.890	Rise	CLK1
2	DEBUG_REG_T0[*]	CLK1	6.058	6.132	Rise	CLK1
1	DEBUG_REG_T0[0]	CLK1	6.594	6.585	Rise	CLK1
2	DEBUG_REG_T0[1]	CLK1	6.721	6.705	Rise	CLK1
3	DEBUG_REG_T0[2]	CLK1	7.264	7.327	Rise	CLK1
4	DEBUG_REG_T0[3]	CLK1	6.350	6.381	Rise	CLK1
5	DEBUG_REG_T0[4]	CLK1	6.295	6.293	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
6	DEBUG_REG_T0[5]	CLK1	6.589	6.619	Rise	CLK1
7	DEBUG_REG_T0[6]	CLK1	6.298	6.297	Rise	CLK1
8	DEBUG_REG_T0[7]	CLK1	6.636	6.661	Rise	CLK1
9	DEBUG_REG_T0[8]	CLK1	6.293	6.300	Rise	CLK1
10	DEBUG_REG_T0[9]	CLK1	6.295	6.271	Rise	CLK1
11	DEBUG_REG_T0[10]	CLK1	7.529	7.514	Rise	CLK1
12	DEBUG_REG_T0[11]	CLK1	6.507	6.487	Rise	CLK1
13	DEBUG_REG_T0[12]	CLK1	6.814	6.791	Rise	CLK1
14	DEBUG_REG_T0[13]	CLK1	6.879	6.878	Rise	CLK1
15	DEBUG_REG_T0[14]	CLK1	6.646	6.638	Rise	CLK1
16	DEBUG_REG_T0[15]	CLK1	6.370	6.385	Rise	CLK1
17	DEBUG_REG_T0[16]	CLK1	6.930	6.914	Rise	CLK1
18	DEBUG_REG_T0[17]	CLK1	6.432	6.463	Rise	CLK1
19	DEBUG_REG_T0[18]	CLK1	6.644	6.614	Rise	CLK1
20	DEBUG_REG_T0[19]	CLK1	6.258	6.292	Rise	CLK1
21	DEBUG_REG_T0[20]	CLK1	6.372	6.374	Rise	CLK1
22	DEBUG_REG_T0[21]	CLK1	6.058	6.132	Rise	CLK1
23	DEBUG_REG_T0[22]	CLK1	6.146	6.147	Rise	CLK1
24	DEBUG_REG_T0[23]	CLK1	6.743	6.760	Rise	CLK1
25	DEBUG_REG_T0[24]	CLK1	7.000	7.049	Rise	CLK1
26	DEBUG_REG_T0[25]	CLK1	7.845	7.989	Rise	CLK1
27	DEBUG_REG_T0[26]	CLK1	6.516	6.493	Rise	CLK1
28	DEBUG_REG_T0[27]	CLK1	6.898	6.867	Rise	CLK1
29	DEBUG_REG_T0[28]	CLK1	6.746	6.785	Rise	CLK1
30	DEBUG_REG_T0[29]	CLK1	6.538	6.546	Rise	CLK1
31	DEBUG_REG_T0[30]	CLK1	7.341	7.330	Rise	CLK1
32	DEBUG_REG_T0[31]	CLK1	6.497	6.516	Rise	CLK1
3	DEBUG_WB_DATA[*]	CLK1	7.073	7.136	Rise	CLK1
1	DEBUG_WB_DATA[0]	CLK1	9.797	9.966	Rise	CLK1
2	DEBUG_WB_DATA[1]	CLK1	7.499	7.582	Rise	CLK1
3	DEBUG_WB_DATA[2]	CLK1	8.164	8.283	Rise	CLK1
4	DEBUG_WB_DATA[3]	CLK1	8.269	8.358	Rise	CLK1
5	DEBUG_WB_DATA[4]	CLK1	8.258	8.312	Rise	CLK1
6	DEBUG_WB_DATA[5]	CLK1	7.926	7.957	Rise	CLK1
7	DEBUG_WB_DATA[6]	CLK1	7.447	7.403	Rise	CLK1
8	DEBUG_WB_DATA[7]	CLK1	8.206	8.262	Rise	CLK1
9	DEBUG_WB_DATA[8]	CLK1	8.454	8.416	Rise	CLK1
10	DEBUG_WB_DATA[9]	CLK1	8.729	8.747	Rise	CLK1
11	DEBUG_WB_DATA[10]	CLK1	8.321	8.476	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
12	DEBUG_WB_DATA[11]	CLK1	7.533	7.585	Rise	CLK1
13	DEBUG_WB_DATA[12]	CLK1	7.073	7.136	Rise	CLK1
14	DEBUG_WB_DATA[13]	CLK1	7.851	7.879	Rise	CLK1
15	DEBUG_WB_DATA[14]	CLK1	7.735	7.813	Rise	CLK1
16	DEBUG_WB_DATA[15]	CLK1	7.445	7.487	Rise	CLK1
17	DEBUG_WB_DATA[16]	CLK1	7.627	7.695	Rise	CLK1
18	DEBUG_WB_DATA[17]	CLK1	7.238	7.279	Rise	CLK1
19	DEBUG_WB_DATA[18]	CLK1	8.300	8.433	Rise	CLK1
20	DEBUG_WB_DATA[19]	CLK1	8.515	8.607	Rise	CLK1
21	DEBUG_WB_DATA[20]	CLK1	7.187	7.250	Rise	CLK1
22	DEBUG_WB_DATA[21]	CLK1	7.324	7.361	Rise	CLK1
23	DEBUG_WB_DATA[22]	CLK1	7.915	8.034	Rise	CLK1
24	DEBUG_WB_DATA[23]	CLK1	7.278	7.306	Rise	CLK1
25	DEBUG_WB_DATA[24]	CLK1	8.181	8.329	Rise	CLK1
26	DEBUG_WB_DATA[25]	CLK1	7.873	7.942	Rise	CLK1
27	DEBUG_WB_DATA[26]	CLK1	8.879	8.868	Rise	CLK1
28	DEBUG_WB_DATA[27]	CLK1	7.832	7.935	Rise	CLK1
29	DEBUG_WB_DATA[28]	CLK1	8.822	8.880	Rise	CLK1
30	DEBUG_WB_DATA[29]	CLK1	8.273	8.410	Rise	CLK1
31	DEBUG_WB_DATA[30]	CLK1	9.242	9.461	Rise	CLK1
32	DEBUG_WB_DATA[31]	CLK1	7.314	7.459	Rise	CLK1
4	INSTR_debug[*]	CLK1	5.581	5.561	Rise	CLK1
1	INSTR_debug[0]	CLK1	6.078	6.126	Rise	CLK1
2	INSTR_debug[1]	CLK1	5.811	5.783	Rise	CLK1
3	INSTR_debug[2]	CLK1	5.584	5.561	Rise	CLK1
4	INSTR_debug[3]	CLK1	6.064	6.078	Rise	CLK1
5	INSTR_debug[4]	CLK1	6.426	6.437	Rise	CLK1
6	INSTR_debug[5]	CLK1	6.245	6.214	Rise	CLK1
7	INSTR_debug[6]	CLK1	5.954	5.931	Rise	CLK1
8	INSTR_debug[7]	CLK1	6.193	6.208	Rise	CLK1
9	INSTR_debug[8]	CLK1	5.955	5.923	Rise	CLK1
10	INSTR_debug[9]	CLK1	6.552	6.550	Rise	CLK1
11	INSTR_debug[10]	CLK1	6.571	6.557	Rise	CLK1
12	INSTR_debug[11]	CLK1	5.806	5.789	Rise	CLK1
13	INSTR_debug[12]	CLK1	7.068	7.072	Rise	CLK1
14	INSTR_debug[13]	CLK1	5.987	5.947	Rise	CLK1
15	INSTR_debug[14]	CLK1	6.213	6.160	Rise	CLK1
16	INSTR_debug[15]	CLK1	8.766	8.823	Rise	CLK1
17	INSTR_debug[16]	CLK1	6.929	6.871	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
18	INSTR_debug[17]	CLK1	7.169	7.206	Rise	CLK1
19	INSTR_debug[18]	CLK1	6.619	6.656	Rise	CLK1
20	INSTR_debug[19]	CLK1	7.464	7.516	Rise	CLK1
21	INSTR_debug[20]	CLK1	7.650	7.725	Rise	CLK1
22	INSTR_debug[21]	CLK1	8.046	8.166	Rise	CLK1
23	INSTR_debug[22]	CLK1	6.239	6.299	Rise	CLK1
24	INSTR_debug[23]	CLK1	8.268	8.453	Rise	CLK1
25	INSTR_debug[24]	CLK1	6.310	6.312	Rise	CLK1
26	INSTR_debug[25]	CLK1	6.325	6.299	Rise	CLK1
27	INSTR_debug[26]	CLK1	5.581	5.569	Rise	CLK1
28	INSTR_debug[27]	CLK1	6.037	6.020	Rise	CLK1
29	INSTR_debug[28]	CLK1	6.382	6.370	Rise	CLK1
30	INSTR_debug[29]	CLK1	7.360	7.498	Rise	CLK1
31	INSTR_debug[30]	CLK1	6.378	6.413	Rise	CLK1
32	INSTR_debug[31]	CLK1	5.822	5.794	Rise	CLK1
5	PC_out[*]	CLK1	5.629	5.620	Rise	CLK1
1	PC_out[0]	CLK1	6.608	6.630	Rise	CLK1
2	PC_out[1]	CLK1	6.428	6.461	Rise	CLK1
3	PC_out[2]	CLK1	6.285	6.264	Rise	CLK1
4	PC_out[3]	CLK1	6.285	6.233	Rise	CLK1
5	PC_out[4]	CLK1	6.041	6.030	Rise	CLK1
6	PC_out[5]	CLK1	6.059	6.049	Rise	CLK1
7	PC_out[6]	CLK1	6.013	5.979	Rise	CLK1
8	PC_out[7]	CLK1	6.183	6.190	Rise	CLK1
9	PC_out[8]	CLK1	7.545	7.656	Rise	CLK1
10	PC_out[9]	CLK1	7.018	6.990	Rise	CLK1
11	PC_out[10]	CLK1	6.410	6.337	Rise	CLK1
12	PC_out[11]	CLK1	6.872	6.901	Rise	CLK1
13	PC_out[12]	CLK1	6.081	6.079	Rise	CLK1
14	PC_out[13]	CLK1	7.675	7.727	Rise	CLK1
15	PC_out[14]	CLK1	5.629	5.620	Rise	CLK1
16	PC_out[15]	CLK1	6.121	6.107	Rise	CLK1
17	PC_out[16]	CLK1	6.375	6.298	Rise	CLK1
18	PC_out[17]	CLK1	5.957	5.930	Rise	CLK1
19	PC_out[18]	CLK1	5.851	5.834	Rise	CLK1
20	PC_out[19]	CLK1	6.207	6.178	Rise	CLK1
21	PC_out[20]	CLK1	6.275	6.222	Rise	CLK1
22	PC_out[21]	CLK1	6.376	6.333	Rise	CLK1
23	PC_out[22]	CLK1	5.766	5.783	Rise	CLK1

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
24	PC_out[23]	CLK1	5.974	5.946	Rise	CLK1
25	PC_out[24]	CLK1	6.137	6.093	Rise	CLK1
26	PC_out[25]	CLK1	6.029	6.029	Rise	CLK1
27	PC_out[26]	CLK1	6.162	6.100	Rise	CLK1
28	PC_out[27]	CLK1	6.439	6.428	Rise	CLK1
29	PC_out[28]	CLK1	7.276	7.428	Rise	CLK1
30	PC_out[29]	CLK1	6.051	6.034	Rise	CLK1
31	PC_out[30]	CLK1	6.050	6.017	Rise	CLK1
32	PC_out[31]	CLK1	6.068	6.037	Rise	CLK1