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# ENCODED BIT MULTIPLIER IN DIGITAL COMMUNICATION SYSTEMS



# MULTIPLIER

- A bit multiplier is a digital circuit or algorithm used to perform multiplication between two binary numbers.
- In a bit multiplier, the multiplication operation is typically performed using a series of AND and/or XOR gates.
- It operates on individual bits of the multiplicand and the multiplier, and produces the corresponding bits of the product.
- The basic principle is to multiply each bit of the multiplicand with each bit of the multiplier and generate partial products. These partial products are then added together to obtain the final product.

# WORKING PROCEDURE OF MULTIPLIER

1. Initialize the product as all zeros.
2. Start with the least significant bit (LSB) of the multiplier and multiply it with each bit of the multiplicand.
3. If the multiplier bit is 0, the corresponding partial product is zero.
4. If the multiplier bit is 1, the corresponding partial product is equal to the multiplicand.
5. Shift the partial products based on their position in the binary number (left shift for higher bits).
6. Add the shifted partial products to the product.
7. Repeat steps 2-6 for each bit of the multiplier, moving from the LSB to the most significant bit (MSB).

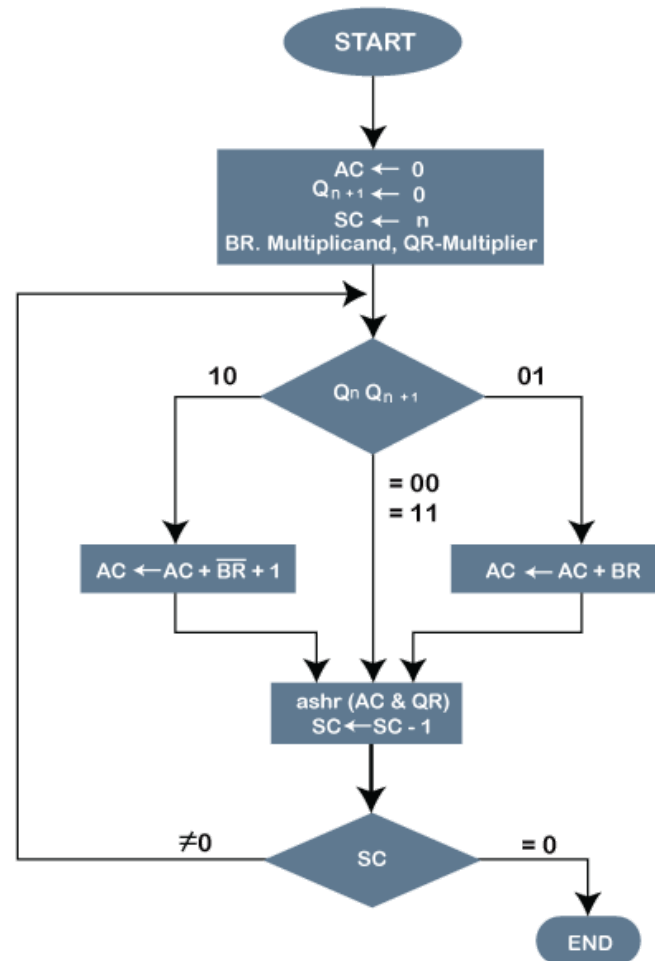
# GREATEST DISADVANTAGE OF BIT MULTIPLIER

- In a traditional unsigned binary multiplication, each bit of the multiplier is multiplied with each bit of the multiplicand, resulting in  $n$  partial products.
- The sum of these partial products gives the final product.
- However, this process requires a large number of additions and shifting operations, leading to increased complexity and longer multiplication times.

# BINARY BOOTH ENCODING

- Binary Booth Encoding addresses this issue by representing the multiplier in a redundant binary format, reducing the number of partial products required.
- Binary Booth Encoding is a technique used to optimize the performance of multiplication algorithms by reducing the number of partial products generated during the multiplication process.
- The encoding scheme takes advantage of the observation that consecutive 1s or 0s in the multiplier can be encoded with fewer partial products.
- The encoding is typically based on a signed-digit representation, such as two's complement encoding. In this encoding, a positive digit represents a regular multiplication, a zero digit represents no operation, and a negative digit represents subtraction of the multiplicand.

# BOOTH MULTIPLICATION ALGORITHM



# ADVANTAGES AND DISADVANTAGES

## ADVANTAGES

1. Reduced computational complexity
2. Faster multiplication
3. Hardware efficiency
4. Compatibility with Hardware description language

## DISADVANTAGES

1. Increased complexity of encoding
2. Limited applicability
3. Additional design constraint
4. Potential latency increase

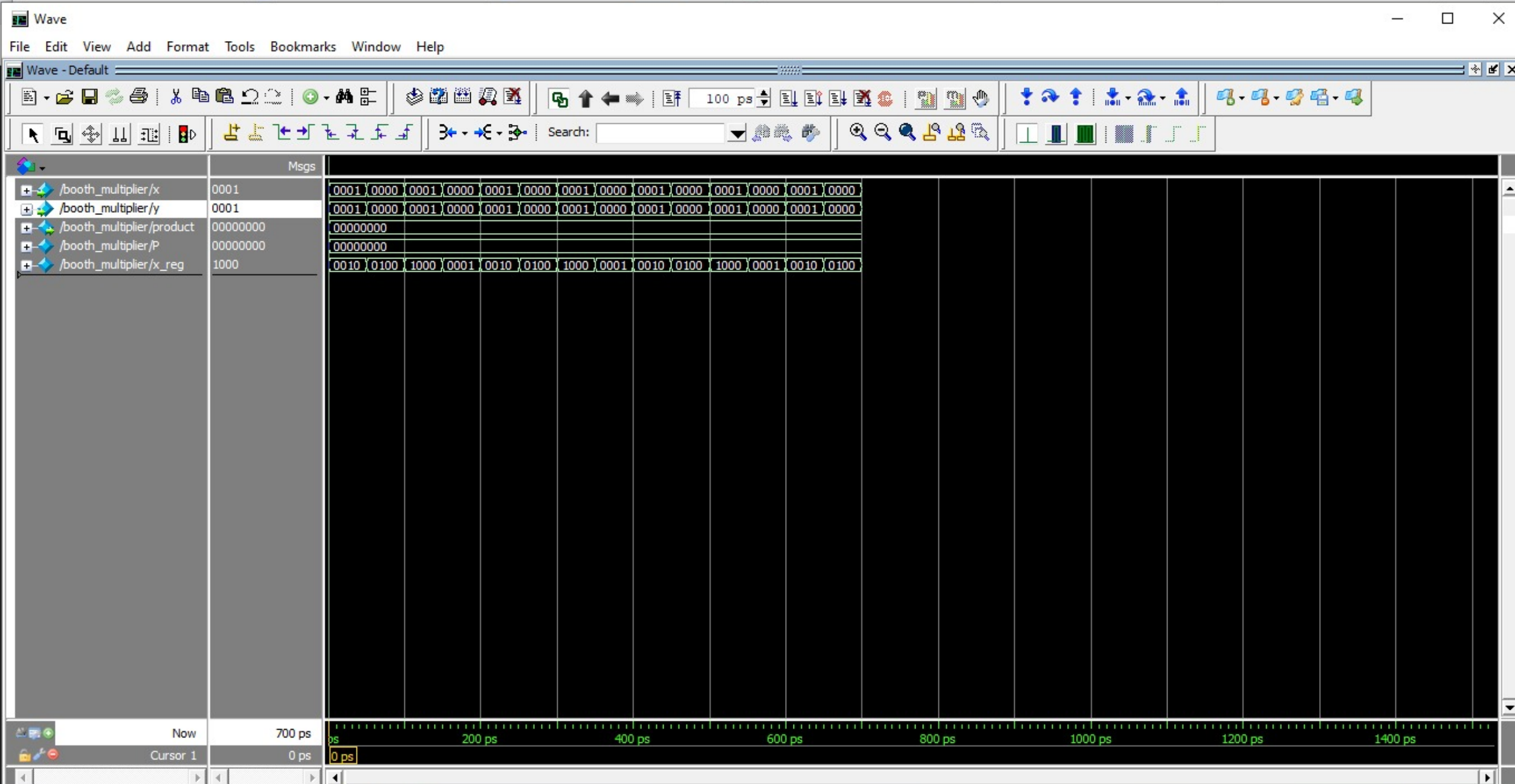
# APPLICATIONS

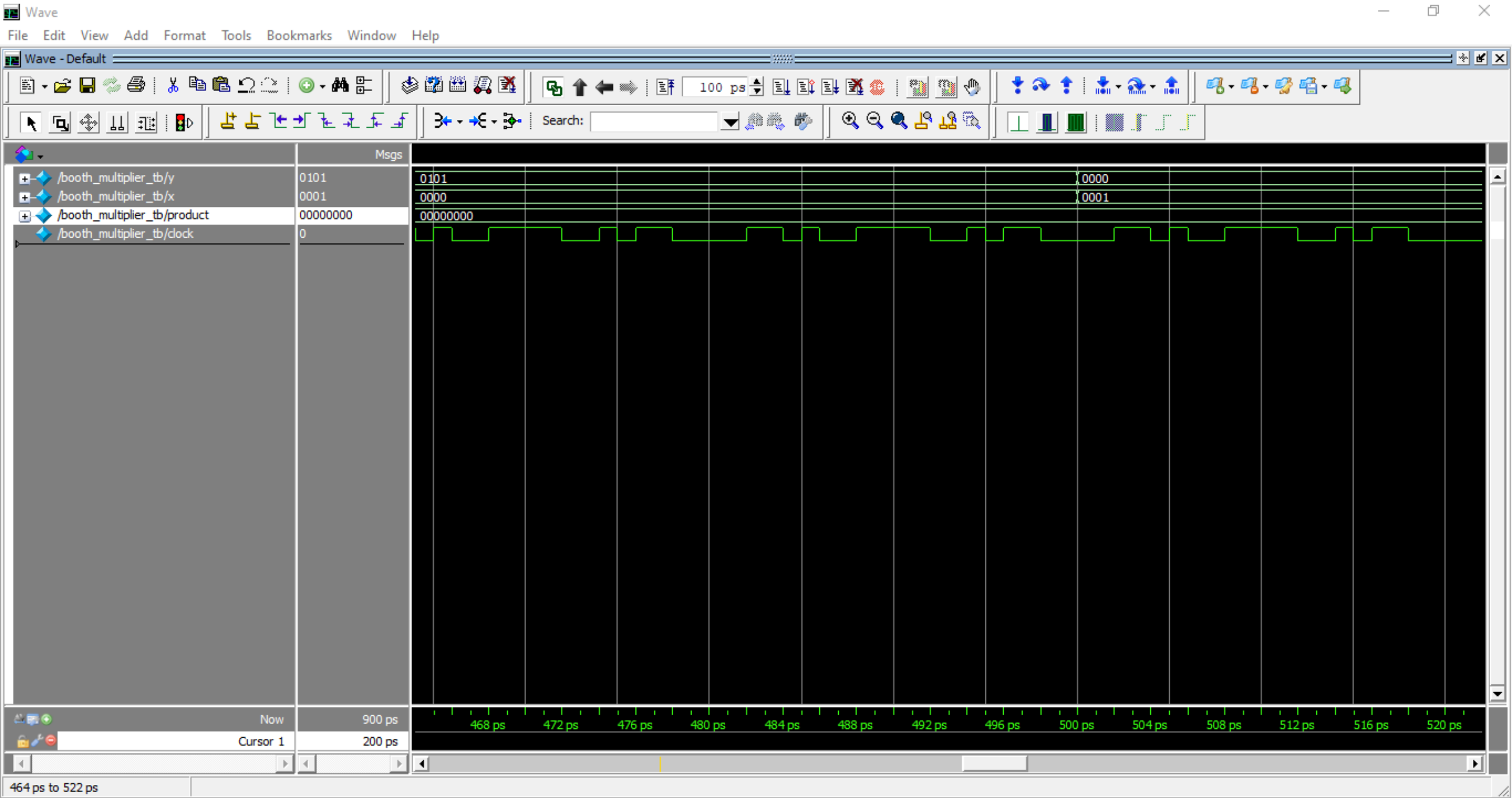
- Digital Signal Processing (DSP)
- Cryptography and Encryption
- Arithmetic Logic Units (ALU)
- Digital filters and equalisers
- Hardware accelerators
- High-performance computing



# WHY VERILOG

- Its suitability for hardware description and digital circuit design.
- Since a multiplier is a hardware component, Verilog is well-suited for expressing its functionality and behavior.
- Verilog supports gate-level modeling, allowing designers to describe the logical operations and circuitry of the multiplier using primitive gates, such as AND, OR, XOR, and others. This low-level modeling capability is essential for designing efficient and optimized digital circuits.
- While other programming languages, such as C or Python, could be used for algorithmic modeling and simulations, they are not typically used for low-level hardware design.







# THANK YOU

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