Power Efficient Synchronous Counter Design

Objectives:

- We present a power efficient design of synchronous counters with efficient clock gating technique with minimum hardware overhead.

- A new combinational logic with minimum hardware across each input of flip-flop is designed, which eliminates clock activity when flip-flop is not active, thereby reducing high clock load and therefore power consumption.

Introduction:

- Power efficient design of synchronous counters that reduces power consumption due to clock distribution for different flip-flops and offers high reliability.
- Most of the computer processes are synchronized with clock cycle, so sequential circuit has major contribution in many VLSI circuits.
- Major power contribution in counters is due to clock which has high load from its driving nets.
- This clock is always present across all flip flops which are not active, contributing large power overhead on designs.
- A simple combinational circuit is placed across the input of each flip-flop, which provides lower power consumption, with minimum area.

Abstract:

The Performance of any VLSI circuit depends on its design architecture, which optimizes power and provides high reliability. To design any circuit with low power, power optimization of circuit at different levels is needed. Most of the system level architectures consists of sequential circuits, design of these circuits plays a pivotal role in reducing overall power of the system. Counters are basic building blocks in many VLSI applications such as timers, memories, ADCs/DACs, frequency dividers etc. It is observed that design of counters has power overhead because of requirement of high power consumption for the clock signal distribution and undesired activity of flip-flops due to presence of clocks. In this brief, we propose a power efficient design of synchronous counters that reduces the power consumption due to clock distribution for different flip-flops and offers high reliability. The proposed counter design is evaluated and analyzed in terms of power in a standard 45 nm CMOS technology in CADENCE and also evaluated in Synopsys Design Compiler and IC Compiler for ASIC (Application Specific Integrated Circuit) synthesis results. The proposed counter design has lower power requirement and power-area product than existing counter architectures and the power reduction is more significant for wide-bit counters.

Highlights of the proposed method:

•Most of the computer processes are synchronized with clock cycle, so sequential circuit has major contribution in many VLSI circuits

•The area of the binary counter and up-down counter using proposed methodology is increased on an average of 4.76% for different bit widths due to the area consumed by the proposed clock gating network when compared to conventional

•For instance the power consumption for 8-bit Up-Down counter is reduced by 47.75% whereas area increased by 5.76% when compared to conventional design

•We present a new clock gating network for the implementation of power efficient synchronous counters

•A simple combinational circuit is placed across the input of each flip-flop, which provides lower power consumption, with minimum area

•The power reduction using proposed methodology will be more significant when the design extended to wide bit widths and with increased bandwidth of operation. It can be inferred that the power consumption in up-down counter is reduced by 30.7%, 42.34%, 47.75% for 4,6,8 bit widths respectively

•The proposed counter has substantial improvement on power reduction and the gain will be exponential when counter is extended for wide-bits

Conventional Binary Counter Design:

There are many different ways to design counters, among them JK flip-flops in master-slave mode (J and K connected to 1) is used widely since JK flip-flops in master-slave mode (Toggle flip-flop) offer a way to toggle only once for clock pulse, which is the fundamental function in order to build a counter.
For k-bit counter design, we need ‘k’ number of flip-flops.
The idea on which synchronous binary counter design is based on the following: the first flip-flop must change in every positive edge and invert its output.
The second flip-flop should be inverted every time the output of the first flip-flop has a negative edge, so output of the first flip-flop is connected to the input of subsequent flip-flop.
For the fourth flip-flop, when all three previous flip-flops output is 1, there is a need to invert the output.
The output of that AND gate controls the fourth flip-flops input

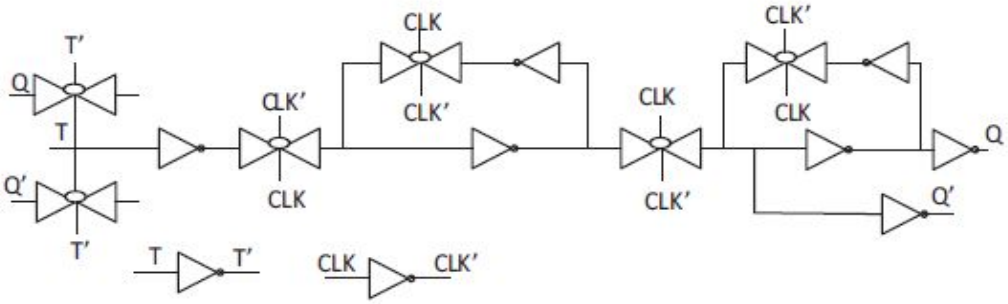


Fig. 1. T flip-flop.

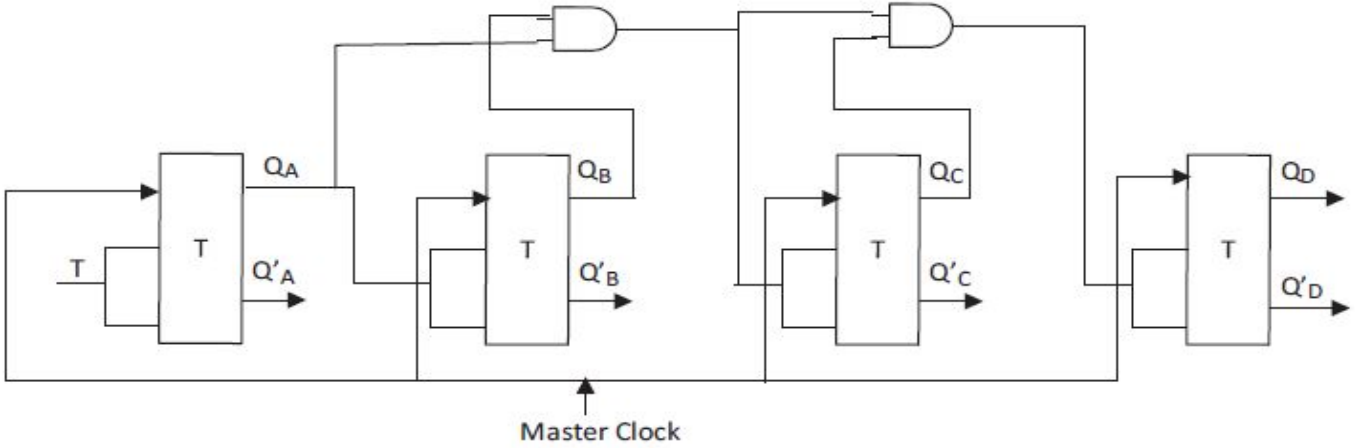
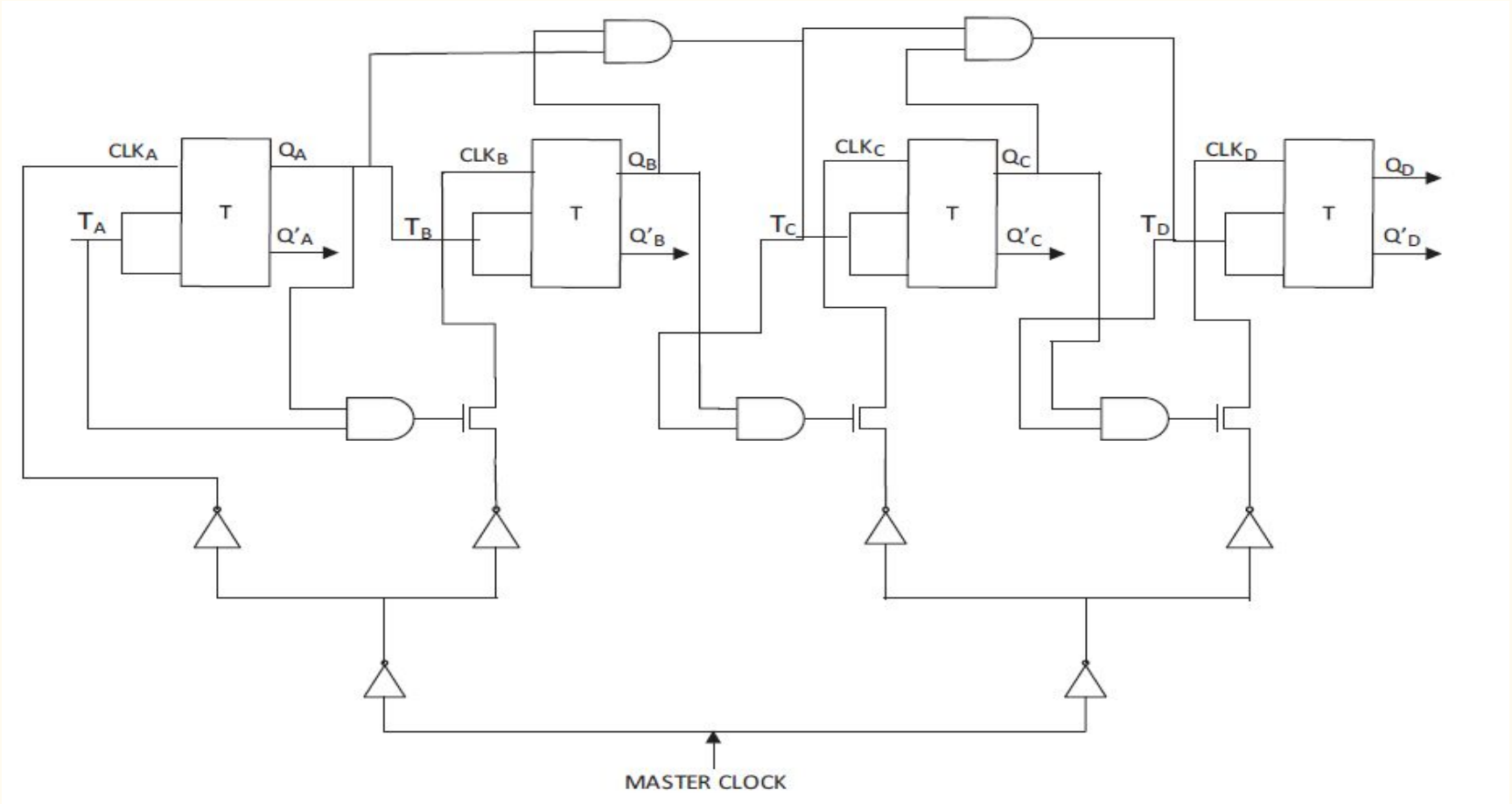


Fig. 2. Synchronous 4-bit binary counter.

Proposed binary counter design:

- We propose a power efficient design of synchronous counter with minimum hardware overhead.
- The proposed design of counter employs a new efficient combinational logic for clock gating based on a simple AND gate and a control transistor.
- Unlike conventional binary counter design, here the master clock to all flip-flops are driven by a new combinational logic.
- The master clock is driven by a control transistor (MOS transistor) which is activated only when precedent flip-flops goes high.
- For wide bit counters, we can adopt clock gating network at each level inside clock buffer network, further optimizing power in clock buffer network
- This has advantage in terms of least power consumption at clock buffer network, by placing a proposed combinational logic, which controls the master clock further down the level, depending on the activity of flip-flops.
- The proposed counter design has three-fold advantage, in terms of optimizing power by eliminating the unwanted clock activity at flip-flops, reduced power consumption in clock buffer network and minimizes the hardware overhead in clock buffer network contrary to the expense of power, complexity and cost using existing clock gating techniques

Proposed 4-bit binary counter design



Proposed 6-bit binary counter design

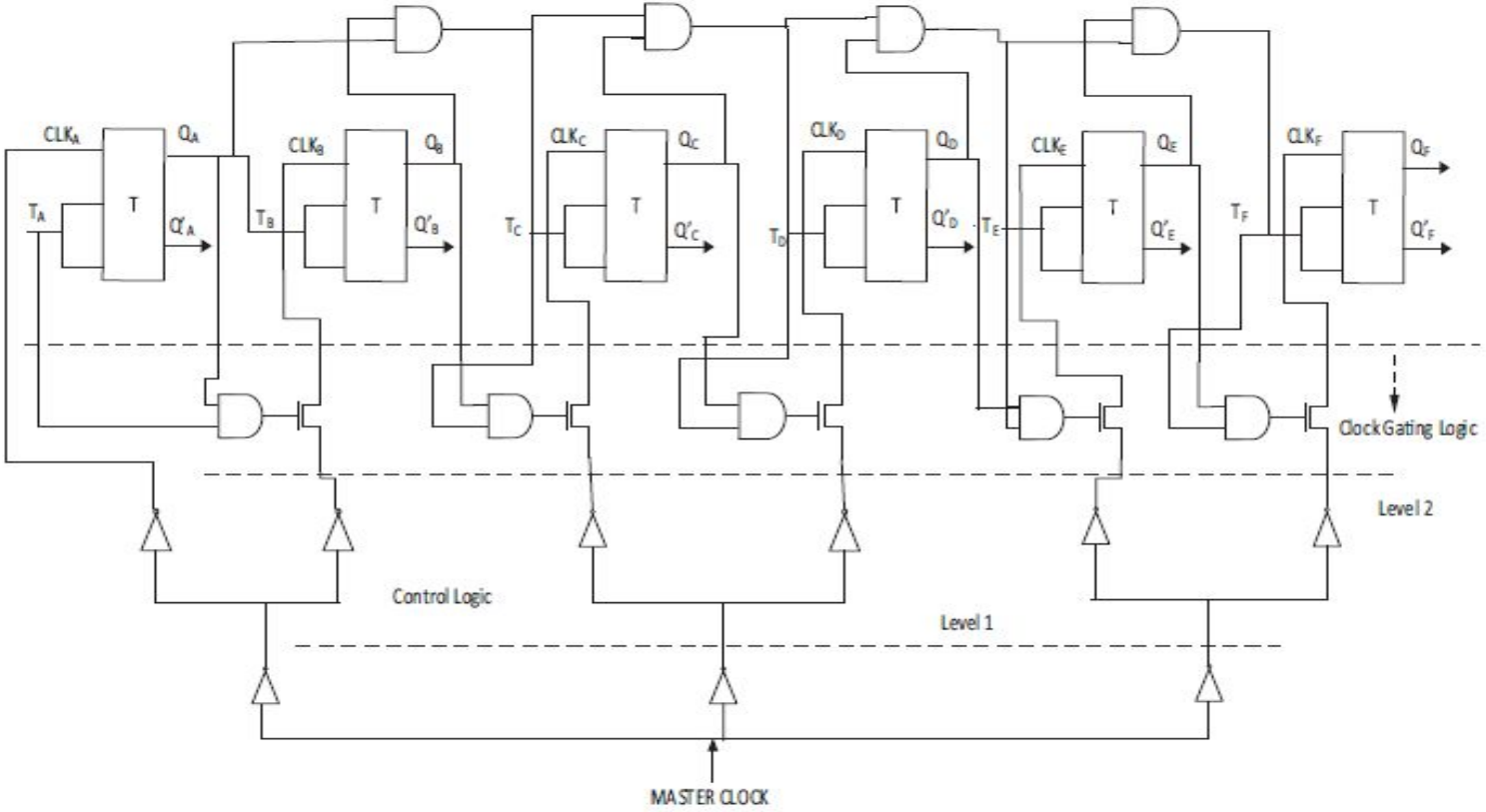


Fig. 4. Proposed 6-bit binary counter design

Truth table for the proposed design:

Table 1
Flip-flop active transitions for 4-bit.

Output transition	FF's active
0000	1
0001	2
0010	1
0011	3
0100	1
0101	2
0110	1
0111	4
1000	1
1001	2
1010	1
1011	3
1100	1
1101	2
1110	1
1111	4

Table 2
Truth table for the proposed binary counter.

Clock at FF's				Input at FF's				FF's output			
C1kA	ClkB	ClkC	ClkD	TA	TB	TC	TD	QA	QB	QC	QD
1	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	0	0	1	0	0	0
1	0	0	0	1	0	0	0	0	1	0	0
1	1	1	0	1	1	1	0	1	1	0	0
1	0	0	0	1	0	0	0	0	0	1	0
1	1	0	0	1	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0	1
1	1	0	0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0	1	0	1
1	1	1	0	1	1	1	0	1	1	0	1
1	0	0	0	1	0	0	0	0	0	1	1
1	1	0	0	1	1	0	0	1	0	1	1
1	0	0	0	1	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1

Equations for 4 bit binary counter design:

The clock equations for proposed 4-bit binary counter design are as below.

$$\text{Clk } 2 = \text{T } 1 \text{ .Q } 1 \qquad (1)$$

$$\text{Clk } 3 = \text{T } 2 \text{ .Q } 2 \qquad (2)$$

$$\text{Clk } 4 = \text{T } 3 \text{ .Q } 3 \qquad (3)$$

$$\text{T i} + 1 = \text{Q i .Q i} - 1 \qquad (4)$$

This basic proposed design can be extended to wide-bit counter design, which gives more substantial gain in terms of power consumption.

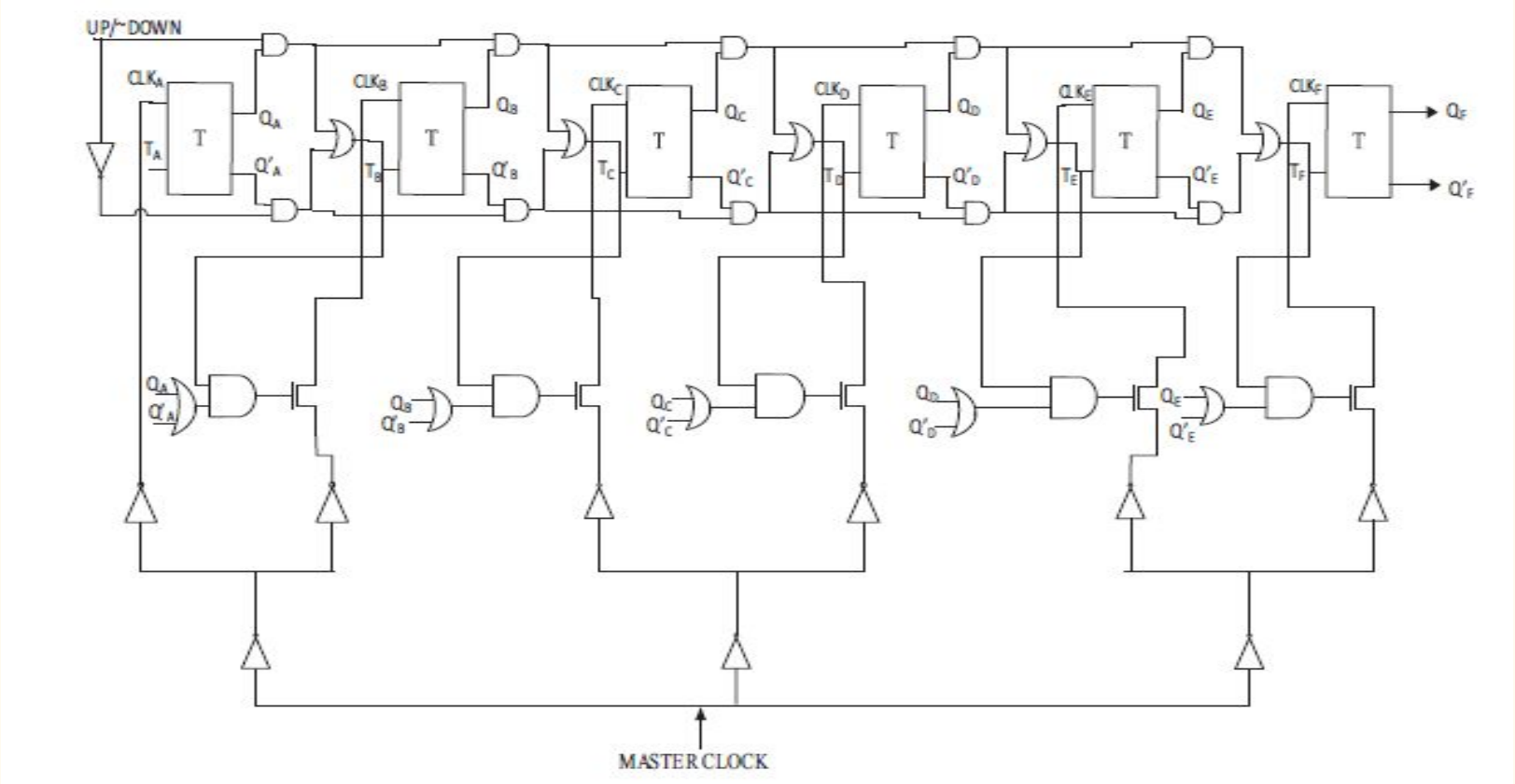
Thus, the proposed counter design has three-fold advantage, interms of optimizing power by eliminating the unwanted clock activity at flip-flops, reduced power consumption in clock buffer network and also minimizes the hardware overhead in clock buffer network contrary to the expense of power, complexity and cost using existing clock gating techniques.

Proposed up-down counter design:

Here we extend the 6-bit binary counter to implement the up-down count modes. The rationale behind implementing 6-bit up-down counter is to estimate the design overhead when compared to proposed binary counter design

It can be seen that the proposed up-down counter design has “up”and “down”count modes which consists of two independent paths of AND gates detecting the relevant bit conditions. The use of OR gates is to combine the AND gate outputs and fed to the input of each succeeding ‘T’ flip-flop. The Up-Down enable signal allows to activate either the upper or lower AND gate paths to allow the Q or Q’ outputs to the succeeding stages of T flip-flops.

Proposed 6 bit up down counter design:



Equations for the 6 bit proposed up down counter:

Clk B = T B . (Q A + Q A)

T B = UP.Q A + DOW N .Q A (5)

Clk C = T C . (Q B + Q B)

T C = UP.Q A .Q B + DOW N .Q A .Q B (6)

Clk D = T D . (Q C + Q C)

T D = UP.Q A .Q B .Q C + DOW N .Q A .Q B .Q C (7)

Clk E = T E . (Q D + Q D)

T E = UP.Q A .Q B .Q C .Q D + DOW N .Q A .Q B .Q C .Q D (8)

Clk F = T F . (Q E + Q E)

T F = UP.Q A .Q B .Q C .Q D .Q E + DOW N .Q A .Q B .Q C .Q D .Q E (9)

- Q A is the output of least significant T flipflop;
- T A , Clk A are inputs to least significant T flipflop;
- Q F is the output of most significant T flipflop;
- T F , Clk F are inputs to most significant T flipflop.

Similarly the generalized clock activation and input for an n-bit up-down counter using proposed technique is given as below.

$$Clk\ n = T\ n\ .\ (Q\ n - 1 + Q\ \ n - 1\ )$$

$$\mathbf{T\ n = UP.\ n\ \ i = 1\ Q\ i + DOW\ N\ \ .\ n\ \ j = 1\ Q\ \ j\ (10)}$$

The proposed design scheme has its main advantage in reducing the power consumed by the clocking network. It is ob- served that clock network in counter designs uses almost 35% of the circuit power.

Performance comparison:

It can be seen that power reduction for binary counter using proposed methodology is 21.5% 32.92% , 39.22% for 4,6,8 bit widths respectively.

The power reduction using proposed methodology will be more significant when the design extended to wide bit widths and also with increased bandwidth of operation. The power consumption in up-down counter is reduced by 30.7% , 42.34% , 47.75% for 4,6,8 bit widths respectively.

The area of the binary counter and up-down counter using proposed methodology is increased on an average of 4.76% for different bit widths due to the area consumed by the proposed clock gating network when compared to conventional.

However this negative gain interms of area is very less when compared to positive power gain. For instance the power consumption for 8-bit Up-Down counter is reduced by 47.75% whereas area increased by 5.76% when compared to conventional design.

Conclusion:

A new clock gating network for power-efficient synchronous counters is designed. The proposed counter has substantial improvement on power reduction and the gain will be exponential when counter is extended for wide-bits. The design shows substantial power improvement when the proposed counter is applied to the digital block of a Successive Approximation Register (SAR). The efficiency of the proposed counter design is supported by simulation results, validating its effectiveness in reducing power consumption.