**AN OPEN-SOURCE RRAM COMPILER**

|  |  |
| --- | --- |
| **SAIPRANAV K** | **21BEC1207** |
| **SANTHOSH KUMAR S** | **21BEC1283** |

A project report submitted to

**Dr. Velmathi G**

**SCHOOL OF ELECTRONICS ENGINEERING**

in partial fulfillment of the requirements for the course of

**BECE303L – VLSI SYSTEM DESIGN**

in

**B.Tech. Electronics and Communication Engineering**



**VIT CHENNAI**

**Vandalur-Kelambakkam Road**

**Chennai – 600127**

**April 2023**

# BONAFIDE CERTIFICATE

Certified that this project report entitled “**AN OPEN-SOURCE RRAM COMPILER**” is a bonafide work of **SAIPRANAV (21BEC1207)** and **SANTHOSH KUMAR (21BEC1283)** who carried out the project work under my supervision and guidance.

**Dr. Velmathi G**

Professor-Higher Academic Grade

School of Electronics Engineering (SENSE),

VIT Chennai

Chennai-600127.

# ABSTRACT

This project focuses on the design and implementation of sense amplifier circuits and related controllers for decoders in large-scale integrated systems (VLSI). The purpose of this project is to improve the efficiency and reliability of memory access in digital integrated circuits.

The initial phase of the project involved using Cadence, a popular electronic design automation (EDA) tool, to design the sense amplifier circuit.

The sense amplifier plays a vital role in improving the read stability and speed of the memory cells. The design process considered factors such as noise margin, power consumption and area utilization to optimize sense amplifier performance.

Further, a controller was designed to manage the selection of the Selector and

Decoder. The controller enables the decoding of address signals and efficient selection

of memory cells based on the desired operation.

# ACKNOWLEDGEMENT

We wish to express our sincere thanks and deep sense of gratitude to our project guide, Dr. Velmathi G, Professor Higher Academic Grade, School of Electronics Engineering, for his consistent encouragement and valuable guidance offered to us in a pleasant manner throughout the course of the project work.

We are extremely grateful to **Dr. Susan Elias,** Dean of the School of Electronics Engineering, VIT Chennai, for extending the facilities of the school towards our project and for her unstinting support.

We also take this opportunity to thank all the faculty of the school for their support and their wisdom imparted to us throughout the course.

We thank our parents, family, and friends for bearing with us throughout the course of our project and for the opportunity they provided us in undergoing this course in such a prestigious institution.

# TABLE OF CONTENTS

|  |  |  |  |
| --- | --- | --- | --- |
| **SNO** |  | **TOPIC** | **PAGE NO** |
| 1 |  | INTRODUCTION | `6 |
|  | 1.1 | OBJECTIVE AND GOALS | 6 |
|  | 1.2 | BENEFITS | 6 |
|  | 1.3 | FEATURES | 7 |
| 2 |  | RELATED WORKS | 8 |
| 3 |  | SENSE AMPLIFIER AND ITS INPUT STAGE |  |
|  | 3.1 | WORKING PRINCIPLE | 9 |
|  | 3.2 | BLOCK DIAGRAM | 10 |
|  | 3.3 | REQUIRED EQUIPMENT | 11 |
|  | 3.4 | SOFTWARE ANALYSIS | 12 |
|  | 3.5 | PROGRAM CODE | 13 |
|  | 3.6 | WORKING | 17 |
| 4 |  | RESULTS | 20 |
| 5 |  | LIMITATIONS | 23 |
| 6 |  | ADVANTAGES | 24 |
| 7 |  | APPLICATION | 25 |
| 8 |  | FUTURE SCOPE | 26 |
| 9 |  | CONCLUSION | 27 |
| 10 |  | REFERENCES | 28 |

# 1.INTRODUCTION

## OBJECTIVES AND GOALS

The primary goal of this project is to design and implement an efficient and reliable sense amplifier circuit and controller for the decoder in VLSI systems. The project aims to enhance the performance of memory access operations, improving read stability and speed.

## 1.2 BENEFITS

* Improved memory access performance
* Enhanced noise margin for accurate data retrieval
* Reduced power consumption for energy-efficient operation
* Increased data throughput for handling larger volumes of data
* Enhanced system reliability through proper timing synchronization
* Faster and more reliable memory access operations
* Minimized risk of data corruption
* Balanced performance and power efficiency
* Efficient communication between memory cells and the decoder

## 1.3 FEATURES

1. Sense Amplifier Circuit: The project involves the design and implementation of a sense amplifier circuit that improves the read stability and speed of memory cells. Key features of this circuit may include noise margin optimization, power consumption reduction, and efficient signal amplification.
2. Input Stage: An input stage is designed to interface with the memory cells, ensuring proper signal conditioning and amplification for reliable data retrieval. This stage may feature impedance matching, signal integrity optimization, and voltage level adjustment capabilities.
3. Controller: A controller is designed to manage the selection of the decoder and word column decoder. This component facilitates precise timing synchronization between the sense amplifier, decoder, and word column decoder, minimizing delays and ensuring efficient memory cell selection.
4. CADENCE Design: The project utilizes Cadence, an EDA tool, for designing and simulating the sense amplifier circuit, input stage, and controller. CADENCE provides a comprehensive environment for designing and verifying VLSI circuits.

# 2. RELATED WORKS

[1] Y. Chen, “ReRAM: History, status, and future,” IEEE Transactions on

Electron Devices, vol. 67, no. 4, pp. 1420–1433, 2020, [Online].

[2] Y. Xu et al., “A flexible embedded SRAM IP compiler,” in 2007 IEEE

ISCAS. IEEE, 2007, pp. 3756–3759, [Online].

[3] M. R. Guthaus et al., “Openram: An open-source memory compiler,” in

2016 IEEE/ACM ICCAD. IEEE, 2016, pp. 1–6, [Online].

[4] T. Shah et al., “FabMem: A multiported RAM and CAM compiler for

superscalar design space exploration.” 2010, [Online].

[5] S. Wu et al., “A 65nm embedded low power SRAM compiler,” in 13th

IEEE Symposium on DDECS. IEEE, 2010, pp. 123–124, [Online].

[6] R. Goldman et al., “Synopsys’ educational generic memory compiler,”

in 10th EWME. IEEE, 2014, pp. 89–92, [Online].

# 3. SENSE AMPLIFIER AND ITS INPUT STAGE

## 3.1 BRIEF DESCRIPTION OF WORKING PRINCIPLE

1. **Sense Amplifier Circuit:**

* The sense amplifier circuit is responsible for improving the read stability and speed of memory cells.
* It operates by sensing and amplifying the small voltage differences produced by the memory cells during the read operation.
* The circuit consists of differential amplifiers and feedback mechanisms to ensure accurate and reliable data retrieval.
* It compares the voltage levels of the memory cell outputs and amplifies the voltage difference to obtain a robust and stable output signal.

1. **Input Stage:**

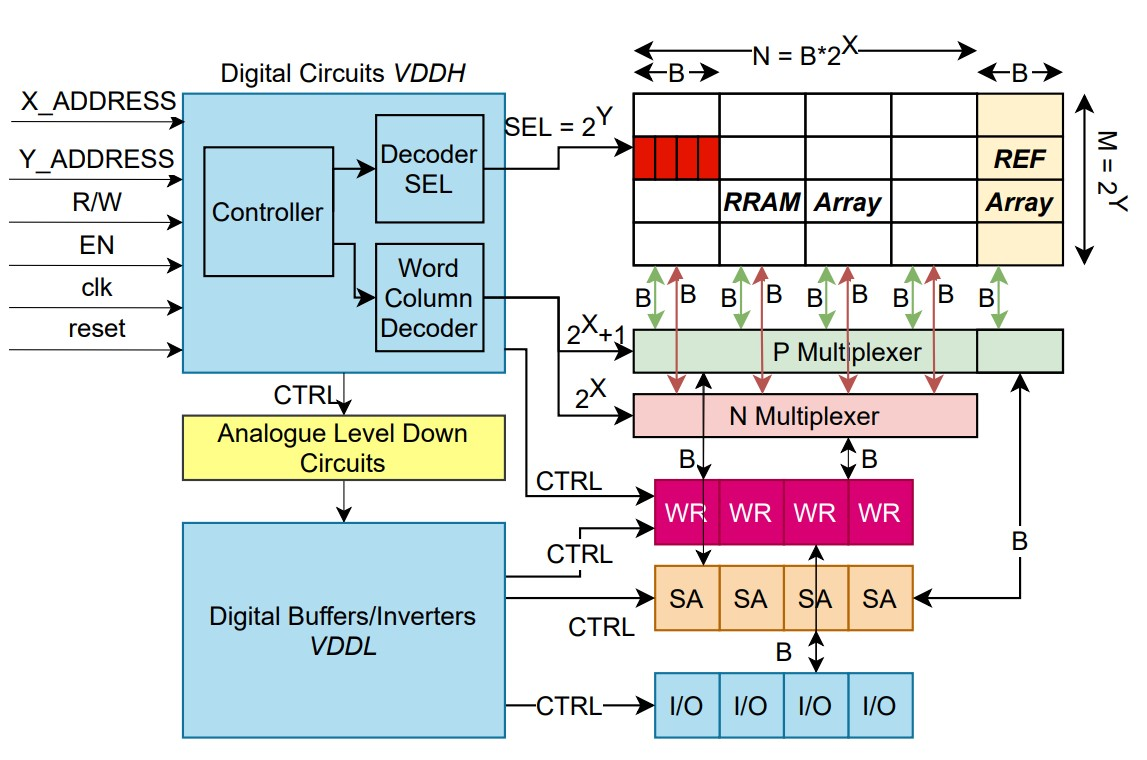
* The input stage interfaces with the memory cells and prepares the incoming signals for further processing.
* It ensures proper signal conditioning, amplification, and level shifting to match the requirements of the sense amplifier circuit.
* The input stage may include various components such as level shifters, preamplifiers, and buffers to achieve efficient signal transfer and compatibility.

1. **Controller:**

* The controller plays a crucial role in managing the selection of the decoder and word column decoder.
* It receives address signals and controls the activation of specific decoders based on the desired memory cell selection.
* The controller ensures precise timing synchronization between the sense amplifier, decoder, and word column decoder to enable accurate data retrieval.

## 3.2 BLOCK DIAGRAM

The main features of the basic block diagram are:



**Figure 1**: Block Diagram

## 3.3 REQUIRED EQUIPMENT

### Software Specifications:

* CADENCE VIRTUOSO
* MODELSIM

## 3.4 SOFTWARE ANALYSIS

The software’s used for this project are: -

1. CADENCE VIRTUOSO

Cadence Virtuoso is a widely-used Electronic Design Automation (EDA) tool suite in the semiconductor industry. It provides a comprehensive set of features and capabilities for designing and verifying complex integrated circuits (ICs). With Virtuoso, engineers can efficiently design, simulate, and layout ICs, ensuring their functionality and performance.

Virtuoso offers a user-friendly environment for circuit design, simulation, and layout. It provides a schematic editor that allows engineers to create and modify circuit schematics, capturing the desired circuit functionality and electrical connectivity.

Simulation capabilities in Virtuoso enable engineers to verify the behavior and performance of their circuit designs. Various simulation types, such as transient analysis, DC analysis, AC analysis, and Monte Carlo analysis, are supported. Engineers can accurately analyze circuit responses under different operating conditions, ensuring reliability and robustness.

2. MODELSIM

ModelSim is a powerful simulation and verification tool used extensively in the field of digital electronics and FPGA (Field Programmable Gate Array) design. It offers a comprehensive set of features and capabilities for simulating and debugging digital designs, ensuring their functionality and correctness.

ModelSim provides a user-friendly simulation environment that supports various HDL (Hardware Description Language) formats, including VHDL and Verilog. Engineers can use these languages to describe and simulate complex digital circuits, allowing them to validate the behavior and functionality of their designs.

One of the key capabilities of ModelSim is functional simulation. It allows engineers to simulate the behavior of their digital designs under different test scenarios and inputs. This enables them to verify the correctness of the circuit and ensure it functions as intended.

**3.5 PROGRAM CODES**

### 3.5.1 MODELSIM VERILOG CODE:

module ControllerBlock (

input wire [7:0] x\_address,

input wire [7:0] y\_address,

input wire r\_w,

input wire en,

input wire clk,

input wire reset,

output wire [1:0] decoder\_SEL,

output wire [3:0] word\_column\_decoder

);

reg [1:0] decoder\_SEL\_reg;

reg [3:0] word\_column\_decoder\_reg;

reg [1:0] state;

// Define the states

localparam IDLE = 2'b00;

localparam WRITE = 2'b01;

localparam READ = 2'b10;

always @(posedge clk or posedge reset) begin

if (reset) begin

decoder\_SEL\_reg <= 2'b00;

word\_column\_decoder\_reg <= 4'b0000;

state <= IDLE;

end else begin

case (state)

IDLE: begin

if (en && r\_w) begin

// Transition to the WRITE state

state <= WRITE;

end else if (en && !r\_w) begin

// Transition to the READ state

state <= READ;

end else begin

// Remain in the IDLE state

state <= IDLE;

end

end

WRITE: begin

// Generate the necessary signals for write operation

decoder\_SEL\_reg <= 2'b01;

word\_column\_decoder\_reg <= {y\_address[7:4], x\_address[7:6]};

state <= IDLE; // Transition back to IDLE state

end

READ: begin

// Generate the necessary signals for read operation

decoder\_SEL\_reg <= 2'b10;

word\_column\_decoder\_reg <= {x\_address[7:6], y\_address[7:4]};

state <= IDLE; // Transition back to IDLE state

end

endcase

end

end

assign decoder\_SEL = decoder\_SEL\_reg;

assign word\_column\_decoder = word\_column\_decoder\_reg;

endmodule

TESTBENCH:

module ControllerBlock\_tb;

// Inputs

reg [7:0] x\_address;

reg [7:0] y\_address;

reg r\_w;

reg en;

reg clk;

reg reset;

// Outputs

wire [1:0] decoder\_SEL;

wire [3:0] word\_column\_decoder;

// Instantiate the ControllerBlock

ControllerBlock dut (

.x\_address(x\_address),

.y\_address(y\_address),

.r\_w(r\_w),

.en(en),

.clk(clk),

.reset(reset),

.decoder\_SEL(decoder\_SEL),

.word\_column\_decoder(word\_column\_decoder)

);

// Clock generation

always begin

#5 clk = ~clk;

end

// Stimulus

initial begin

// Initialize inputs

x\_address = 8'b00000000;

y\_address = 8'b00000000;

r\_w = 0;

en = 0;

reset = 1;

clk = 0; // Initialize clock to a specific value

// Reset

@(posedge clk);

reset = 0;

@(posedge clk);

// Test Case 1: Write operation

$display("Test Case 1: Write operation");

en = 1;

r\_w = 1;

@(posedge clk);

x\_address = 8'b01010101;

y\_address = 8'b10101010;

@(posedge clk);

$display("decoder\_SEL: %b", decoder\_SEL);

$display("word\_column\_decoder: %b", word\_column\_decoder);

// Test Case 2: Read operation

$display("Test Case 2: Read operation");

en = 1;

r\_w = 0;

@(posedge clk);

x\_address = 8'b11001100;

y\_address = 8'b00110011;

@(posedge clk);

$display("decoder\_SEL: %b", decoder\_SEL);

$display("word\_column\_decoder: %b", word\_column\_decoder);

// Test Case 3: No operation (idle state)

$display("Test Case 3: No operation (idle state)");

en = 0;

r\_w = 0;

@(posedge clk);

$display("decoder\_SEL: %b", decoder\_SEL);

$display("word\_column\_decoder: %b", word\_column\_decoder);

// Test Case 4: Write operation with different addresses

$display("Test Case 4: Write operation with different addresses");

en = 1;

r\_w = 1;

@(posedge clk);

x\_address = 8'b01110010;

y\_address = 8'b10100111;

@(posedge clk);

$display("decoder\_SEL: %b", decoder\_SEL);

$display("word\_column\_decoder: %b", word\_column\_decoder);

// Test Case 5: Read operation with different addresses

$display("Test Case 5: Read operation with different addresses");

en = 1;

r\_w = 0;

@(posedge clk);

x\_address = 8'b10101010;

y\_address = 8'b01010101;

@(posedge clk);

$display("decoder\_SEL: %b", decoder\_SEL);

$display("word\_column\_decoder: %b", word\_column\_decoder);

// End simulation

$finish;

  end

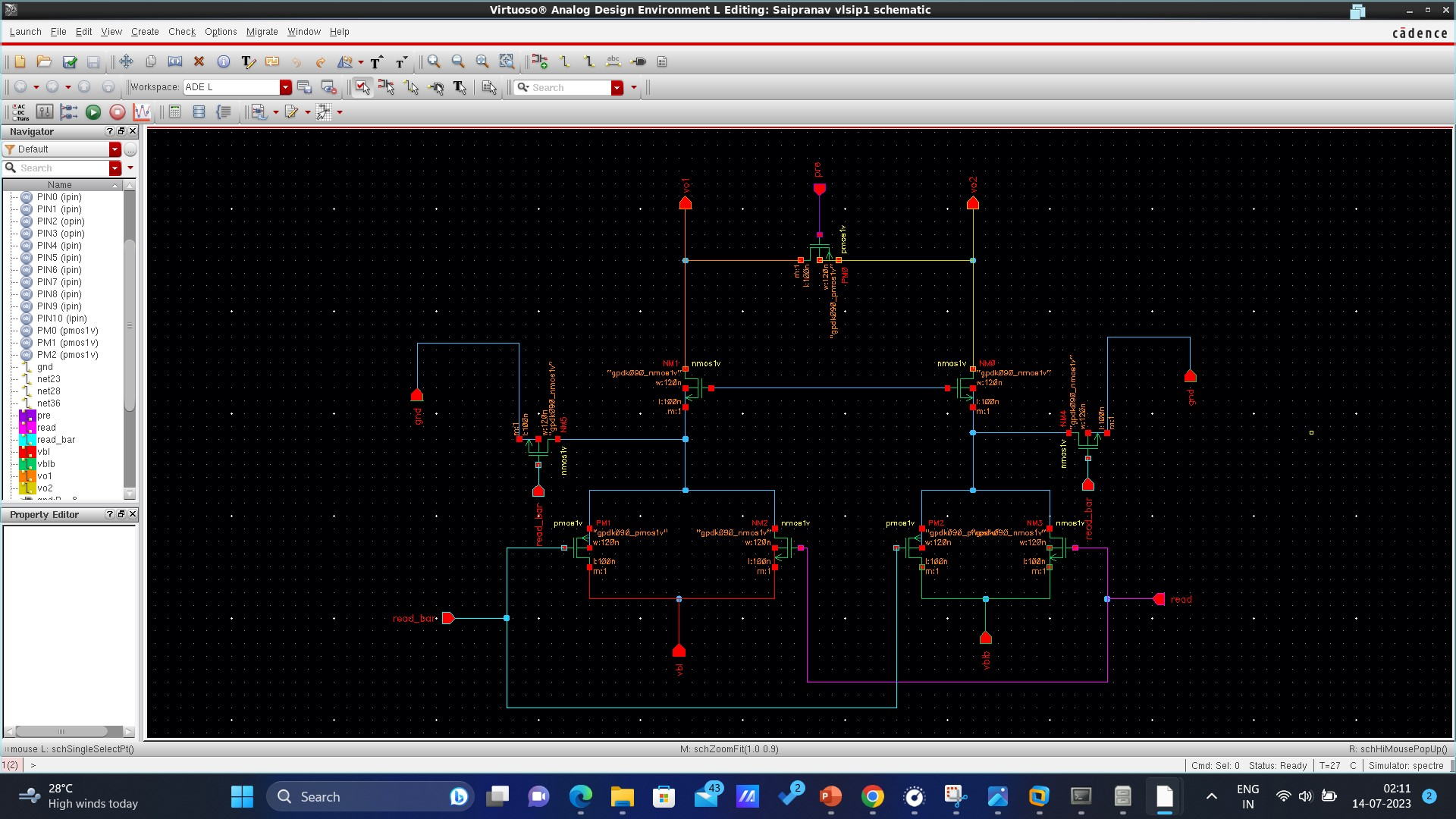
endmodule

## 3.6 How the system Works?

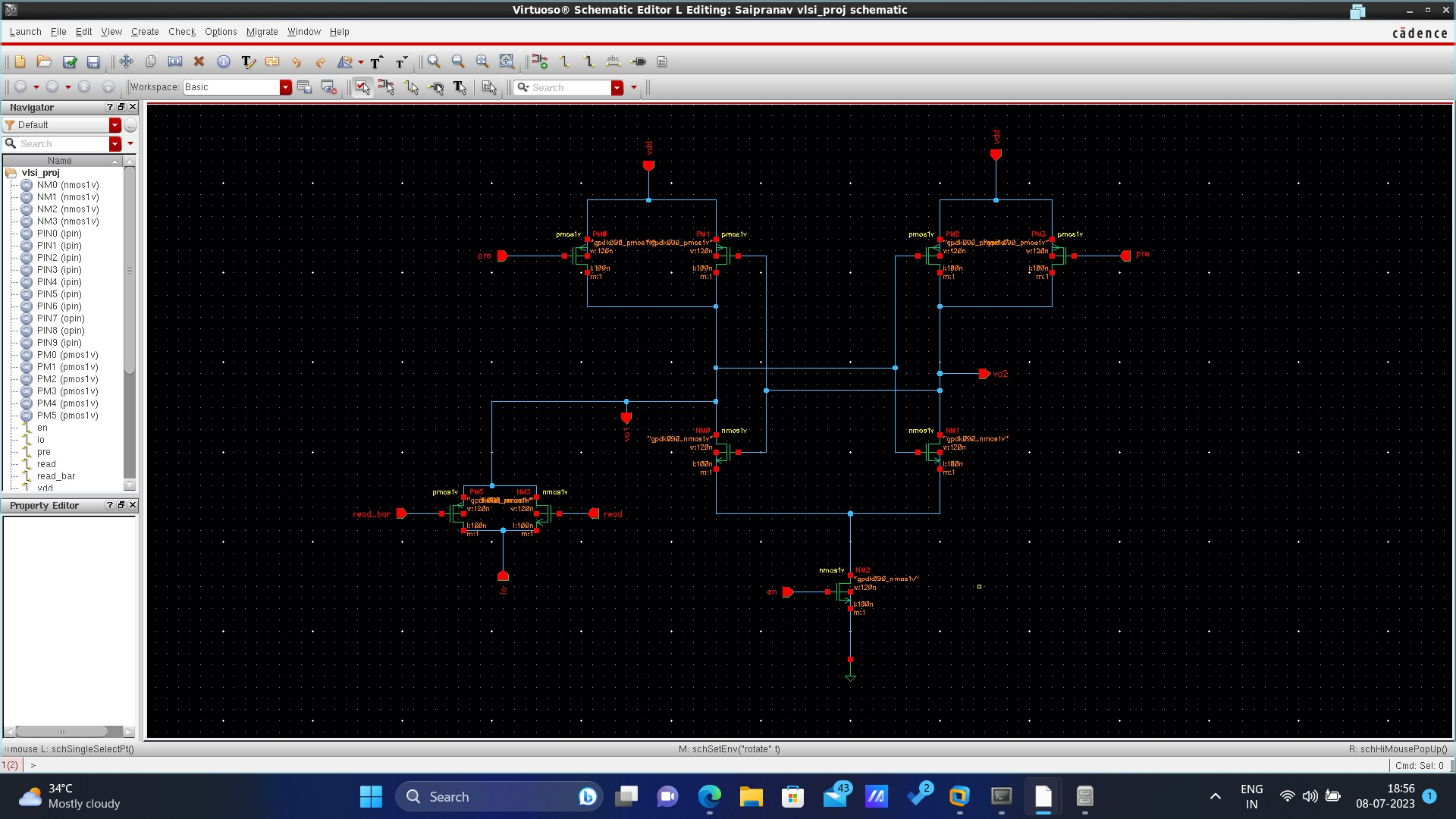
### 3.6.1 Working of the circuit

A cross-coupled sense amplifier circuit is a fundamental component used in memory applications to enhance the read stability and speed of memory cells. This circuit operates on the principle of positive feedback to amplify and detect small voltage differences. During a read operation, the circuit begins by precharging the bitlines to a known state. When the selected memory cell is activated, it causes one bitline to discharge while the other remains precharged, creating a voltage imbalance. The cross-coupled sense amplifier then amplifies this voltage difference through positive feedback, further strengthening the imbalance. As the voltage separation reaches a threshold, the circuit latches to one of the memory cell states based on the bitline voltage levels. This latched state represents the data read from the memory cell. By leveraging positive feedback and amplification, the cross-coupled sense amplifier ensures accurate detection and amplification of small voltage differences, resulting in improved read stability and faster memory access operations.

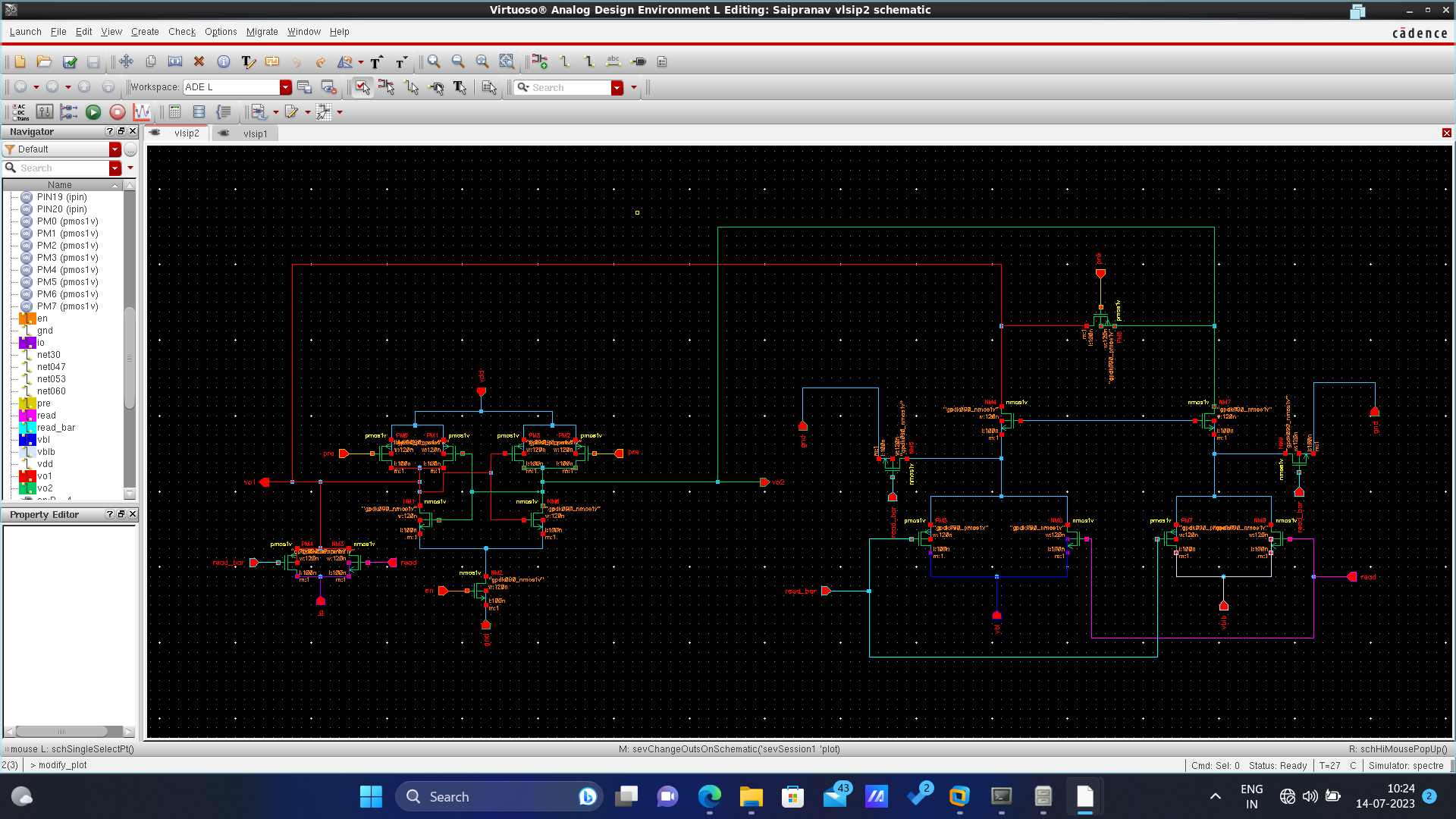
INPUT STAGE:



CROSS COUPLED SENSE AMPLIFIER:

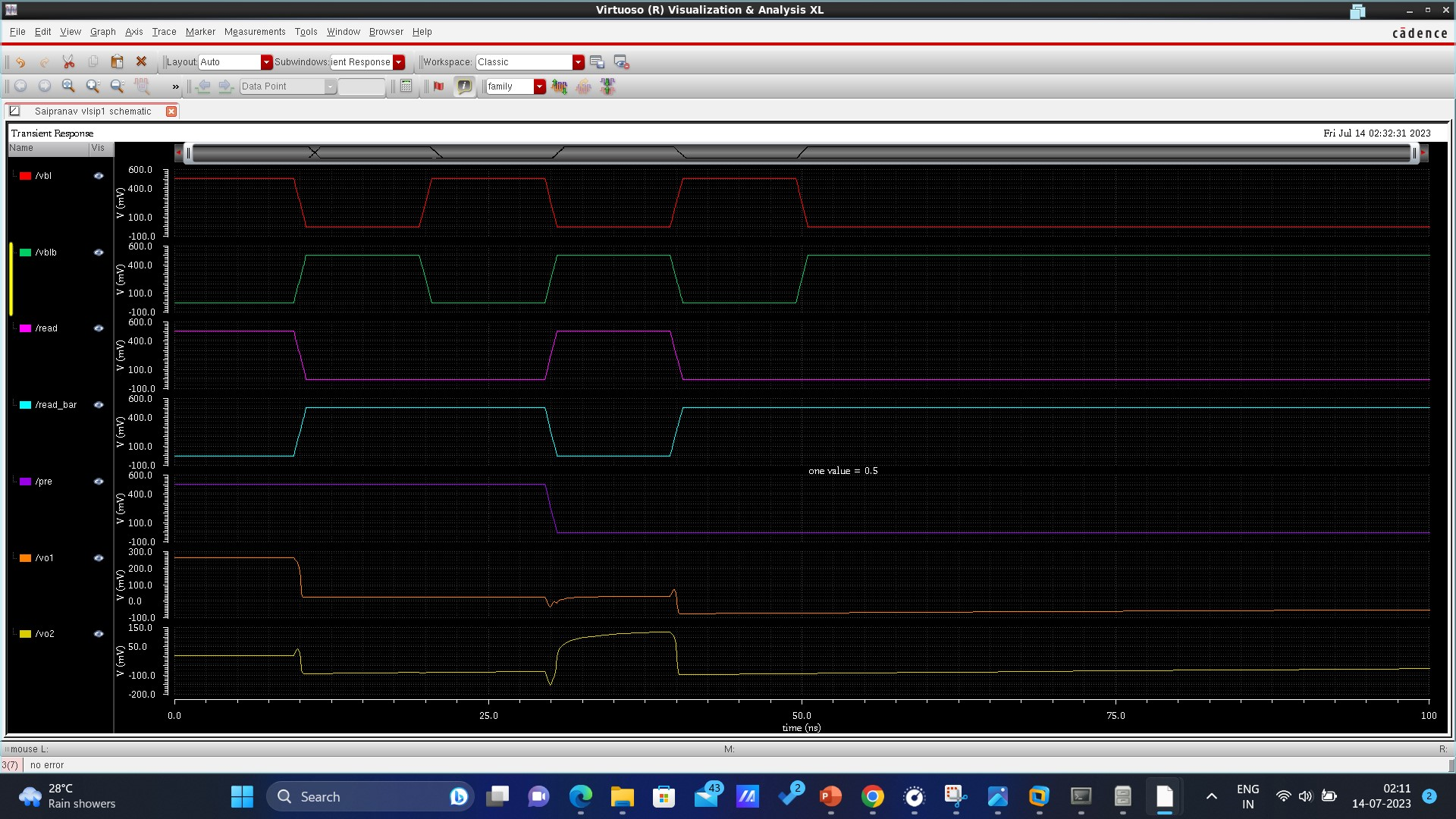


WHOLE CIRCUIT:

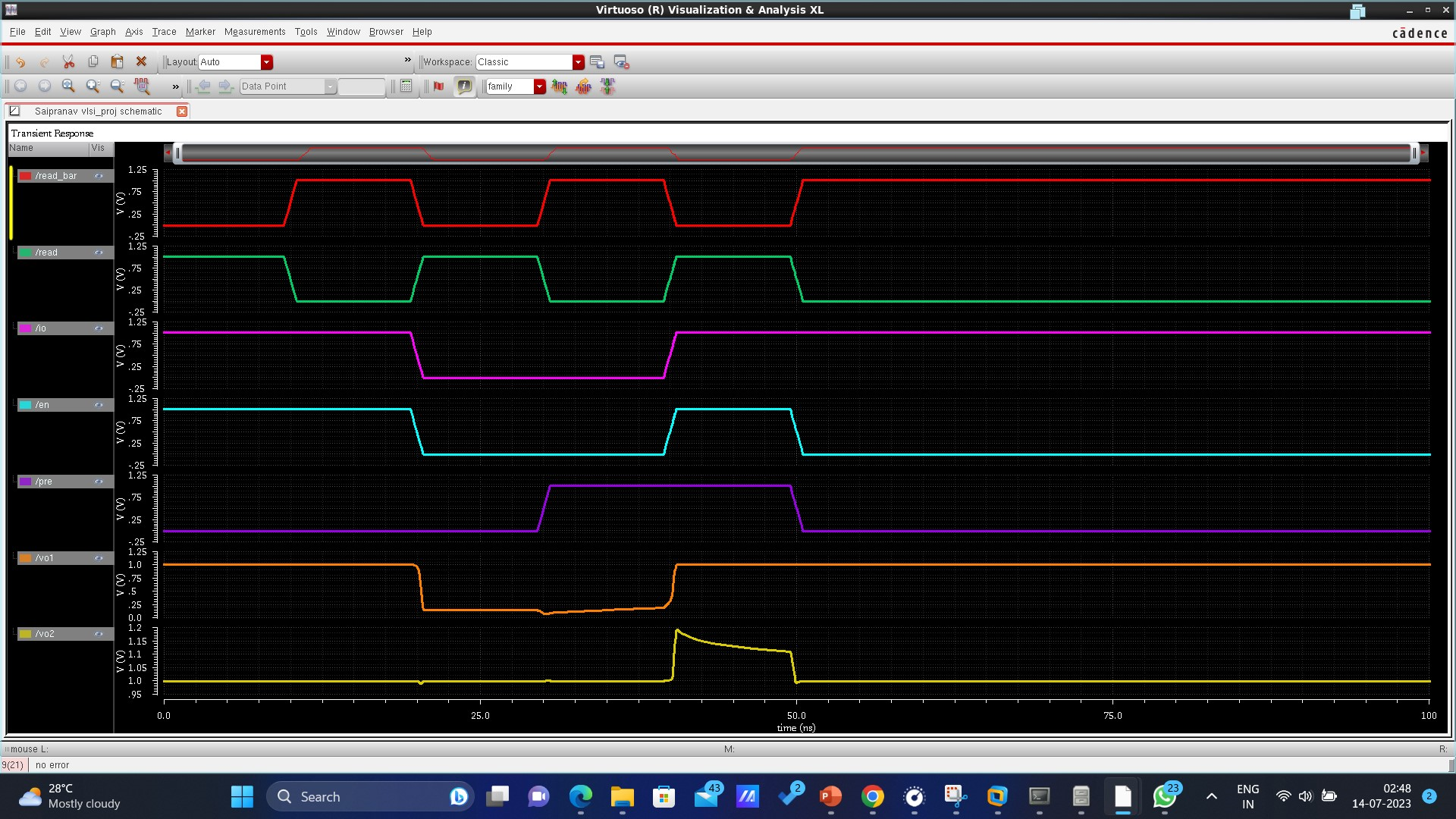


**4. RESULTS:**

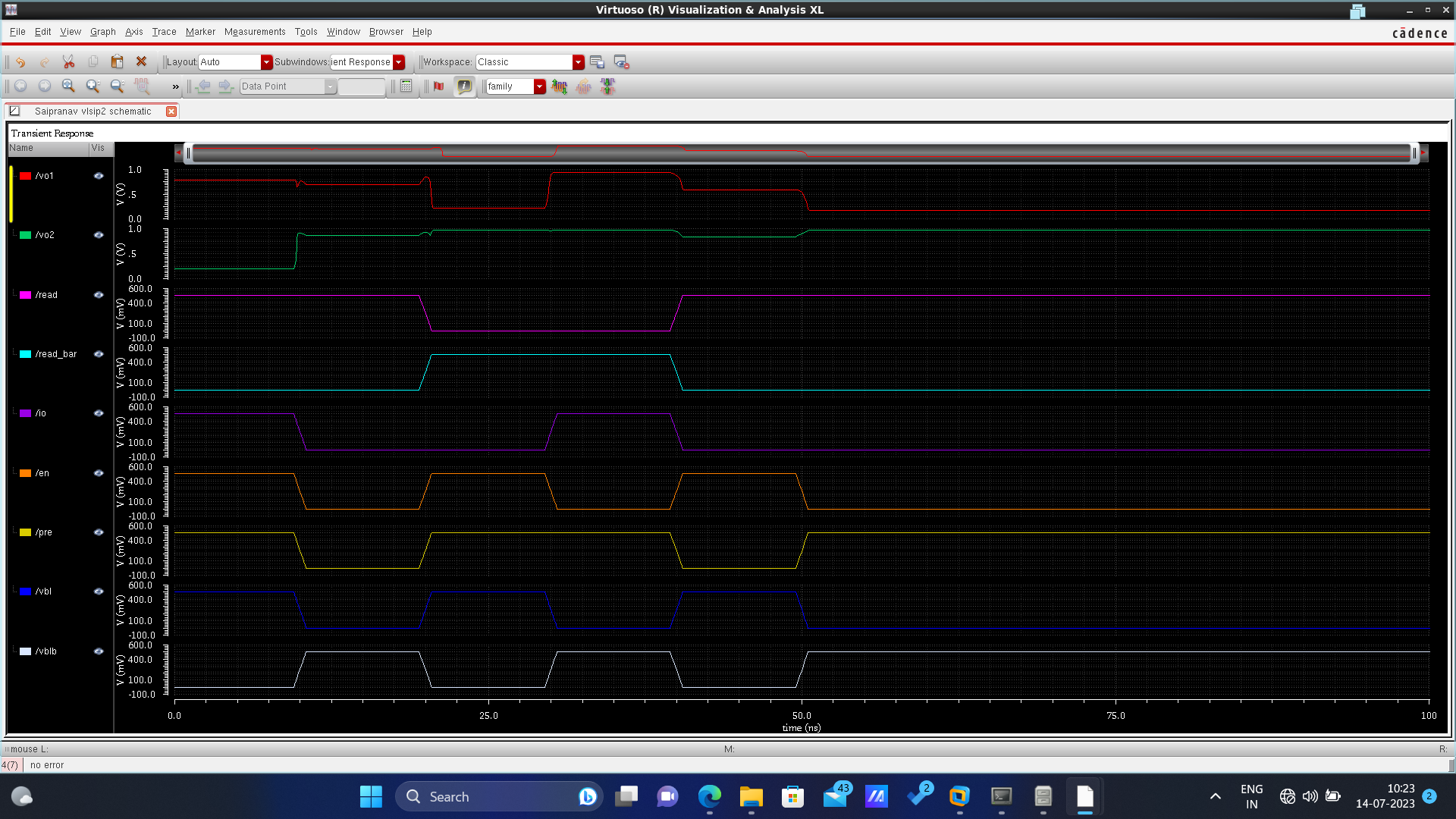
**INPUT STAGE:**



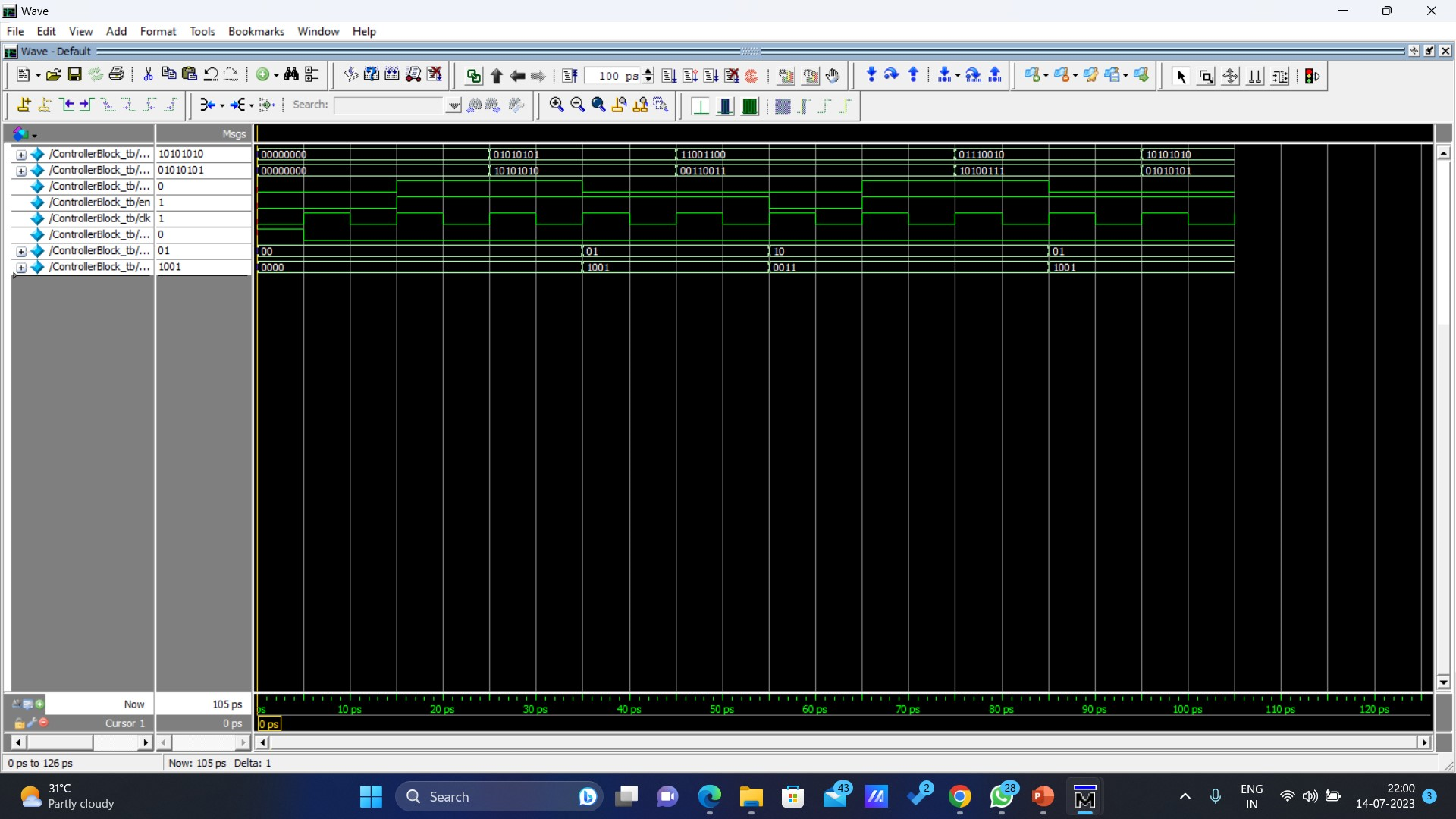
**CROSS COUPLED SENSE AMPLIFIER CIRCUIT:**



**WHOLE CIRCUIT:**



**VERILOG CODE OUTPUT:**



# 5. LIMITATIONS OF PROJECT CIRCUIT

1. **Sensitivity to Process Variations:** The performance of a cross-coupled sense amplifier circuit is highly sensitive to process variations during fabrication. Variations in transistor characteristics, such as threshold voltage or channel length, can impact the circuit's stability and overall performance.
2. **Voltage Noise Sensitivity**: Cross-coupled sense amplifiers are susceptible to voltage noise present on the bit lines. Noise can introduce false transitions or errors in the amplified voltage levels, leading to inaccurate data retrieval.
3. **Power Consumption:** The positive feedback mechanism used in the circuit contributes to increased power consumption. The continuous amplification and regeneration of signals require additional power, which can be a concern for low-power applications or systems with strict power constraints.
4. **Trade-off between Speed and Sensitivity:** There is a trade-off between the speed and sensitivity of a cross-coupled sense amplifier. While it provides faster operation by amplifying voltage differences, it may become more sensitive to noise and can be susceptible to false transitions or glitches in certain scenarios.

# 

# 6. ADVANTAGES:

1. **Improved Read Stability:** The positive feedback mechanism in the circuit enhances the stability of read operations. It amplifies small voltage differences, ensuring accurate detection and retrieval of data from memory cells, even in the presence of noise or signal degradation.
2. **Enhanced Read Speed:** By amplifying voltage differences, the cross-coupled sense amplifier circuit enables faster read operations. It reduces the time required to detect and latch the state of the memory cell, resulting in improved data access speed.
3. **Robustness to Process Variations:** Despite sensitivity to process variations being a limitation, the cross-coupled sense amplifier circuit can also exhibit robustness. The positive feedback mechanism can compensate for certain process variations, helping to maintain stable and reliable circuit performance.
4. **Reduced Sensitivity to Voltage Levels:** The circuit's design allows it to operate across a wide range of voltage levels, providing flexibility in different voltage domain environments.
5. **Compatible with Various Memory Cell Technologies:** The cross-coupled sense amplifier circuit is compatible with various memory cell technologies, including SRAM (Static Random-Access Memory) and DRAM (Dynamic Random-Access Memory). It can be adapted and optimized for different memory architectures and applications.

**7. APPLICATION**  
The cross-coupled sense amplifier circuit finds applications in various memory-intensive systems, particularly in the field of digital integrated circuits. Some of the key applications include:

1. **Static Random-Access Memory (SRAM):** The circuit is commonly used in SRAM designs as it improves the read stability and speed of memory cells, leading to reliable and fast data retrieval. SRAM is widely used in cache memories, registers, and other high-speed memory applications.
2. **Dynamic Random-Access Memory (DRAM):** The circuit is also employed in DRAM designs to enhance the read stability and speed. DRAM is used as the main memory in computers and other digital systems, and the cross-coupled sense amplifier contributes to efficient and reliable data access in DRAM arrays.
3. **Embedded Systems:** Embedded systems, such as microcontrollers and system-on-chip (SoC) designs, often utilize the cross-coupled sense amplifier circuit in on-chip memory components. It ensures reliable and fast access to memory cells, critical for the performance and functionality of embedded systems.
4. **Networking and Telecommunications:** In networking and telecommunications systems, where fast data processing and memory access are crucial, the circuit is employed to enhance the read stability and speed of memory cells in packet buffers, routers, and network switches.
5. **Consumer Electronics:** The circuit finds applications in various consumer electronic devices, such as smartphones, tablets, and gaming consoles, where efficient memory access is essential for smooth operation and fast data processing.

# 8. FUTURE SCOPE

1. **Increased Memory Density:** As memory technologies continue to evolve, the need for higher memory densities becomes crucial. The cross-coupled sense amplifier circuit can be optimized to support increased memory density by addressing challenges such as reduced noise margins and improved sensitivity to process variations.
2. **Low-Power Design:** Power efficiency is a critical concern in modern electronic devices. Future advancements in the cross-coupled sense amplifier circuit can focus on reducing power consumption without compromising read stability and speed. Techniques such as voltage scaling, adaptive biasing, and power gating can be explored to achieve low-power designs.
3. **Advanced Noise Immunity:** The circuit's sensitivity to noise can be further mitigated by incorporating advanced noise cancellation techniques. Future research may focus on the development of noise-tolerant architectures, signal filtering etc.
4. **Integration with Emerging Memory Technologies:** Emerging memory technologies, such as Resistive RAM (RRAM), Phase Change Memory (PCM), and Magnetic RAM (MRAM), offer potential alternatives to traditional memory technologies. Future developments of the cross-coupled sense amplifier circuit can explore its integration and optimization with these emerging memory technologies for improved performance and compatibility.
5. **Compatibility and Optimization for Hybrid Memory Systems:** Hybrid memory systems that combine different memory technologies to leverage their respective advantages are gaining attention. Future advancements in the cross-coupled sense amplifier circuit can focus on enabling seamless integration and efficient operation within hybrid memory architectures, optimizing performance and reliability.

# 9. CONCLUSION

* In conclusion, our project focused on the design and implementation of a cross-coupled sense amplifier circuit, an essential component in memory-intensive systems. The circuit's working principle, advantages, limitations, and future scopes were explored.
* The cross-coupled sense amplifier circuit demonstrated its ability to improve read stability and speed, enabling accurate data retrieval from memory cells. Its positive feedback mechanism and amplification capabilities contributed to enhanced circuit performance.
* While the circuit exhibited certain limitations such as sensitivity to process variations and voltage noise, future advancements can address these challenges. The future scopes of the circuit include increased memory density, low-power design, advanced noise immunity, integration with emerging memory technologies, compatibility with hybrid memory systems, and leveraging advancements in semiconductor process technologies.
* By understanding the principles and possibilities of the cross-coupled sense amplifier circuit, this project provides valuable insights for the development of memory systems in various applications. Further research and innovation in this field have the potential to enhance memory performance, efficiency, and reliability, driving advancements in the semiconductor industry and enabling the realization of more powerful and efficient electronic devices.

**10. REFERENCES**

[1] Y. Chen, “ReRAM: History, status, and future,” IEEE Transactions on

Electron Devices, vol. 67, no. 4, pp. 1420–1433, 2020, [Online].

[2] Y. Xu et al., “A flexible embedded SRAM IP compiler,” in 2007 IEEE

ISCAS. IEEE, 2007, pp. 3756–3759, [Online].

[3] M. R. Guthaus et al., “Openram: An open-source memory compiler,” in

2016 IEEE/ACM ICCAD. IEEE, 2016, pp. 1–6, [Online].

[4] T. Shah et al., “FabMem: A multiported RAM and CAM compiler for

superscalar design space exploration.” 2010, [Online].

[5] S. Wu et al., “A 65nm embedded low power SRAM compiler,” in 13th

IEEE Symposium on DDECS. IEEE, 2010, pp. 123–124, [Online].

[6] R. Goldman et al., “Synopsys’ educational generic memory compiler,”

in 10th EWME. IEEE, 2014, pp. 89–92, [Online].

[7] M. Clinton et al., “A 5GHz 7nm L1 cache memory compiler for high speed computing and mobile applications,” in 2018 IEEE ISSCC. IEEE,

2018, pp. 200–201, [Online].

[8] A. Chen, “A review of emerging non-volatile memory (NVM) technologies and applications,” Solid-State Electronics, vol. 125, pp. 25–38,

2016, [Online].

[9] F. Zahoor et al., “Resistive random access memory (RRAM): an

overview of materials, switching mechanism, performance, multilevel

cell (MLC) storage, modeling, and applications,” Nanoscale research

letters, vol. 15, no. 1, pp. 1–26, 2020, [Online].

[10] S. Maheshwari et al., “Hybrid CMOS/memristor circuit design methodology,” arXiv preprint arXiv:2012.02267, 2021, [Online].