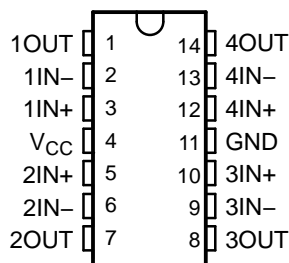


## FEATURES

- Low Supply Current . . . 85  $\mu$ A Typ
- Low Offset Voltage . . . 2 mV Typ
- Low Input Bias Current . . . 2 nA Typ
- Input Common Mode to GND
- Wide Supply Voltage . . . 3 V <  $V_{CC}$  < 32 V
- Pin Compatible With LM324
- Applications
  - LCD Displays
  - Portable Instrumentation
  - Sensor/Metering Equipment
  - Consumer Electronics (MP3 Players, Toys, Etc.)
  - Power Supplies

D, N, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The LP324 and LP2902 are quadruple low-power operational amplifiers especially suited for battery-operated applications. Good input specifications and wide supply-voltage range still are achieved, despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes GND.

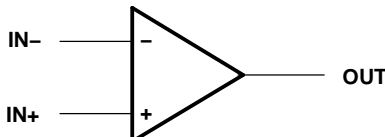
The LP324 and LP2902 are ideal in applications where wide supply voltage and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, etc.), and power supplies.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 25	LP324N	LP324N
		Tube of 50	LP324D	LP324
	SOIC – D	Reel of 2500	LP324DR	
		Tube of 90	LP324PW	LP324
	TSSOP – PW	Reel of 2000	LP324PWR	
–40°C to 85°C	PDIP – N	Tube of 25	LP2902N	LP2902N
		Tube of 50	LP2902D	LP2902
	SOIC – D	Reel of 2500	LP2902DR	
		Tube of 50	LP2902PW	LP2902
	TSSOP – PW	Reel of 2500	LP2902PWR	

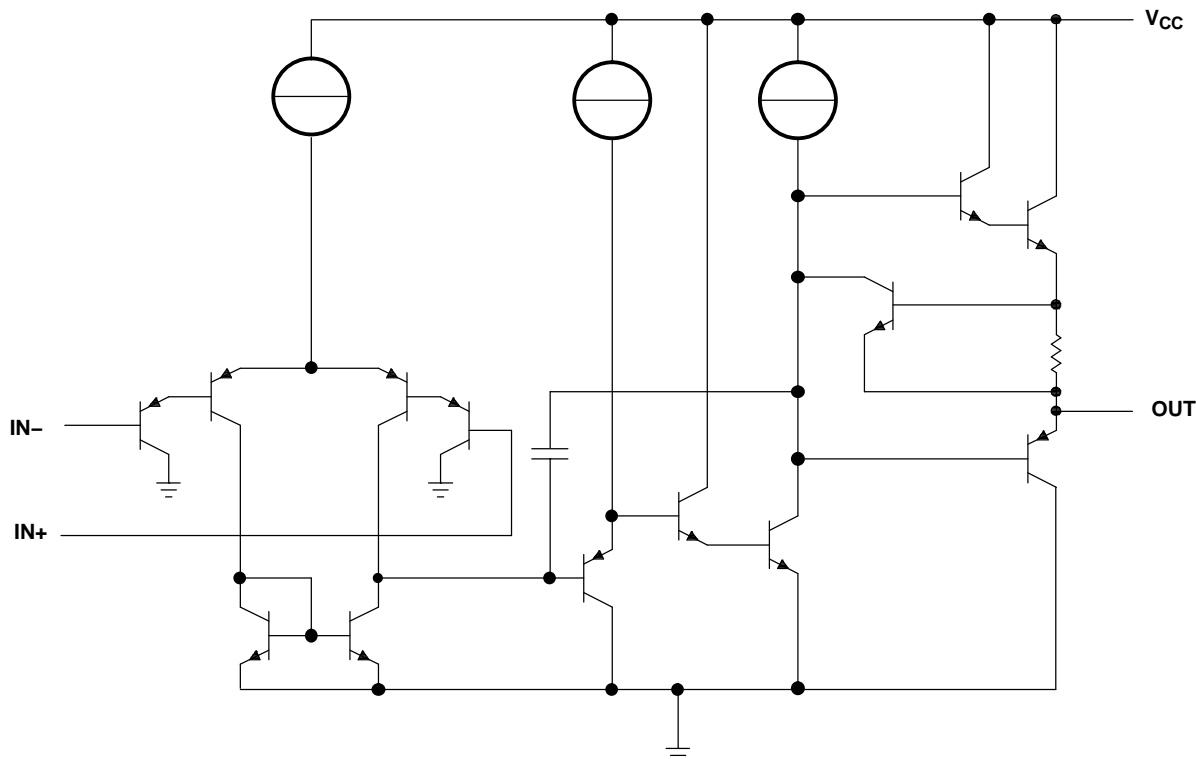
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## SYMBOL (EACH AMPLIFIER)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCHEMATIC (EACH AMPLIFIER)



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>		$\pm 16$ or 32	V
$V_{ID}$	Differential input voltage <sup>(3)</sup>		$\pm 32$	V
$V_I$	Input voltage (either input)	-0.3	32	V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$ , $V_{CC} \leq 15\text{ V}$ <sup>(4)</sup>			Unlimited	
$\theta_{JA}$	Package thermal impedance <sup>(5)(6)</sup>	D package	86	$^\circ\text{C/W}$
		N package	80	
		PW package	113	
$T_J$	Operating virtual junction temperature		150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range	-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and  $V_{CC}$  specified for the measurement of  $I_{OS}$ ) are with respect to the network GND.
- (3) Differential voltages are at IN+, with respect to IN-.
- (4) Short circuits from outputs to  $V_{CC}$  can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of  $150^\circ\text{C}$  can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

## ESD Protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	$\pm 2$	kV

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{IC} = V_{CC}/2$ ,  $R_L = 100\text{ k}\Omega$  to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	T <sub>A</sub> <sup>(2)</sup>	LP324			LP2902			UNIT
				MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	
V <sub>IO</sub>	Input offset voltage		25°C		2	4		2	4	mV
			Full range			9		10		
I <sub>IB</sub>	Input bias current		25°C		2	10		2	20	nA
			Full range			20		40		
I <sub>IO</sub>	Input offset current		25°C		0.2	2		0.5	4	nA
			Full range			4		8		
A <sub>V</sub>	Large-signal voltage gain	R <sub>L</sub> = 10 kΩ to GND, V <sub>CC</sub> = 30 V	25°C		50	100		40	70	V/mV
			Full range		40			30		
CMRR	Common-mode rejection ratio	V <sub>CC</sub> = 30 V, V <sub>IC</sub> = 0 V to V <sub>CC</sub> – 1.5 V	25°C		80	90		80	90	dB
			Full range		75			75		
k <sub>VSR</sub>	Power-supply rejection ratio	V <sub>CC</sub> = 5 V to 30 V	25°C		80	90		80	90	V
			Full range		75			75		
I <sub>CC</sub>	Supply current	R <sub>L</sub> = ∞	25°C		85	150		85	150	μA
			Full range			250		275		
V <sub>OH</sub>	Output voltage swing (high)	I <sub>L</sub> = 0.35 mA to GND, V <sub>IC</sub> = 0 V	25°C		3.4	3.6		3.4	3.6	V
			Full range		V <sub>CC</sub> – 1.9			V <sub>CC</sub> – 1.9		
V <sub>OL</sub>	Output voltage swing (low)	I <sub>L</sub> = 0.35 mA from V <sub>CC</sub> , V <sub>IC</sub> = 0 V	25°C		0.82	0.7		0.82	0.7	V
			Full range		1			1		
I <sub>O</sub>	Output source current	V <sub>O</sub> = 3 V, V <sub>ID</sub> = 1 V	25°C		7	10		7	10	mA
			Full range		4			4		
I <sub>O</sub>	Output sink current	V <sub>O</sub> = 1.5 V, V <sub>ID</sub> = –1 V	25°C		4	5		4	5	mA
			Full range		3			3		
		V <sub>O</sub> = 1.5 V, V <sub>ID</sub> = –1 V, V <sub>IC</sub> = 0 V	25°C		2	4		2	4	
			Full range		1			1		
I <sub>OS,GND</sub>	Output short to GND	V <sub>ID</sub> = 1 V	25°C		20	35		20	35	mA
			Full range			40		40		
I <sub>OS,VCC</sub>	Output short to V <sub>CC</sub>	V <sub>ID</sub> = –1 V	25°C		15	30		15	30	mA
			Full range			45		45		
∞V <sub>IO</sub>	Input offset voltage drift		25°C		10			10		μV/°C
∞I <sub>IO</sub>	Input offset current drift		25°C		10			10		pA/°C

(1) For full-range temperature limits:  $V_{CC} = 3\text{ V}$  to  $32\text{ V}$ ,  $V_{ICR} = 0\text{ V}$  to  $V_{CC} - 1.5\text{ V}$  (unless otherwise noted)

(2) Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for LP324 and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for LP2902.

(3) All typical values are at  $T_A = 25^\circ\text{C}$ .

## Operating Conditions

$V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
GBW	Gain bandwidth product	100	kHz
SR	Slew rate	50	V/ms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2902D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	<a href="#">Samples</a>
LP2902DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	<a href="#">Samples</a>
LP2902N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	LP2902N	<a href="#">Samples</a>
LP2902PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	<a href="#">Samples</a>
LP2902PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	<a href="#">Samples</a>
LP2902PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2902	<a href="#">Samples</a>
LP324D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>
LP324DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>
LP324DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>
LP324DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>
LP324N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	LP324N	<a href="#">Samples</a>
LP324PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>
LP324PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LP324	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
LP324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LP324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902DR	SOIC	D	14	2500	333.2	345.9	28.6
LP2902PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LP324DR	SOIC	D	14	2500	364.0	364.0	27.0
LP324DR	SOIC	D	14	2500	333.2	345.9	28.6
LP324DRG4	SOIC	D	14	2500	333.2	345.9	28.6
LP324PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

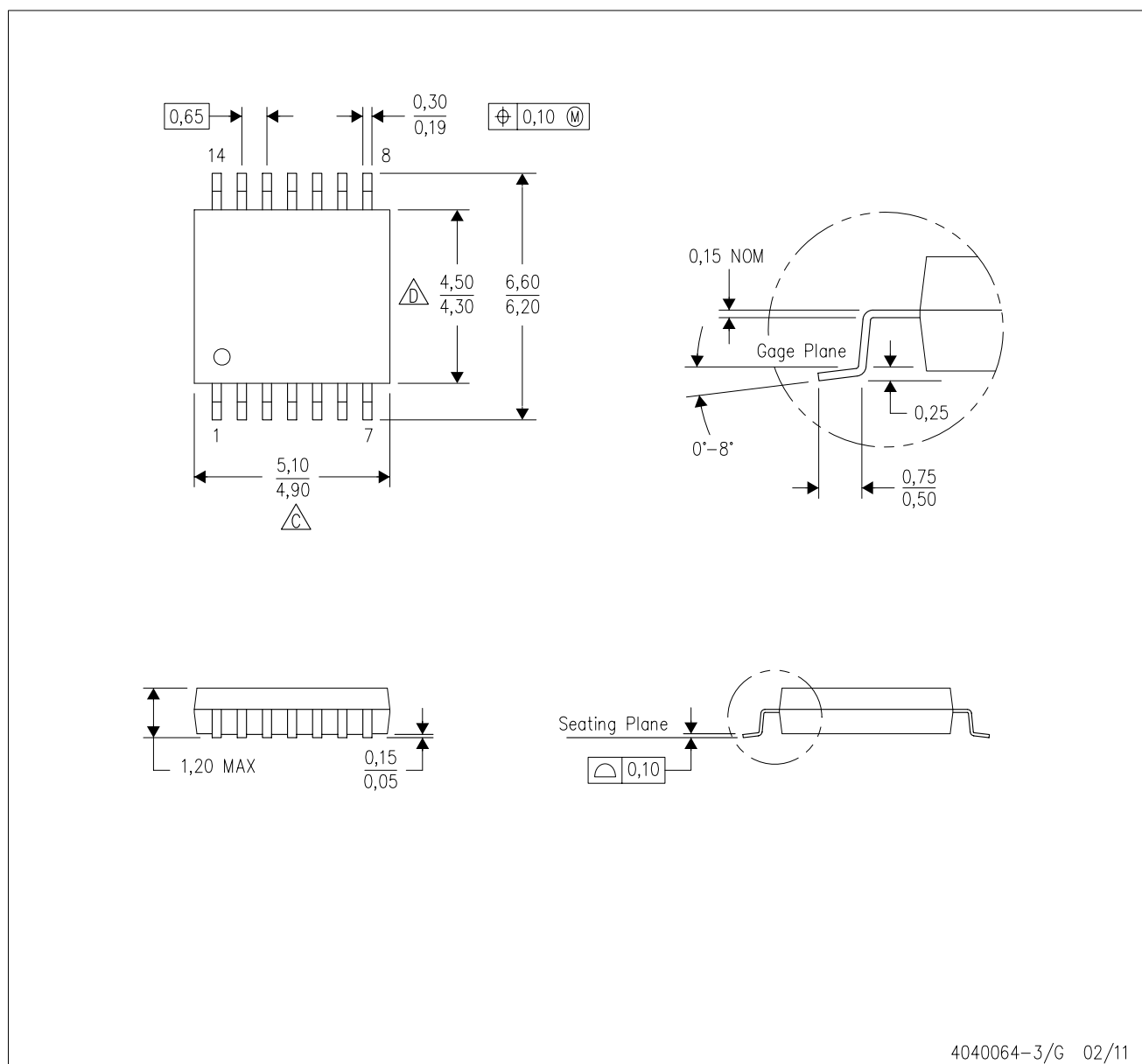
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

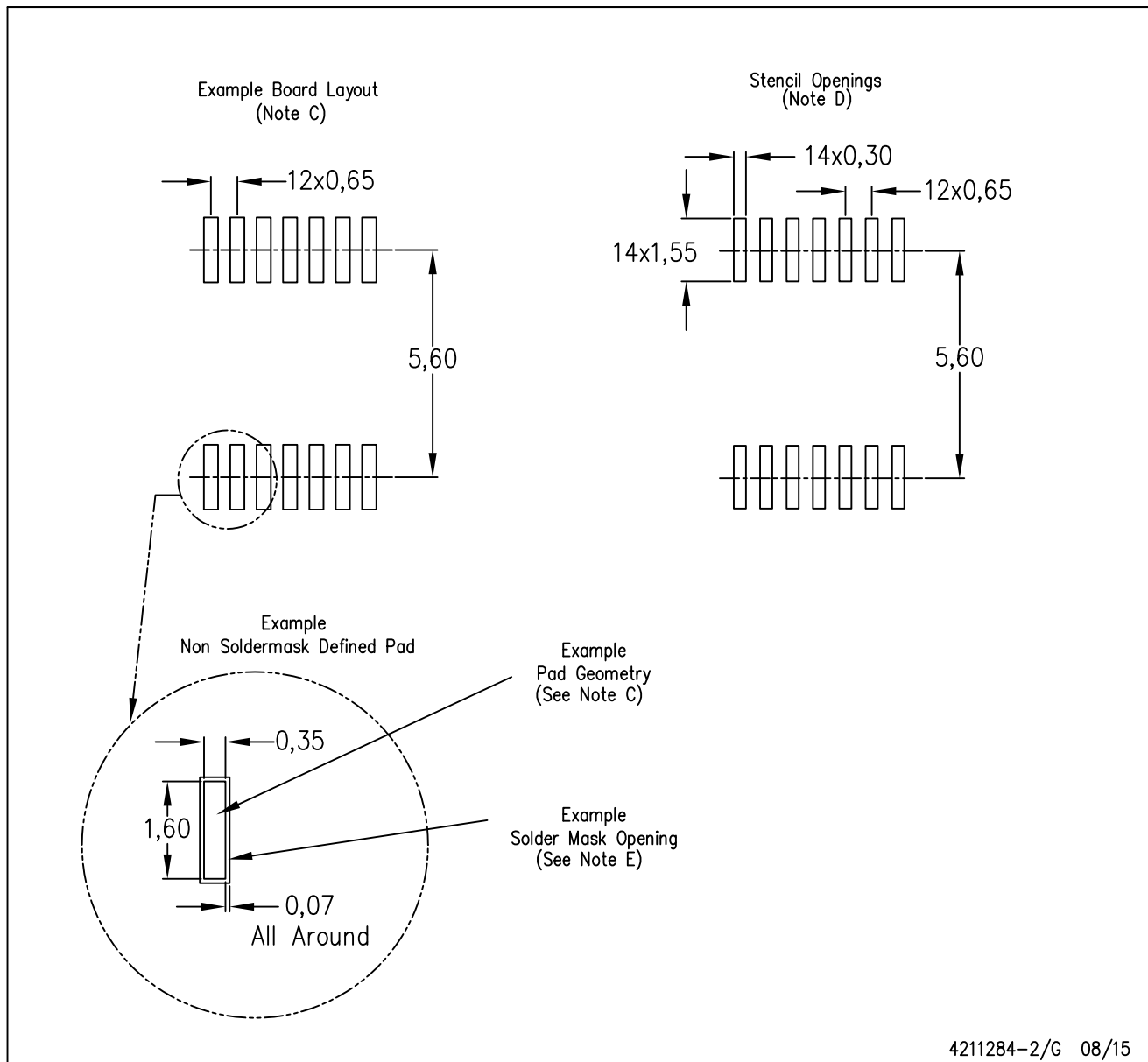
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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