Design Rule Verification Report

Date:	2019-02-20
Time:	6:25:45 PM
Elapsed Time:	00:00:01
Filename:	C:\Users\Santhosh Nagendran\Desktop\ESHD\EECE8010_Template (2-26-2018 11-03-01 AM)\Layout\Template.PcbDoc

Warnings:	0
Rule Violations:	0

Summary

Warnings	**Count**
Total	**0**

Rule Violations	**Count**
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) (All)	0
Minimum Annular Ring (Minimum=10mil) (All)	0
Hole Size Constraint (Min=20mil) (Max=150mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0

Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Silk primitive without silk layer	0
Total	**0**