RECONFIGURABLE SYSTEMS PRINCIPLE

EECE8020

MILESTONE #1

PROJECT DEFINITION

LCD INTERFACE WITH MICROPROCESSOR

EMBEDDED SYSTEM DEVELOPMENT

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CONESTOGA

Connect Life and Learning

DESIGN PURPOSE

The main purpose of the project is to create an LCD interface with the micro processor. And make it work. Creating an interface with the processor means developing the peripherals to make it work with the processor with the provided signals to it. Based on the register selection and data to be given into the peripheral it should react accordingly, by showing some values on the output.

We will be learning how the LCD module is interfaced with the microprocessor and then after clear understanding the working of LCD interface, we will be creating the functional blocks to implement the logics of the processor involved into a file using some code and then to make it work, we will be creating some test bench file with test vectors to see how the functional block reacts to it.

The test vector created along with the test bench will show us whether the functional block works as per the expectations or not.

REGISTER LIST

The LCD module is 16*2 which means 16 columns and 2 rows. It has different pins with it, the pins involved are totally 16 pins.

Power Supply: Vss, Vcc, VEE (+5v and Gnd) (3 pins) this is the main supply for the module

Back Light: LED+ and LED- (+5v and Gnd) (2 pins) to adjust the back light and adjust the contrast

Register: RS, R/W and E (3 pins) this is to select the registers and to decide whether to read or write, followed by the enable pin.

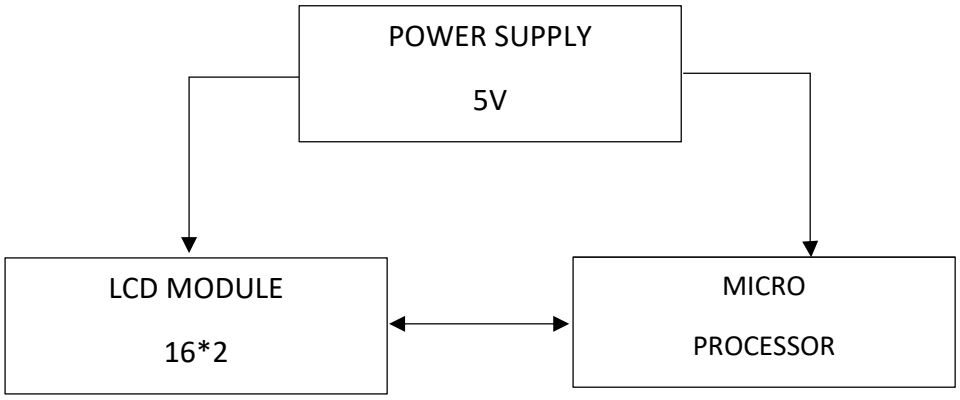
Data bus: These are the main pins where the real data will be moving from the processor to the module or module to the processor (8 pins) (DB0 to DB7). In this section the important section considered is the register selection part. The bits involved in the register could be of 16 bits wide. To know more about all the pins into the register file, the **E** pin is called the enable pin which is used for enabling the module by giving 0 or 1 which represents on and off respectively.

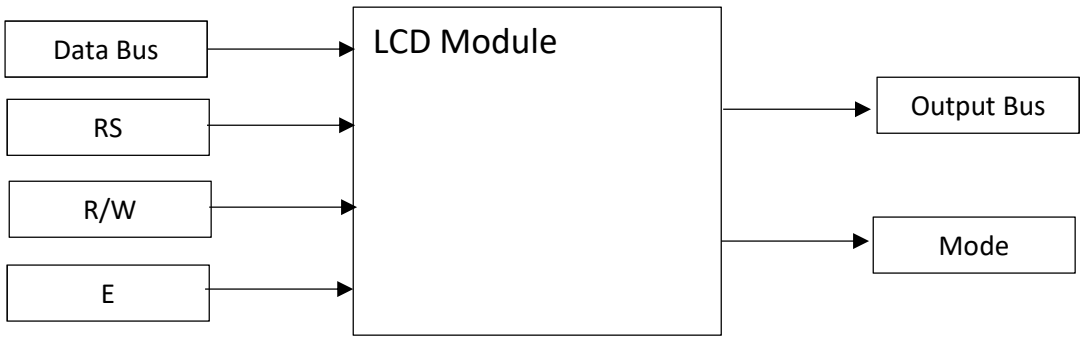
RS: is the register selection pin, which is used to switch modes of operation of the module with the processor. The two different registers involved in the register selection are command register and data register. Logic HIGH at RS pin selects data register and logic LOW at RS pin selects command register. If we make the RS pin HIGH and feed an input to the data lines (DB0 to DB7), this input will be treated as data to display on LCD screen. If we make the RS pin LOW and feed an input to data lines, then this will be treated as a command (a command to be written to LCD controller – like positioning cursor or clear screen or scroll).

R/W Read or write mode pins are used for selecting between read and write modes. Logic HIGH at this pin activates read mode and logic LOW at this pin activates write mode.

DB0 – DB7 are the data pins where the command and the data are fed to the LCD module.

BLOCK DIAGRAM





PIN SPECIFICATIONS

DATA BUS - Unsigned 15 down to 0

RS - std_logic

R/W - std_logic

E - std_logic

OUTPUT Bus - Unsigned 15 down to 0

MODE - std_logic

TESTING

- First, we will be creating a file named LCD module.
- Declare the necessary variables to be used inside the process including the temporary variables along with the name, size and type.
- Crate a module or entity with the same name and write the functional blocks with the necessary case statements followed by some assignment statements.
- Create the test bench file to create some test vectors.
- In this file, we will be creating a vector to print some letter or word in the screen.
- If the expected result appears in the simulation, then the system passes.
- Add some print statements in the test bench to make it easy to debug the errors and it will also be easy to develop the process.

BACKGROUND INFORMATION

This design is going to be the same as the module available in the market, we are trying to imitate the actions and structure of the module by re creating it. After creating a strong test vectors for it, this will be known whether the module fine as expected and the one which are already available in the market.