RECONFIGURABLE SYSTEMS PRINCIPLE

EECE8020

MILESTONE #2

REGISTER DEFINITIONS AND FUNCTIONAL

SPECIFICATIONS

LCD INTERFACE WITH MICROPROCESSOR

EMBEDDED SYSTEM DEVELOPMENT

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REGISTER DEFINITIONS

The LCD module is 16*2 which means 16 columns and 2 rows. It has different pins with it, the pins involved are totally 16 pins.

Power Supply: Vss, Vcc, VEE (+5v and Gnd) (3 pins) this is the main supply for the module

Back Light: LED+ and LED- (+5v and Gnd) (2 pins) to adjust the back light and adjust the contrast

Register: RS, R/W and E (3 pins) this is to select the registers and to decide whether to read or write, followed by the enable pin.

Data bus: These are the main pins where the real data will be moving from the processor to the module or module to the processor (8 pins) (DB0 to DB7). In this section the important section considered is the register selection part. The bits involved in the register could be of 16 bits wide. To know more about all the pins into the register file, the **E** pin is called the enable pin which is used for enabling the module by giving 0 or 1 which represents on and off respectively.

RS: is the register selection pin, which is used to switch modes of operation of the module with the processor. The two different registers involved in the register selection are command register and data register. Logic HIGH at RS pin selects data register and logic LOW at RS pin selects command register. If we make the RS pin HIGH and feed an input to the data lines (DB0 to DB7), this input will be treated as data to display on LCD screen. If we make the RS pin LOW and feed an input to data lines, then this will be treated as a command (a command to be written to LCD controller – like positioning cursor or clear screen or scroll).
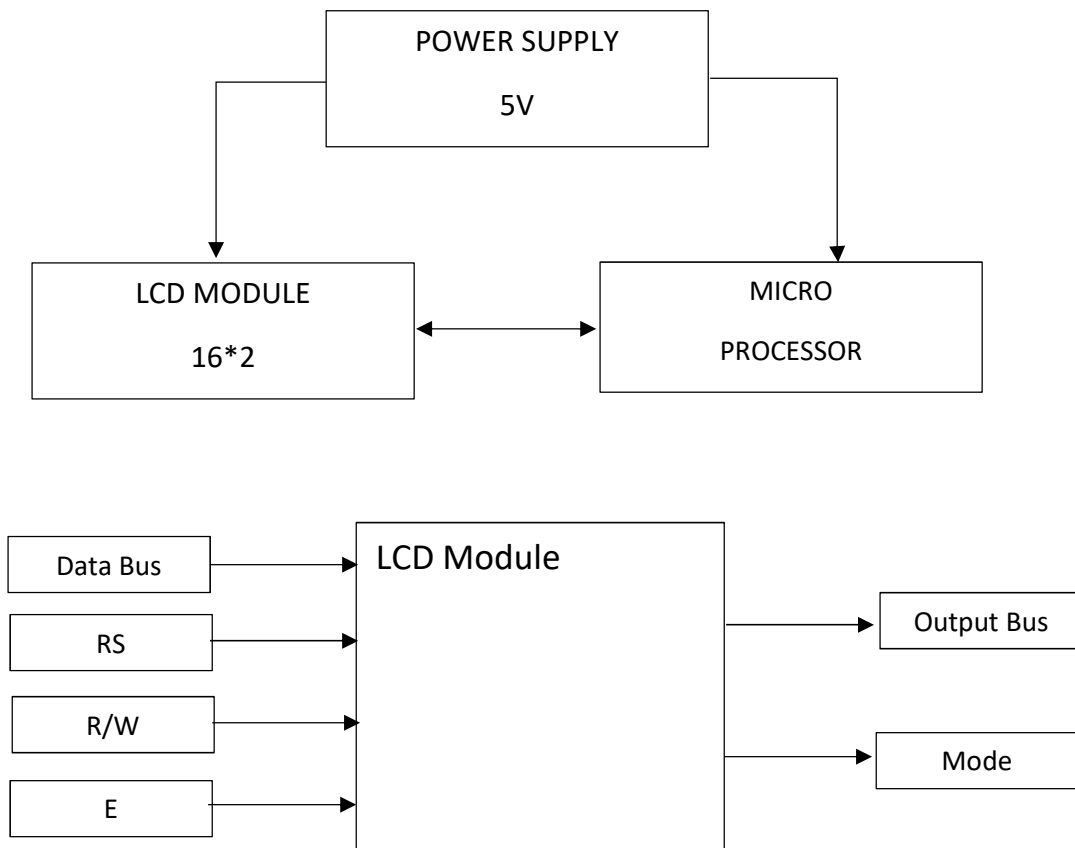
R/W Read or write mode pins are used for selecting between read and write modes. Logic HIGH at this pin activates read mode and logic LOW at this pin activates write mode.

DB0 – DB7 are the data pins where the command and the data are fed to the LCD module.

Apart from these register files, the main thing to be concentrated in this interface is the timing.

The clock signal should be generated at a nominal level of about 24MHZ, slower clocks are also should make this interface work. The timing interval is necessary to make the steps involved in this interface executable. After performing each line of code written in this interface will wait for some period of time by introducing some flags in the middle to look at the check points.

BLOCK DIAGRAM

```
                    ┌──────────────────┐
                    │  POWER SUPPLY    │
                    │       5V         │
                    └──────────────────┘
                     │                │
                     ▼                ▼
        ┌──────────────────┐   ┌──────────────────┐
        │   LCD MODULE     │◄─►│     MICRO        │
        │      16*2        │   │   PROCESSOR      │
        └──────────────────┘   └──────────────────┘
```

```
  ┌──────────────┐
  │  Data Bus    │────►┌──────────────────────┐
  └──────────────┘     │  LCD Module          │
  ┌──────────────┐     │                      │────►┌──────────────┐
  │     RS       │────►│                      │     │  Output Bus  │
  └──────────────┘     │                      │     └──────────────┘
  ┌──────────────┐     │                      │
  │     R/W      │────►│                      │────►┌──────────────┐
  └──────────────┘     │                      │     │    Mode      │
  ┌──────────────┐     │                      │     └──────────────┘
  │      E       │────►│                      │
  └──────────────┘     └──────────────────────┘
```

PIN SPECIFICATIONS

DATA BUS   - Unsigned 7 down to 0

RS   - std_logic

R/W   - std_logic

E   - std_logic

OUTPUT Bus   - Unsigned 7 down to 0

MODE   - std_logic

CLK   - timescale

RST   - Reset switch

These are the specifications of the pins which were given already, but apart from these pins two other special pins are to be added in the interface to make the work simpler so that when making the code and writing the test bench to check the operations included in this, they are

RDY   - Ready signal

OPER   - Operation mode

this mode is similar to that of the previously written Mode selection which will lets to understand whether the process is under data transfer which hold data or instruction set to the LCD module.

The above mentioned are the necessary things regards to the register set files.

FUNCTIONAL SPECIFICATIONS

Basically, the code will contain some declaration variable necessary for the interface, along with that the interface will contain some always blocks which will be sensitive for the raising edge of the clock and some conformation on the timing clock generated. The next sensitivity list will also check the raising edge of the clock which will this time contain the state machine operation to perform the task automatically by itself to see whether the development of the interface goes as per the plans. Just by incrementing the current state value, it starts executing the automatic function to perform to the next tasks where it will perform all the basic testing by proving some data to the LCD to print followed by some instruction set functions to change the mode of the LCD interfaced. Some of the common steps that will be implemented in the interfacing of LCD will contain the steps as follows,

- Once the initialization is done, the module should take in the data and process it according to the mode of operation asserted.
- When the state is in idle, the module should indicate ready state by the switch attached with it.
- When enable switch is sensed, this means that the DATA and the mode of operation are valid and the module should start to read the lines that is sent to the interface.