Hardwired Control Unit Design Exercises
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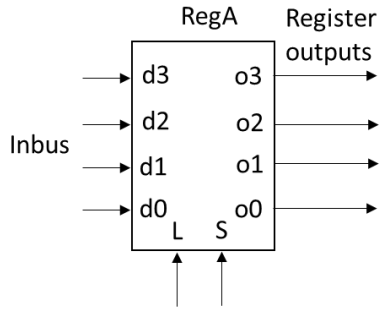
Design the hardwired control unit that loads a value from the inbus to a 4-bit shift register and shifts the bits left (i.e. towards the MSB) until the most significant bit becomes 0. When the most significant bit is 0, the operation stops. The register transfer language (RTL) description for each micro-operation is given below:

Start: RegA <- inbus;
Loop: RegA << 1;
If RegA[3] $\neq$ 0 then goto Loop;
Stop: goto Stop;

The register hardware and its function table are given as follows:

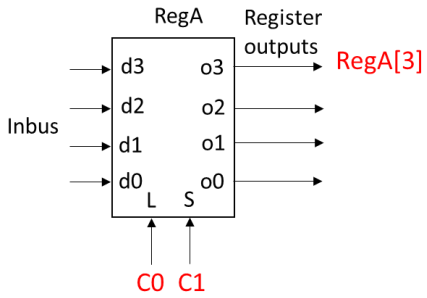



| Function Table | | |
|---|---|---|
| **L** | **S** | **Function** |
| 0 | 1 | Shift Left |
| 1 | 0 | Load external inputs |
| 0 | 0 | No change |

Note: A zero is inserted in the LSB as the bits shift left.

Solution:

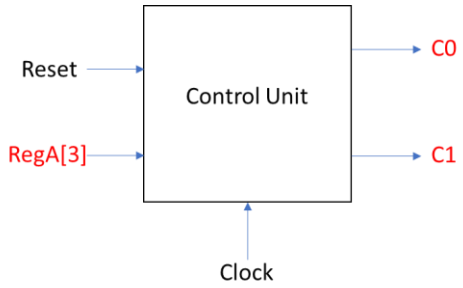
1) Establish the necessary control signals and the condition signal.




Show which control signal would be generated in which RTL step, i.e. for which micro-operation.

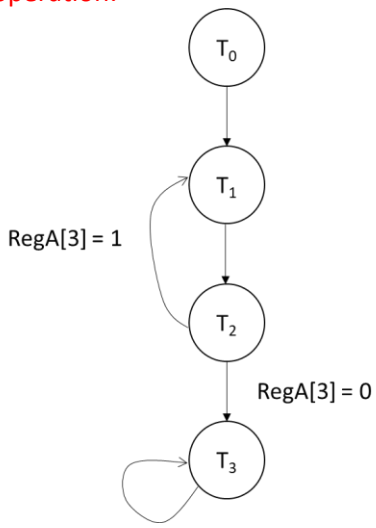
Start: RegA <- inbus; C0
Loop: RegA << 1; C1
If RegA[3] ≠ 0, goto Loop; No-op
Stop: goto Stop; No-op

2) Determine the block diagram of the controller:




(Per the question, ignore reset).

3) Construct the state transition diagram and show in a table which state corresponds to which micro-operation:



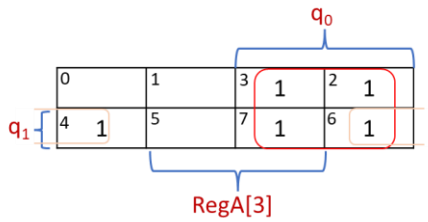
T0: Start: RegA <- inbus; C0
T1: Loop: RegA << 1; C1
T2: If RegA[3] ≠ 0, goto Loop; No-op
T3: Stop: goto Stop; No-op

4) Construct the state transition table:

| Present State | $q_1$ $q_0$ | RegA[3] | $q_1^+$ $q_0^+$ | Next State |
|---|---|---|---|---|
| T0 | 0 0 | X | 0 1 | T1 |
| T1 | 0 1 | X | 1 0 | T2 |
| T2 | 1 0 | 0 | 1 1 | T3 |
| T2 | 1 0 | 1 | 0 1 | T1 |
| T3 | 1 1 | X | 1 1 | T3 |

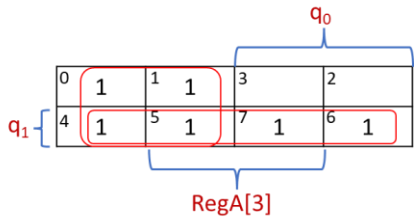
5) Boolean equations for the state variables $q_1^+$ and $q_0^+$:

$q_1^+$:




$q_1^+ = q_0 + q_1 \, RegA[3]'$

$q_0^+$:




$q_0^+ = q_0' + q_1$

6) Construct the output table.

| State | $q_1$ $q_0$ | C1 C0 |
|---|---|---|
| T0 | 0 0 | 0 1 |
| T1 | 0 1 | 1 0 |
| T2 | 1 0 | 0 0 |
| T3 | 1 1 | 0 0 |

7) Boolean equations the outputs:
C0 = $q_1'q_0'$
C1 = $q_1'q_0$

8) Hardwired control unit circuit: