CSC 137 MOCK MIDTERM 1

Show your work clearly to earn points. Work not shown will not earn any points.
Date: Instructor: Dr. Ilkan Çokgör Total: 20 points

Student Name: Student Number:

1) The binary numbers below are in signed 2's compliment representation.

01001 + 01000

a) Perform the given binary operation. (1 point)
b) Is there an overflow condition, and explain why or why not? (2 points)

2) a) Generate the truth table for the following function: (2 points)
F = XY + X'Z + YZ

b) Write the Boolean equation of this function in canonical sum-of-products form. (3 points)

c) Use K-maps to simplify the Boolean equation. (3 points)

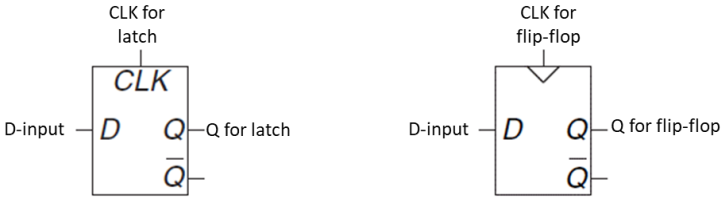
d) Draw the logic diagram of the simplified function using NOT, AND, OR gates. (2 points)

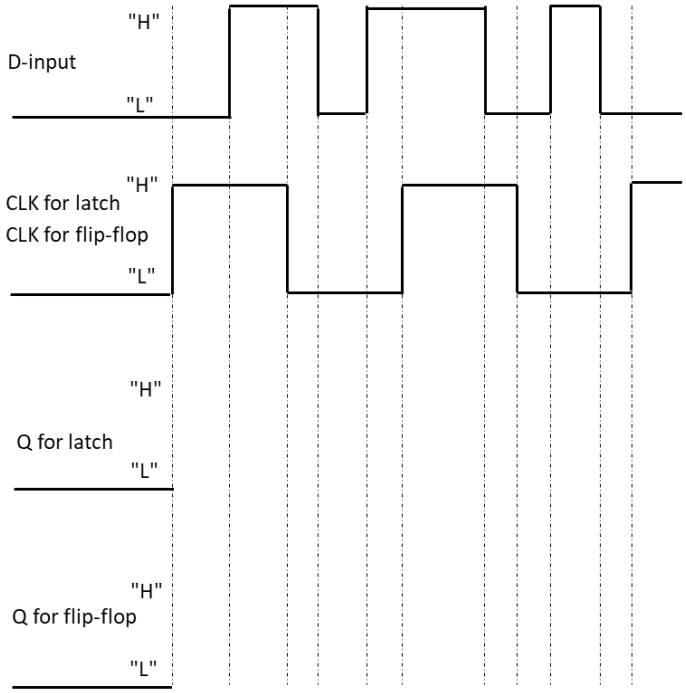
3) Implement the following truth table using an 8:1 multiplexer. (3 points)

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Exam continues on the next page.

4) In the following diagrams, the signals are connected to a D-latch and a D-Flip Flop as shown. Draw the timing diagrams for the "Q for latch" and the "Q for Flip Flop" outputs. (4 points)





Solutions:

1) The binary numbers below are in signed 2's compliment representation.

01001 + 01000

a) Perform the given binary operation. (1 point)
b) Is there an overflow condition, and explain why or why not? (3 points)

a)
  01001
+ 01000

  10001

b) Yes, there is an overflow condition because adding two positive numbers resulted in a negative number.

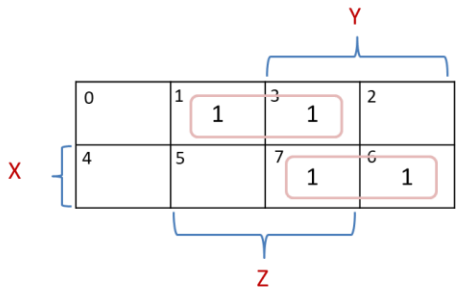
2) a) Generate the truth table for the following function: (3 points)
F = XY + X'Z + YZ

X	Y	Z	XY	X'Z	YZ	F
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	0	0
0	1	1	0	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	1

b) Write the Boolean equation of this function in canonical sum-of-products form. (3 points)

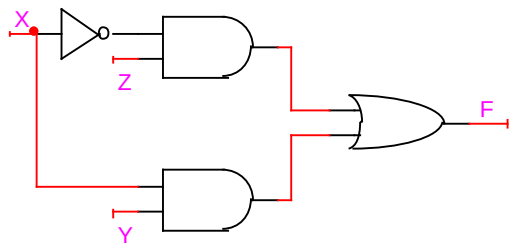
F = X'Y'Z + X'YZ + XYZ' + XYZ

c) Use K-maps to simplify the Boolean equation. (3 points)



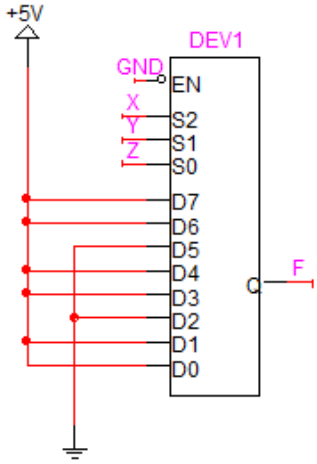
F = X'Z + XY

d) Draw the logic diagram of the simplified function using NOT, AND, OR gates. (2 points)



3) Implement the following truth table using an 8:1 multiplexer. (4 points)

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



4) In the following diagrams, the signals are connected to a D-latch and a D-Flip Flop as shown. Draw the timing diagrams for the "Q for latch" and the "Q for Flip Flop" outputs. (4 points)