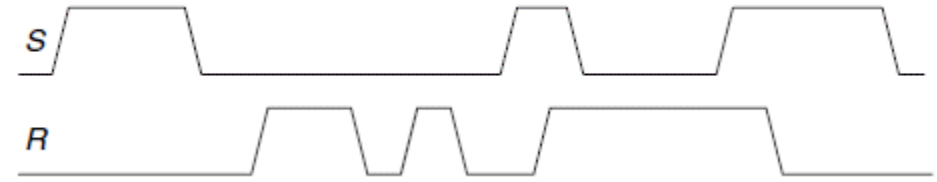
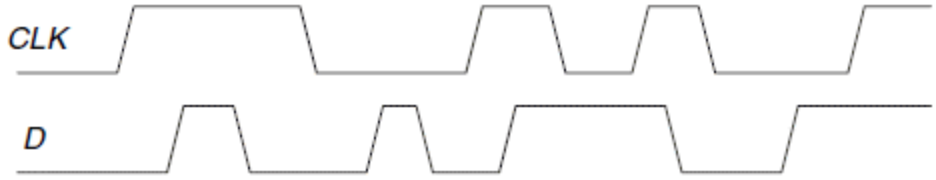
CSC 137 – Cokgor - Sequential Logic Design Exercises (answers are at the back)

(Exercises reference: David M. Harris, Sarah L. Harris, Digital Design and Computer Architecture, 2nd Edition, Elsevier, 2013, ISBN-13: 978-0-12-394424-5)

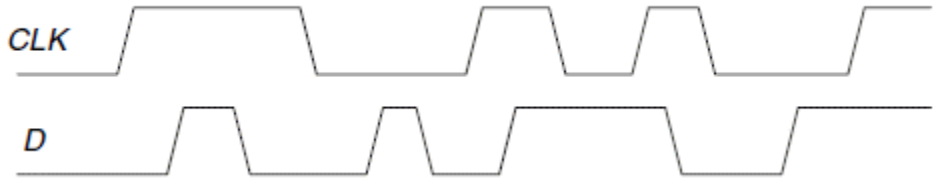
1) Given the input waveforms shown in figure below, sketch the output, Q, of an SR latch.



2) Given the input waveforms shown in figure below, sketch the output, Q, of a D latch.



3) Given the input waveforms shown in figure below, sketch the output, Q, of a D flip-flop.



4) The toggle (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value. Draw a schematic for a T flip-flop using a D flip-flop and an inverter.

5) Design a synchronously settable D flip-flop using logic gates.

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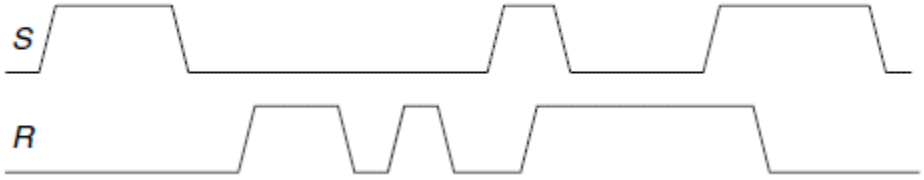

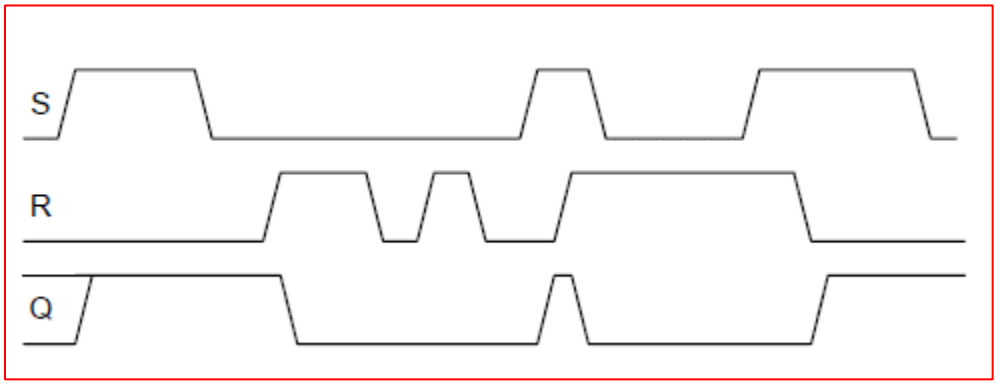

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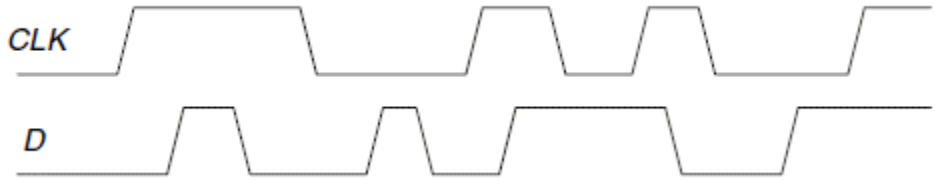

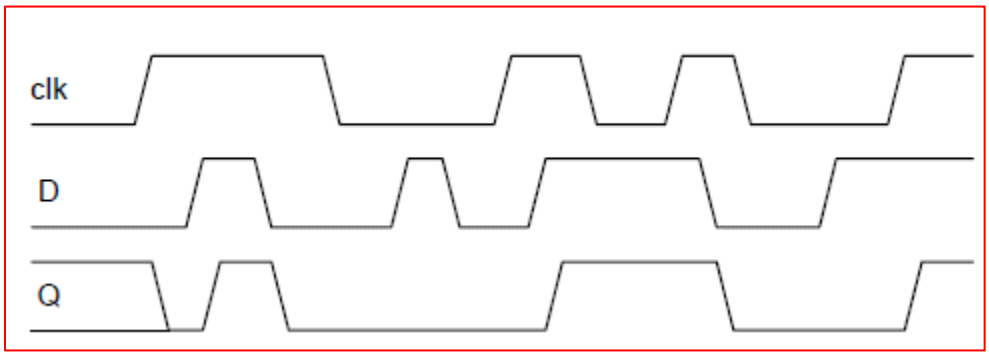

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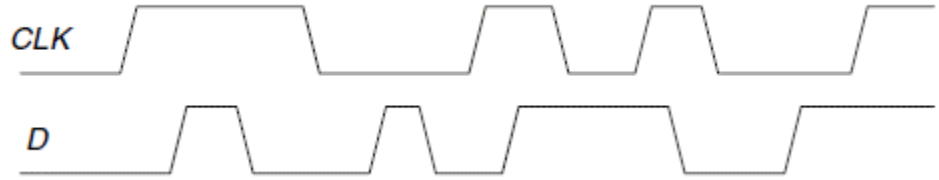

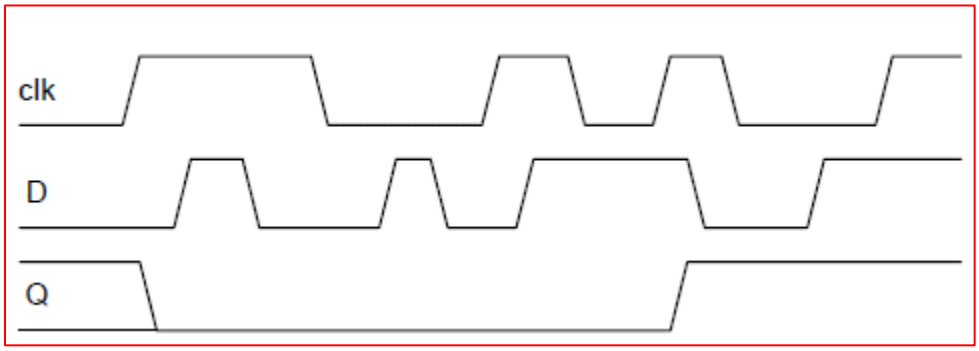

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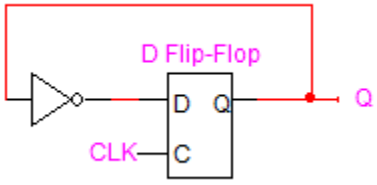

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