CSC 137 Cokgor Homework 5 (5 points)
Show your work. Work not shown will not earn points.

1) How many hexadecimal digits are needed to represent a binary number with 32 digits? (0.1 point)

2) A microprocessor can access any memory location by outputting the address of that location onto its address bus. You have designed a microprocessor and have made available 12 address lines for the address bus. You are using a memory device that is 8 bits wide (i.e. each memory location holds 1 Byte).
    a. How many Kilobytes is your microprocessor's memory capacity? (State your answer in Kilobytes) (0.1 point)

    b. You have decided that you will need more memory capacity. How many address lines do you need to make available if you wanted to double the memory capacity? (0.1 point)

3) How many address lines are required for a 2MByte memory? (0.1 point)

4) You will be building a memory with 14-bit address and 8-bit data word size. If this memory were constructed from 1K x 1-bit RAM chips, how many chips would be required? (0.2 point)

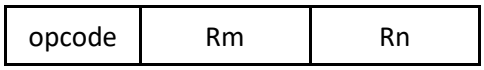
5) Can you build a computer with non-volatile memory (e.g. ROM) only? Explain your answer. (0.1 point)

6) Can you build a computer with volatile memory (e.g. RAM) only? Explain your answer. (0.1 point)

7) What does the Program Counter register (or the Instruction Pointer register) do? (0.1 point)

8) You are designing a simple microprocessor for a specific application. You have determined that you will need 32 unique operations in the instruction set. Each instruction needs two register fields to hold the operands. Each register field can address 16 internal registers.
    a. How many bits does your op-code field need to be? (0.1 point)
    b. How many bits does each of your register fields need to be? (0.1 point)

9) We have seen that fields of an instruction encoding can be mixed to achieve different goals depending on the instruction type. Refer to page 20 of the Instruction Set Architecture lecture notes. As examples, the Rm field of an R-format instruction is 5 bits, whereas the address offset field of a D-format instruction is 9-bits. Or, the opcode field of a D-format instruction is 11 bits, whereas the opcode field of an I-format instruction is 10-bits. Answer the following questions with field mixing in mind.
   Assume the following instruction format:



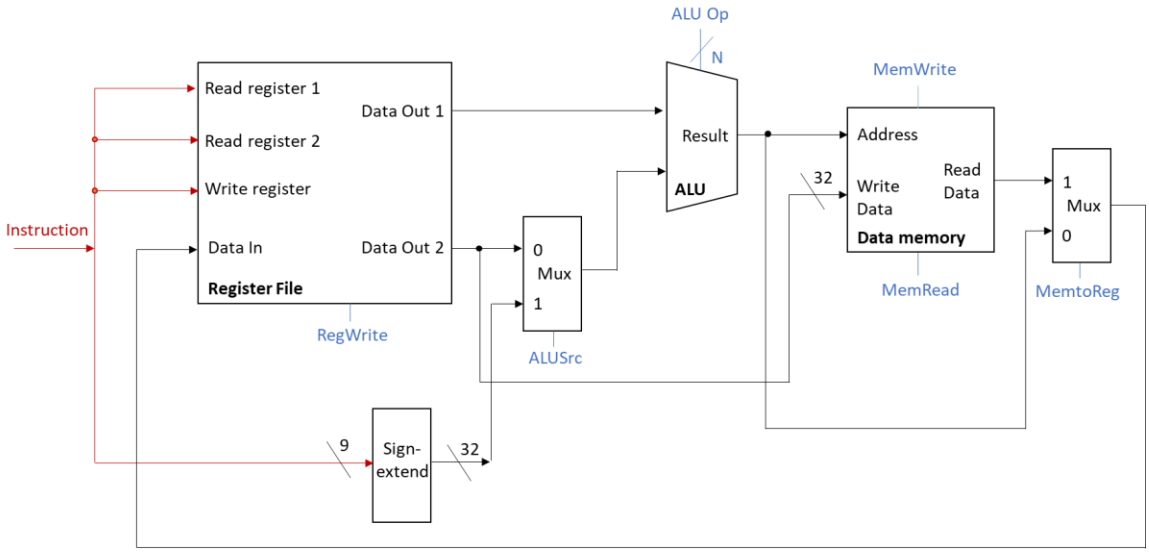
    a. The overall instruction length is 8 bits, the register fields (R1, R2) are 3 bits each. How many unique opcodes can you have? (0.1 point)

b. If you mix the fields, can you have 3 x two address and 8 one address instructions? Justify your answer. (0.2 point)

10) If the data storage is arranged according to the little-endian representation, how is the word 0x4CE3F90A stored in memory location 0x080001AC. (0.1 point)

Memory	Address
	0x080001AF
	0x080001AE
	0x080001AD
	0x080001AC
	0x080001AB
	0x080001AA
	0x080001A9

11) Consider the datapath developed during the class lectures for R-format and D-format instructions (shown below) and answer the following questions.



a. If the RegWrite control signal is stuck at 0 (i.e. not asserted), which instructions shown below would malfunction: (0.4 point)

i. ADD R0, R1, R2
ii. SUB R0, R1, R2
iii. LDR R0, [R1, #4]
iv. STR R1, [R0, #]

b. If the MemWrite control signal is stuck at 0 (i.e. not asserted), which instructions shown below would malfunction: (0.4 point)

i. ADD R0, R1, R2

ii. SUB R0, R1, R2
iii. LDR R0, [R1, #4]
iv. STR R1, [R0, #4]

c. If the ALUSrc control signal is stuck at 0, which instructions shown below would malfunction: (0.4 point)
   i. ADD R0, R1, R2
   ii. SUB R0, R1, R2
   iii. LDR R0, [R1, #4]
   iv. STR R1, [R0, #4]

12) Consider the instruction execution timing table of a single cycle processor given below and answer the following questions:

Instruction	Instruction Fetch	Register Read	ALU Operation	Data Access	Register Write	**Total Time**
LDR (Load Register)	200 ps	100 ps	200 ps	200 ps	100 ps	**800 ps**
STR (Store Register)	200 ps	100 ps	200 ps	200 ps		**700 ps**
ADD	200 ps	100 ps	200 ps		100 ps	**600 ps**
SUB	200 ps	100 ps	200 ps		100 ps	**600 ps**

a) If every instruction in the table takes exactly one clock cycle, what must be the clock cycle time to accommodate all instructions. (0.1 point)
b) What would be the clock speed of the processor with the cycle time you calculated above? (0.1 point)
c) Assume that both instructions and data are in the same memory space, i.e. there is a single address and data bus pair for memory access. What will be the clock cycle time if you reduce the delay of the memory access by half. (0.1 point)
d) What would be the clock speed of the processor after the reduction of memory access time as in (c) above. (0.1 point)

13) Consider the instruction execution for a 5 stage pipelined processor for all instructions as shown below. Each phase takes 200 ps. Instruction Fetch and Data Access use the same memory. Assume that Reg Read and Reg Write phases do not conflict.

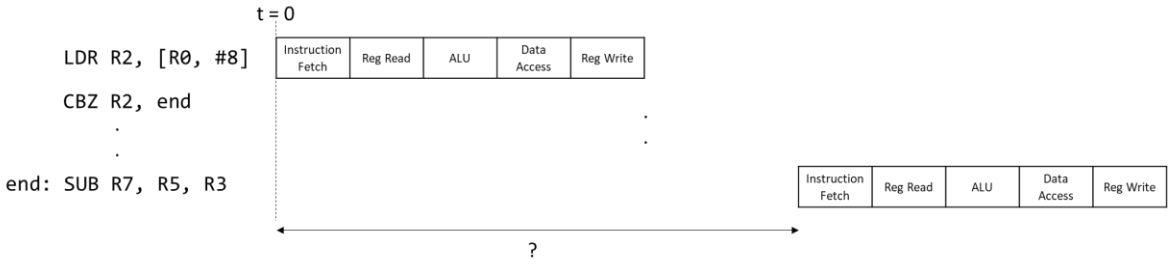
Instruction Fetch	Reg Read	ALU	Data Access	Reg Write

Answer the following questions:

a) Can the following program segment be executed without a pipeline hazard? If there is a hazard, then what type? (0.3 point)
LDR R1, [R0, #4]
ADD R6, R5, R1

b) Can the following program segment be executed without a pipeline hazard? If there is a hazard, then what type? (0.3 point)
ADD R6, R5, R3
STR R1, [R0, #4]
LDR R2, [R0, #8]
SUB R7, R5, R3

c) The LDR instruction in the program segment shown below is fetched at t=0. If the branch is taken as a result of the CBZ instruction, when will the SUB instruction be fetched? Justify your answer by showing the pipeline. You must avoid any hazards by stalling the pipeline when necessary. (0.4 point)



14) Consider the memory map of a hypothetical processor below. Does this processor implement memory mapped I/O or isolated I/O? Explain your reasoning. (0.1 point)

Flash
DRAM
Peripherals
SRAM
ROM

15) Given the Interrupt Vector Table and the memory contents below, answer the following questions: (0.4 point)

Interrupt	*Vector Address*
. .	. .
EXTI3	0x00000064
. . .	. . .
Reset	0x00000004
Initial Stack Pointer Value	0x00000000

Memory Address	*Memory Content*
. .	. .
0x00000064	0x0800030C
. .	. .
0x00000004	0x2000020C
0x00000000	0x20000068

a) Which address is the Interrupt Vector for Reset located?
b) Which address is the Interrupt Vector for EXTI3 interrupt located?
c) What is the interrupt vector for Reset?
d) What is the address of the EXTI3 Interrupt Service Routine?

16) Direct Memory Access (DMA):

A program needs to transfer a block of data from the computer hard drive to the main memory. A DMA request is initiated via the DMA controller. Answer the following questions based on what you learned in the class: (0.4 point)

a) Is this a DMA read or a DMA write transfer?
b) Will the data that is being transferred be loaded to the microprocessor register, or will the data be transferred between the peripheral and the memory directly?
c) Is it the DMA controller or the processor that generates the corresponding hard drive and memory control signals?
d) Can the processor initiate a separate transfer between an Ethernet port and the main memory during this data transfer?