CSC 137 Cokgor – Memory Hierarchy Exercises

1) Given the cache performance example in the lecture notes (page 25), what will be the amount of execution time spent on memory stalls if the processor is twice as fast (i.e., Process clock cycles per instruction is 1 without any memory stalls)?

2) Consider a small cache which consists of four one-word blocks. Find the number of misses given the following sequence of block address requests
0000
1000
0000
0110
1000

   a) if the cache is a direct-mapped.
   b) if the cache is fully associative.

3) Suppose we have a processor that executes one instruction per clock cycle and with a clock rate of 4GHz. Assume a main memory access time of 100ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%.
   a. What is the total cycles per instruction including the memory stalls?
   b. If we add a second level cache that has 5ns access time and is large enough to reduce the miss rate to main memory to 0.5%, what will be the total cycles per instruction including the memory stalls?
   c. How much faster will the processor be with the second level cache?

4) Consider a virtual memory system that can address a total of 2^{50} bytes (1 petabytes). You have unlimited hard drive space, but are limited to 2 GB of main (physical) memory. Assume that virtual and physical pages are each 4 KB in size.
   a) How many bits is the physical address?
   b) What is the maximum number of virtual pages in the system?
   c) How many physical pages are in the system?
   d) How many page table entries will the page table contain?
   e) Assume that, in addition to the physical page number, each page table entry also contains some status information in the form of a valid bit (V) and a dirty bit (D). How many bytes long is each page table entry? (Round up to an integer number of bytes.)

CSC 137 Cokgor – Memory Hierarchy Exercises Solutions

1) Given the cache performance example in the lecture notes (page 25), what will be the amount of execution time spent on memory stalls if the processor is twice as fast (i.e. Process clock cycles per instruction is 1 without any memory stalls?

Total cycles per instruction including memory stalls would then be = 1 + 3.44 = 4.44
Amount of execution time spent on memory stalls would then be = 3.44 / 4.44 = 77%.
The amount of time spent on memory stalls will take up an increasing fraction of the execution time.

2) Consider a small cache which consists of four one-word blocks. Find the number of misses given the following sequence of block address requests
0000
1000
0000
0110
1000

a) if the cache is a direct-mapped.

Since the cache is four blocks, we need two bits of the address as index bits. The rightmost two bits will be for index.

Index	Tag	Data
00		
01		
10		
11		

Running through the sequence of address requests:

0000 – Miss. Retrieve the data at 0000.

Index	Tag	Data
00	00	Data at 0000
01		
10		
11		

1000 – Miss. Replace the data at 00.

Index	Tag	Data
00	10	Data at 1000
01		
10		
11		

0000 – Miss. Replace the data at 00.

Index	Tag	Data
00	00	Data at 0000
01		
10		
11		

0110 – Miss. Retrieve the data at 0110.

Index	Tag	Data
00	00	Data at 0000
01		
10	01	Data at 0110
11		

1000 – Miss. Retrieve the data at 1000.

Index	Tag	Data
00	10	Data at 1000
01		
10	01	Data at 0110
11		

5 Misses.

b) if the cache is fully associative.
Any address can go to any block. There is no indexing.

0000 – Miss.

Tag	Data
0000	Data at 0000

1000 – Miss.

Tag	Data
0000	Data at 0000
1000	Data at 1000

0000 – Hit

Tag	Data
0000	Data at 0000

1000	Data at 1000

0110 – Miss.

Tag	Data
0000	Data at 0000
1000	Data at 1000
0110	Data at 0110

1000 – Hit

Tag	Data
0000	Data at 0000
1000	Data at 1000
0110	Data at 0110

3 Misses.

3) Suppose we have a processor that executes one instruction per clock cycle and with a clock rate of 4GHz. Assume a main memory access time of 100ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%.

   a. What is the total cycles per instruction including the memory stalls?
   b. If we add a second level cache that has 5ns access time and is large enough to reduce the miss rate to main memory to 0.5%, what will be the total cycles per instruction including the memory stalls?
   c. How much faster will the processor be with the second level cache?

a) 4GHz clock => 1/4GHz = 0.25 ns per clock cycle.
Memory stall clock cycles = 100ns / 0.25ns = 400 clock cycles.
Memory stall cycles per instruction = 400 X 2% = 8
Total cycles per instruction including the memory stalls = 1 + 8 = 9

b) With two levels of caching, a miss in the primary (or the first-level) cache can be satisfied by the secondary cache or by main memory.
Memory stall cycles to access the secondary cache = 5ns/0.25ns = 20 clock cycles.
If the miss is satisfied in the secondary cache, then this is the entire miss penalty. If the miss needs to go to main memory, then the total miss penalty is the sum of the secondary cache access time and the main memory access time. Thus, for a two-level cache, total cycles per instruction is the sum of the stall cycles from both levels of cache and the base (i.e., one instruction per clock cycle):
Total cycles per instruction including the memory stalls = 1 + 2% x 20 + 0.5% x 400 = 3.4

c) The processor with the second level cache will be 9/3.4 = 2.6 times faster.

4) Consider a virtual memory system that can address a total of 2^{50} bytes (1 petabytes). You have unlimited hard drive space, but are limited to 2 GB of main (physical) memory. Assume that virtual and physical pages are each 4 KB in size.

a) How many bits is the physical address?
Physical memory: 2GB = 2^{31} Bytes. => 31 bits physical address.

b) What is the maximum number of virtual pages in the system?
# of virtual address bits = 50.
Page size = 4KB = 2^2 x 2^{10} Bytes = 2^{12} Bytes. => # of Page offset bits = 12
Virtual page number bits = 50-12 = 38. => # of virtual pages = 2^{38}

c) How many physical pages are in the system?
# of Page offset bits = 12.
Physical page number bits = 31 – 12 =19. => # of physical pages = 2^{19}

d) How many page table entries will the page table contain?
2^{38} page table entries; one for each virtual page.

e) Assume that, in addition to the physical page number, each page table entry also contains some status information in the form of a valid bit (V) and a dirty bit (D). How many bytes long is each page table entry? (Round up to an integer number of bytes.)
19 bits of physical page number + 1 valid bit + 1 Dirty bit = 21 bits. Round up to an integer byte = 3 Bytes each.