Operating Systems - Chapter 19 Summary

Paging: Faster Translations (TLBs)

• Paging requires extra memory access per translation, slowing performance.
• Solution: Translation Lookaside Buffer (TLB), a hardware cache in the MMU.
• TLB stores recent virtual-to-physical translations, avoiding repeated page table lookups.

TLB Basic Algorithm

• On memory access:
• Extract VPN (virtual page number).
• Check TLB for translation (VPN→PFN).
• If found (TLB hit): combine PFN + offset → physical address (fast).
• If not found (TLB miss): access page table in memory, update TLB, retry instruction.

How a TLB Works

• A small, fast hardware cache located near CPU core.
• Typically 32–128 entries, fully associative (any VPN can be stored anywhere).
• Uses parallel search to quickly match VPNs.
• Entries include: VPN, PFN, valid bit, protection bits, ASID (address-space ID).
• TLB relies on locality:
– Spatial: nearby addresses often accessed together.
– Temporal: recently accessed addresses likely reused soon.

Handling TLB Misses

• Hardware-managed TLB: hardware walks page table and refills TLB.
• Software-managed TLB: OS trap handler refills TLB (flexible, but slower).

TLB and Context Switches

• Problem: TLB entries valid only for one process; switching causes confusion.
• Solutions:
– Flush TLB on context switch (simple, but costly).
– Use Address Space Identifiers (ASIDs) to distinguish processes and avoid flushes.

TLB Replacement

• When TLB is full, a new entry replaces an old one.
• Policies:
– LRU (least recently used): evict old entries, assumes locality.
– Random: simple, avoids pathological cases.

Example and Performance

• Array access example: only first access per page misses, subsequent accesses hit.
• TLB hit rate improves with locality, often close to 100% in practice.
• Performance impact: TLB makes paging practical; without it, overhead would be prohibitive.

Real TLB Example (MIPS R4000)

• Supports 32-bit virtual addresses, 4KB pages.
• TLB entries include VPN, PFN, ASID, global bit, dirty bit, valid bit, cache control.
• Provides instructions (TLBP, TLBR, TLBWI, TLBWR) for OS to manage entries.

Summary

The TLB is a small hardware cache that stores recent address translations, making virtual memory practical by avoiding frequent page table lookups. Hits are fast; misses are handled by hardware or OS, then cached. Key issues: handling context switches (flush vs ASIDs), replacement policies (LRU, random), and limited size (TLB coverage). Despite being small, TLBs drastically improve memory performance.