

Diseño Digital Avanzado

Unidad 1 - Herramientas

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Proyecto Leds

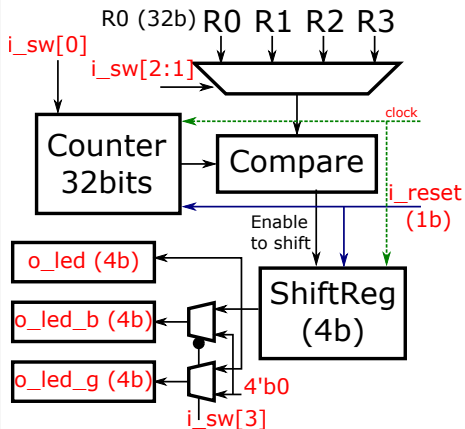


Proyecto LEDS

Implementación en FPGA - Leds

Descripción

- Los nombres en **ROJO** son puertos.
- *ck_rst* es el reset del sistema, el cual pone a cero el contador e inicializa el shiftregister (SR).
- *i_sw[0]* controla el enable (1) del contador. En estado (0) todo se detiene sin alterar el estado actual del contador y del SR.
- El SR se desplaza únicamente cuando el contador llegó a algún límite R0-R3.
- La elección del límite se puede realizar en cualquier momento del funcionamiento.
- *i_sw[3]* elije el color de los leds RGB.



Proyecto LEDS

Test Bench

Descripción

- El test bench (banco de pruebas) es un módulo que no tiene puertos declarados.
- Genera los estímulos de reloj y señales de control para modelar un escenario de prueba.
- Las variables utilizadas para estimular los puertos de entrada son declaradas como tipo **reg**.
- Las variables utilizadas para conectar los puertos de salida son declaradas como tipo **wire**.
- Lectura y cambio de estado de variables internas a los módulos
 - Definiendo las instancias se puede leer las variables internas
Ejemplo, assign `tb_count = tb_shiftleds.u_shiftleds.counter;`
 - Utilizando **force** se cambia el valor de una variable en una instancia. Se debe definir dentro de un bloque de procesamiento **initial**.
Ejemplo, force `tb_shiftleds.u_shiftleds.o_led = 4'b0001;`

Proyecto LEDS

Test Bench

Ejemplo - Generando Estímulos

```
1 'define N_LEDS 4
2 'define NB_SW 4
3
4 'timescale 1ns/100ps
5
6 module tb_shiftleds();
7
8     parameter N_LEDS = 'N_LEDS ;
9
10    wire [N_LEDS - 1 : 0] o_led ;
11    reg [NB_SW - 1 : 0] i_sw ;
12    reg ck_rst ;
13    reg CLK100MHZ;
14
15    initial begin
16        i_sw = 4'b0000 ;
17        CLK100MHZ = 1'b0 ;
18        ck_rst = 1'b0 ;
19        #100 ck_rst = 1'b1 ;
20        #100 i_sw = 4'b0001 ;
21        #1000000 i_sw = 4'b0011 ;
22        #1000000 i_sw = 4'b1011 ;
23        #1000000 $finish;
24    end
```

```
1
2 always #5 CLK100MHZ = ~CLK100MHZ;
3
4 shiftleds
5     #(N_LEDS (N_LEDS) ,
6       .NB_SW (NB_SW)
7     )
8 u_shiftleds
9     (.o_led (o_led) ,
10     .i_sw (i_sw) ,
11     .ck_rst (ck_rst) ,
12     .CLK100MHZ (CLK100MHZ)
13     );
14
15 endmodule // tb_shiftleds
```

Proyecto LEDS

Test Bench

Ejemplo - Estímulos desde Archivos

```
1 'define N_LEDS 4
2 'define NB_SW 4
3
4 'timescale 1ns/100ps
5
6 module tb_shiftleds_file();
7
8     parameter N_LEDS = 'N_LEDS ;
9     parameter NB_SW   = 'NB_SW   ;
10
11     wire [N_LEDS - 1 : 0] o_led ;
12     reg [NB_SW - 1 : 0] i_sw ;
13     reg [NB_SW - 1 : 0] sw_tmp ;
14     reg ck_rst, CLK100MHZ, reset_tmp;
15
16     integer fid_reset, fid_sw;
17     integer code_error, code_error1;
18     integer ptr_sw;
19
20     initial begin
21         fid_reset = $fopen("./vectors/reset.out"
22             , "r");
23         if (fid_reset==0) $stop;
24         fid_sw = $fopen("./vectors/switch.out", "r"
25             );
26         if (fid_sw==0) $stop;
27         CLK100MHZ = 1'b0 ;
28     end
```

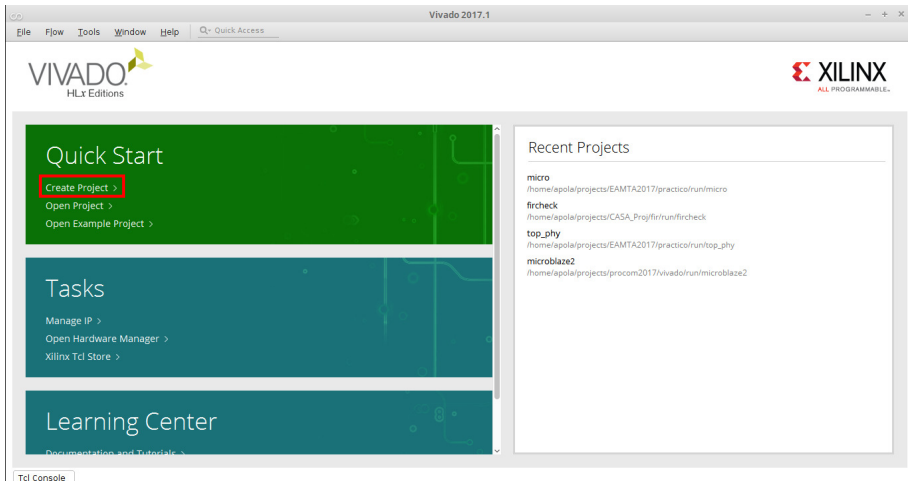
```
1 always #5 CLK100MHZ = ~CLK100MHZ;
2
3 always@(posedge CLK100MHZ) begin
4     code_error <=
5         $fscanf(fid_reset, "%d", reset_tmp);
6     if (code_error!=1) $stop;
7
8     for (ptr_sw=0; ptr_sw<NB_SW;
9         ptr_sw = ptr_sw+1) begin
10         code_error1 <=
11             $fscanf(fid_sw, "%d", sw_tmp[(ptr_sw+1)
12                 -1 -: 1]);
13         if (code_error1!=1) $stop;
14     end
15
16     ck_rst <= reset_tmp;
17     i_sw <= sw_tmp;
18     $display("%d", ck_rst);
19 end
20
21 shiftleds
22     u_shiftleds
23         (.o_led (o_led) ,
24         .i_sw (i_sw) ,
25         .ck_rst (ck_rst) ,
26         .CLK100MHZ (CLK100MHZ));
27 endmodule // tb_shiftleds
```

Herramienta Vivado



Herramienta Vivado

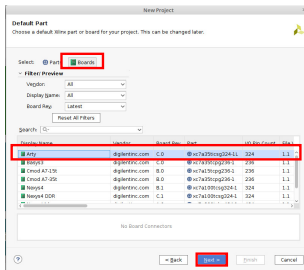
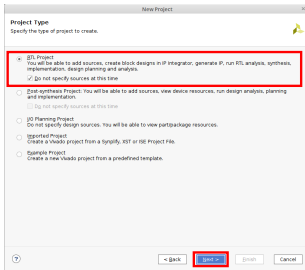
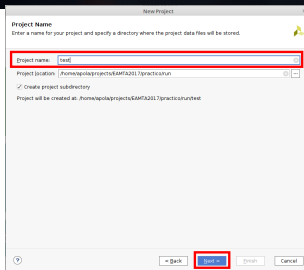
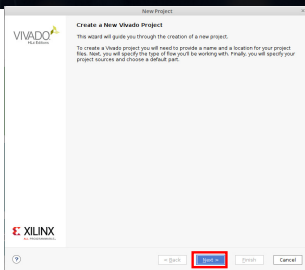
Vivado



Crea un nuevo proyecto

Herramienta Vivado

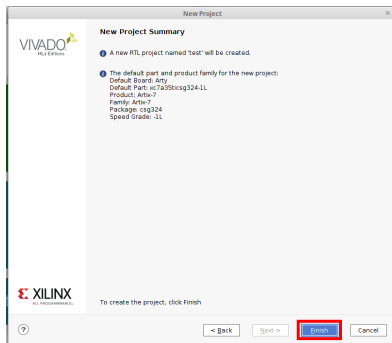
Vivado



Configura el kit de trabajo

Herramienta Vivado

Vivado



Configura el kit de trabajo

Herramienta Vivado

Vivado

The screenshot displays the Vivado 2017.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The main workspace is divided into several panels:

- Flow Navigator:** Located on the left, it shows the project hierarchy with options like Settings, Add Sources (highlighted with a red box), Language Templates, IP Catalog, and various design steps under IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, and IMPLEMENTATION.
- PROJECT MANAGER - test:** The central panel, which contains:
 - Sources:** A list of design sources including Design Sources, Constraints, and Simulation Sources. The 'Add Sources' button is highlighted.
 - Properties:** A panel below Sources, currently empty with the text 'Select an object to see properties'.
- Project Summary:** A panel on the right showing project details such as Project name, Project location, Product family, Project part, Top module name, Target language, and Simulator language.
- Design Runs:** A table at the bottom showing the status of design runs.

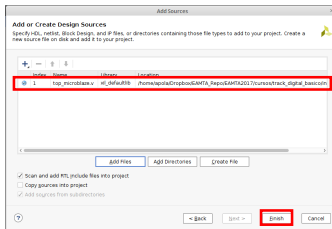
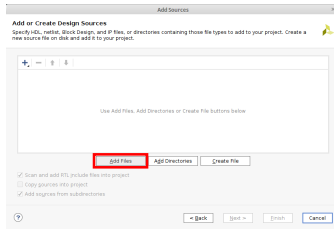
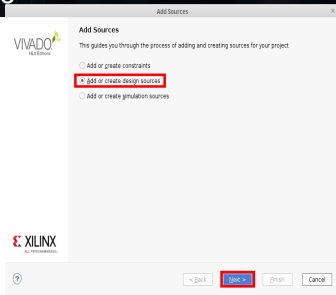
The Design Runs table is as follows:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Agrega nuevas fuentes a *Design Sources*

Herramienta Vivado

Vivado



Seleccionar todos los archivos verilog relacionados al diseño

Herramienta Vivado

Vivado

The screenshot displays the Vivado IDE interface for a project named 'test'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left lists project stages: PROJECT MANAGER (with 'Add Sources' highlighted), IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, and IMPLEMENTATION. The 'PROJECT MANAGER - test' window shows a 'Sources' list with 'Design Sources', 'Constraints', and 'Simulation Sources'. The 'Properties' window is empty, prompting the user to 'Select an object to see properties'. The 'Project Summary' window shows details for 'test', including project location, product family (Artix-7), project part (Arty (xc7a35ticsg324-1L)), and target language (Verilog). The 'Design Runs' tab at the bottom shows a table of synthesis runs.

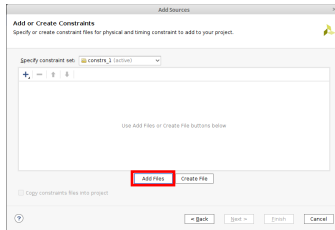
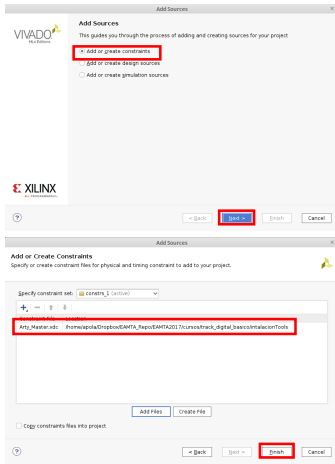
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Specify and/or create source files to add to the project

Agrega nuevas fuentes a *Constraints*

Herramienta Vivado

Vivado



Selecciona el archivo xdc

Herramienta Vivado

Vivado

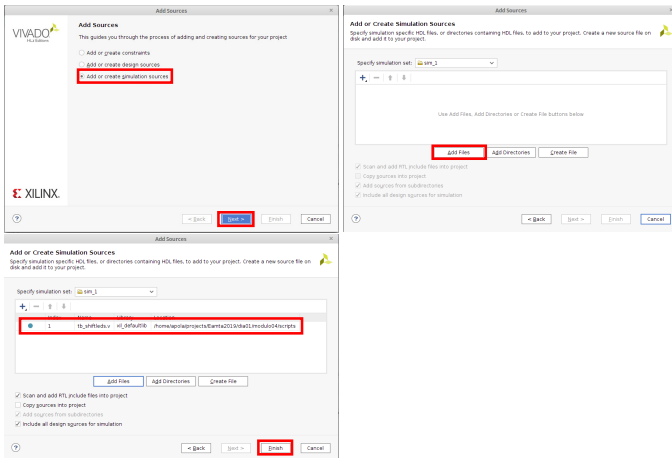
The screenshot displays the Vivado IDE interface for a project named 'test'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left shows the project hierarchy with 'Add Sources' highlighted under 'PROJECT MANAGER'. The 'PROJECT MANAGER - test' window is open, showing 'Sources' with 'Design Sources', 'Constraints', and 'Simulation Sources'. The 'Simulation Sources' section is expanded, showing 'sim_1'. The 'Properties' window is also open, displaying 'Select an object to see properties'. The 'Project Summary' window on the right shows project details: Project name: test, Project location: /home/apola/projects/EAMTA2017/practico/run/test, Product family: Artix-7, Project part: Arty (xc7a35ticsg324-1L), Top module name: Not defined, Target language: Verilog, and Simulator language: Mixed. The 'Design Runs' table at the bottom shows the status of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Agrega nuevas fuentes a *Simulation Sources*

Herramienta Vivado

Vivado



Selecciona el archivo verilog para simulación

Herramienta Vivado

Run Simulation - Run Behavioral Simulation

The screenshot displays the Vivado IDE interface for a project named 'leds'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, Run, and Help. The 'Run' menu is open, showing 'Run' and 'Re-Load' options, both highlighted with red boxes. The 'Run' button in the toolbar is also highlighted with a red box. The 'Flow Navigator' on the left shows the 'SIMULATION' tab selected, with 'Run Simulation' highlighted. The 'Run Behavioral Simulation' option is also highlighted. The main workspace shows a 'Zoom Fit' button in the toolbar. The 'Name' and 'Value' table lists various signals and their values. The waveform viewer on the right shows a timing diagram for signals like o_led[3:0], o_led_b[3:0], o_led_g[3:0], i_sw[3:0], ck_rst, CLK100MHZ, N_LEDS[31:0], NB_SEL[31:0], NB_COUNT[31:0], and NB_SW[31:0]. The simulation time is 1 us.

Name	Value
> o_led[3:0]	1
> o_led_b[3:0]	1
> o_led_g[3:0]	0
> i_sw[3:0]	1
ck_rst	1
CLK100MHZ	0
> N_LEDS[31:0]	00000004
> NB_SEL[31:0]	00000002
> NB_COUNT[31:0]	0000000e
> NB_SW[31:0]	00000004

Simulando el comportamiento del diseño

Herramienta Vivado

Vivado

The screenshot shows the Vivado IDE interface for a project named 'test'. The title bar indicates the path: 'test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1'. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The 'Flow Navigator' on the left lists various project steps: IP Catalog, IP INTEGRATOR (Create Block Design, Open Block Design, Generate Block Design), SIMULATION (Run Simulation), RTL ANALYSIS (Open Elaborated Design), SYNTHESIS (Run Synthesis, Open Synthesized Design), IMPLEMENTATION (Run Implementation, Open Implemented Design), and PROGRAM AND DEBUG (Generate Bitstream, Open Hardware Manager). The 'Generate Bitstream' option is highlighted with a red box. The 'PROJECT MANAGER' pane shows the 'Sources' tab with a hierarchy of 'constrs_1 (1)' containing 'Arty_Master.xdc' and 'Simulation Sources (1)' containing 'sim_1 (1)'. The 'Properties' tab is empty, showing 'Select an object to see properties'. The 'Project Summary' pane on the right displays project details: Project name: test, Project location: /home/apola/projects/EAMTA2017/practico/run/test, Product family: Artix-7, Project part: Arty (xc7a35ticsg324-1L), Top module name: top_microblaze, Target language: Verilog, and Simulator language: Mixed. The 'Board Part' section is also visible. At the bottom, the 'Design Runs' table shows the status of synthesis and implementation runs.

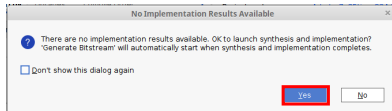
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed
synth_1	constrs_1	Not started														
impl_1	constrs_1	Not started														

Generate a programming file after implementation

Generar el *bitstream*

Herramienta Vivado

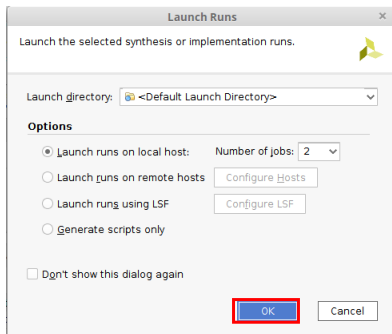
Vivado



Generar el *bitstream*

Herramienta Vivado

Vivado



Generar el *bitstream*

Herramienta Vivado

Vivado

The screenshot displays the Vivado 2017.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The title bar shows the project path: test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1. A red box highlights the 'Running synth_design' button in the top right corner, with a 'Cancel' link and a green checkmark icon next to it.

The left sidebar contains the 'Flow Navigator' with the following sections:

- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis**
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

The main workspace is divided into several panels:

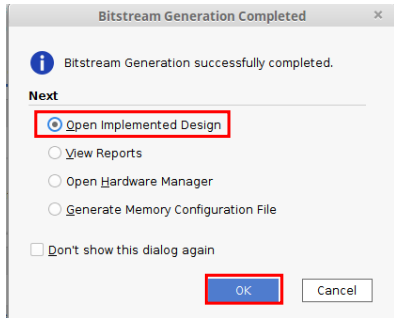
- PROJECT MANAGER - test**: Contains the 'Sources' panel showing a hierarchy of files (constrs_1, Arty_Master.xdc, Simulation Sources, sim_1) and the 'Properties' panel.
- Project Summary**: Displays project details such as Project name (test), Project location, Product family (Artix-7), Project part (Arty (xc7a35ticsg324-1L)), Top module name (top_microblaze), Target language (Verilog), and Simulator language (Mixed).
- Design Runs**: A table showing the progress of synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start
synth_1	constrs_1	Running synth_design...													7/1...
impl_1	constrs_1	Queued...													

Ejecutando tareas de implementación

Herramienta Vivado

Vivado



Abriendo el modelo implementado

Herramienta Vivado

Vivado

test - [/home/apola/projects/EAMTA2017/practico/run/test/test.xpr] - Vivado 2017.1

write_bitstream Complete

Default Layout

Flow Navigator

- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION**
 - Run Implementation
 - Open Implemented Design**
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks

Implemented DESIGN - xc7a35ticsg324-1L (active)

Sources Netlist x

- top_microblaze
- Nets (21)
- Leaf Cells (19)

Properties

Select an object to see properties

Project Summary x Device x

Timing x

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 7.592 ns	Worst Hold Slack (WHS): 0.130 ns	Worst Pulse Width Slack (WPWS):
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:
Total Number of Endpoints: 6	Total Number of Endpoints: 6	Total Number of Endpoints:

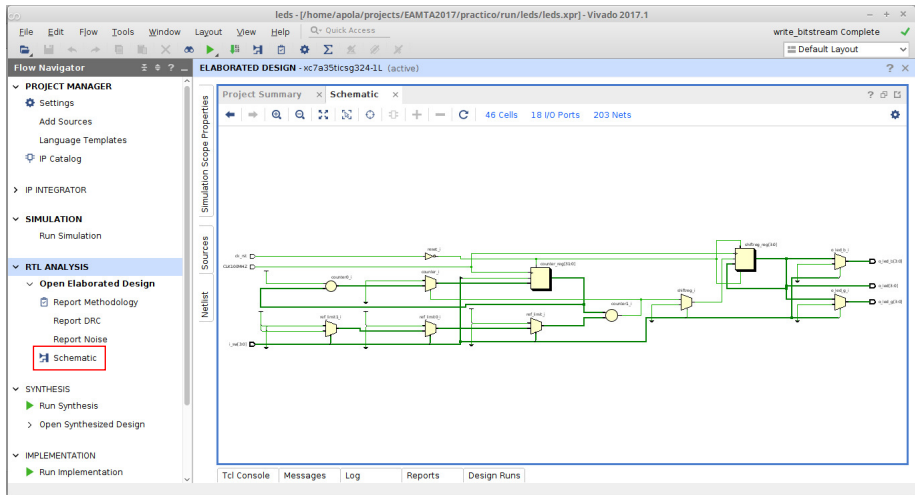
All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

Diseño implementado

Herramienta Vivado

RTL Schematic



Esquemático RTL

Herramienta Vivado

Synthesis - Schematic

The screenshot displays the Vivado 2017.1 interface. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The title bar shows the project path: `leds - [/home/apola/projects/EAMTA2017/practico/run/leds/leds.xpr] - Vivado 2017.1`. The right side of the top bar indicates `write_bitstream Complete` with a green checkmark and a dropdown menu set to `Default Layout`.

The left sidebar contains the **Flow Navigator** with the following sections:

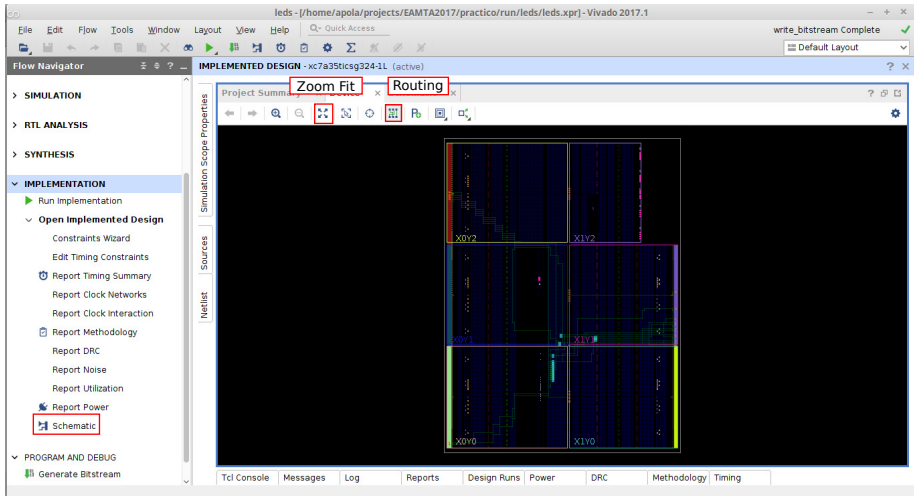
- SIMULATION**
- RTL ANALYSIS**
- SYNTHESIS** (highlighted)
 - Run Synthesis
 - Open Synthesized Design**
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic** (highlighted with a red box)
- IMPLEMENTATION**
 - Run Implementation
 - Open Implemented Design

The main workspace shows the **SYNTHESIZED DESIGN - xc7a35ticsg324-1L (active)**. The top of the workspace has tabs for `Project Summary`, `Device`, and `Schematic` (selected). Below the tabs, a status bar indicates `131 Cells 18 I/O Ports 206 Nets`. The central area displays a complex schematic diagram with numerous logic blocks (represented by yellow squares) interconnected by a dense network of green lines. On the left side of the workspace, there are vertical tabs for `Simulation Scope Properties`, `Sources`, and `Netlist`. At the bottom of the workspace, there are tabs for `Tcl Console`, `Messages`, `Log`, `Reports`, and `Design Runs`.

Esquemático Implementación

Herramienta Vivado

Implementation - Schematic



Implementation