High Speed CMOS Logic – 74HC4060

14-Stage Binary Ripple Counter / Divider with Oscillator in bare die form

Rev 1.0
26/11/17

Description

The 74HC4060 is produced on a 2.5µm 5V CMOS process with high speed LSTTL performance combined with CMOS low power consumption. The device consists of 14 master–slave flip–flops & an oscillator with frequency controlled either by crystal or by external RC circuit. Each flip–flop output feeds the next where each output frequency is half the preceding one. A high-to-low transition on the clock input increments the counter. The active–high Reset is asynchronous & disables the oscillator for low standby power consumption. Ten kinds of divided output are provided; 4 to 10 & 12 to 14 stage inclusive. Maximum division available at Q12 is 1/16384 of oscillator frequency.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with CD4060B.

Ordering Information

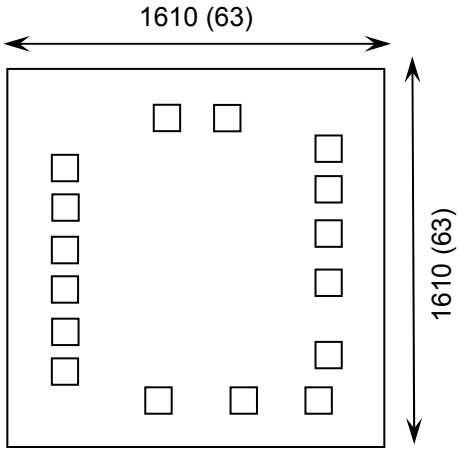
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC4060

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1610 x 1610 63 x 63	µm mils
Minimum Bond Pad Size	110 x 110 4 x 4	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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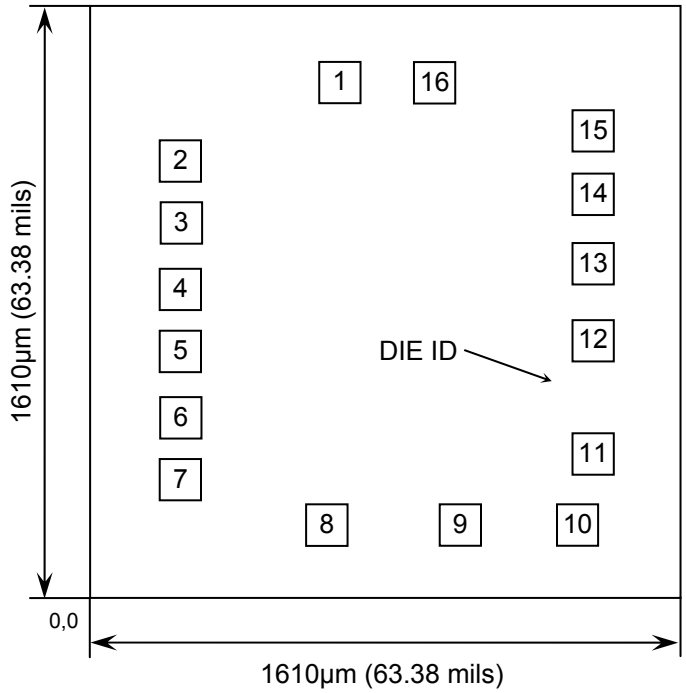
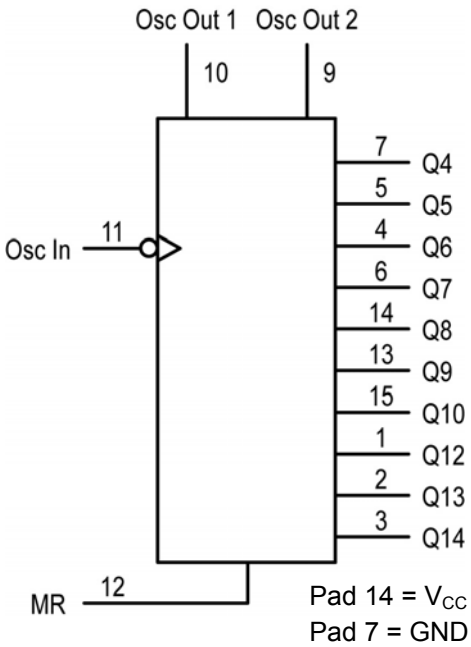
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	Q12	0.610	1.350
2	Q13	0.190	1.140
3	Q14	0.190	0.970
4	Q6	0.190	0.790
5	Q5	0.190	0.620
6	Q7	0.190	0.440
7	Q4	0.190	0.270
8	GND	0.590	0.150
9	O_{SC} OUT2	0.950	0.150
10	O_{SC} OUT1	1.270	0.150
11	O_{SC} IN	1.310	0.340
12	MR	1.310	0.650
13	Q9	1.310	0.860
14	Q8	1.310	1.050
15	Q10	1.310	1.220
16	V_{CC}	0.880	1.350
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Function Table

CLOCK	RESET	OUTPUT STAGE
⌐	L	NO CHANGE
¬	L	ADVANCE TO NEXT STATE
X	H	ALL OUTPUTS ARE LOW

Pad Descriptions

INPUTS
Osc IN (Pad 11)
Negative–edge triggering clock input. A high–to–low transition on this input advances the state of the counter. Osc IN may be driven by an external clock source.

CONTROL INPUTS
MR (Pad 12)
Active–high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS
Q4—Q10, Q12–Q14 (Pads 7, 5, 4, 6, 13, 15, 1, 2, 3) Active–high outputs. Each Qn output divides the Clock input frequency by 2^N. The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc OUT1, Osc OUT2 (Pads 9, 10)
Oscillator outputs. These pads are used in conjunction with Osc IN and the external components to form an oscillator. When Osc IN is being driven with an external clock source, Osc OUT1 and Osc OUT2 must be left open circuited. With the crystal oscillator in RC configuration, Osc OUT2 must be left open circuited.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2[4]	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	0	+85	°C
Input Rise or Fall Times	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.
4. The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0V by driving Pad 11 with an external clock source.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage (Q4–Q10, Q12–Q14)	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 2.4mA$	2.48	2.34	2.34	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0mA$	3.98	3.84	3.84	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 5.2mA$	5.48	5.34	5.34	
Maximum Low-Level Output Voltage (Q4–Q10, Q12–Q14)	V_{OL}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 2.4mA$	0.26	0.33	0.33	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0mA$	0.26	0.33	0.33	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 5.2mA$	0.26	0.33	0.33	
Minimum High-Level Output Voltage ($O_{SC}OUT1$, $O_{SC}OUT2$)	V_{OH}	2.0V	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \le 0.7mA$	2.48	2.34	2.34	V
		4.5V	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \le 1.0mA$	3.98	3.84	3.84	
		6.0V	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \le 1.3mA$	5.48	5.34	5.34	

5. $0^{\circ}C \le T_J \le +85^{\circ}C$

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Low-Level Output Voltage ($O_{SC}OUT1$, $O_{SC}OUT2$)	V_{OL}	2.0V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 0.7mA$	0.26	0.33	0.33	V
		4.5V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 1.0mA$	0.26	0.33	0.33	
		6.0V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 1.3mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	4	80	80	µA

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1,4)	f_{max}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	6	9	9	MHz
		3.0V		10	14	14	
		4.5V		30	28	28	
		6.0V		50	45	45	
Maximum Propagation Delay, O_{SC} IN to Q4[7] (Figure 1,4)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	300	375	375	ns
		3.0V		180	200	200	
		4.5V		60	75	75	
		6.0V		51	64	64	
Maximum Propagation Delay, O_{SC} IN to Q14[7] (Figure 1,4)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	500	750	750	ns
		3.0V		350	450	450	
		4.5V		250	275	275	
		6.0V		200	220	220	
Maximum Propagation Delay, Reset to any Q (Figure 2,4)	t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	195	245	245	ns
		3.0V		75	100	100	
		4.5V		39	49	49	
		6.0V		33	42	42	

6. Not production tested in die form, characterized by chip design and tested in package.

7. For $T_J = 25°C$ and $C_L = 50$ pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$V_{CC} = 2.0$ V: $t_P = [93.7 + 59.3 (n–1)]$ ns $V_{CC} = 3.0$ V: $t_P = [61.5+ 34.4 (n–1)]$ ns

$V_{CC} = 4.5$ V: $t_P = [30.25 + 14.6 (n–1)]$ ns $V_{CC} = 6.0$ V: $t_P = [24.4 + 12 (n–1)]$ ns

AC Electrical Characteristics continued[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Propagation Delay, Qn to Qn+1 (Figure 3,4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		60	75	75	
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Output Transition Time, any output (Figure 1,4)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		27	32	32	
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance[8]	C_{PD}	-	T_A = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				35			

8. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	t_{rec}	2.0V	$t_r = t_f$ = 6ns	100	125	125	ns
		3.0V		75	100	100	
		4.5V		20	25	25	
		6.0V		17	21	21	
Minimum Pulse Width, Clock (Figure 1)	t_w	2.0V	$t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		27	32	32	
		4.5V		15	19	19	
		6.0V		13	16	16	
Minimum Pulse Width, Reset (Figure 2)	t_w	2.0V	$t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		27	32	32	
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0V	$t_r = t_f$ = 6ns	1000	1000	1000	ns
		3.0V		800	800	800	
		4.5V		500	500	500	
		6.0V		400	400	400	

Switching Waveforms

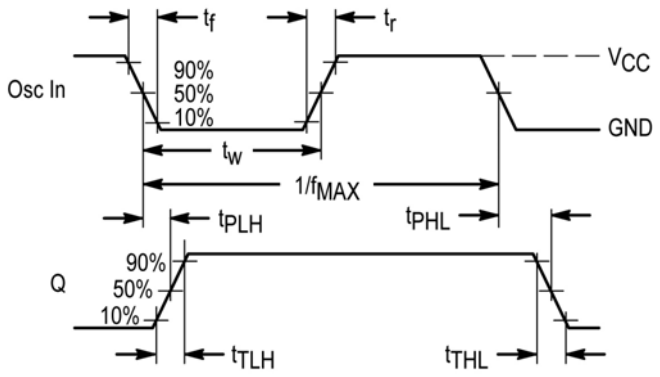


Figure 1 – Input to Output Propagation Delay & Timing

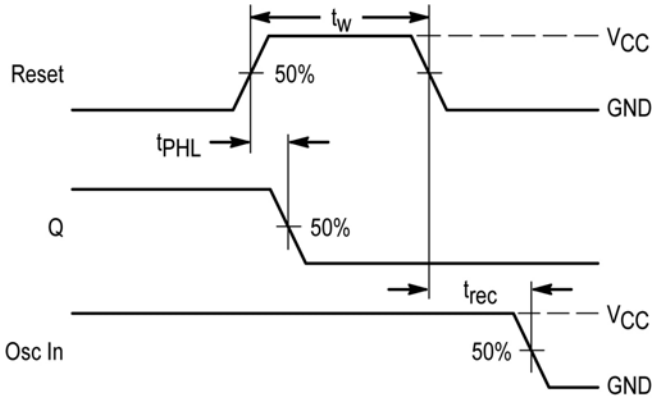


Figure 2 – Reset Timing

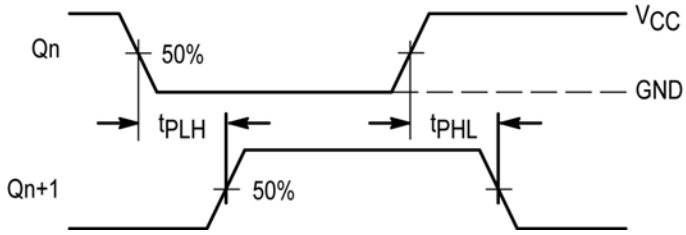
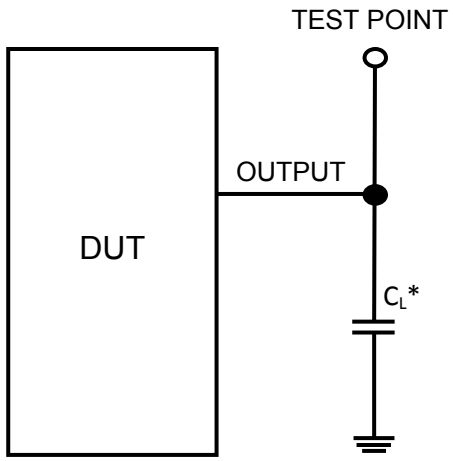


Figure 3 – Ripple output timing

Test Circuit



* Includes all probe and jig capacitance

Figure 4 – Test Setup