SAR ADC Finite State Machine
8-bit Successive Approximation Algorithm

start=0

IDLE

Store result
conversion_done=1

DONE

start=1

INIT

Set MSB=1
settle_counter=0

counter++
(settling...)

WAIT_SETTLE

counter >=
SETTLE_CYCLES

COMPARE

Sample
comparator

DECIDE

bit_index = 0
(conversion complete)

bit_index > 0
Keep/clear bit
bit_index--

NEXT_BIT

Set next bit=1
settle_counter=0