LECTURE NOTES

ON

MICROPROCESSORS AND MICROCONTROLLERS

Electronics and Communication Engineering

(UNIT-3: I/O Interface)

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Mrs.K.JEEVANA JYOTHI M.Tech
Asst.Proff in ECE Dept
Ramachandra College of Engineering

DepartmentofElectronicsandCommunicationEngineering
RAMACHANDRACOLLEGEOFENGINEERING
(Approved by AICTE, New Delhi, Permanently Affiliatedto JNTUK:Kakinada)
AccreditedByNAAC&NBA,AnISO9001:2015 certifiedInstitution
NH5BypassRoad,Vatluru(V),ELURU-534 007,W.G.Dist.,A.P,
Website:www.rcee.ac.in.

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RAMACHANDRACOLLEGE OF ENGINEERING

UNIT–III

I/O Interface:

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Concept: 1 8255 PPI– Architecture of 8255–Modes of operation

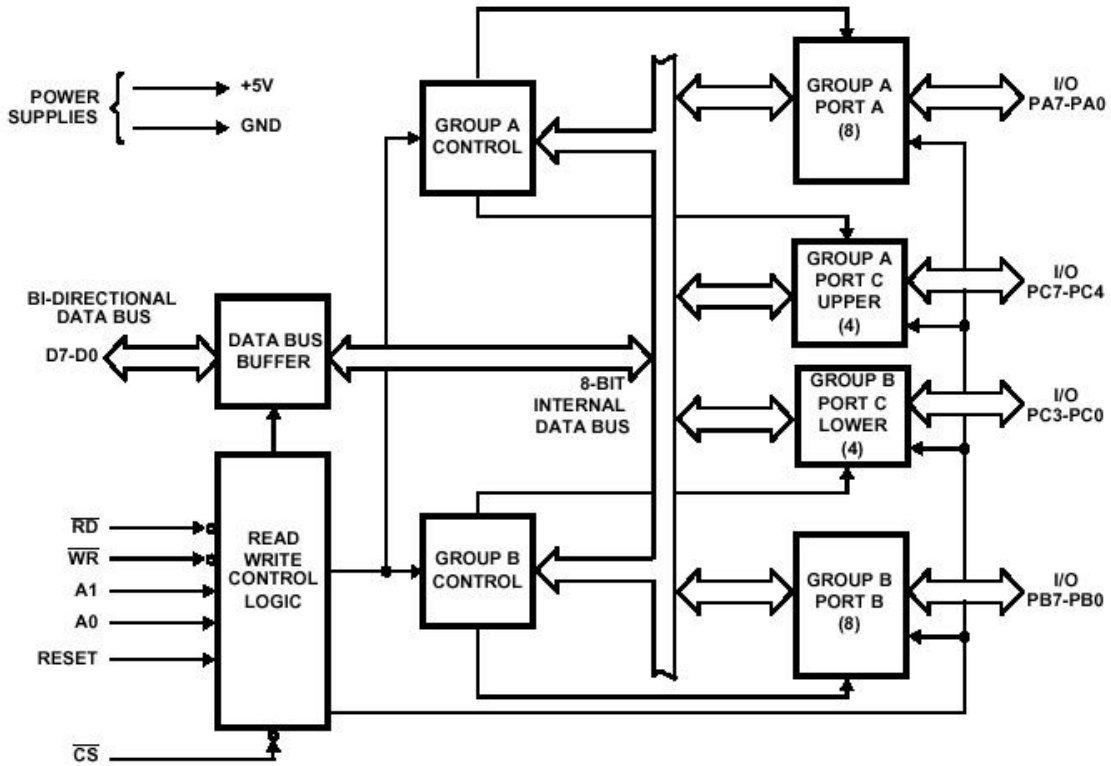
8255 has 24 I/O lines which may be individually programmed in two groups of 12 lines each or three groups of eight lines. The two groups of I/O pins are named as **Group-A** and **Group-B**.

There are three ports

- Port-A can be used as an 8-bit I/O port
- Port-B can be used as an 8-bit I/O port
- Port-C can be used as an 8-bit I/O port as two 4-bit ports, or to produce handshake signals for ports A&B.

Internal Architecture of 8255:

8255 is a widely used programmable parallel I/O device. This is also named as programmable peripheral input output port. 8255 is designed to use with 8 bit, 16 bit and higher capability microprocessor. This 8255 has 24 input/output lines, which can be individually programmed. These I/O lines can be grouped as Group A and Group B. Group A contains an 8-bit port A along with a 4-bit port C upper. Group B contains an 8-bit port B along with a 4-bit port, c lower. The C upper and C lower ports can be combined be use as an 8-bit port. Thus for an 8255 we can have either three 8 bit I/O ports or two 8 bit and two 4 bit ports. All these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register called as Control Word Register (CWR). The internal block diagram is shown in the fig.



Data Bus Buffer: This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the microprocessor. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic: The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the microprocessor Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls: The functional configuration of each port is programmed by the systems software. In essence, the microprocessor ``outputs" a control word to the 8255A. The control word contains information such as ``mode", ``bit set", ``bit reset", etc., that initializes the functional configuration of the 8255A. Each of the Control blocks (Group A and Group B) accepts ``commands" from the Read/Write Control Logic, receives ``control words" from the internal data bus and issues the proper commands to its associated ports. Control Group A - Port A and Port C upper (C7-C4) Control Group B - Port B and Port C lower (C3-C0)

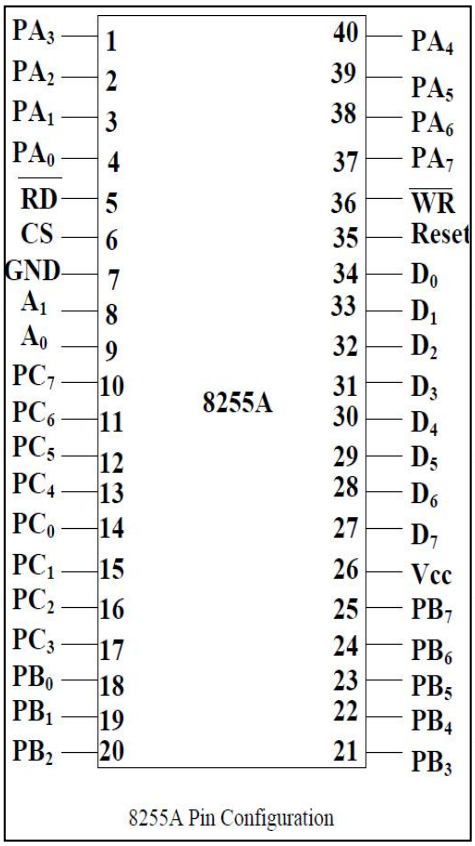
Ports A, B, and C: The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or ``personality" to further enhance the power and flexibility of the 8255A.

- Port A- One 8-bit data output latch/buffer and one 8-bit input latch buffer.
- Port B- One 8-bit data input/output latch/buffer.
- Port C-One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

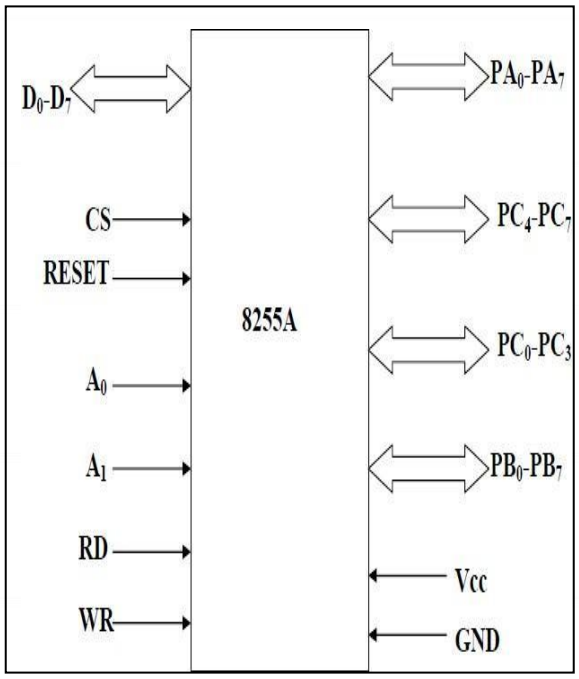
The read/write control logic controls the 8-bit data bus buffer. The read/write control logic manages all the internal and external transfers of both the data and control words. RD, WR, A1, A0 and RESET ate the input provided by the microprocessor to read/write control logic of 8255.

The bidirectional 8-bit data buffer is used to interface the 8255's internal data bus with the external system data bus. This buffer receives or transmits data up on the execution of input or output instructions by the microprocessor. The control word or the status information is also transferred through the buffer.

Signal Descriptions of 8255



8255A Pin Configuration



The Read/write control logic is having six signal lines. Which are RD, WR, RESET, CS, A0 and A1

RD [READ] :- This control signal enables the read operation. When the signal is low, the microprocessor reads data from a selected I/O port of 8255

WR [WRITE] :- This control signal enables the write operation. When the signal goes low the MPU (microprocessor) writes into a selected I/O port or the control register.

RESET :- This is an active high signal, A logic high on this line clears the control word register and set all ports in the input mode. (that is , set as input port by default after reset)

$\overline{\text{CS}}$ [CHIP SELECT] :- This is a Chip Select line. If the line goes low it enables the 8255 to respond to RD and WR signals.

A1 – A0 :- These are address lines driven by the microprocessor. These address lines are used for selecting any one of the three ports or a control word.

$\overline{\text{CS}}$	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 is not selected.

$PA_7 – PA_0$:- These are eight port A lines that act either as input or output lines depending up on the control word loaded into the control word register.

PC7 – PC4 :- These are four Port C upper lines that can act as input or output lines. This port can be used for the generation of handshake lines.

PC3 – PC0 : - These are four port C lower lines that can act as input or output lines. This port can also be used for the generation of handshake lines.

PB0 – PB7 :- These are 8 port B lines which can be input or output lines in the same way as port A

D0 – D7 :- These are the data bus lines that carry data or control word to/from the microprocessor.

This 8255 is a widely used, flexible and economical I/O device that can be used with almost all microprocessors when multiple I/O ports are required. 8255 is a 40 pin IC.

MODES OF OPERATION OF 8255

These are two basic modes of operation of 8255.

- Bit Set-Reset mode (BSR)
- I/O mode

In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.

In I/O mode, the 8255 ports work as programmable I/O ports. Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications.

- Mode 0 (Basic I/O mode)
- Mode 1 (Strobed input/output mode)
- Mode 2 (Strobed bidirectional I/O)

All these modes can be selected by programming a register internal to 8255 known as CWR (Control Word Register) which has two formats. One is for BSR mode of operation and second one is for I/O mode of operation.

BSR Mode:

In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR as given in table.

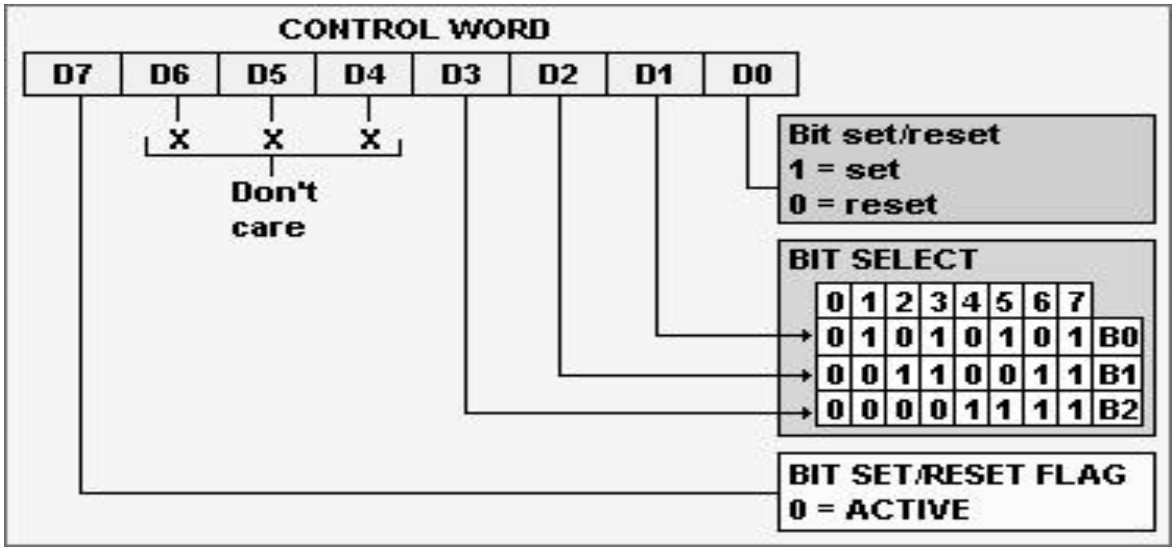


Fig. Control Word Register Format for BSR mode

I/O Modes: The Control Word Register format for I/O mode of operation is shown below.

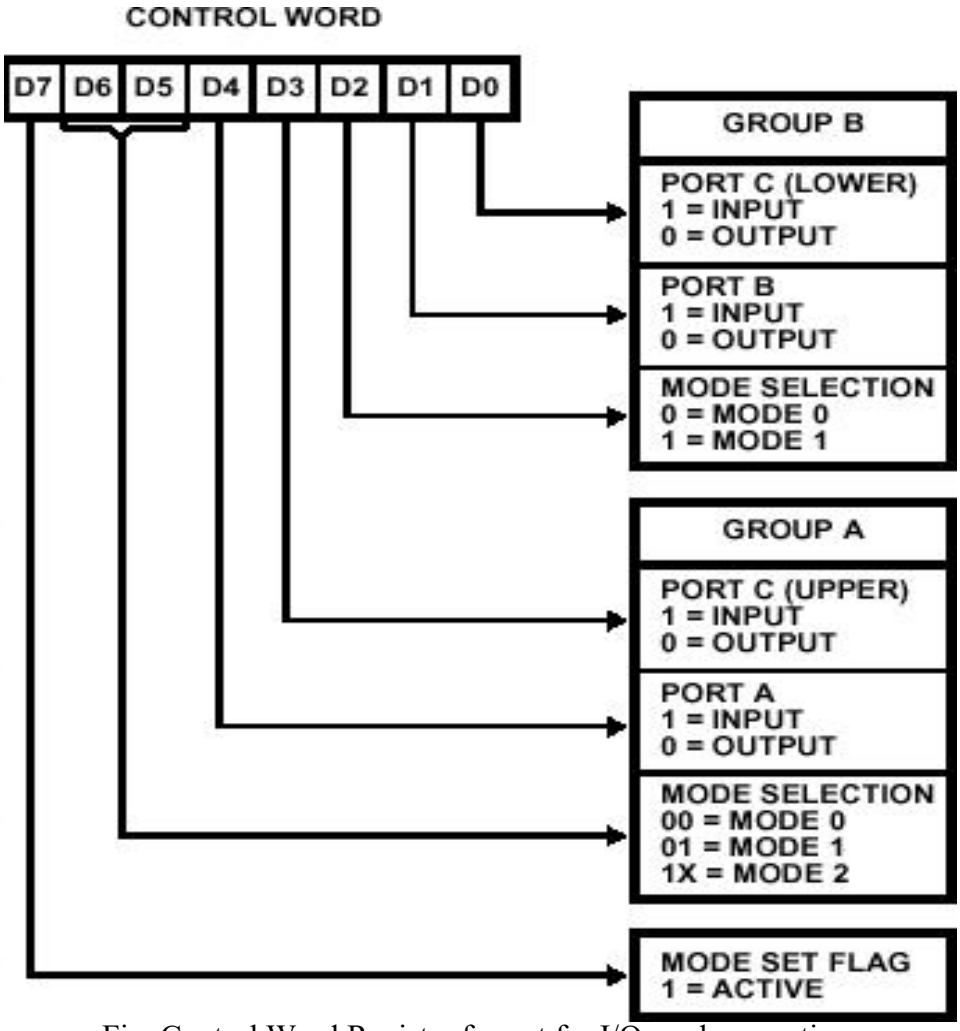


Fig. Control Word Register format for I/O mode operation

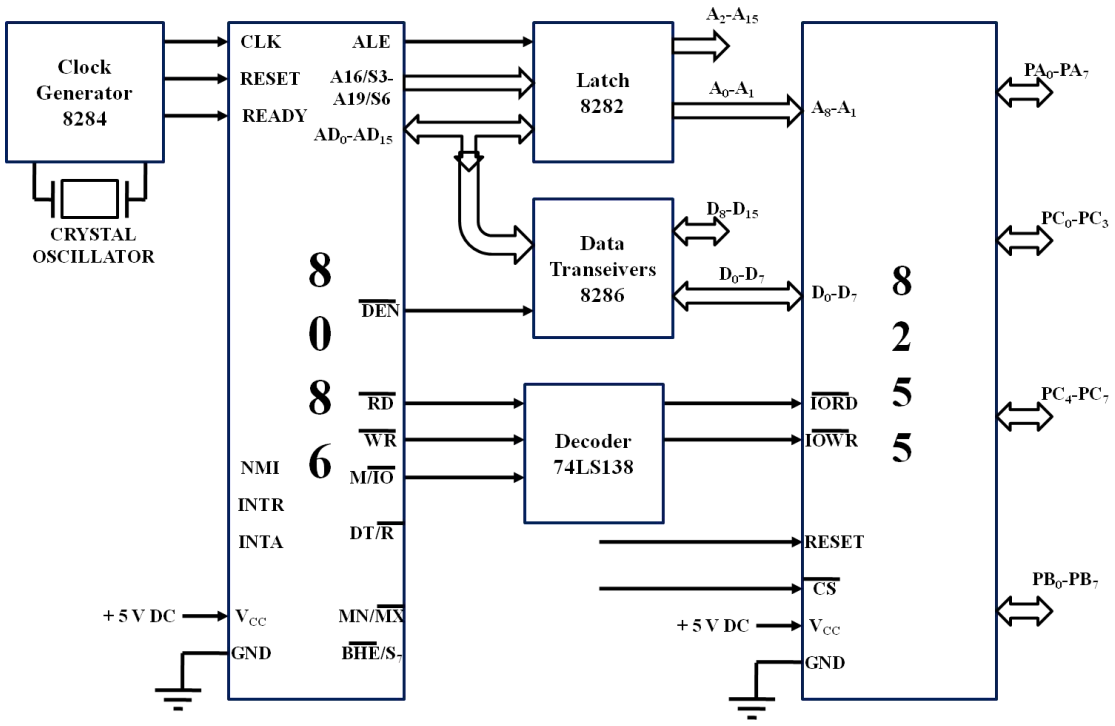
Mode 0 (Basic I/O mode): This mode is also called as basic input/output mode. When u want to use a port for simple input or output without handshaking, u initialize that port in mode 0.If both the port A and port B are initialized in mode 0, then the two halves of port C can be used together as an additional 8-bit port, or they can be used individually as two 4-bit ports. When used as outputs, the port C lines can be individually

set or reset by sending a special control word to the control register address. The two halves of port C are independent, so one half can be initialized as input, and the other half initialized as output.

Mode 1: (Strobed input/output mode): when you want to use port A or port B for a handshake (strobed) input or output operation, you initialize that port in mode 1. In this mode, some of ht epins of port C function as handshake lines. Pins PC0, PC1, and PC2 function as handshake lines for port B if it is initialized in mode 1. If port A is initialized as a handshake (mode 1) input port, then three pins PC3, PC4, and PC5 function as handshake signals. Pins PC6 and PC7 are available for use as input lines or output lines. If port A is initialized as a handshake output port, then port C pins PC3,PC6,and PC7 function as handshake signals. Port C pins PC4 and PC5 are available for use as input or output lines.

Mode 2 (Strobed bidirectional I/O): This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow

Concept: 2– Interfacing I/O devices to 8086 using 8255



Concept: 3–Interfacing A to D converters– Interfacing D to A converters

- In most of the cases, the PPI 8255 is used for interfacing the analog to digital converters with a microprocessor. The analog to digital converter is treated as an input device by the microprocessor, that sends an initializing signal to the ADC to start the analog to digital data conversion process.
- The process of analog to digital conversion is a slow process, and the microprocessor has to wait for the digital data till the conversion is over. After the conversion is over, the ADC sends end of

conversion EOC signal to inform the microprocessor about it and the result is ready at the output buffer of the ADC.

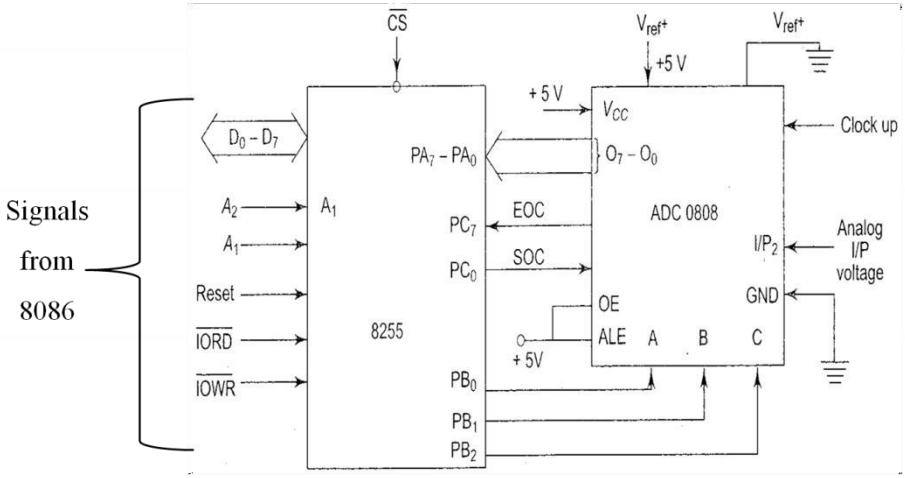
- These tasks of issuing an SOC pulse to ADC, reading EOC signal from the ADC and reading the digital output of the ADC are carried out by the CPU using 8255 I/O ports.
- The time taken by the ADC from the active edge of SOC pulse till the active edge of EOC signal is called as the conversion delay of the ADC.
- The selection of ADC for a particular application is done, keeping in mind the required speed, resolution and the cost factor.

General algorithm for ADC interfacing contains the following steps

- Ensure the stability of analog input, applied to the ADC
- Issue start of conversion SOC pulse to ADC
- Read end of conversion EOC signal to mark the end of conversion process
- Read digital data output of the ADC as equivalent digital output.

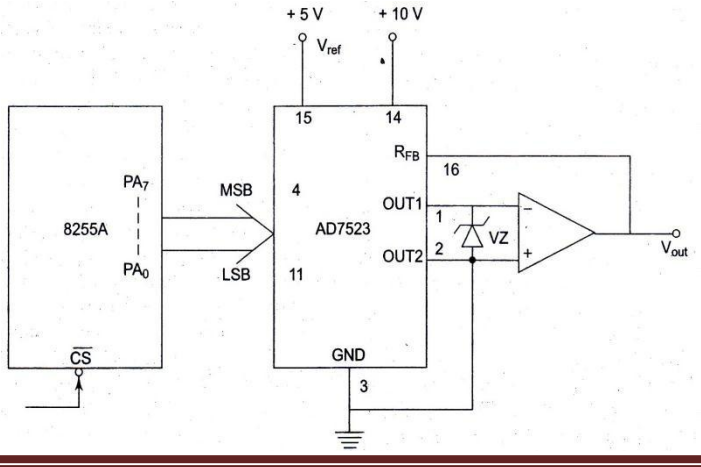
If may be noted that the analog input voltage must be a constant at the input of the ADC right from the beginning to the end of the conversion to get correct result. **Sample & hold** circuit which sample the analog signal and holds it constant for a specified time duration.

The analog to digital converter chips 0808 and 0809 are 8-bit CMOS, successive approximation converters. It is fastest technique. The conversion delay is 100 μs at a clock frequency of 640 kHz, which is quite low as compared to other converters.

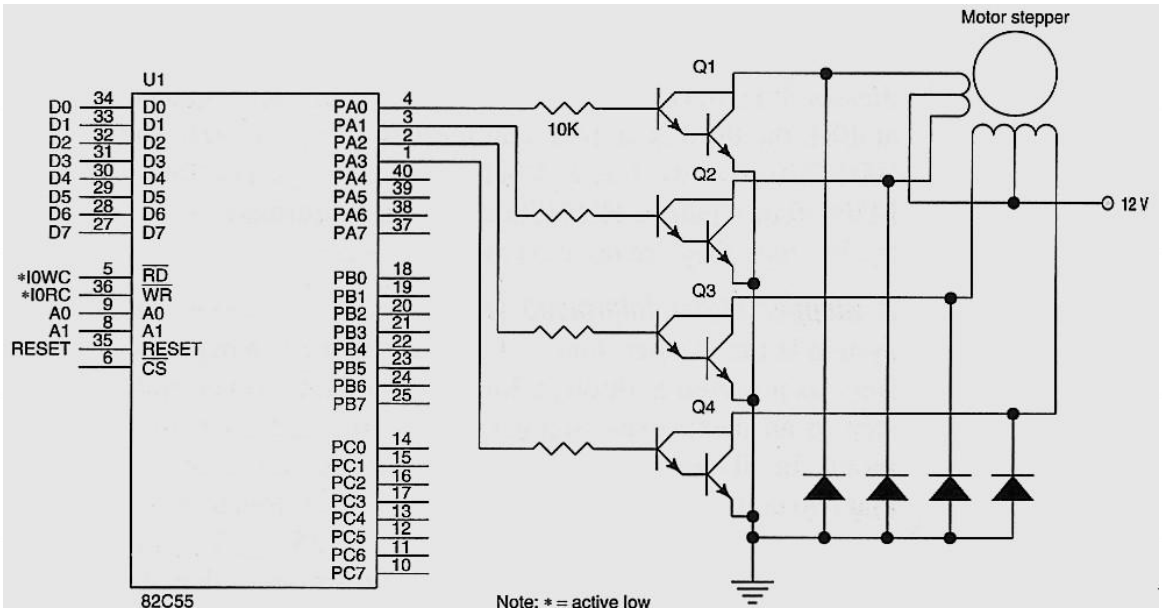


Interfacing Digital to Analog Converters (DAC)

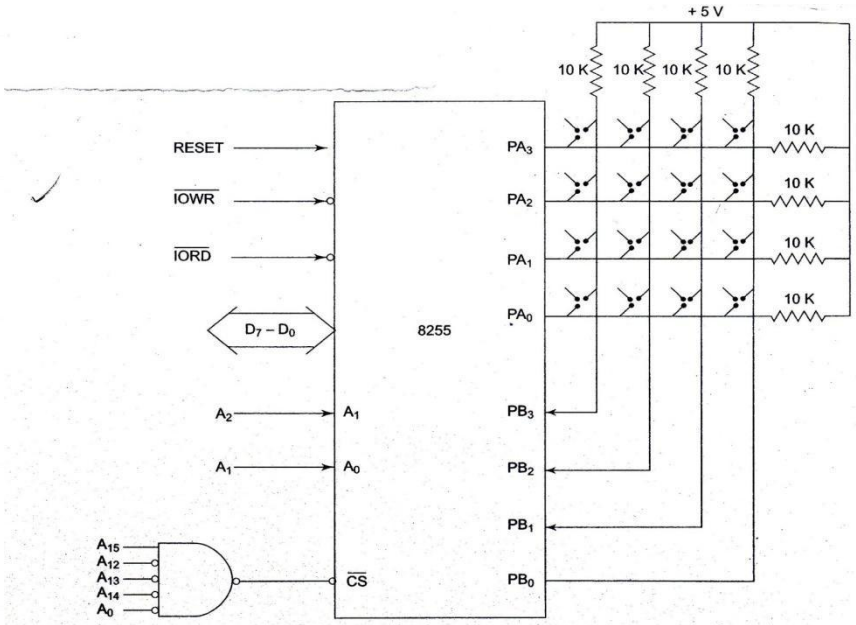
The Digital to Analog Converters (DAC) convert binary numbers into their analog equivalent voltages. The DAC find applications in areas like Digitally controlled gains, Motor speed controls, Programmable gain amplifiers etc.



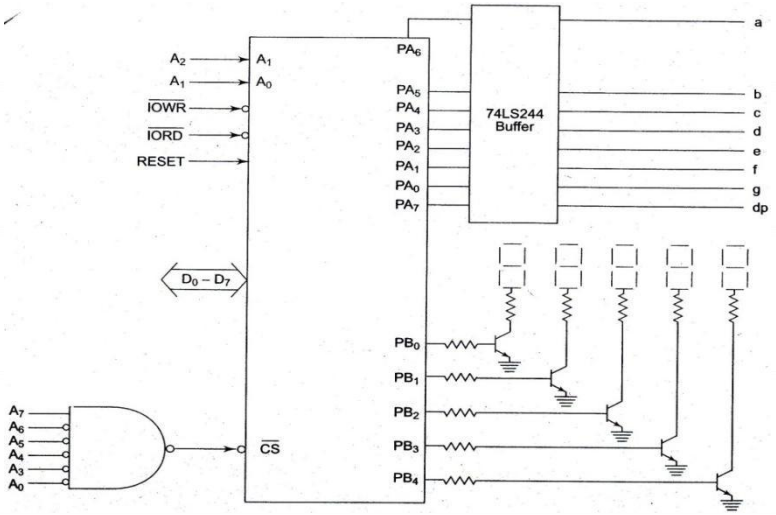
Concept: 4– Stepper motor interfacing



Keyboard interfacing with 8086 through 8255



7 segment display interfacing with 8086 through 8255



- In the design of all computers, semiconductor memories are used as primary storage for data and code. They are connected directly to the CPU and they are the memory that the CPU asks for information (code or data). Among the most widely used are **RAM and ROM.**

Memory Capacity

- The number of bits that a semiconductor memory chip can store is called its chip capacity (bits or bytes)

Memory Organization

- Each memory chip contains 2^x locations where x is the number of address pins on the chip
- Each location contains y bits, where y is the number of data pins on the chip
- The entire chip will contain 2^x *y bits

Memory Speed (access time)

- Each memory device has at least one chip select (CS) or chip enable (CE) or select (S) pin that enables the memory device. This enables read and/or write operations.
- Each memory device has at least one control pin. For ROMs, an output enable (OE) or gate (G) is present. The OE pin enables and disables a set of tristate buffers. For RAMs, a read-write (R/W) or write enable (WE) and read enable (OE) are present.

ROM (Read Only Memory)

- ROM is the type of memory that does not lose its contents when power is turned off. It is also called nonvolatile memory.

PROM (Programmable Memory)

- User programmable (one-time programmable) memory

EEPROM (Electrically Erasable ROM)

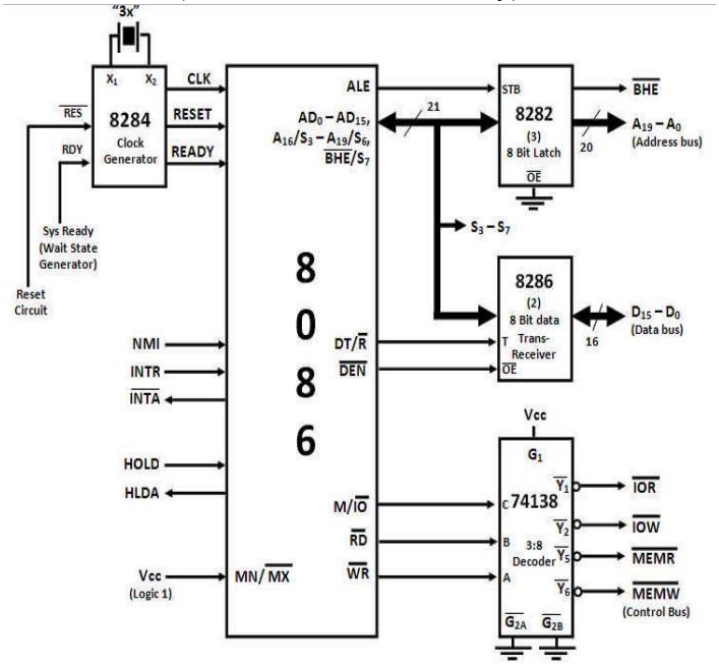
- Method of erasure is electrical

Flash Memory EPROM

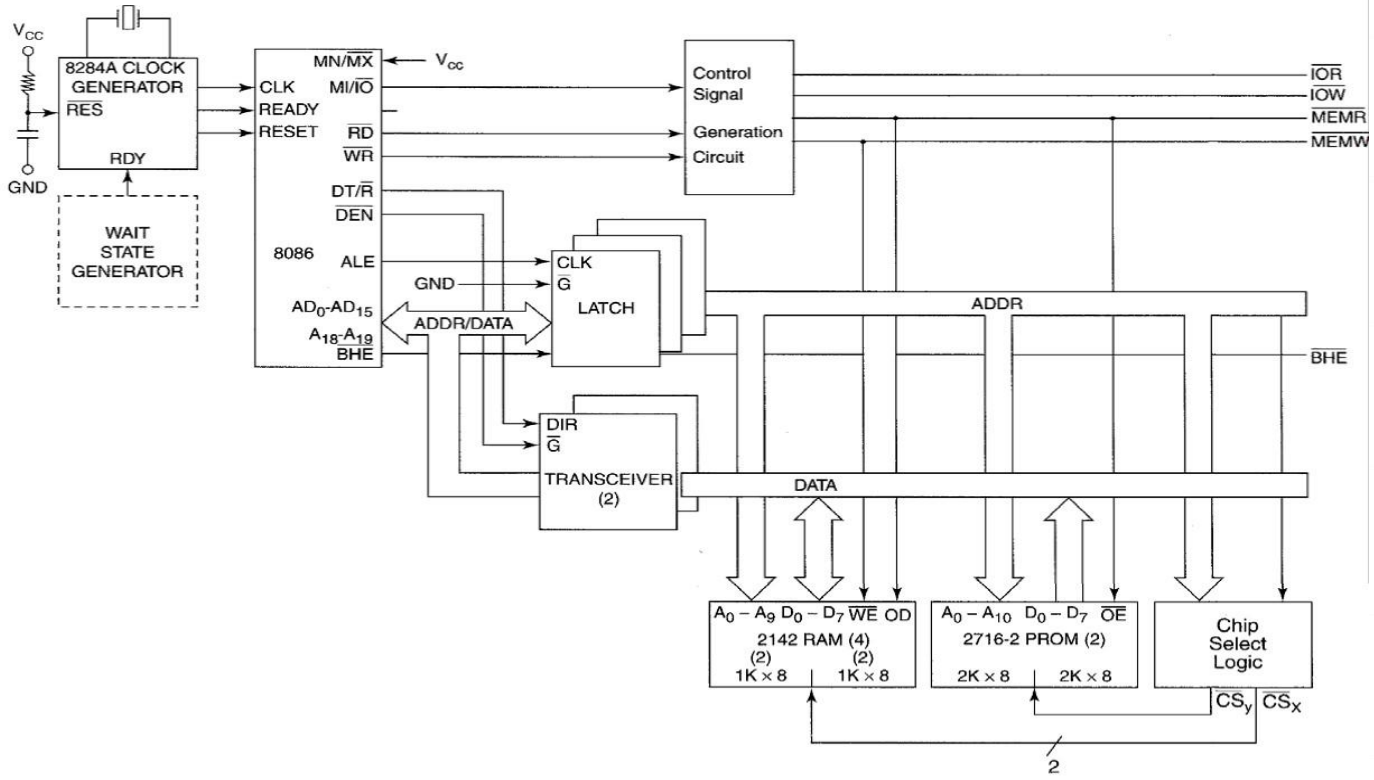
- First, the process of erasure of the entire contents takes less than a second, or one might say in a flash, hence its name: flash memory. When flash memory's contents are erased, the entire device is erased. Even though flash memories are writeable, like EPROMs they find their widest use in microcomputer systems for storage of firmware

RAM (Random Access Memory)

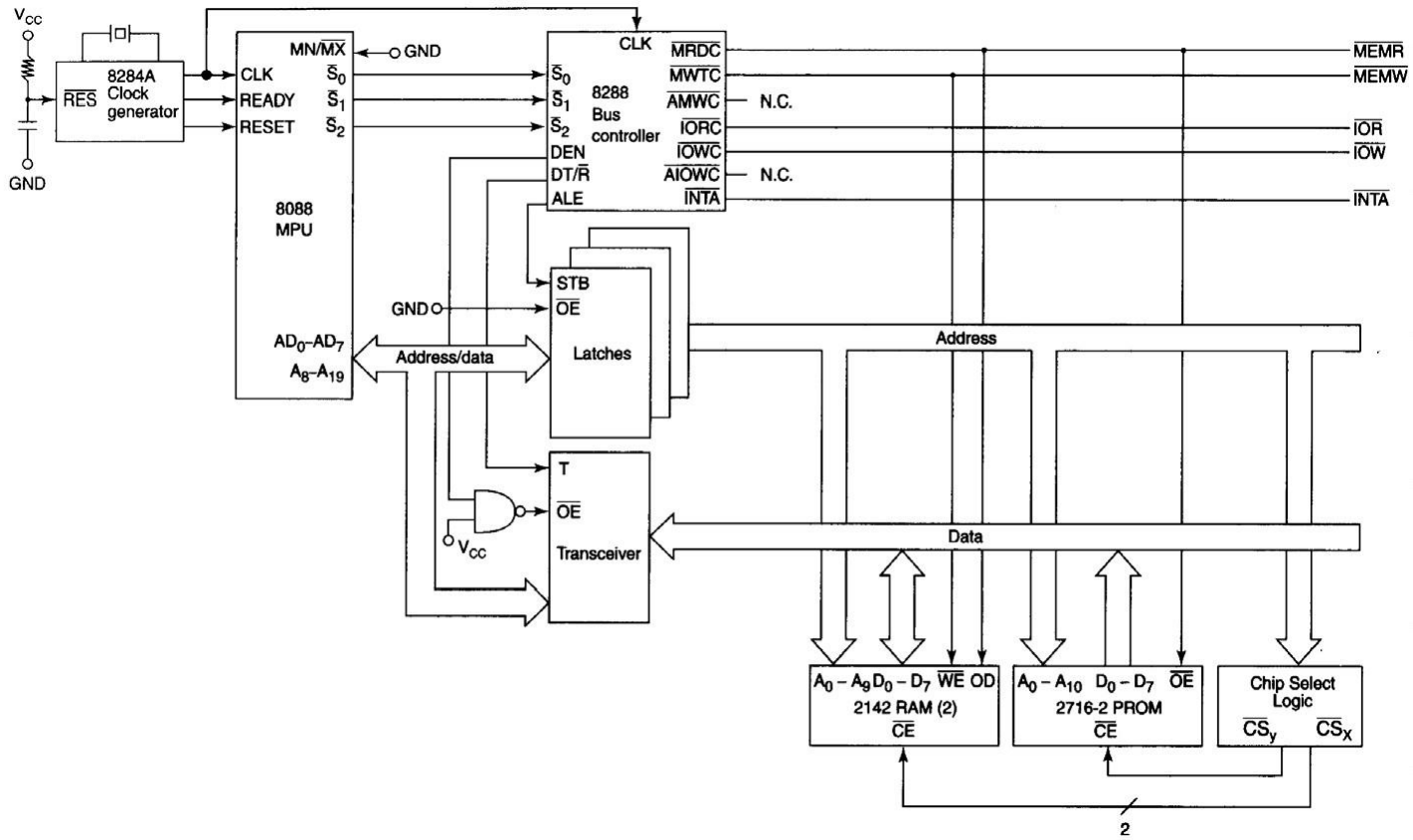
- RAM memory is called volatile memory since cutting off the power to the IC will mean the loss of data. Also referred to as R/W M (Read And Write Memory)



Memory Interfacing Circuit for 8086

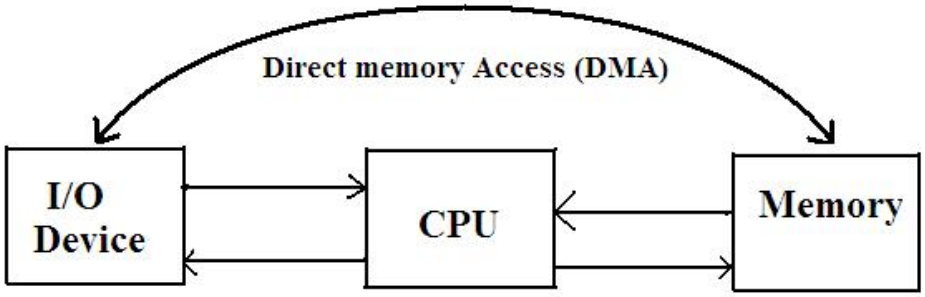


Memory Interfacing circuit with 8086 (Minimum mode)



Memory Interfacing circuit with 8086 (Maximum mode)

time consuming operation and the CPUs time is wasted. If the I/O port can directly access memory for data transfer, without CPU intervention, that will be more efficient. So, in any microprocessor system, if the data transfer occurs without the intervention of the CPU, that method is known as Direct Memory Transfer technique (DMA). This is explained in the figure below.



As an example , the data transfer between a floppy disk and a R/W memory in a computer system is based on DMA. To perform the DMA transfer in 8085 based systems two pins HOLD and HLDA (Hold Acknowledge) are used. An I/O device which wishes to transfer data using DMA scheme, sends the HOLD signal to the CPU. On receiving the HOLD signal from an I/O device, the CPU sends a hold acknowledge signal (HLDA) to the I/O device to indicate that it has received the HOLD request and it will give-up the buses in the next machine cycle. The I/O device takes over the control of buses and directly transfer data to the memory or reads data from the memory.

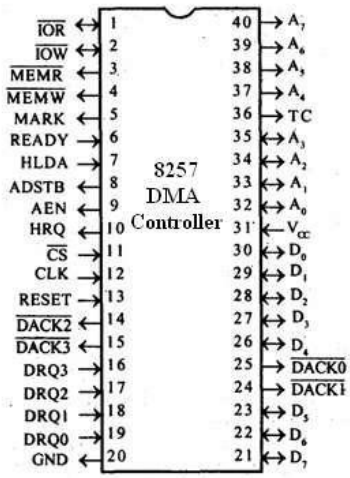
DMA Controller - Intel 8237/8257

In Direct Memory Access technique, the data transfer takes place without the intervention of CPU, so there must be a controller circuit which is programmable and which can perform the data transfer effectively. For this purpose Intel introduced the controller chip 8257 which is known as DMA controller. A DMA controller temporarily borrows the address bus, data bus and control bus from the microprocessor and transfers the data bytes directly from the port to memory devices. As the transfer is handled totally by hardware, it is much faster than software program instructions. A DMA controller can also transfer data from memory to a port.

Salient Features

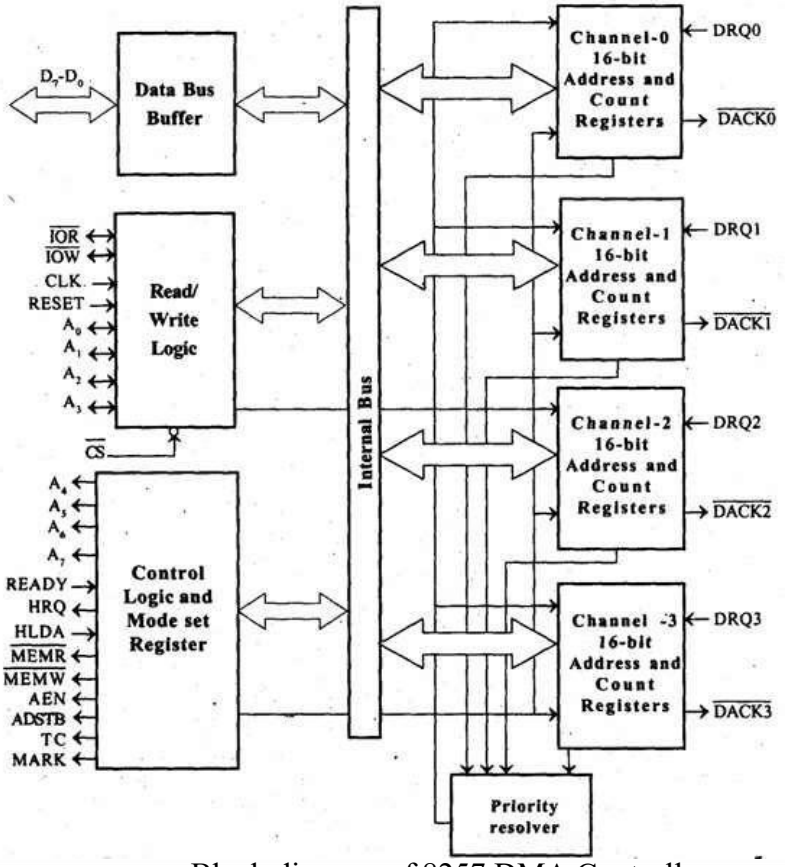
Intel 8257 is a programmable, 4-channel direct memory access controller i.e., four peripheral devices can request data transfer at any instant. The request priorities are decided internally. Each channel has two signals, DRQ (DMA Request) and (DMA acknowledge). Each channel has two 16 bit registers. One for the memory address where the data transfer should being and the second for a 14-bit count. There are also two 8-bit registers one is the mode set register and the other is status register. It can operate both in slave and master mode. It is a totally TTL compatible chip.

Pin Diagram: 8257 is a 40 pin IC package which requires a single +5V supply for its operation. The pin details are as follows. The pin diagram is shown in Fig below.



Block Diagram: The functional block diagram is shown below. It consists of

- Data bus buffer
- Read/Write logic
- DMA channels
- Control logic
- Mode set Register
- Priority resolver



Block diagram of 8257 DMA Controller

Data Bus Buffer: Three state bidirectional, 8 bit buffer interfaces the 8257 to the system data bus. When the 8257 is being programmed by the CPU, eight bits of data for DMA address register, a terminal count register or the mode set register are received on the data bus. When the CPU reads the DMA address register, a terminal count register or status register, the data is sent to the CPU over the data bus. When 8257 is operating as Master, during a DMA cycle, it gains control over the system buses.

Read/Write Logic: In the slave mode, when the CPU reads data from or writes data to the 8257, the read/write logic accepts the I/OR (or) I/OW signals and decodes the least significant 4 address bits (A_0 - A_3). During DMA cycles, when 8257 is the master, the read/write logic generates the I/O read and memory write or I/O write and memory read signals which controls the data link with the peripheral that has been granted DMA cycle. The different signals are

(I/O Read): It is active low bidirectional three-state line. In the slave mode, it is an input, which allows the 8-bit status register or upper/lower byte of a 16 bit DMA address register of terminal count register to be read. In the master mode, is a control output, which is used to access data from a peripheral during the DMA write cycle.

(I/O Write): It is an active low bi-directional tri-state line. In slave mode, it is an input, which allows microprocessor to write. In the master mode, is a control output, which allows data to be output in the peripheral during DMA read cycle.

CLK (Clock Input): This is the clock output of the microprocessor.

RESET: It is an asynchronous input from the microprocessor which disables all DMA channels by clearing the mode register and tri-states all control lines.

A_0 - A_3 (Address Lines): These least significant four address lines are bidirectional. In the slave mode they are inputs, which select one of the registers to be read or programmed. In the master mode, they are outputs, which constitute the most significant 4 bits of the 16 bit memory address generated by the 8257.

CS(Chip Select) It is an active low input which enables the I/O read or I/O write input when the 8257 is being read or programmed in the slave mode. In the master mode, is automatically disabled to prevent the chip from selecting while performing the DMA function.

Control Logic Block: This block controls the sequence operations during all DMA cycles by generating the appropriate control signals and 16 bit address that specifies the memory relations to be accessed.

A_4 - A_7 (Address Lines): These four address lines are tri-stated outputs which contains 4 to 7 of the 16 bit memory address generated by the 8257 during all DMA cycles.

READY: This is an asynchronous input used to insert wait states during DMA read or write machine cycles. Wait states are included between S_3 and S_4 states of the duty transfer.

HRQ (Hold Request): This output line requests the control of the system bus. This is connected to the HOLD input of 8086.

DMA Channels: The 8257 has four separate DMA channels each channel with two 16 bit registers (1) a DMA address register (2) Counter register. Both these registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low order 14 bits of the terminal count register specifies the number of DMA cycles minus one before the terminal count output is activated.

DRQ_0 - DRQ_3 (DMA Request): These are active low signals one for each of the four DMA channels. The output acts as a chip select for the peripheral device requesting service. The DACK line becomes 0 and then 1 for each byte of DMA data transfer.

Mode Set Register: This register is used to set the mode of operation of 8257. It is normally programmed by the CPU after the DMA address register and terminal count registers are initialized. This register is cleared by RESET input, by disabling all options. The mode set register is shown in Fig. By setting the 4th bit we can opt for rotating priority. Normally DRQ_0 has highest priority and DRQ_3 has lowest priority. But in the rotating priority mode the priority of the channels has a circular sequence and after each DMA cycle, the priority of each channel changes. If the rotating priority bit is reset, (is a zero) each DMA channel has a fixed priority in the fixed priority mode. i.e., channel 0 has highest priority and channel-3 has lowest priority.

DMA Working

In 8086 microprocessor two lines dedicated for DMA operation. They are HOLD and HLDA. If any device is in need of DMA service it activates a DRQ line. Now the 8257 in turn sends out HOLD request (HRQ) to microprocessor on HOLD line. The microprocessor then completes the current machine cycle and then goes to HOLD state, where the address bus, data bus and the related control bus signals are tri-stated. Now the HLDA signal is activated. The DMA controller which is a slave to the microprocessor so far will now become the master. The DMA controller resolves the priorities of the requesting I/O devices and accordingly sends a signal to the suitable I/O device. The 8257, after sending out a signal to the requesting I/O device, generates and signals if it is a DMA read operation. 8257 generates and signals for DMA write operation. Then a byte of data is transferred between I/O device and memory directly in 4 clock cycles. This is known as a DMA machine cycle.

Concept: 8– Programmable Interrupt Controller (8259)

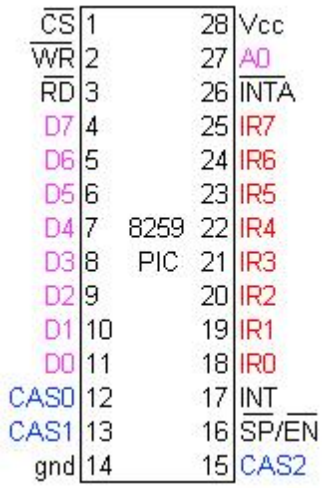
There is an absolute need of this Programmable Interrupt Controller for Interfacing I/O devices to the microprocessor. The 8086 processor has 2 interrupt lines namely, NMI and INTR. So, we can interface two I/O devices, which can perform the interrupt driven data transfer safely. But, suppose we wish to connect more than two I/O devices, to the microprocessor, then we may have to connect more than one I/O device to the interrupt lines. This will affect the interrupt driven data transfer and the microprocessor has to perform polling. i.e, it has to check each device, which is in need of interrupt service. This polling has the dis-advantage of long time and slow interrupt response. Hence to overcome all these problems, INTEL introduced the 28 pin DIP chip -8259. This device accepts interrupt requests from as many as 8 devices independently and as many as 64 I/O devices by cascading method.

Salient Features

INTEL 8259 is a single chip programmable interrupt controller which is compatible with 8085, 8086 and 8088 processors. It is a 28 pin DIP IC with N-mos technology and requires a single +5 DC supply. It handles up to eight vectored priority interrupts for the CPU and cascadable for up to 64 vectored priority interrupts without the need of any additional circuitry. when two 8259s are cascaded through cascade lines the first 8259 will act as master and the second 8259 will act as a slave.

Pin Description

The pin diagram of 8259 is shown below . The pin details are given below



D_0-D_7: Bi-directional, tristated, buffered data lines. Connected to data bus directly or through buffers.

RD-bar: Active low read control

WR-bar: Active low write control

A_0: Address input line, used to select control register.

CS-bar: Active low chip select

CAS_0-CAS_2: Bi-directional, 3 bit cascade lines. In master mode, PIC places slave ID no. on these lines. In slave mode, the PIC reads slave ID no. from master on these lines. It may be regarded as slave-select.

SP-bar / EN-bar: Slave program / enable. In non-buffered mode, it is SP-bar input, used to distinguish master/slave PIC. In buffered mode, it is output line used to enable buffers.

INT: Interrupt line, connected to INTR of microprocessor.

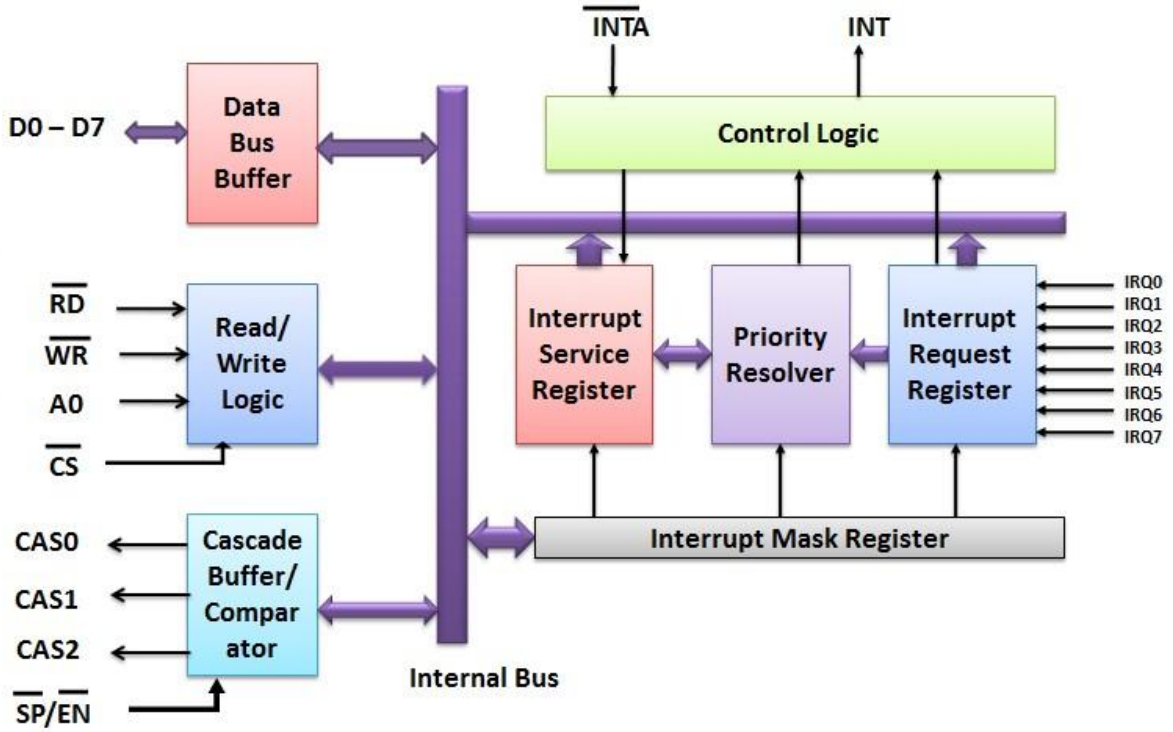
INTA-bar: Interrupt ack, received active low from microprocessor.

IR_0-IR_7: Asynchronous IRQ input lines, generated by peripherals.

Block Diagram of 8259 PIC: The block diagram of programmable interrupt controller is shown in Fig. below. The block diagram consists of eight sub units. They are Control logic, Read/write logic, Data bus buffer. Three register (IRR, ISR and IMR), 5 priority resolver and cascade buffer. The functions of each unit are explained below.

Priority Resolver This logic unit determines the priorities of the bits set in the IRR. The highest priority is

selected and strobed in to the corresponding bit of the ISR during pulse.



Interrupt Mask Register (IMR) The IMR stores the bits which mask the interrupt lines. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

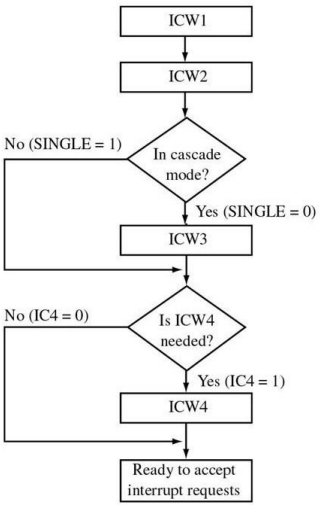
Control Logic This unit has two pins. INT (Interrupt) as an output pin and (interrupt acknowledge) as an input pin. The INT is connected to the interrupt pin of the microprocessor unit. Whenever an interrupt is noticed by the CPU, it generates signal.

Working of 8259

- The 8259 accepts interrupt requests from any one of the 8 I/O lines (IR_0 - IR_7). Then it ascertains the priority of the interrupt lines. Then it ascertains the priority of the interrupt lines. Suppose, the received interrupt has higher priority than currently serviced, it interrupts the microprocessor and after receiving the interrupt acknowledgement from microprocessor.
- It provides a 3 byte CALL instruction. The sequence of steps that occur when an interrupt request line of 8259 goes high is as follows.
- The 8259 accepts the requests on IR_0 - IR_7 in IRR. Then it checks the contents of IMR whether that request is masked or not. The 8259, then checks ISR to know the interrupt levels that are being currently serviced.
- After this 8259 sends a high INT to 8086 processor. Normally, it is the job of the priority resolver to check the contents of IRR, IMR and ISR and decide whether to activate INT output of 8259 or not.
- Now 8085 processor responds by suspending the program flow at the end of the current instruction and makes low. On receiving, 8259 sends code for CALL to the microprocessor on D_{7-0} bus.
- This code for CALL in IR register of 8259 causes the 8086 to issue two more signals. When goes low the second time, 8259 places LSB of ISS address on the data bus. When goes low the third time, 8259 places the MSB of ISS address on the data bus. Now, the microprocessor branches to the ISS after saving the contents of program counter on the stack top. After finishing the ISS, the control returns to the main program by popping the top of stack to PC.

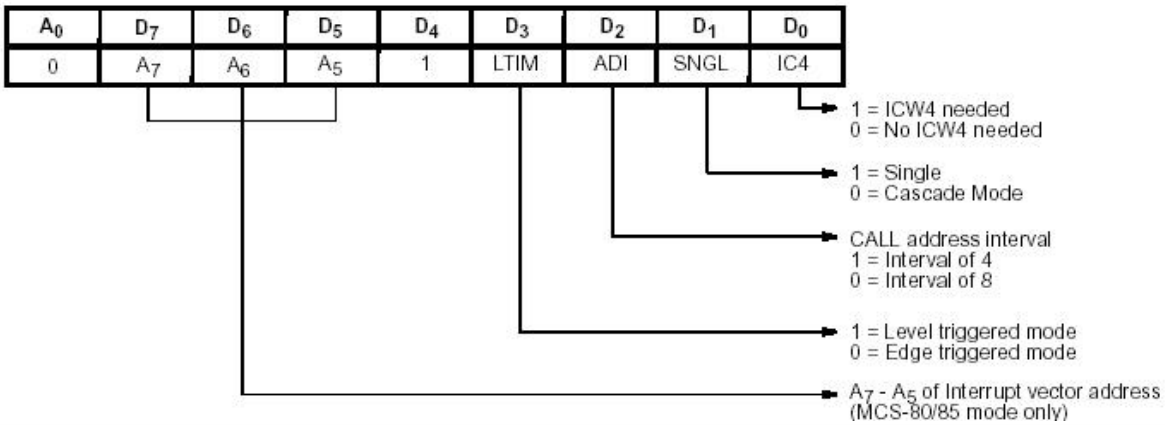
Programming 8259

The 8259 requires two types of command words namely, Initialization Command Words (ICW) and Operational Command Words (OCW). The 8259 can be initialized with four ICWs, the first two are essential and the other two are optional based on the modes being used. These words must be issued in a sequence. Once the 8259 is initialized, the 8259 can operate in various modes by using three different OCWs.

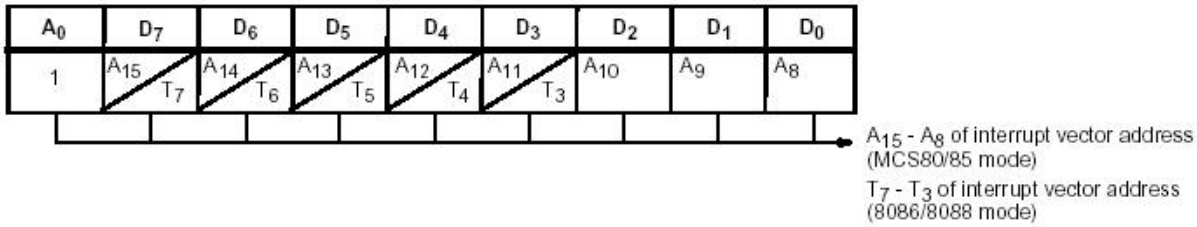


Flow chart for initializing 8259 PIC

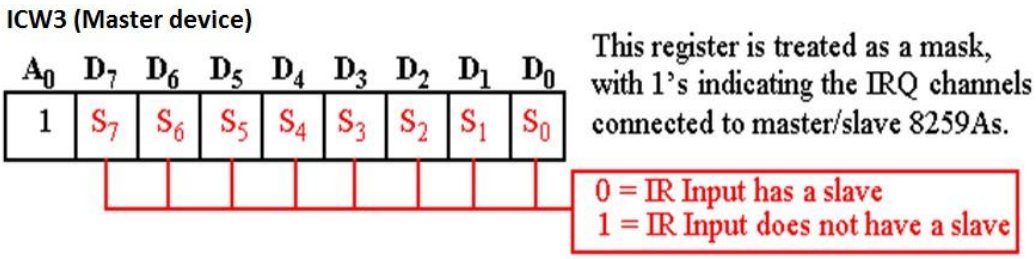
ICW1 Format:



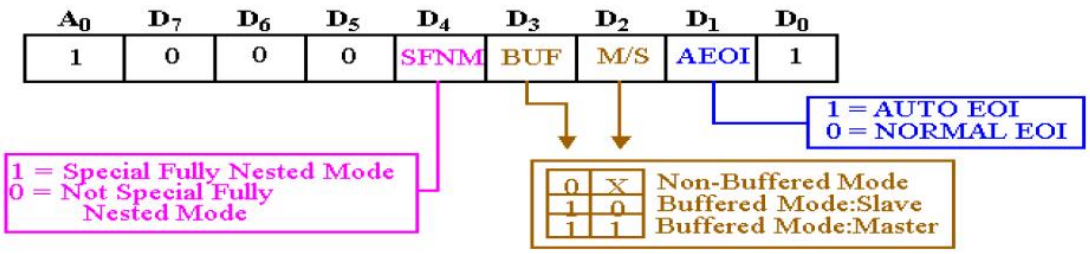
ICW2 Format:



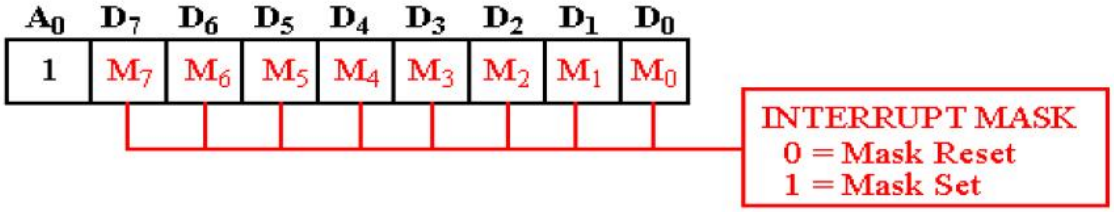
ICW3 Format:



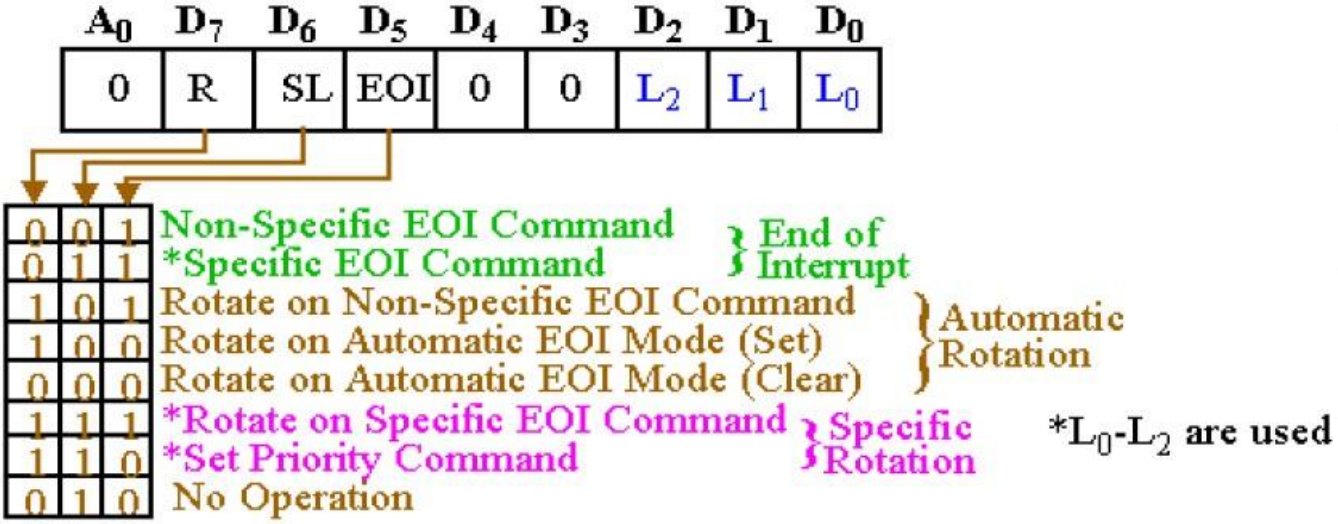
ICW4 Format:



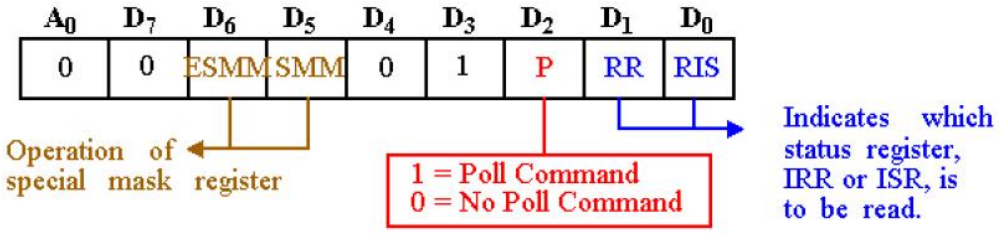
OCW1 Format:



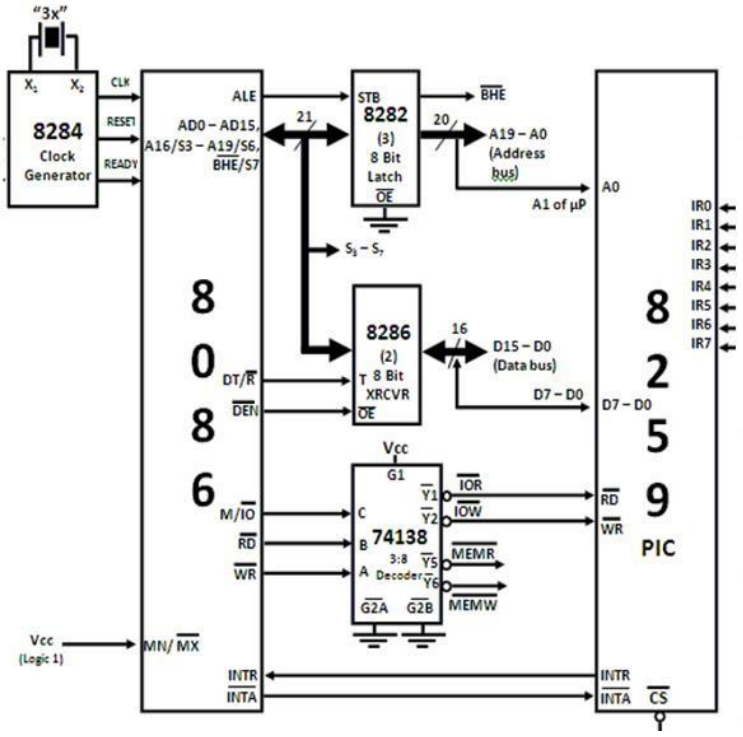
OCW2 Format:



OCW3 Format:



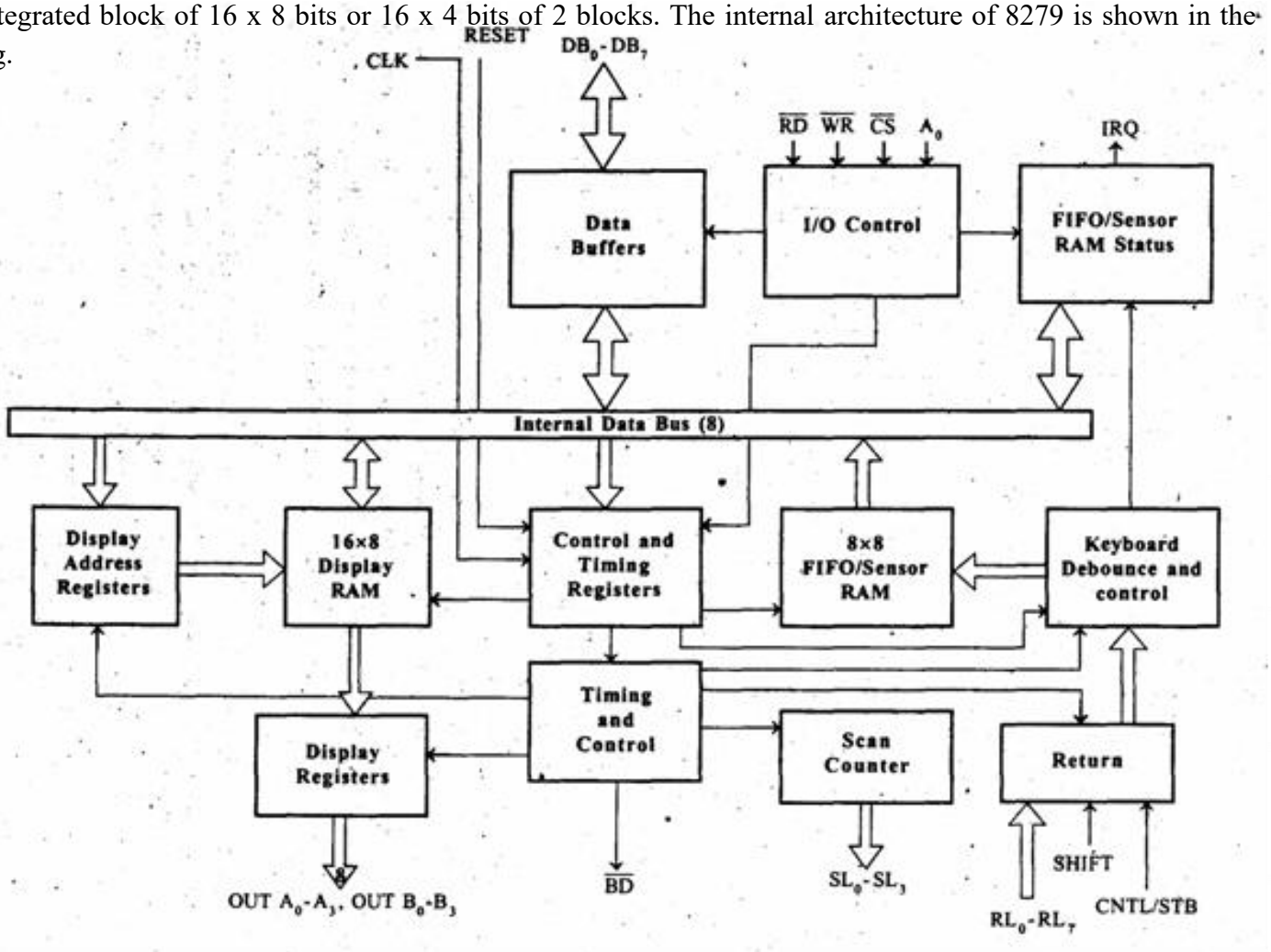
Interfacing 8259 with 8086:



Concept: 10– Interfacing of 8259–Keyboard/display controller (8279)

Intel's 8279 is a general purpose keyboard display controller that simultaneously drives the display of a system and interfaces a keyboard with the CPU leaving the CPU free for its routine task. The keyboard display interface scans the keyboard to identify if any key has been pressed and sends the code if the pressed key to the CPU. This also transmits the data received from the CPU to the display device. The controller performs both of these operations without involving the CPU.

The 8279 is a 40 pin drive with two major segments, Keyboard and Display. The keyboard can be connected to a max of 64 – contact ky matrix. Keyboard entries are denounced and stored in the internal FIFO RAM and an interrupt signal is generated with each entry. The display segment can provide a 16 character (byte) scanned display. This segment contains 16 x 8 R/w memory (RAM), which can be used to read or write information for the display purposes. This 16-byte display RAM can be used either as an integrated block of 16 x 8 bits or 16 x 4 bits of 2 blocks. The internal architecture of 8279 is shown in the fig.



The keyboard display controller 8279 is provided with

a) set of four scan lines and eight return lines for interfacing keyboards.

b) a set of eight output lines for interfacing the display.

I/O CONTROL :- This I/O control block controls the flow of data to or from the 8279. This A_0, RD, WR Select the command, status or data read/write operations carried out by the CPU with 8279.

DATA BUFFER:- This data buffer interface the internal bus of the 8279 with the external system bus. This can be used to transfer data, status/ control word.

CONTROL AND TIMING REGISTER :- These registers store the keyboard and the display modes and other operating conditions programmed by the CPU. These registers are writer with $A_0 = 1$ and WR = 0.

TIMING AND CONTROL UNIT :- Timing and control unit controls the basic timings for the operation of the circuit.

SCAN COUNTER :- Scan Counter divide down the operating frequency of 8279 to device scan keyboard and refresh display frequencies. The scan counter has two modes to scan the key matrix and refresh the display which are encoded scan mode and decoded scan more.

RETURN BUFFER AND DEBOUNCE AND CONTROL :- This section scans for a key closure row wise. If a key closure is detected the keyboard denounce unit denounces the key entry. After the denounce period if the key continues to be detected the code of the key is directly transferred to the FIFO RAM along with SHIFT and CONTROL key status.

FIFO /SENSOR RAM AND STATUS LOGIC :- In keyboard or strobed input mode this FIFO / Sensor RAM act as a 8 byte first in first out RAM [FIFO RAM] . Each key code of the pressed key is entered in the order of entry is read by the CPU. The status logic generates an interrupt for each FIFO read operation.

In scanned sensor matrix mode this unit acts as sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of the sensors in the matrix. If the sensor changes its state the IRZ line goes high to interrupt the CPU.

DISPLAY ADDRESS REGISTER

The display address register hold the address of the word currently being written or read by the CPU to or from the display RAM.

DISPLAY RAM:- This 16 byte display RAM contains the 16 bytes of data to be displayed on the 16 seven segment displays.

SIGNAL DESCRIPTION OF 8279

$DB_0 – DB_7$:- These are bidirectional data bus lines. The data and command words to and from the CPU are transferred on these lines.

CLK :- This is a clock input used to generate internal timings required by 8279.

RESET:- This pin is used to reset 8279. A high on this line resets 8279. After resetting 8279 is in sixteen 8 bit display, left entry display mode and 2 key lock out mode.

CS [CHIP SELECT] :- A low on this line enables 8279 for the read or write operations.

A_0 :- A high on this line indicates the transfer of a command or status information. A low on this line indicates the transfer of data. This can be used to select one of the internal registers of 8279.

RD, WR [READ, WRITE] :- These signal allows the data buffer to receive or send data over the data bus.

IRQ :- The interrupt line goes high when there is data in the FIFO/Sensor RAM. This line goes low with each FIFO RAM read operation. If the FIFO RAM again contain any key code entry to be read by CPU this pin again goes high to generate an interrupt to the CPU.

$SL_0 – SL_3$ [SCAN LINES] :- These lines are used to Scan the key board matrix are used to scan the key board matrix and to refresh the display. These lines can be programmed as encoded or decoded using the mode control register.

$RL_0 – RL_7$:- These are the input lines one terminal of the key is connected to this line and other terminal is connected to the scan lines. These are normally high and pulled low when a key is pressed.

SHIFT :- The status if the Shift input is stored along with each key code in FIFO; in scanned key board mode.

CNTL/STB CONTROL/STROBED I/P MODE:- In the keyboard mode this line is used as a control input and is stored in the FIFO on a key closure. In the strobe input mode this line is a strobe line that enters the data into the FIFO RAM.

BD [BLANK DISPLAY]:- This is an output pin and is used to blank the display.

OUT A_0 – OUT A_3 and OUT B_0 – OUT B_3 :- These are the output lines of two 16 x 4 or 16 x 8 internal display registers. The data from these lines are synchronized with the scan lines to refresh the display. The two 4-bit ports can also be used as one 8 bit port.

Concept: 11 and 12–Architecture–Modes of operation–Command words of 8279

I) Input or Keyboard Mode.
II) Output or Display Mode.

a) Scanned Keyboard Mode
b) Scanned Sensor Matrix Mode.
c) Strobed Input Mode.

I. Input or Keyboard Mode

8279 provides 3 input modes. Which are

a) **Scanned Keyboard Mode** :- This mode allows a key matrix to be interfaced using either encoded or decoded scan. In encoded scan an 8 x 8 keyboard or in decoded scan a 4 x 8 keyboard can be interfaced. The code of the pressed key along with the status of the control and shift is stored into the FIFO RAM. This can be performed in 3 methods, which are

1) Scanned Keyboard Mode with 2 key LOCKOUT.
2) Scanned Keyboard with N – Key Rollover.
3) Scanned Keyboard Special error Mode.

2) Output or Display Mode :- 8279 provides two output mode for the display

a) Display Scan
b) Display Entry

a) Display Scan

In this mode 8279 provide 8 or 16 character multiplexed display and can be organized as dual 16 x 4 or single 16 x 8 display units.

b) Display Entry

This mode provides two options for data entry on the displays. First one is known as left entry mode and the second as right entry mode. This left entry mode is also known as typewriter mode and right entry mode is known as calculator mode.

Left Entry Mode: In this mode data is entered from the left side of the display unit. Address 0 of the display RAM contains the left most display character and the address 15 of the RAM contains the right most display character. The display RAM address is on the auto increment mode. The first entry is displayed on the left most display and the sixteenth entry on the right most display. The seventeenth entry is again displayed at the leftmost display section.

Right Entry Mode: In this mode the first display character is entered on the right most display. The next entry is also placed on the right most display by shifting the previous display by one display position. The left most display character is shifted out of the display at the seventeenth entry and is lost ie., it pushed out of the display RAM.