LECTURE 26 - NXP HPC2148 PLL

* STEPS FOR PLL CONFIGURATION:

(FOSC = 12 MHz, CLLK - GOMHZ, PULK - 15 MHZ)

- @ Enable PIV and Disconnect PIV from CPV and ather peripherals
 PHOCON = 0x01;
- D Configure M value and P value
 PHOCEG = 0x24;
- B Feed sequence for locking to desired frequency
 PHOFEED = 0XAA; PHOFEED = 0X55;
- Thick whether the PIND has locked on to the desired frequency while (1(PINOSTAT & OXDDODDOGOD)); PLOCK = 0
- E) Enable (again) Per and connect the Per to CPV PROCON = 0x03;
- (B) Feed sequence for connecting the PHO as system clock
 PHOFFED = DXAA; PHOFFED = 0×55;
- (D) configure PCLK at 1/4 frequency of System Clock VPBDIV = 0x00; CCLK = 60 MHZ and PCLK = 15MHZ

* STEP 1 - PLLOCON & OXOI;

Table- PLL Control negister (PLIOCON-address Dx EOIF COSO, PLHCON-address Ox EOIF COAO) bit description

	-	-	/ V V		
	Bit	Symbol	Description	Reset	
	0	PHE	PH Charles holes and all	value	1
			PIL Gnakle. When one, and after a valid PIL	0	1
			feed, this bit wall activate the PIN and allow		
	-		it to lock to the requested frequency.		
	1	PILL	PIL Connect. When PLIC and PLIE are both set	0	
			to one, and after a valid PII feed, connects the		
			PH as the clock source from the microcontroller		
			otherwise, the oscillator clock is used directly		_
			by the microcontroller.		
1	-		g^{-1}		

7:2	_	Reserved, user softmere should not write ones	NA	
		to reserved bits. The value read from a		
		neserved bit is not defined.		

* STEP 2 - PHOCEG - ax24;

Table-PH configuration register (PLLOGFG - address Ox EDIF COS4, PHICFG - address OxEDIF COR4) but description

				Name and Address of the Owner, where the Owner, which is the Owne	-
And the second	Bit	Symbol	Description	Reset Value	
	4:0	1 (/)	PH multiplier value supplies the value "m"	0	
			in the pu frequency calculations.		_
	6:5	PSEL	PH Divider value supplies the value "P" in	0	
			the PI Anguency calculations		-
	1	. 5	Reserved, wer software should not write ones	NA	_
			to reserved bits. The value read from a		
			reserved bit is not defined.		
_	4				

CCLK = MX FOSC

FOR = 12 MHZ, CCIK = 60 MHZ, M= ? -- 5

Fee = CCLK X 2X P

FCCO = 156 MHz to 320 MHz, CCLK = 60 MHz, P= ? -- 2

Table - PH multiplier values

	MSEL Bits (PLLCFG bits [4:0])	Value of M	1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
	MSEL BUS (PHILTY EUS !!		r other
	00000	1 6 37 - 100	Fox 2142 Fasc = 10 - 25 MHZ
	00001	2	Tasc = 10 - 25 MINZ
	00010	3	max. CCLK > 60 MH2
-		31	80 Max. MSEL = 6 for 214 x
	11110	32	
	11111		

1	Table - PH Dinder value		· ^						
	PSEL Bits (PHLFG bits 66:	5) Value of P							
	00								
	01	2							
	10	4							
	11	8							
2	PSEL	1ACC I		100					
P240CFG = 0×24	0 0 1	0 0 1	0 0						
	2		ly	and the same of th					
مد	* STEP 3 - PLLOFEED = DXAA; PLLOFEED = DX55; Table - PLL Feed register (PLLOFEED - address OXEOIF COSC, PHIFEED - address OXEDIF COAC) but description								
	Bit Symbol Description			Reset					
		ACCUI ON CO	0	Amaria					
	7:0 PHFTED The PIV feed register in a	y der for on and	written to the	1 0x00					
	control negis	uder for pu conf	guration and						
	COS 8 00 10 12 12 12 12 12 12 12 12 12 12 12 12 12	ter changes to tak	e effect.						
j	+ STEP 4 - While ((PLIOSTAT & OX 00000400) == 0); PHOCK = 0;								
	It can also be written as while (((PHOSTAT & 0x00000400)).								
		0	V (Surveyor)						
→	PH status Register (PHOS	101)4							
	Table-PH Status negister	(PLUSTAT - addy	M PARTE AND						
	PHISTAT - address Ox EDIF (CDAS) but descript	WAN COSS						
	PD		0.0~						

		2/11/2	SEA DAY MAN TO THE COURSE MINE TO THE	746.	
	Bot	Symbal	Description	Roset	
	4:0	msel	Read back for the PH multiplier value. This is	0	
	`		the value currently used by the PH.		_
	6:5	PSEL	Read-back for the PH Divider value. This is	0	_
		2.00 miles (M. 1000 M. 2.00) (M. 10.1) (M. 10.1)	the value currently used by the PH.		_
	7	_	Reserved, user software should not write	NA	
			ones to reserved bits. The value read from	4-	_
			a reserved bit is not defined.		_
	8	PHE	Read-back for the PH Enable bit. When one,	0	
		•	the PH is currently activated when zero the	25000	
			Pl as turned off. This but is automatically	1 1	
			cleared when Power-down made is activated.	1	4
	a	PHC	Read-back for the PH Connect bit when PHL	0	_
			and PHE are both one, the PH is connected as		_
			the clock source for the microcontroller.		_
	1		When either PUC or PUE is serve, the PH is	11111	_
			bypassed and the oxillator clock is used		_
			directly by the microcontholler. This but is		_
			automatically cleared when Power-down		_
			mode is artifated.	0	_
	10	PLOCK	Reflects the PH tock status. When zero, the		_
			PH is not locked when one, the PH is		
_			locked onto the requested forequency.		_
		1			_

STEP 5 - PLLOCON = 0x03)

* STEP 6 - PHOFEED = OXAA; PHOFEED = OX55;

PD

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						. A BOLK	- IEIMHOI		
*	* STEP 1 - VABDIV = axto; CLIK = 60 MHz and PCLK = 15 MHz; Table - VAB divider register map								
	and the second s	Descripti	mercon de consensatorio men			- Annual Control	Access	Reset	Addres
	VPBDIV	controls.	the rate	of the	VPB Clo	ick in	R/W	OXOD	OX FOIF
					sov w	1		-	
*	REGIST	er Summa	RY - PLL						
,	1	6.	5	4	3	2	1	0	
PLUPTED	X		. 1	PLLF	EED				
PHOCON			a second	de la constitución de la constit	and the same of th	e com establishment	PLLC	PLLE	84
PLLDIFF	1. 3.	PS	EL .		1 1,10,4	MSEL			
MPBDIV						7 12003	VPE	DIV	
, ÷	1. 1.		_121_15			111 74.	Section 1 Communication desired to		
	10	1009	8	7 3	6	1 5	4	0	
PHOSTAT	PLOCK	PLLC	PHE	1 43 21	PSE		me	EL	
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	V8 3.	52 - mer 1	in Walleit	Wilm. 3	it has the	03: 00);			
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