

## LECTURE 24 - EXTERNAL INTERRUPTS

Whenever a signal is given to a pin, the processor will identify that an external interrupt is generated, thereby automatically stopping the main program and interrupt service routine is executed.

In LPC2148, we have 9 external interrupt pins. It is named as -

EINT0 - P0.1, P0.16

EINT1 - P0.3, P0.14

EINT2 - P0.1, P0.15

EINT3 - P0.9, P0.20, P0.30

### \* STEPS TO CONTROL AN LED WITH EXTERNAL INTERRUPT:

① Configure P0.14 as EINT1

PINSEL0 <29:28> = 10

② Configure Edge sensitive / Level sensitive Interrupt for EINT1

EXTMODE <1> = 1 (Edge sensitive)

③ Configure Rising / Falling edge sensitive Interrupt for EINT1

EXTPOLAR <1> = 0 (Falling)

④ Clear EINT1 Interrupt Flag Bit

EXTINT <1> = 1

⑤ Configure EINT1 (Interrupt No. 15) as FIG/IRQ

VICIntSelect <15> = 0 (IRQ)

⑥ Enable EINT1 Interrupt

VICIntEnable <15> = 1

⑦ Configure the Interrupt Number of Interrupt Request assigned to Vectored IRQ slot (IRQ slot 5)

VICVectCtrl5 <4:0> = 1111 (Decimal 15)

⑧ Enable Vectored IRQ slot (IRQ slot 5)

VICVectCtrl5 <5> = 1

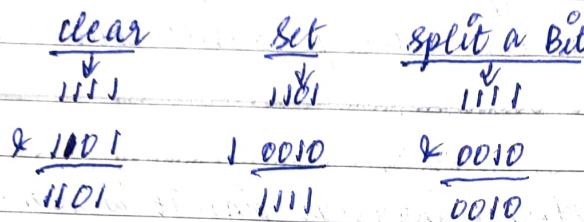
⑨ Configure ISR Vector Address to VIC IRQ slot

VICVectAddr5 = (unsigned int)Ext\_ISR;

\* STEP 1 - PINSEL0 <29:28> = 10

$$\text{PINSEL0} = (\text{PINSEL0} \& 0x(CFFFFFFF)) | (1 \ll 29);$$

First make Bit 28 & 29 as '0' then make Bit 29 as '1'



### EXTERNAL INTERRUPT REGISTERS -

Table - External Interrupt registers

Name	Description	Access	Reset value	Address
EXTINT	The External Interrupt Flag Register contains interrupt flags for EINT0, EINT1, EINT2 and EINT3.	R/W	0	0xE01F 0140
INTNAKE	The Interrupt Wakeup Register contains four enable bits that control whether each external interrupt will cause the processor to wake up from Power-down mode.	R/W	0	0xE01F 0144
EXTMDDE	The External Interrupt mode Register controls whether each pin is edge- or level sensitive.	R/W	0	0xE01F 0148
EXTPOLAR	The External Interrupt Polarity Register controls which level or edge on each pin will cause an interrupt.	R/W	0	0xE01F 014C

\* STEP 2 - EXTMODE  $\langle 1 \rangle = 1$  (edge sensitive)

$\text{EXTMODE} = 0x2j$

Table - External Interrupt Mode register (EXTMODE - address 0x EDIF (148)) bit description

Bit	Symbol	Value	Description	Reset value
0	EXTMODE0	0	level-sensitivity is selected for EINT0.	0
		1	EINT0 is edge sensitive.	
1	EXTMODE1	0	level-sensitivity is selected for EINT1.	0
		1	EINT1 is edge sensitive.	
2	EXTMODE2	0	level-sensitivity is selected for EINT2.	0
		1	EINT2 is edge sensitive.	
3	EXTMODE3	0	level-sensitivity is selected for EINT3.	0
		1	EINT3 is edge sensitive.	
7:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

+ STEP 3 - EXTPOLAR  $\langle 1 \rangle = 0$  (Falling)

$\text{EXTPOLAR} b = 0xFFFFFFF0;$

Table - External Interrupt Polarity register (EXTPOLAR - address 0x EDIF (14C)) bit description

Bit	Symbol	Value	Description	Reset Value
0	EXTPOLARD	0	EINTD is low-active or falling-edge sensitive (depending on EXTMODED).	0
		1	EINTD is high-active or rising-edge sensitive (depending on EXTMODED).	
1	EXTPOLARI	0	EINTI is low-active or falling-edge sensitive (depending on EXTMODE1).	0
		1	EINTI is high-active or rising-edge sensitive (depending on EXTMODE1).	
2	EXTPOLAR2	0	EINT2 is low-active or falling-edge sensitive (depending on EXTMODE2).	0
		1	EINT2 is high-active or rising-edge sensitive (depending on EXTMODE2).	
3	EXTPOLAR3	0	EINT3 is low-active or falling-edge sensitive (depending on EXTMODE 3).	0
		1	EINT3 is high-active or rising-edge sensitive (depending on EXTMODE 3).	
7:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

\* STEP 4 - EXTINT <1> = 1

EXTINT |= 0x02;

Flag bit is cleared by writing '1' to it.

Table - External Interrupt Flag register (EXTINT - address 0XE01F (140) bit description

Bit	Symbol	Description	Reset value
0	EINT0	<p>In level-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT0 function is selected for its pin, and the selected edge occurs on the pin.</p> <p>Up to two pins can be selected to perform the EINT0 function (see PD.1 and PD.16 description in "Pin configuration").</p> <p>This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state (e.g. if EINT0 is selected to be low level sensitive and a low level is present on the corresponding pin, this bit can not be cleared; this bit can be cleared only when the signal on the pin becomes high).</p>	0
1	EINT1	<p>In level-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT1 function is selected for its pin, and the selected edge occurs on the pin.</p> <p>Up to two pins can be selected to perform the EINT1 function (see PD.3 and PD.14 description in "Pin configuration").</p> <p>This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state (e.g. if EINT1</p>	0

is selected to be low level sensitive and a low level is present on the corresponding pin, this bit can not be cleared; this bit can be cleared only when the signal on the pin becomes high).

## 2 EINT2

In level-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT2 function is selected for its pin, and the selected edge occurs on the pin.

Up to two pins can be selected to perform the EINT2 function (see P0.7 and P0.15 description in "Pin Configuration")

This bit is cleared by writing a one to it, except in level-sensitive mode when the pin is in its active state (e.g. if EINT2 is selected to be low level sensitive and a low level is present on the corresponding pin, this bit can not be cleared; this bit can be cleared only when the signal on the pin becomes high).

## 3 EINT3

In level-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the pin is in its active state. In edge-sensitive mode, this bit is set if the EINT3 function is selected for its pin, and the selected edge occurs on the pin.

Up to three pins can be selected to perform the EINT3 function (see P0.9, P0.20 and P0.30).

description in "Pin configuration").

This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its native state i.e.g. If TINT3 is selected to be low level sensitive and a low level is present on the corresponding pin, this bit can not be cleared; this bit can be cleared only when the signal on the pin becomes high).

1:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
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### → VIC Registers -

Table - VIC register map .

Name	Description	Access	Reset Value	Address
VICIntSelect	Interrupt Select Register. This register classifies each of the 32 interrupt requests as contributing to FIG or IRg.	R/W	0	0xFFFF F00C
VICIntEnable	Interrupt Enable Register. This register controls which of the 32 interrupt requests and software interrupts are enabled to contribute to FIG or IRg.	R/W	0	0xFFFF F010
VICVectCtrl0	Vector control 0 register. Vector Control Registers 0-15 each control one of the 16 reserved IRg slots. Slot 0 has the highest priority and slot 15 the lowest.	R/W	0	0xFFFF F200

VICVectCtrl1	Vector control 1 register.	R/W	0	0xFFFF F204
VICVectCtrl2	Vector control 2 register.	R/W	0	0xFFFF F208
VICVectCtrl15	Vector control 15 register.	R/W	0	0xFFFF F23C
VICVectAddr	Vector Address Register. When an IRQ interrupt occurs, the IRQ service routine can read this register and jump to the value read.	R/W	0	0xFFFF F030
VICVectAdd0	Vector address 0 register. Vector Address Registers 0-15 hold the addresses of the interrupt service routines (ISRs) for the 16 vectored IRQ slots.	R/W	0	0xFFFF F100
VICVectAddr1	Vector address 1 register.	R/W	0	0xFFFF F104
VICVectAddr2	Vector address 2 register.	R/W	0	0xFFFF F108
VICVectAddr15	Vector address 15 register.	R/W	0	0xFFFF F13C

STEP 5 - VIC Int Select & = 0xFFFF1FFF ; VICIntSelect  $\ll 15$  > 0 (Rg)  
Table- Interrupt Select Register /VICIntSelect - address 0xFFFF F000  
bit allocation  
Reset value: 0x0000 0000

bit	7	6	5	4	3	2	1	0
symbol	VARTI	VARTD	TIMER1	TIMER0	ARMCore1	ARMCore0	-	WDT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	symbol	value	Description	Reset value
31:0	See VICIntSelect bit allocation table	0	The interrupt request with this bit number is assigned to the IRQ category.	0
		1	The interrupt request with this bit number is assigned to the FIQ category.	

\* STEP 6 - VICIntEnable  $\ll 15 = 1$

$$\text{VICIntEnable} = 1 \ll 15;$$

Table - Interrupt Enable register (VICIntEnable - address 0xFFFFF010) bit allocation

Reset value: 0x0000 0000

[same as Interrupt Select Register]

bit	symbol	Description	Reset value
31:0	See VICIntEnable bit allocation table	When this register is read, it indicates interrupt requests or software interrupts that are enabled to contribute to FIQ or IRQ.	0
		When this register is written, ones enable interrupt requests or software interrupts to contribute to FIQ or IRQ, zeroes have no effect.	

\* STEP 7 - VICVectCntl5 <4:0> = 1111 (Decimal 15)

Table - Vector control registers 0-15 (VICVectCntl 0-15 - 0xFFFF F200-23C) bit description

Bit	Symbol	Description
4:0	int-request	The number of the interrupt request or software interrupt assigned to this vectored IRQ slot. As a matter of good programming practice, software should not assign the same interrupt number to more than one enabled vectored IRQ slot. But if this does occur, the lower numbered slot will be used when the interrupt request or software interrupt is enabled, classified as IRQ, and asserted.
5	IRQ slot-en	When 1, this vectored IRQ slot is enabled, and can produce a unique ISR address when its assigned interrupt request or software interrupt is enabled, classified as IRQ, and asserted.
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.

\* STEP 8 - VICVectCntl5 <5> = 1

VICVectCntl5[1] = 1 & 5;

\* STEP 9 - VICVectAddr5 = (unsigned int) Ext\_ISR;  
ISR should have "irq" as the keyword.  
void Ext\_ISR() - irq

→ VIC Vector Address Registers (VICVectAddr0-15)

Table - Vector Address registers (VICVectAddr 0-15 - addresses 0xFFFF F100-13C) bit description

Bit	Symbol	Description	Reset Value
31:0	IRQ-Vector	When one or more interrupt request or software interrupt is (are) enabled, classified as IRQ, asserted, and assigned to an enabled vectored IRQ slot, the value from this register for the highest-priority such slot will be provided when the IRQ service routine reads the Vector Address register - VICVectAddr	0x0000 0000

#### \* EXTERNAL INTERRUPT REGISTERS :

31-4	3	2	1	0
EXTMODE	EXTMODE3	EXTMODE2	EXTMODE1	EXTMODE0
EXTPolar	EXTPOLAR3	EXTPOLAR2	EXTPOLAR1	EXTPOLAR0
EXTINT	EINT3	EINT2	EINT1	EINT0

#### \* VIC CONTROL AND ADDRESS REGISTERS :

31-6	5	4-0
VICVectCntl0-15	IRQslot-en	Int-request
		31-0
VICVectAddr0-15		IRQ-Vector