LECTURE 26 - NXP LPC2148 PLL

* STEPS FOR PLL CONFIGURATION :

(FOSC = 12MHz, CCLK = 60MHz, PCLK = 15MHz)

① Enable PLL and Disconnect PLL from CPU and other peripherals
PLL0CON = 0x01;

② Configure M value and P value
PLL0CFG = 0x24;

③ Feed sequence for locking to desired frequency
PLL0FEED = 0xAA; PLL0FEED = 0x55;

④ Check whether the PLL0 has locked on to the desired frequency
while (!(PLL0STAT & 0x00000400)); PLOCK = 0

⑤ Enable (again) PLL and connect the PLL to CPU
PLL0CON = 0x03;

⑥ Feed sequence for connecting the PLL0 as system clock
PLL0FEED = 0xAA; PLL0FEED = 0x55;

⑦ Configure PCLK at 1/4 frequency of System clock
VPBDIV = 0x00; CCLK = 60MHz and PCLK = 15MHz

* STEP 1 - PLL0CON = 0x01;

Table - PLL control register (PLL0CON - address 0xE01F C080, PLL1CON - address 0xE01F C0A0) bit description

Bit	Symbol	Description	Reset value
0	PLLE	PLL Enable. When one, and after a valid PLL feed, this bit will activate the PLL and allow it to lock to the requested frequency.	0
1	PLLC	PLL Connect. When PLLC and PLLE are both set to one, and after a valid PLL feed, connects the PLL as the clock source for the microcontroller. Otherwise, the oscillator clock is used directly by the microcontroller.	0

7:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

* STEP 2 - PLLOCFG = 0x24;

Table - PLL configuration register (PLLOCFG - address 0xE01F C084, PLLCFG - address 0xE01F C0A4) bit description

Bit	Symbol	Description	Reset Value
4:0	MSEL	PLL Multiplier value. Supplies the value "m" in the PLL frequency calculations.	0
6:5	PSEL	PLL Divider value. Supplies the value "P" in the PLL frequency calculations.	0
7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

$$CCLK = M \times F_{OSC}$$

$F_{OSC} = 12\,MHz$, $CCLK = 60\,MHz$, $M = ? \rightarrow 5$

$$F_{CCO} = CCLK \times 2 \times P$$

$F_{CCO} = 156\,MHz$ to $320\,MHz$, $CCLK = 60\,MHz$, $P = ? \rightarrow 2$

Table - PLL Multiplier values

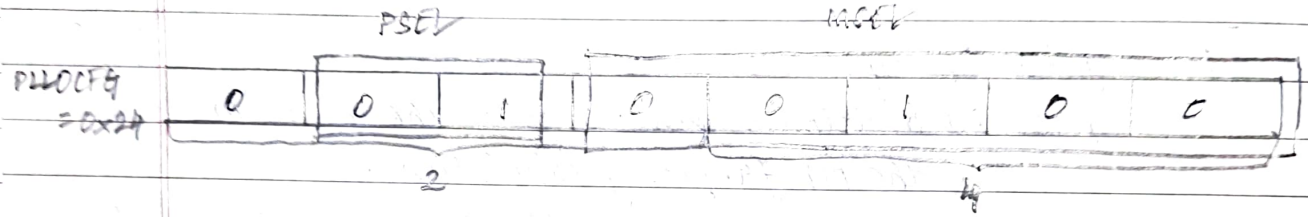
MSEL Bits (PLLCFG bits [4:0])	Value of M
00000	1
00001	2
00010	3
...	...
11110	31
11111	32

For 214x
$F_{OSC} = 10 - 25\,MHz$
Max. CCLK = 60 MHz

So Max. MSEL = 6 for 214x

Table - PLL Divider values

PSEL Bits (PLLCFG bits [6:5])	Value of P
00	1
01	2
10	4
11	8



* STEP 3 - PLL0FEED = 0xAA ; PLL0FEED = 0x55;

Table - PLL Feed register (PLL0FEED - address 0xE01F C08C, PLL1FEED - address 0xE01F C0AC) bit description

Bit	Symbol	Description	Reset value
7:0	PLLFEED	The PLL feed sequence must be written to this register in order for PLL configuration and control register changes to take effect.	0x00

* STEP 4 - while ((PLL0STAT & 0x00000400) == 0) ; PLOCK = 0 ;

It can also be written as while (!(PLL0STAT & 0x00000400)).

→ PLL status Register (PLL0STAT) -

Table - PLL status register (PLL0STAT - address 0xE01F C088, PLL1STAT - address 0xE01F C0A8) bit description

PTO

Bit	Symbol	Description	Reset value
4:0	MSEL	Read-back for the PLL multiplier value. This is the value currently used by the PLL.	0
6:5	PSEL	Read-back for the PLL Divider value. This is the value currently used by the PLL.	0
7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	PLLE	Read-back for the PLL Enable bit. When one, the PLL is currently activated. When zero, the PLL is turned off. This bit is automatically cleared when Power-down mode is activated.	0
9	PLLC	Read-back for the PLL Connect bit. When PLLC and PLLE are both one, the PLL is connected as the clock source for the microcontroller. When either PLLC or PLLE is zero, the PLL is bypassed and the oscillator clock is used directly by the microcontroller. This bit is automatically cleared when Power-down mode is activated.	0
10	PLOCK	Reflects the PLL Lock status. When zero, the PLL is not locked. When one, the PLL is locked onto the requested frequency.	0

* STEP 5 - PLLOCON = 0x03;

* STEP 6 - PLLOFEED = 0xAA; PLLOFEED = 0x55;

PTO

* STEP 7 - VPBDIV = 0x00; CCLK = 60MHz and PCLK = 15MHz;

Table - VPB divider register map

Name	Description	Access	Reset Value	Address
VPBDIV	Controls the rate of the VPB clock in relation to the processor clock.	R/W	0x00	0xE01F C100

* REGISTER SUMMARY - PLL:

	7	6	5	4	3	2	1	0
PLL0FEED	PLLFEED							
PLL0CON							PLLC	PLLE
PLL0CFG		PSEL		MSEL				
VPBDIV							VPBDIV	

	10	9	8	7	6	5	4	0
PLL0STAT	PLOCK	PLLC	PLLE		PSEL		MSEL	