

LECTURE 23 - ADC

## (ANALOG - TO - DIGITAL CONVERTER)

LPC2148 contains only one ADC, i.e., ADC0. The resolution of the ADC is 10-Bit, i.e., the smallest possible value that can be measured by the ADC is 10-bit. Voltage is measured from 0V to  $\pm 3.3V$ . The ADC can be  $2^{10}$  values, therefore the voltage can be divided from 0V to  $\pm 3.3V$  in  $2^{10}$  steps.

Therefore, smallest voltage level measured =  $\frac{\pm 3.3V}{1024}$

The ADC has 6 channels, i.e., six inputs can be taken but only one output will be converted to corresponding digital data for which we use a multiplexer. Each channel is referred by the terminology of ADD.14 & ADD.6:7 ; ADD.5 is not present.

★ STEPS FOR AD CONVERSION:

- ① Set P0.30 pin as ADD.3 (ADC Input Pin for ADC channel 3)  
 $\text{PINSEL1} \&= 0xFFFFFFFF; // x0101xx xxxx xxxx ... xxxx}$   
 $\text{PINSEL1} |= 0x10000000; // x01xxxx xxxx xxxx xxxx ... xxxx}$
- ② Enable Power / clock to ADC0  
 $\text{PCONP} |= (\text{unsigned long})(0x00000001) \ll 12; // \text{Power control for peripheral}$
- ③ Select ADC channel 3 (ADD.3)  
 $\text{ADOCR} |= 0x00000008; // \text{control Register (bits 7:0)}$
- ④ Set ADC clock as IPB or (PCLK) /8  
 $\text{ADOCR} |= 0x00000700; // (\text{CLKDIV} = 00000111) (\text{bits 15:8})$
- ⑤ Disable Burst mode  
 $\text{ADOCR} \&= 0xFFFFEFFF; // \text{Burst} = 0 (\text{bit 16})$
- ⑥ Set Resolution as 10 bit in 11 clock cycles  
 $\text{ADOCR} \&= 0xFFFF1FFF; // \text{CLKS} = 000 (\text{bits 19:17})$
- ⑦ Activate ADC module  
 $\text{ADOCR} |= 0x00200000; // \text{PDN} = 1 (\text{bit 21})$

⑨ Start the conversion Now

ADOCR 1 = 0x01000000; //START = 001 (Bits 26:24)

⑩ Wait ADC conversion to complete (global data register)

while ((ADOGDR & 0x80000000) == 0); //DONE = 1 (bit 31)

⑪ Read ADC Data Register

val = (ADD.R3 >> 6) & 0x000003FF; //RESULT = 10 Bit Data (15:6)

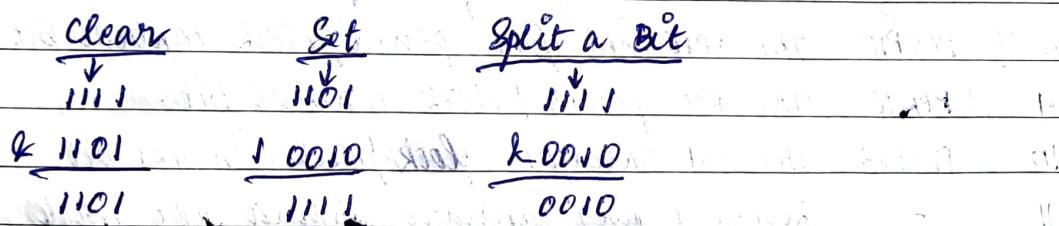
⑫ Deactivate ADC module (No Start)

ADOCR 4 = 0xF8FFFFFF; //START = 000 (Bits 26:24)

\* STEP 1 - PINSEL1 <29:28> = 01 :

PINSEL1 & = 0xFFFFFFFF; //ND1 1111 1111 1111 1111 1111 1111 1111

PINSEL1 >= 0x10000000; //0000 0000 0000 0000 0000 0000 0000 0000



Bit clear/set

11100101  $\times$  1 000001010  
11111100  $\rightarrow$  11100110  
 11100000  
1 000001010  
 11100010

\* STEP 2 - PCONP 1 = (unsigned long)(0x00000001) << 12;

→ PCONP (Power Control for Peripherals) -

PTD

| Bit | Symbol  | Description                                                                                                        | Reset Value |
|-----|---------|--------------------------------------------------------------------------------------------------------------------|-------------|
| 0   | -       | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA          |
| 1   | PC0TMO  | Timer / Counter 0 power / clock control bit.                                                                       | 1           |
| 2   | PC1TMI  | Timer / Counter 1 power / clock control bit.                                                                       | 1           |
| 3   | PCVARTD | VARTD power / clock control bit.                                                                                   | 1           |
| 4   | PCVARTI | VARTI power / clock control bit.                                                                                   | 1           |
| 5   | PCPWMD  | PWMD power / clock control bit.                                                                                    | 1           |
| 6   | -       | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA          |
| 7   | PC12C0  | The I <sup>2</sup> C interface power / clock control bit.                                                          | 1           |
| 8   | PCSP10  | The SPI0 interface power / clock control bit.                                                                      | 1           |
| 9   | PERTC   | The RTC power / clock control bit.                                                                                 | 1           |
| 10  | PCSP11  | The SSP interface power / clock control bit.                                                                       | 1           |
| 11  | -       | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA          |
| 12  | PCADO   | A/D converter 0 (ADC0) power / clock control bit.                                                                  | 1           |

Note - clear the PDN bit in the ADCCR before clearing this bit and set this bit before setting PDN.

|   |   |   |   |   |   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

\* STEP 3 - ADCCR If. 0x00000008;

→ ADCCR (Control Register) -

| Bit | Symbol | Value | Description                                                                                                                                                                                                                                                                                                              | Reset value |
|-----|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 7:0 | SEL    |       | <p>Selects which of the ADO.1:0/ADI.7:0 pins is (are) to be sampled and converted. For ADO, bit 0 selects pin ADO.0, and bit 1 selects pin ADO.1.</p> <p>In software-controlled mode, only one of these bits should be 1. In hardware scan mode, any value containing 1 to 8 ones. All zeroes is equivalent to 0x01.</p> | 0x01        |

|          |                        |
|----------|------------------------|
| 00000001 | ADO.0 (ADCO channel 0) |
| 00000010 | ADO.1 (ADCO channel 1) |
| 00000100 | ADO.2 (ADCO channel 2) |
| 00001000 | ADO.3 (ADCO channel 3) |
| 00010000 | ADO.4 (ADCO channel 4) |
| 00100000 | ADO.5 (ADCO channel 5) |
| 01000000 | ADO.6 (ADCO channel 6) |
| 10000000 | ADO.7 (ADCO channel 7) |

\* STEP 4 - ADCCR  $\leftarrow$  0x00000100;  
 → ADCCR (control Register) -

|      |       |                                                                                                                                                                                                                                                                                                                                 |   |
|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| 15:8 | UKDIV | The VFB clock (PCLK) is divided by (this value plus one) to produce the clock for the A/D converter, which should be less than or equal to 4.5 MHz. Typically, software should program the smallest value in this field that yields a clock of 4.5 MHz or slightly less, but in certain cases, (such as a high-impedance analog | 0 |
|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|

source) a slower clock may be desirable:

00000000 ADC Clock = (PCLK)/1

00000001 ADC Clock = (PCLK)/2

00000010 ADC Clock = (PCLK)/3

00000011 ADC Clock = (PCLK)/4

00000100 ADC Clock = (PCLK)/5

00000101 ADC Clock = (PCLK)/6

00000110 ADC Clock = (PCLK)/7

00000111 ADC Clock = (PCLK)/8

# STEP 5 - ADDCR 9 = 0xFFFFFFF ;  
 → ADDCR (control Register) -

16

BURST

The AD converter does repeated conversions at the rate selected by the CKS field, scanning (if necessary) through the pins selected by 1s in the SEL field. The first conversion after the start corresponds to the least-significant 1 in the SEL field, then higher numbered 1-bits (pins) if applicable. Repeated conversions can be terminated by clearing this bit, but the conversion that's in progress when this bit is cleared will be completed.

Important - START bits must be 000 when BURST=1 or conversions will not start.

|   |                                                            |
|---|------------------------------------------------------------|
| 0 | Conversions are software controlled and require 11 clocks. |
|---|------------------------------------------------------------|

\* STEP 6 - ADDCR & = 0xFFFFFFF;

→ ADDCR (Control Registers) -

|       |       |                                                                                                                                                                                                                 |     |
|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 19:17 | CLKS. | This field selects the number of clocks used for each conversion in burst mode, and the number of bits of accuracy of the result in the RESULT bits of ADDR, between 11 clocks (10 bits) and 4 clocks (3 bits). | 000 |
|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

000 11 clocks / 10 bits

001 10 clocks / 9 bits

010 9 clocks / 8 bits

011 8 clocks / 7 bits

100 7 clocks / 6 bits

101 6 clocks / 5 bits

110 5 clocks / 4 bits

111 4 clocks / 3 bits

\* STEP 7 - ADDCR 1 = 0x00200000;

|    |     |   |                                          |   |
|----|-----|---|------------------------------------------|---|
| 21 | PDN | 1 | The A/D converter is operational.        | 0 |
|    |     | 0 | The A/D converter is in power-down mode. |   |

\* STEP 8 - ADDCR 1 = 0x01000000;

→ ADCR (Control Registers) -

26: 24

START

When this BURST bit is 0, these bits control whether and when an A/D conversion is started:

|     |                                                                                            |
|-----|--------------------------------------------------------------------------------------------|
| 000 | No start (this value should be used when clearing PDN to 0).                               |
| 001 | start conversion now.                                                                      |
| 010 | start conversion when the edge selected by bit 27 occurs on P0.16/EINT0/MAT0.2/CAP0.2 pin. |
| 011 | start conversion when the edge selected by bit 27 occurs on P0.22/TD3/CAP0.0/MAT0.0 pin.   |
| 100 | start conversion when the edge selected by bit 27 occurs on MAT0.1.                        |
| 101 | start conversion when the edge selected by bit 27 occurs on MAT0.3.                        |
| 110 | start conversion when the edge selected by bit 27 occurs on MAT1.0.                        |
| 111 | start conversion when the edge selected by bit 27 occurs on MAT1.1.                        |

\* STEP 9 - while (ADGDR & 0x80000000)  $\neq 0$ :

→ ADGDR (global data Register) -

| Bit  | Symbol | Description                                                                                                                                                                           | Reset Value |
|------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 5:0  | -      | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.                                                                    | NA          |
| 15:6 | RESULT | When DONE is 1, this field contains a binary fraction representing the voltage on the Ain pin selected by the SEL field, divided by the voltage on the VDDA pin ( $V/V_{REF}$ ). Zero | NA          |

in the field indicates that the voltage on the AIN pin was less than, equal to, or close to that on V<sub>SSA</sub>, while 0x3FF indicates that the voltage on AIN was close to, equal to, or greater than that on V<sub>REF</sub>.

23:16 - Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.

26:24 CHN These bits contain the channel from which the RESULT bits were converted (e.g. 000 identifies channel 0, 001 channel 1...).

29:27 - Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.

30 OVERRUN This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the RESULT bits. This bit is cleared by reading this register.

31 DONE This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read and when the ADCR is written. If the ADCR is written while a conversion is still in progress, this bit is set and a new conversion is started.

\* STEP 10 - val = (ADDDR3 >> 6) & 0x000003FF;

→ ADDDR3 (Data Register) -

| Bit   | Symbol  | Description                                                                                                                                                                                                                                                                                                                                                                                               | Reset Value |
|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 5:0   | -       | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.                                                                                                                                                                                                                                                                                        | NA          |
| 15:6  | RESULT  | When DONE is 1, the field contains a binary fraction representing the voltage of the $A_{in}$ pin, dividing by the voltage on the $V_{REF}$ pin ( $V/V_{REF}$ ). Zero in the field indicates that the voltage on the $A_{in}$ pin was less than, equal to, or close to that on $V_{SSA}$ , while 0x3FF indicates that the voltage on $A_{in}$ was close to, equal to, or greater than that on $V_{REF}$ . | NA          |
| 29:16 | -       | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.                                                                                                                                                                                                                                                                                        | NA          |
| 30    | OVERRUN | This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced in the result in the RESULT bits. The bit is cleared by reading this register.                                                                                                                                                                                  |             |
| 31    | DONE    | The bit is set to 1 when an A/D conversion completes. It is cleared when this register is read.                                                                                                                                                                                                                                                                                                           | NA          |

\* STEP II - ADDCR & = 0xFFFFFFFF;