Project Plan report format – Your first page MUST match this format

/10

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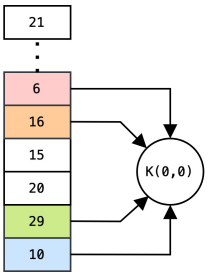
Summary Risk Plan:

1. I am reading 16 values from the input SRAM corresponding to a set four 3x3 matrices and storing them in a buffer.
2. I was not able to figure out a way to multiply the values in the buffer with the corresponding kernel element while simultaneously filling the buffer
3. Hence, the input SRAM is idle while I am multiplying the matric and kernel elements together

Schedule:
11-07: Create project skeleton
11-12: Design input SRAM read
11-13: Design input buffer
11-14: Design MACC, max pool, and ReLu.
11-16: Complete RTL Implementation
11-19: Synthesize design

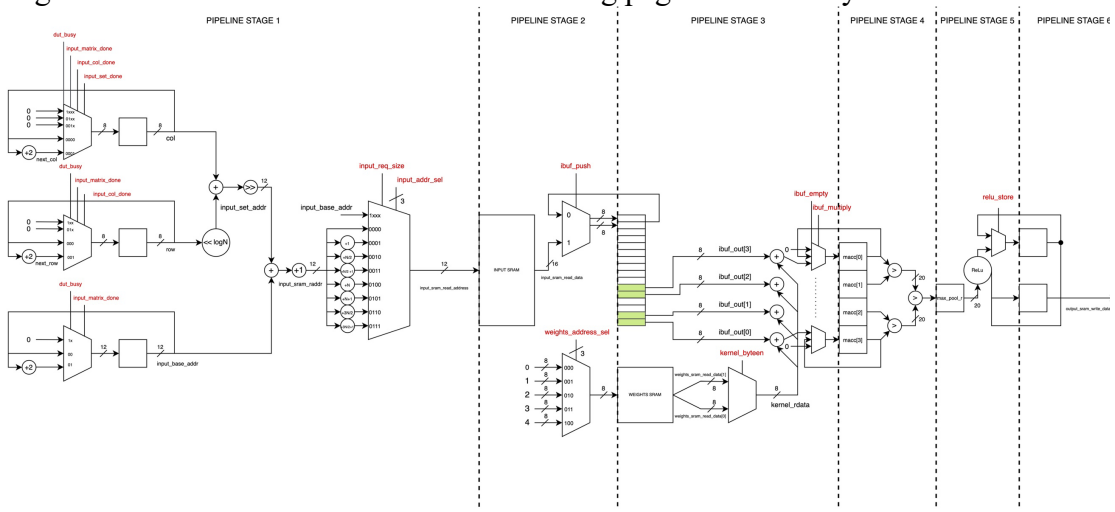
Brief Description of Mode of operation, including selected algorithms

10	29	20	15	30	14	0	30
16	6	0	24	5	15	26	4
20	6	20	33	10	20	1	34
26	19	23	21	18	4	33	27
9	2	13	15	7	20	1	31
19	29	17	32	32	23	31	7
18	6	32	19	6	10	28	1
9	1	6	12	15	10	8	13



The blue, green, orange, and red elements correspond to the first elements of each matrix among the set of four 3x3 matrices.
These four elements are multiplied with the same kernel element
The input buffer is a *shift register*. Once the first multiplication is done, the elements are shifted down by 1 position.
Thus, the elements 29, 20, 6, and 0 are multiplied with the second kernel element

High level sketch. Add details on the following pages if necessary



Final Project Report First Page. Must match this format (Title)

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Delay (ns to run provided example). Clock period: 4.8ns # cycles": 5104 + 1936 = 7040 Delay: 33,792 ns	Logic Area: 6612.2280 (um^2)	1/(delay.area): 4.475466×10^{-9} ($ns^{-1}.um^{-2}$)
Delay (TA provided example. TA to complete)		1/(delay.area) (TA)

Abstract

Abstract should briefly summarize that the hardware function is (remember a future employer might be reading this), what your approach was, and the main results achieved.

Project Title
Student names

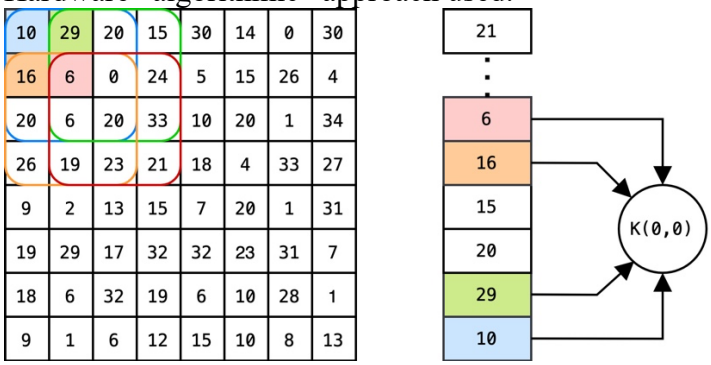
Abstract
This report describes a high level overview of the design process for the convolution stage of a convolutional neural network

1. Introduction

- What hardware is being designed here
  - The hardware being designed is the convolution stage of a convolutional neural network including a max pooling and a ReLu activation layer.
- Summary of key innovations if any claimed
- Summary of results achieved.
- Structure of the rest of this report

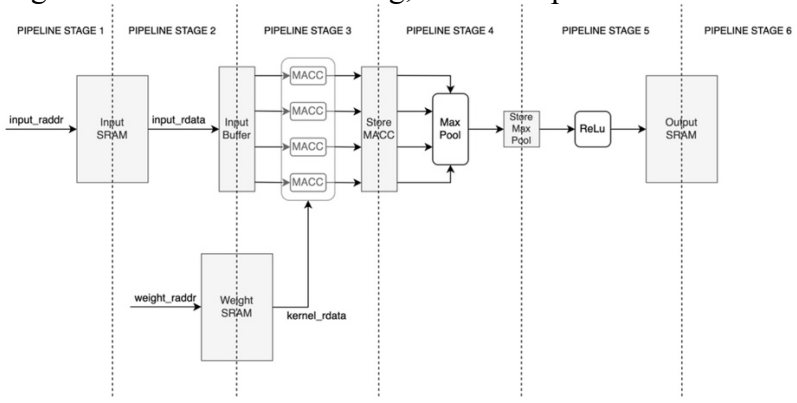
2. Micro-Architecture

- Hardware "algorithmic" approach used.



- The blue, green, orange, and red elements correspond to the first elements of each matrix among the set of four 3x3 matrices.
- These four elements are multiplied with the same kernel element
- The input buffer is a *shift register*. Once the first multiplication is done, the elements are shifted down by 1 position.
- Thus, on the next cycle the elements 29, 20, 6, and 0 are multiplied with the second kernel element

- High level architecture drawing, and description of data flow



3. Interface Specification

- Detailed description of top level interface to your design
- Include a table listing each signal, its width and function
- Include an interface timing diagram if needed

4. Technical Implementation

- Discussion of high level modeling (if used) and results achieved
- Discussion of any hierarchy
- Discussion, if needed, of detailed implementation

5. Verification

- Description of approach used to verify correctness.
  - Values of intermediate stages are generated from the python script provided with the project
  - I verified my design by comparing the output of `$display` with these intermediate values

6. Results Achieved

- Throughput, area, power/energy (if applicable), etc.
  - Cycles = 7040
  - Clock period = 4.8ns
  - Delay = 33,792 ns
  - Area = 6612.2280 um^{-2}

7. Conclusions

- Summary of project and key results