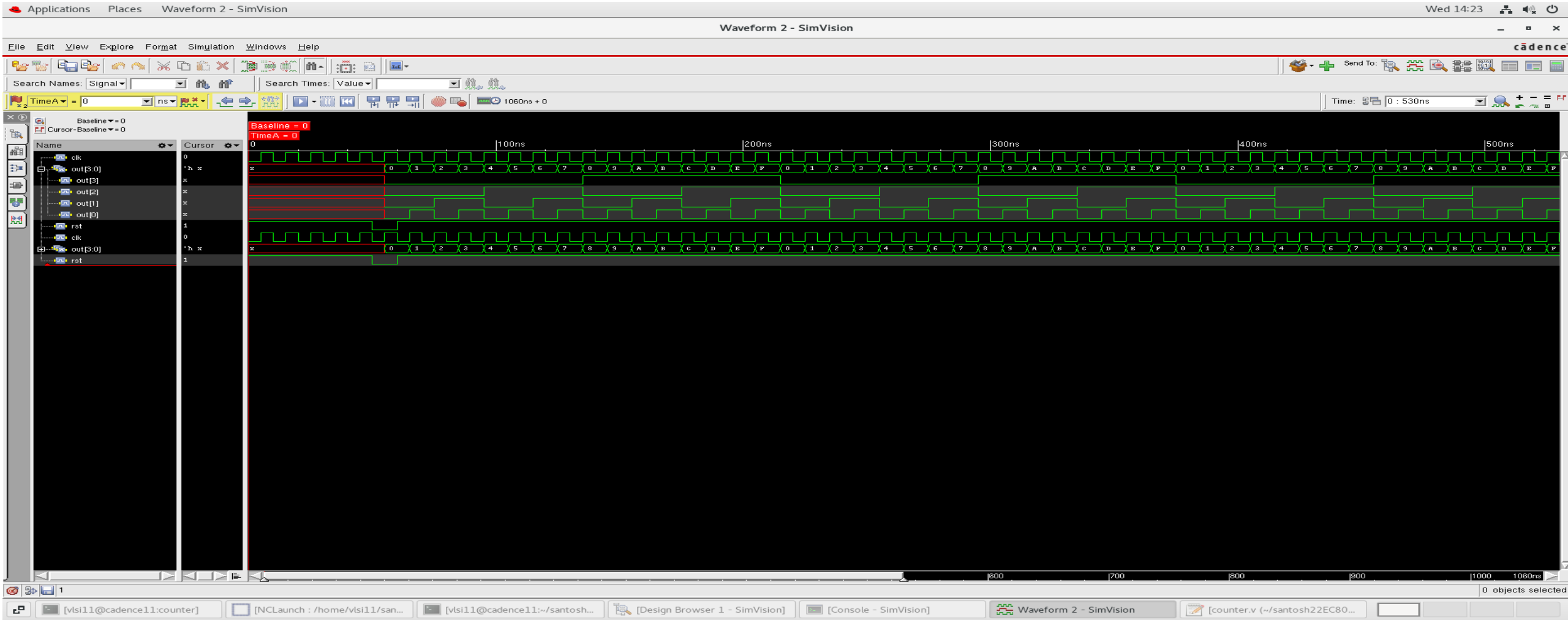
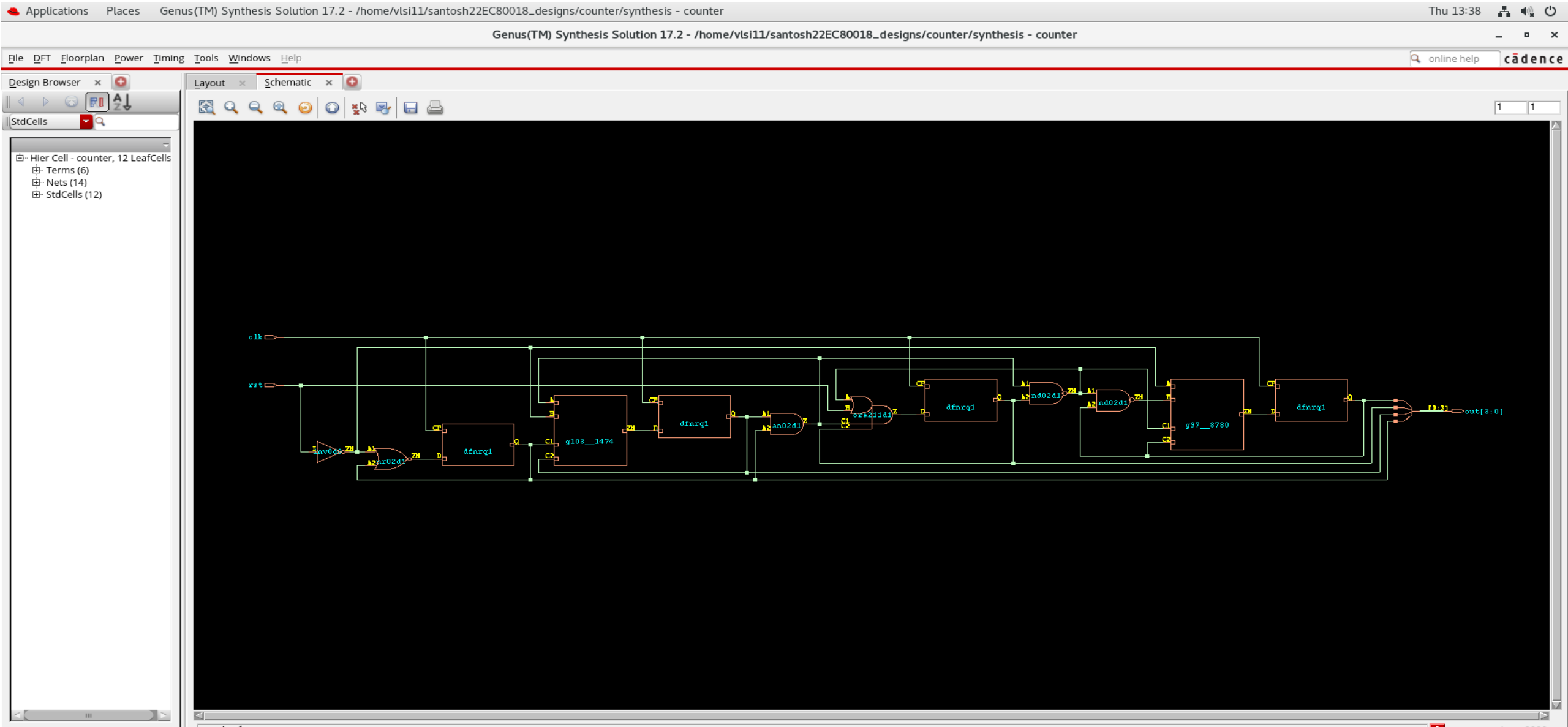
4-BIT UP COUNTER

Compilation & Elaboration of counter Verilog Code and its test_bench .
After that next step is Simulation
then this waveform will get generated.



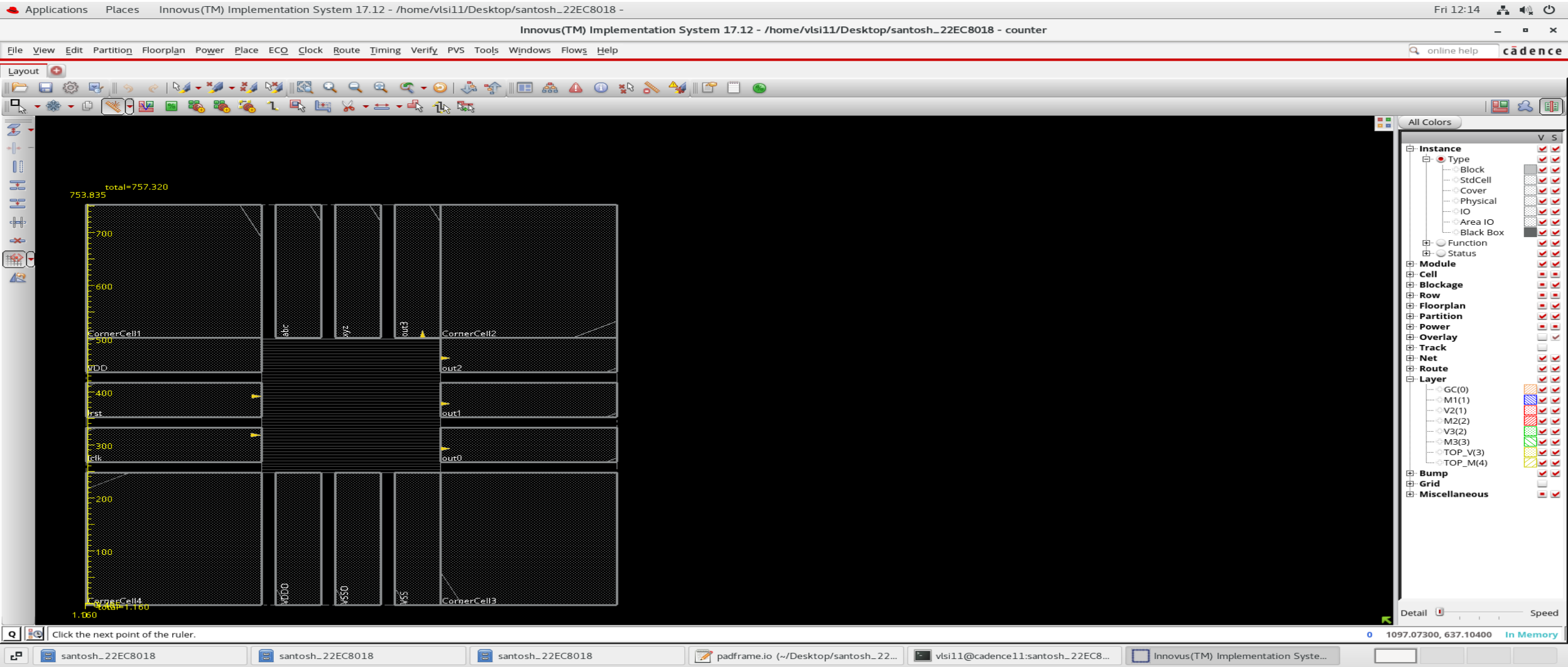
LOGIC SYNTHESIS USING CADENCE GENUS TOOL

Genus is a next-generation RTL synthesis and physical synthesis tool
A “Gate Level Netlist” will generated after synthesis

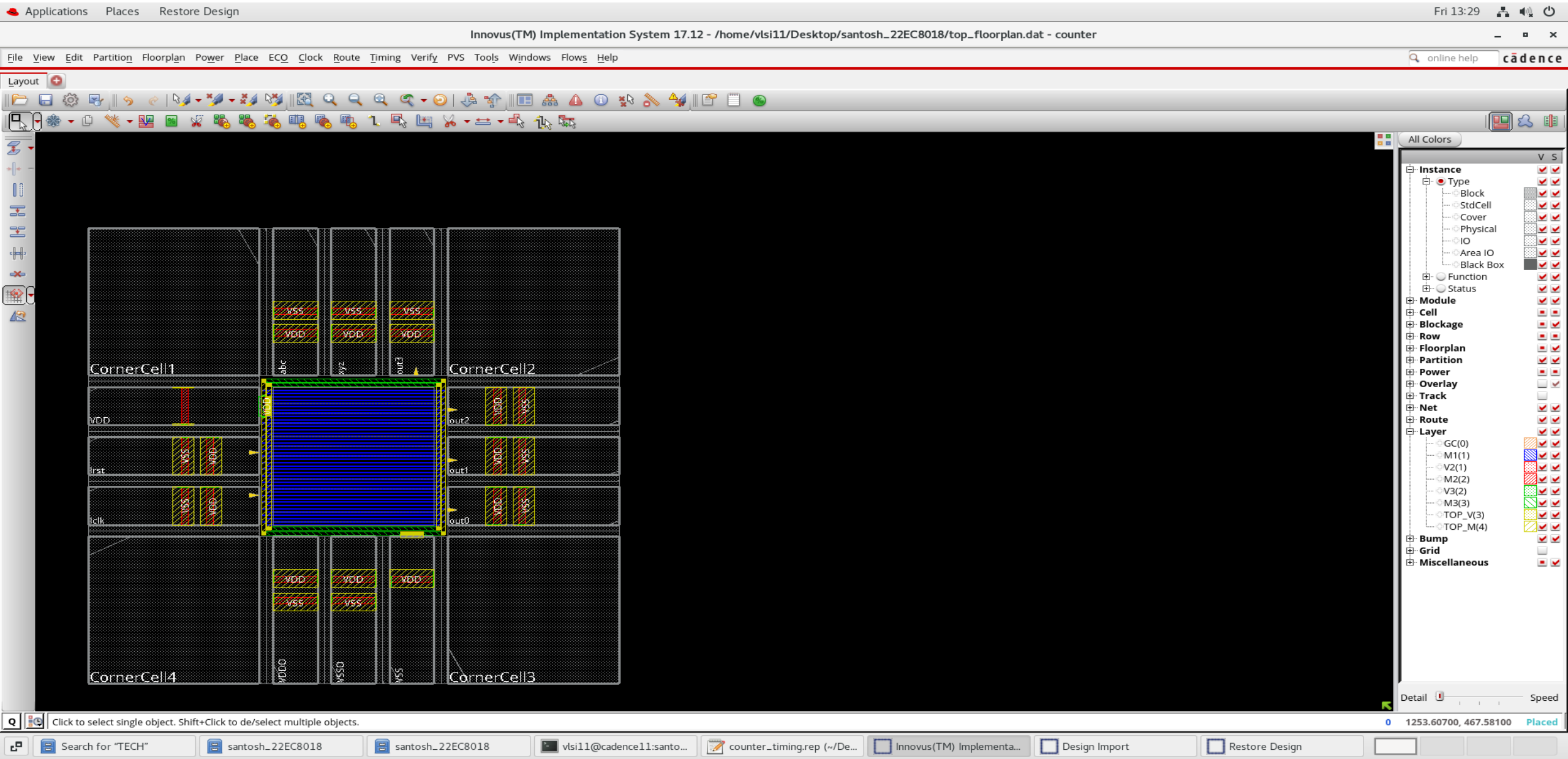


PHYSICAL DESIGN USING CADENCE INNOVUS TOOL

a blank chip with auto-placed IO pads



Power Planning :

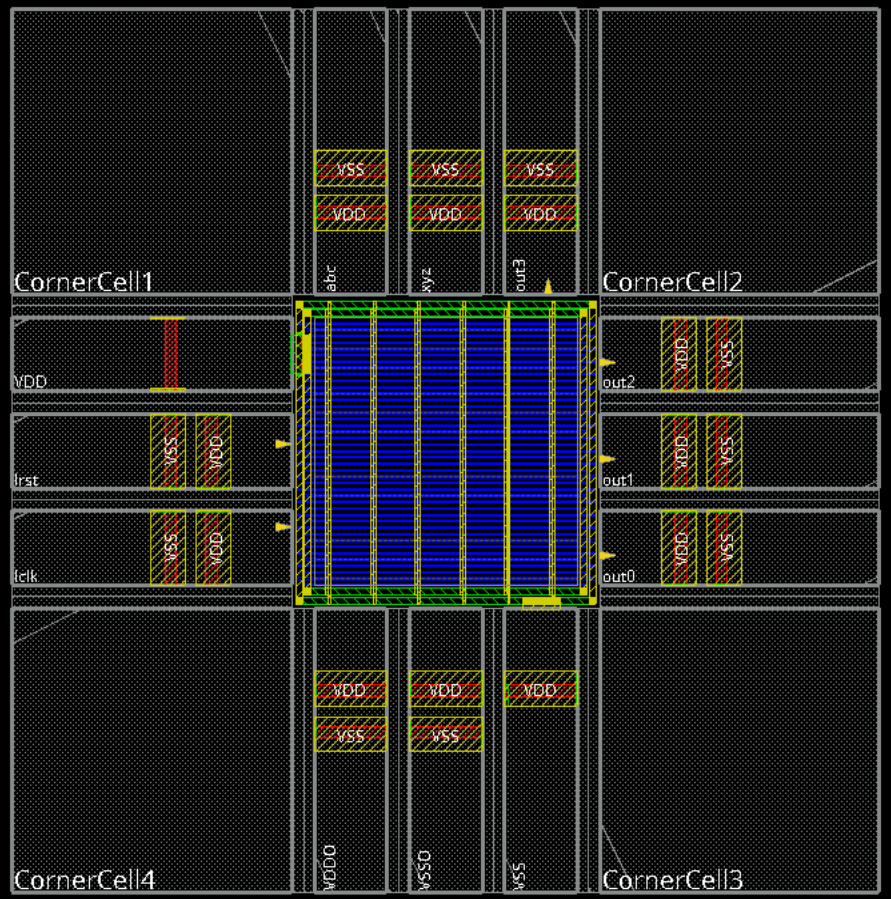


Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter

File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help

online help cadence

Layout



All Colors

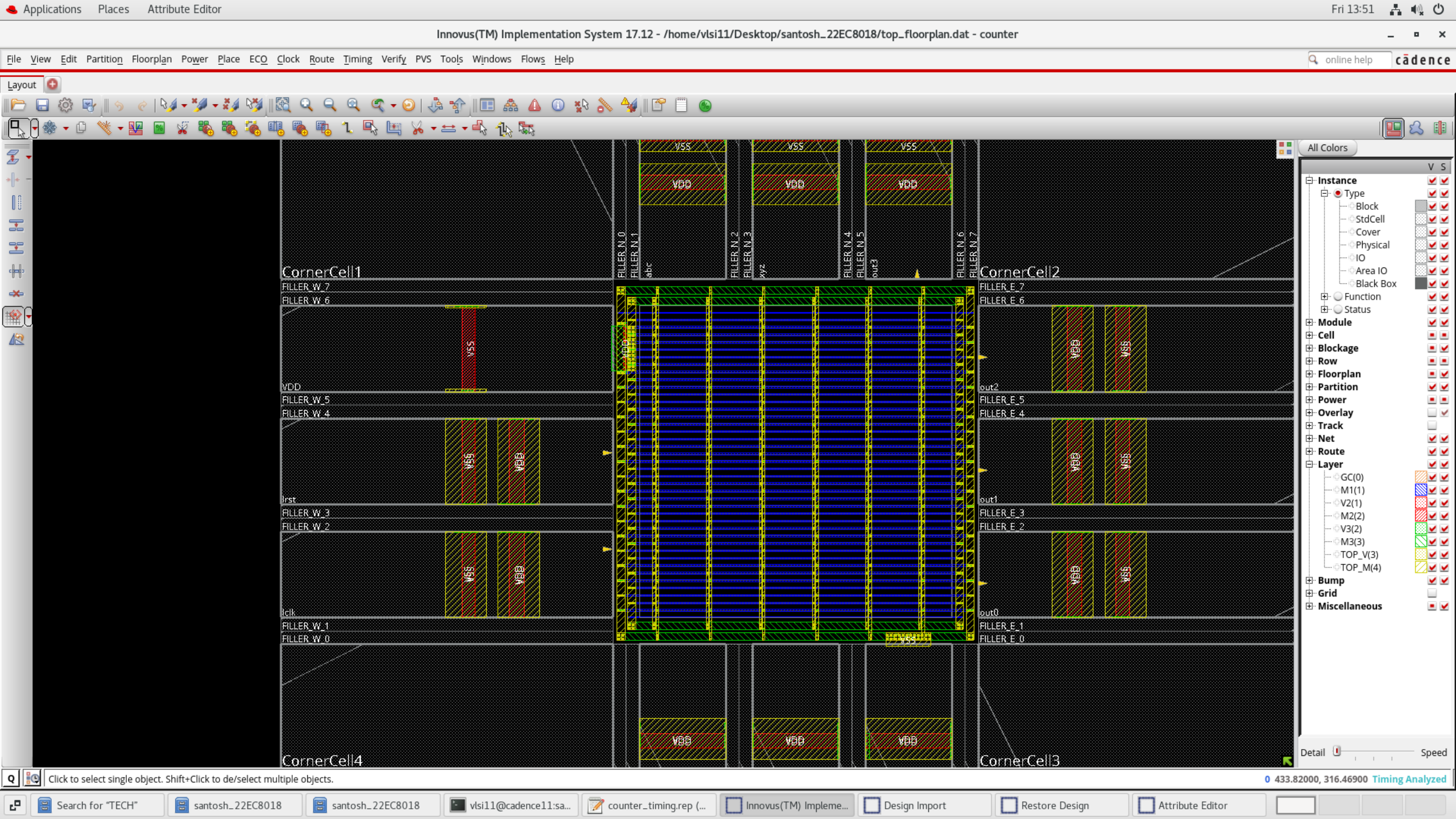
V S

- Instance
  - Type
    - Block
    - StdCell
    - Cover
    - Physical
    - IO
    - Area IO
    - Black Box
  - Function
  - Status
- Module
- Cell
- Blockage
- Row
- Floorplan
- Partition
- Power
- Overlay
- Track
- Net
- Route
- Layer
  - GC(0)
  - M1(1)
  - V2(1)
  - M2(2)
  - V3(2)
  - M3(3)
  - TOP_V(3)
  - TOP_M(4)
- Bump
- Grid
- Miscellaneous

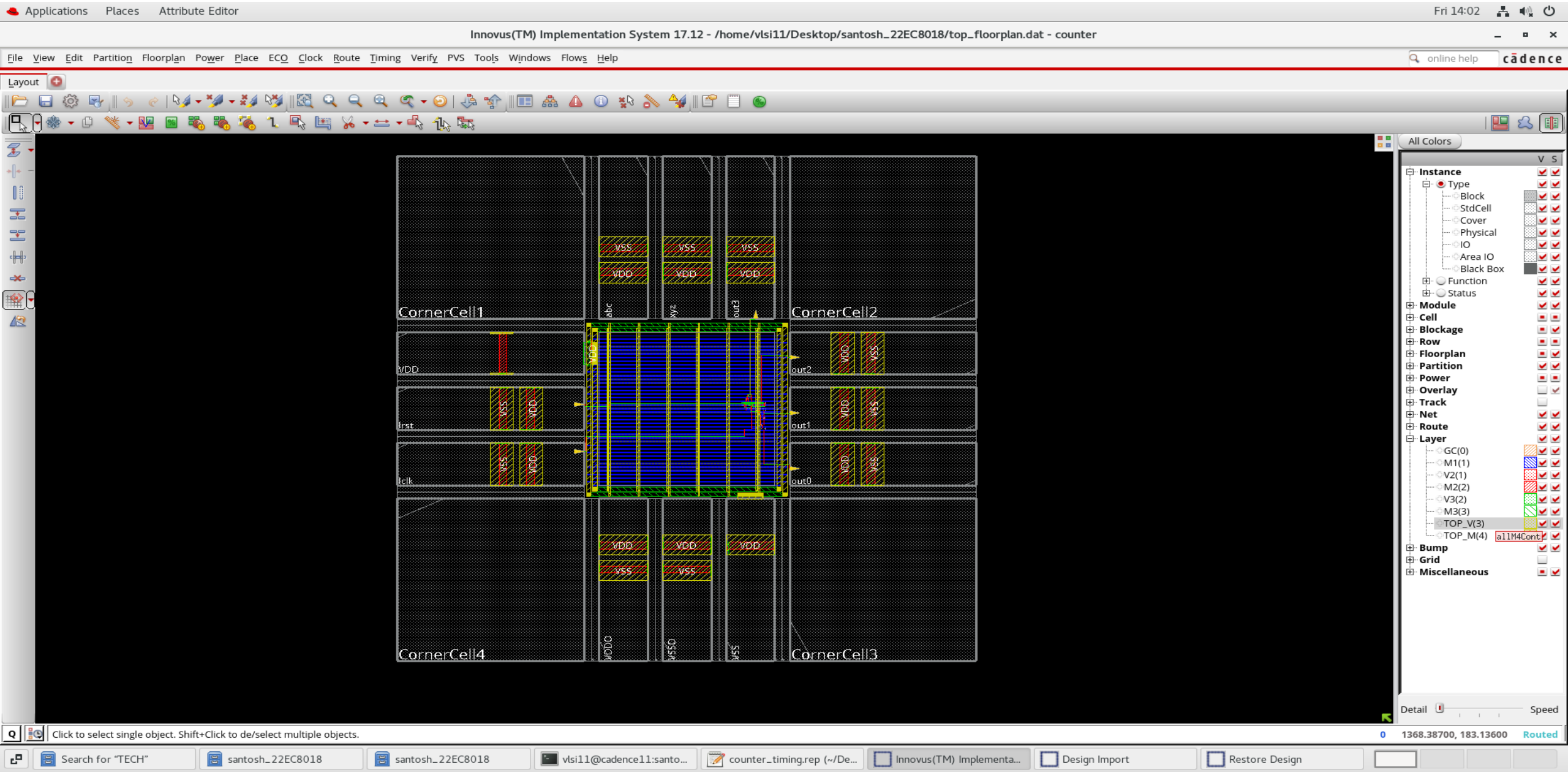
Detail Speed

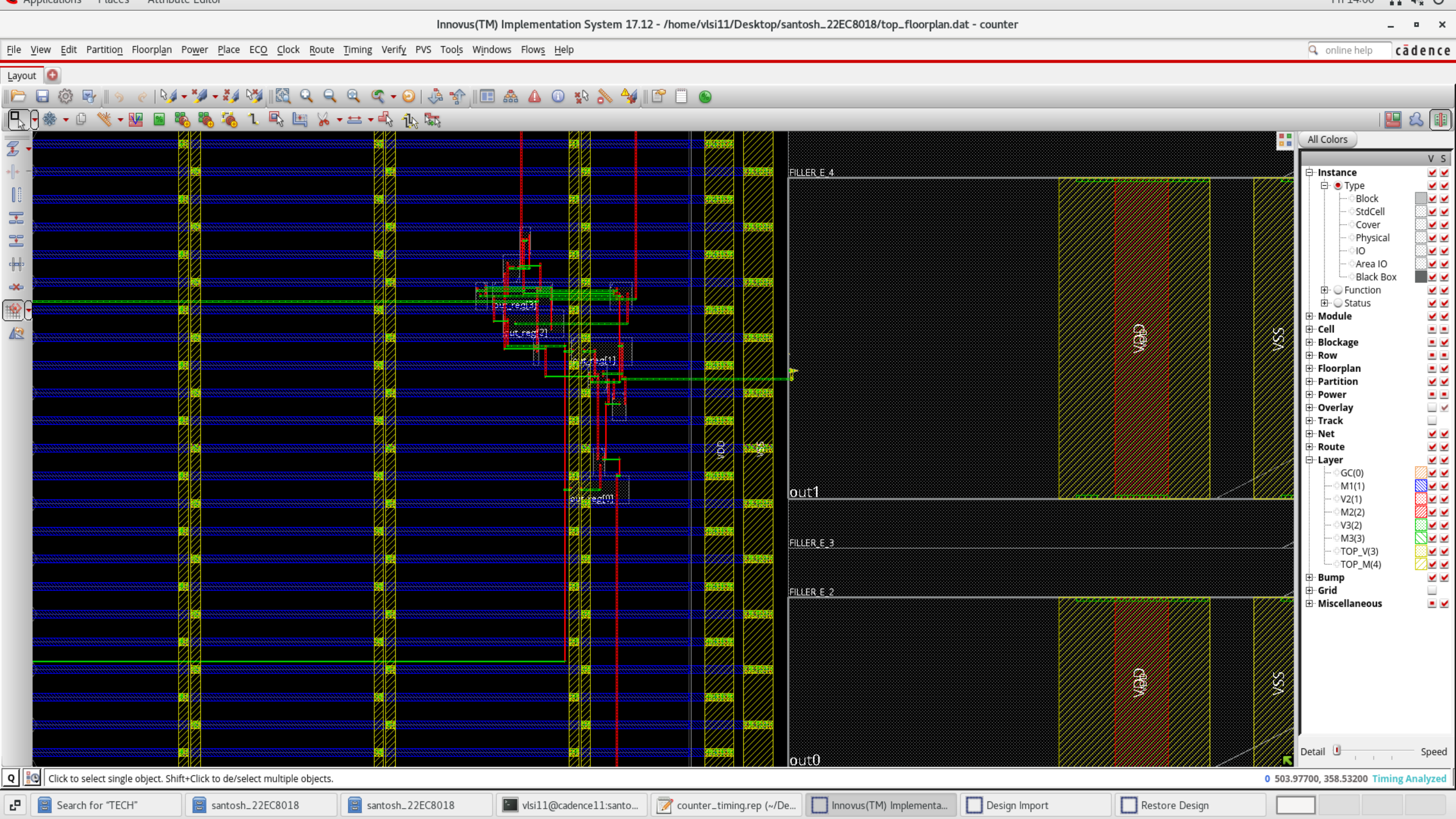
0 810.24000, 264.99600 Routed

Search for "TECH" | santosh_22EC8018 | santosh_22EC8018 | vlsi11@cadence11:santo... | counter_timing.rep (~/De... | Innovus(TM) Implementa... | Design Import | Restore Design


Applications
Places
Attribute Editor
Fri 13:51
Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
V S
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
GC(0)
M1(1)
V2(1)
M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
CornerCell1
CornerCell2
CornerCell3
CornerCell4
FILLER_W_7
FILLER_W_6
FILLER_W_5
FILLER_W_4
FILLER_W_3
FILLER_W_2
FILLER_W_1
FILLER_W_0
FILLER_E_7
FILLER_E_6
FILLER_E_5
FILLER_E_4
FILLER_E_3
FILLER_E_2
FILLER_E_1
FILLER_E_0
VDD
VSS
lrst
lclk
out2
out1
out0
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
0 433.82000, 316.46900 Timing Analyzed
Search for "TECH"
santosh_22EC8018
santosh_22EC8018
vlsi11@cadence11:sa...
counter_timing.rep (...
Innovus(TM) Impleme...
Design Import
Restore Design
Attribute Editor

Placement & Clock Tree Synthesis




Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
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cadence
Layout
All Colors
V S
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StdCell
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IO
Area IO
Black Box
Function
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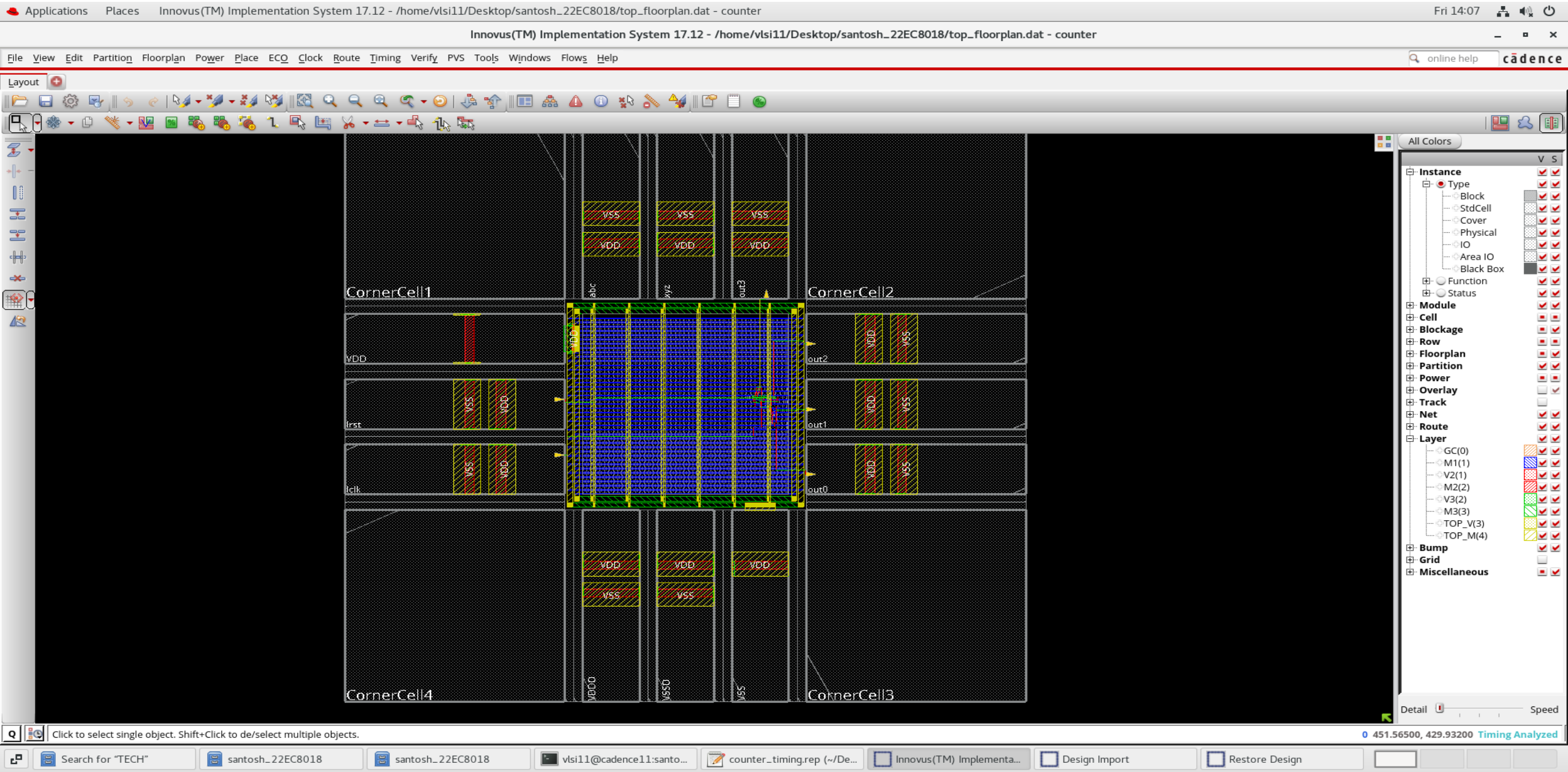
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
GC(0)
M1(1)
V2(1)
M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
FILLER_E_4
FILLER_E_3
FILLER_E_2
out1
out0
VDD
VSS
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
0 503.97700, 358.53200 Timing Analyzed
Search for "TECH"
santosh_22EC8018
santosh_22EC8018
vlsi11@cadence11:santo...
counter_timing.rep (~/De...
Innovus(TM) Implementa...
Design Import
Restore Design

Routing


Applications
Places
Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter
Fri 14:07
Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
CornerCell1
CornerCell2
CornerCell3
CornerCell4
VDD
VSS
lrst
lclk
out2
out1
out0
Instance
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Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
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Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
GC(0)
M1(1)
V2(1)
M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
0 451.56500, 429.93200 Timing Analyzed
Search for "TECH"
santosh_22EC8018
santosh_22EC8018
vlsi11@cadence11:santo...
counter_timing.rep (~/De...
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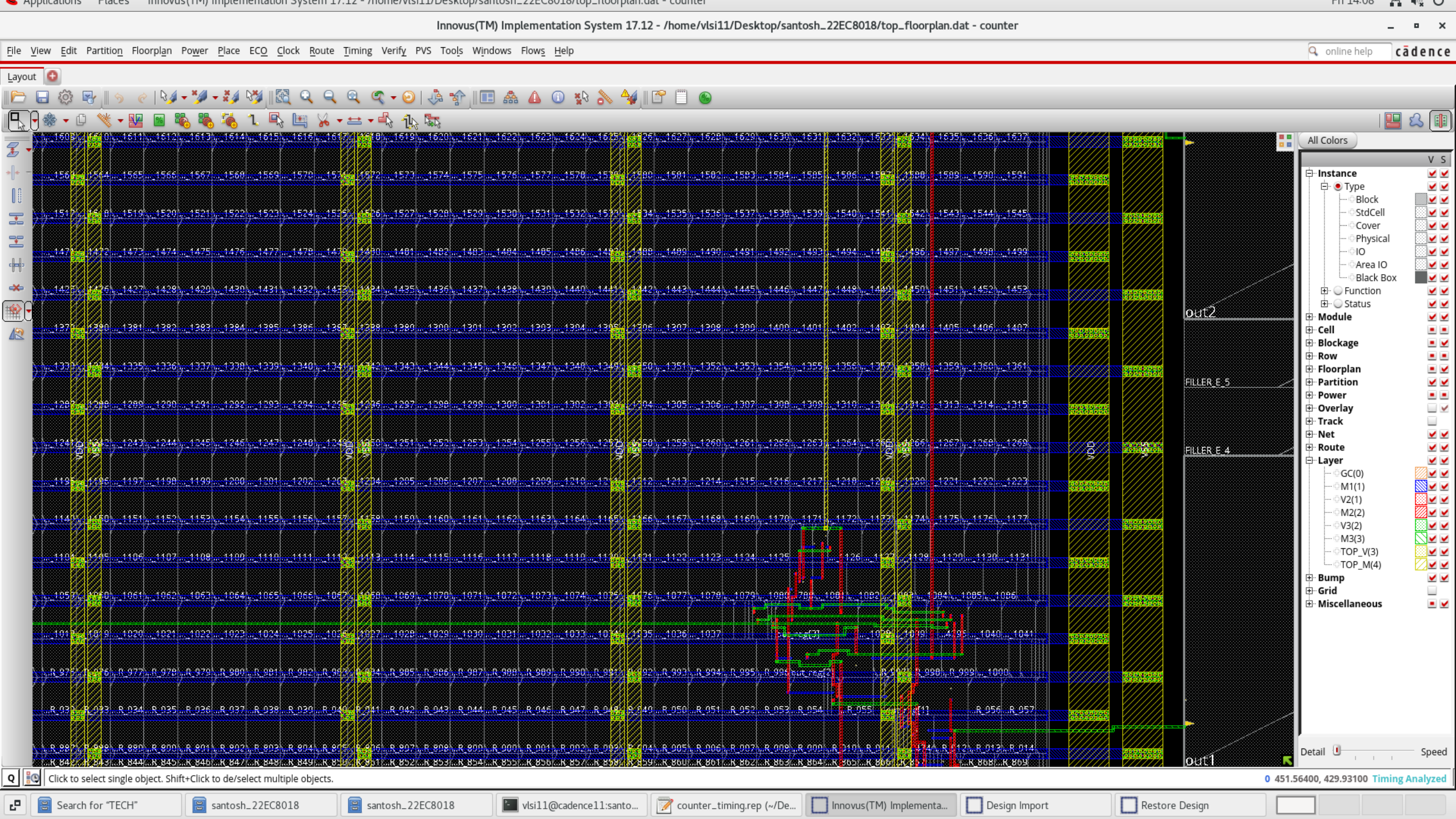
Design Import
Restore Design


Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22EC8018/top_floorplan.dat - counter
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
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StdCell
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Area IO
Black Box
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Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
GC(0)
M1(1)
V2(1)
M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
out2
FILLER_E_5
FILLER_E_4
out1
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
0 451.56400, 429.93100 Timing Analyzed
Search for "TECH"
santosh_22EC8018
santosh_22EC8018
vlsi11@cadence11:santo...
counter_timing.rep (~/De...
Innovus(TM) Implementa...
Design Import
Restore Design

Final Layout