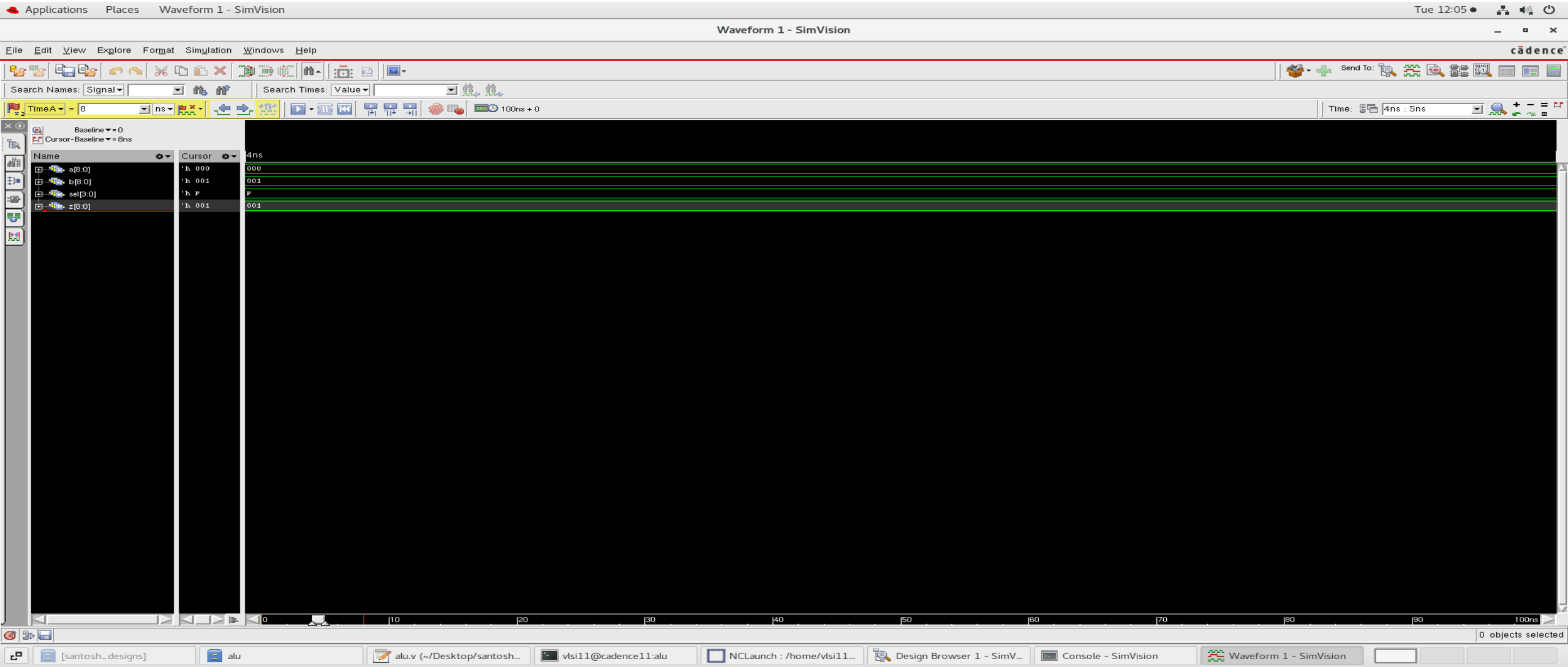
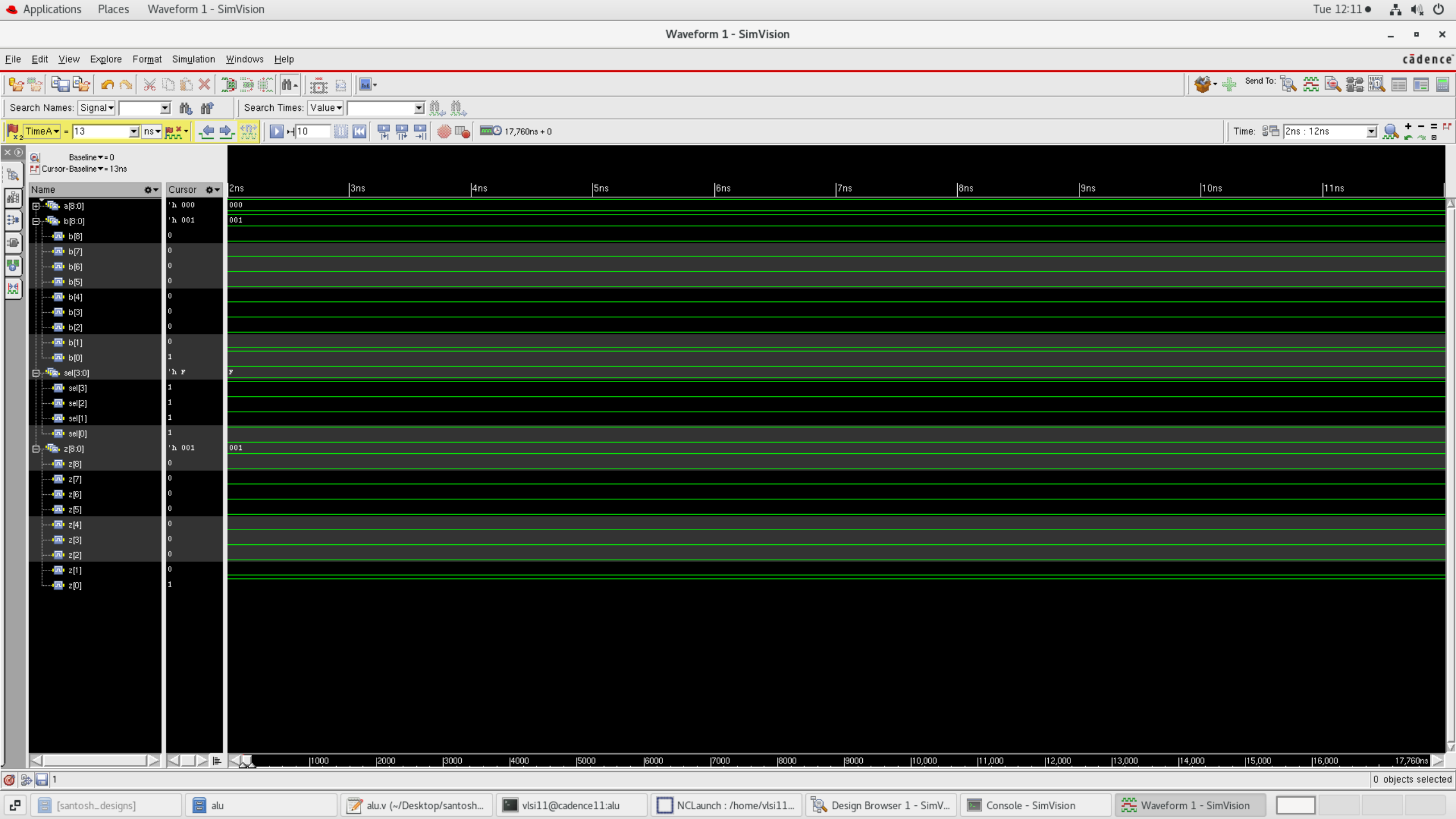
4-Bit ALU

Compilation & Elaboration of counter Verilog Code and its test_bench .
After that next step is Simulation
then this waveform will get generated

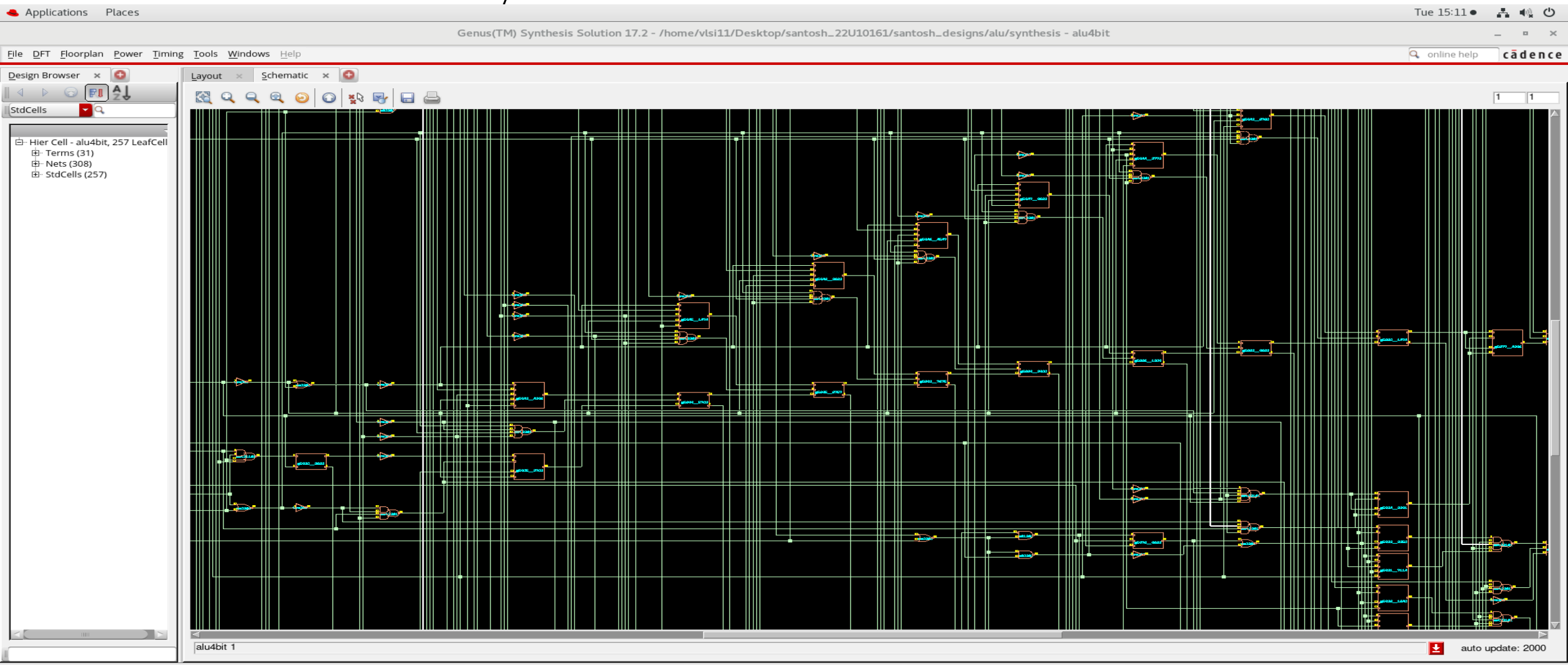



Applications
Places
Waveform 1 - SimVision
Tue 12:11
Waveform 1 - SimVision
File
Edit
View
Explore
Format
Simulation
Windows
Help
cadence
Send To:
Search Names:
Signal
Search Times:
Value
TimeA
13
ns
10
17,760ns + 0
Time:
2ns : 12ns
Baseline = 0
Cursor-Baseline = 13ns
Name
Cursor
a[8:0]
'h 000
b[8:0]
'h 001
b[8]
b[7]
b[6]
b[5]
b[4]
b[3]
b[2]
b[1]
b[0]
sel[3:0]
'h F
sel[3]
sel[2]
sel[1]
sel[0]
z[8:0]
'h 001
z[8]
z[7]
z[6]
z[5]
z[4]
z[3]
z[2]
z[1]
z[0]
2ns
3ns
4ns
5ns
6ns
7ns
8ns
9ns
10ns
11ns
000
001
F
001
1000
2000
3000
4000
5000
6000
7000
8000
9000
10,000
11,000
12,000
13,000
14,000
15,000
16,000
17,760ns
0 objects selected
[santosh_designs]
alu
alu.v (~/Desktop/santosh...
vlsi11@cadence11:alu
NCLaunch : /home/vlsi11...
Design Browser 1 - SimV...
Console - SimVision
Waveform 1 - SimVision

LOGIC SYNTHESIS USING CADENCE GENUS TOOL

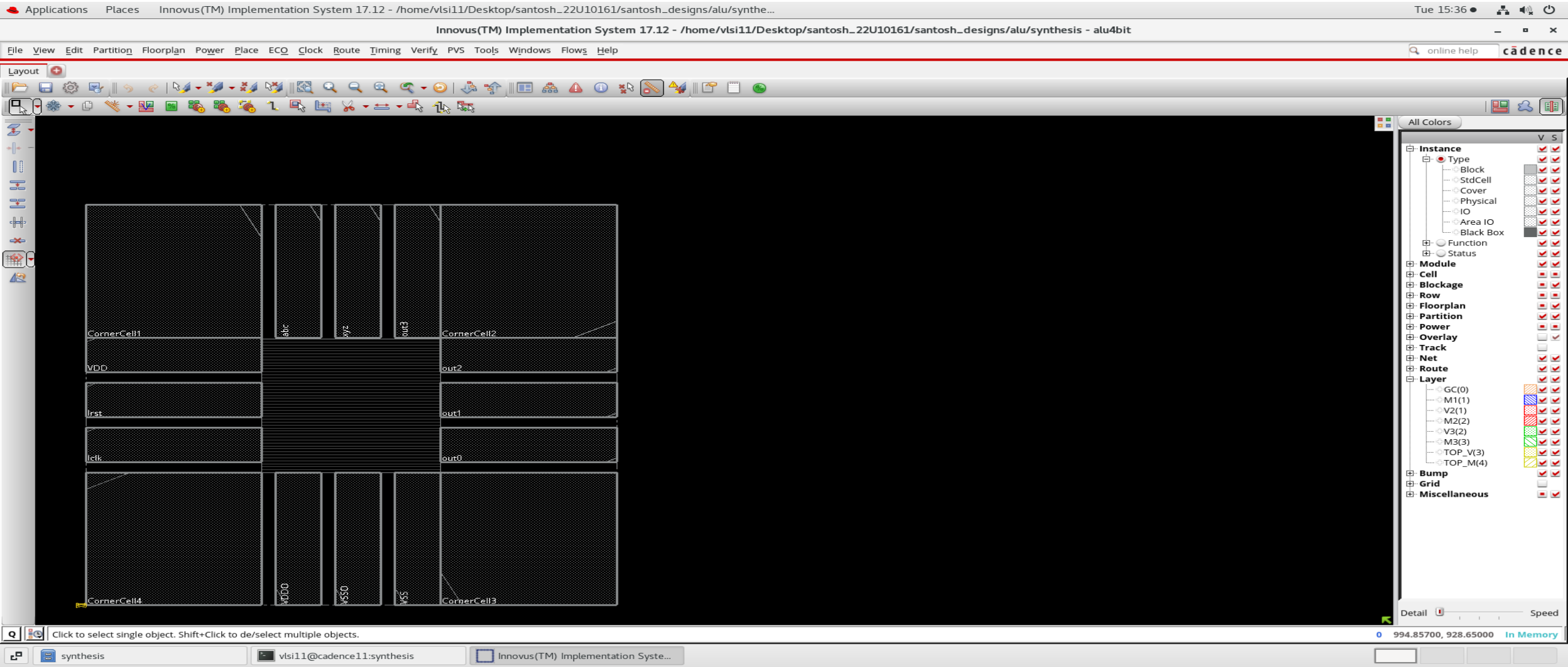
Genus is a next-generation RTL synthesis and physical synthesis tool

A “Gate Level Netlist” after synthesis

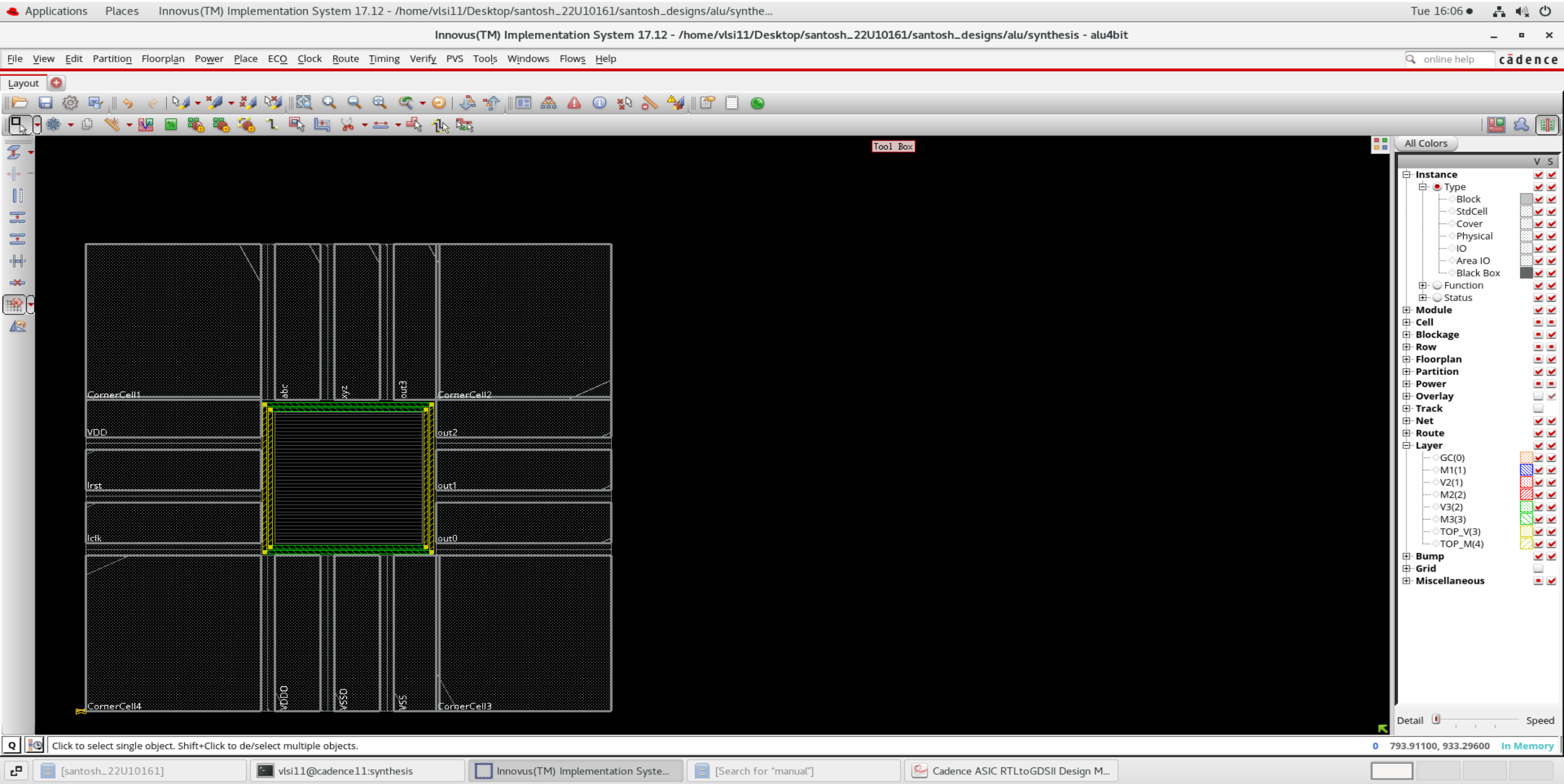


PHYSICAL DESIGN USING CADENCE INNOVUS TOOL

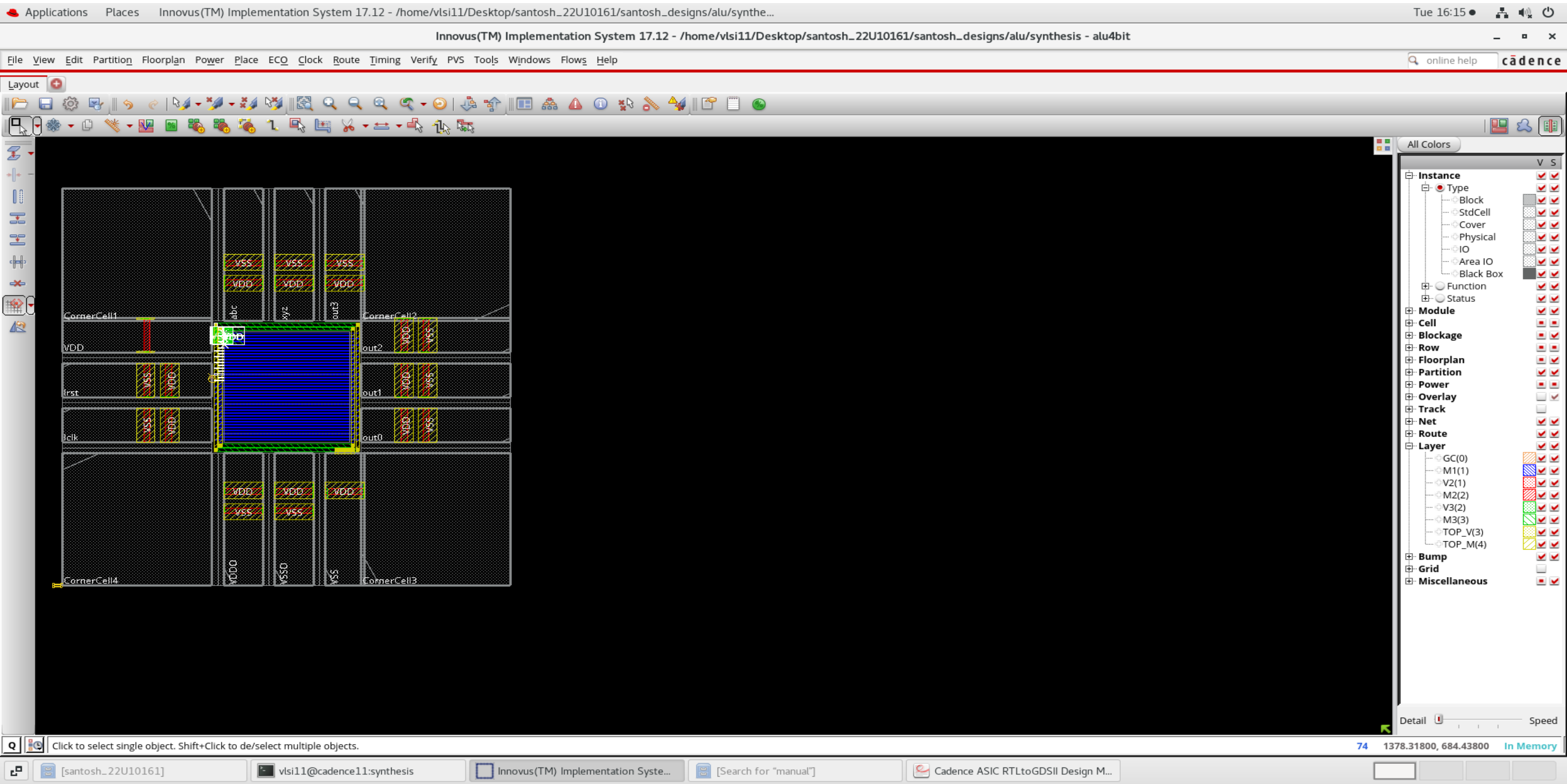
a blank chip with auto-placed IO pads

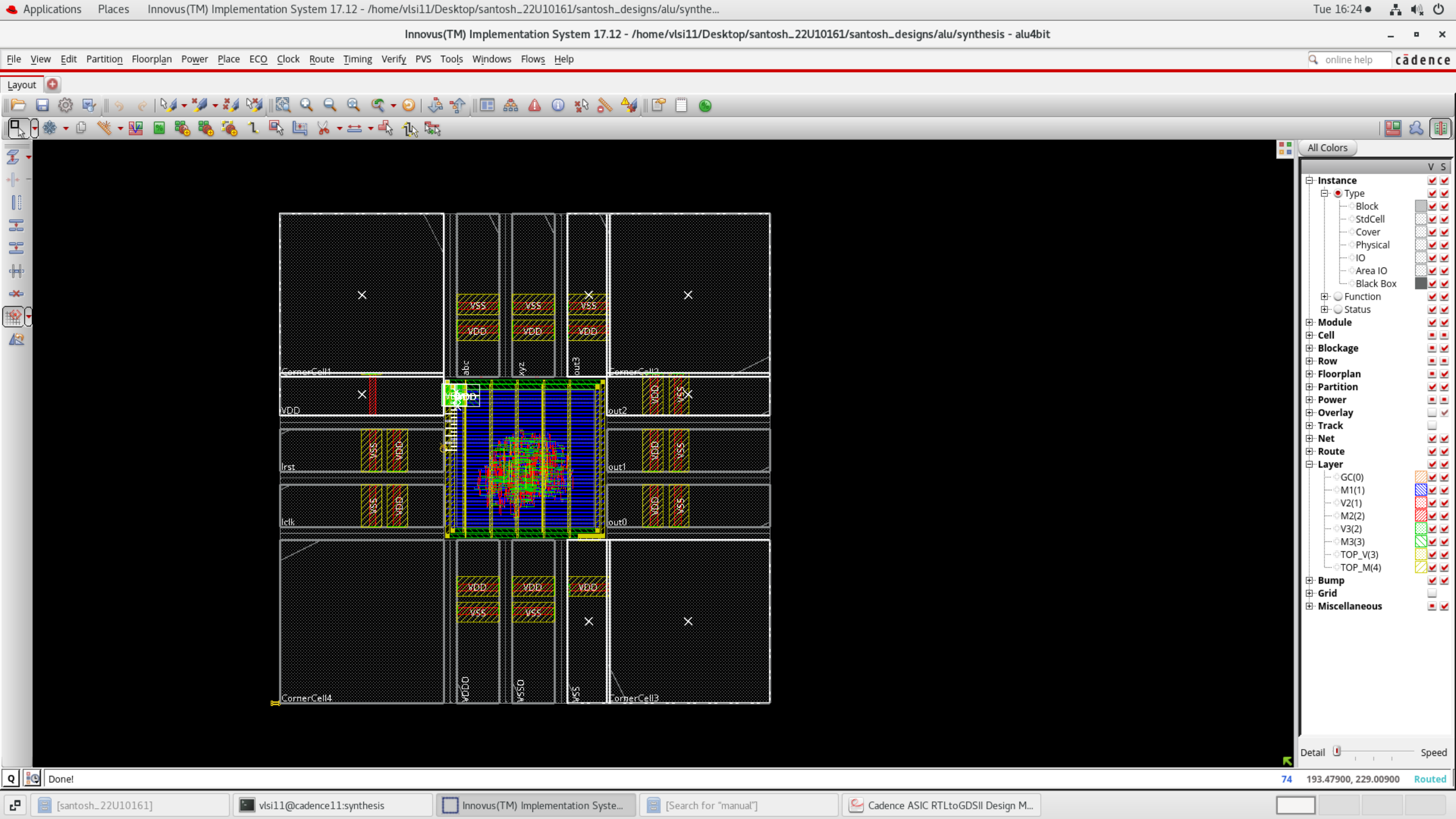


INNOVUS IMPLEMENTATION



POWER PLANNING




Applications
Places
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Tue 16:24
Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22U10161/santosh_designs/alu/synthesis - alu4bit
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
V S
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
GC(0)
M1(1)
V2(1)
M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
CornerCell1
CornerCell2
CornerCell4
CornerCell3
VDD
VSS
abc
xyz
out3
out2
out1
out0
lrst
lclk
VDDO
VSSO
Detail
Speed
Done!
74
193.47900, 229.00900
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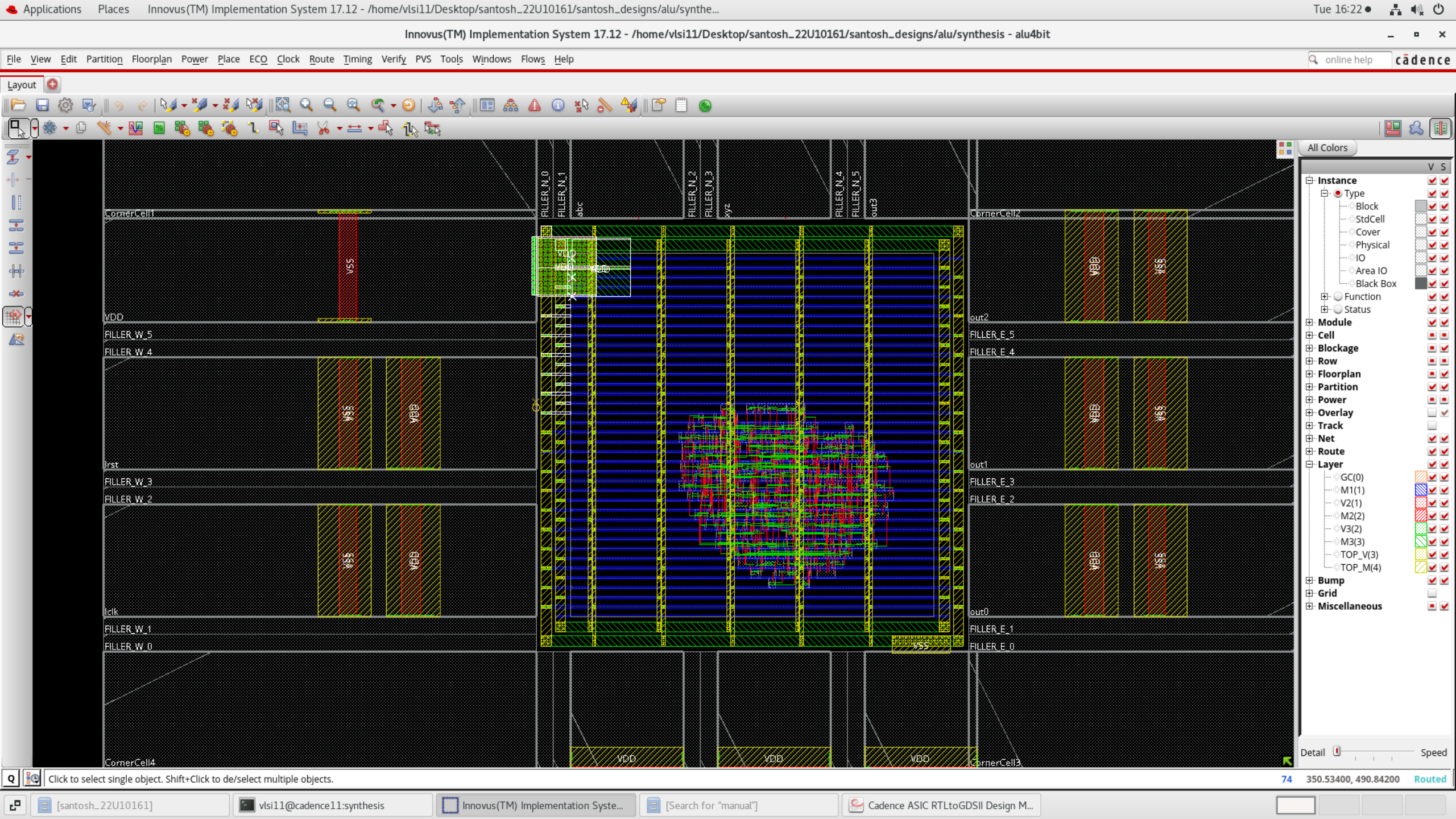
vlsi11@cadence11:synthesis
Innovus(TM) Implementation Syste...
[Search for "manual"]
Cadence ASIC RTLtoGDSII Design M...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Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22U10161/santosh_designs/alu/synthesis - alu4bit
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TOP_V(3)
TOP_M(4)
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Miscellaneous
Detail
Speed
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CornerCell2
CornerCell3
CornerCell4
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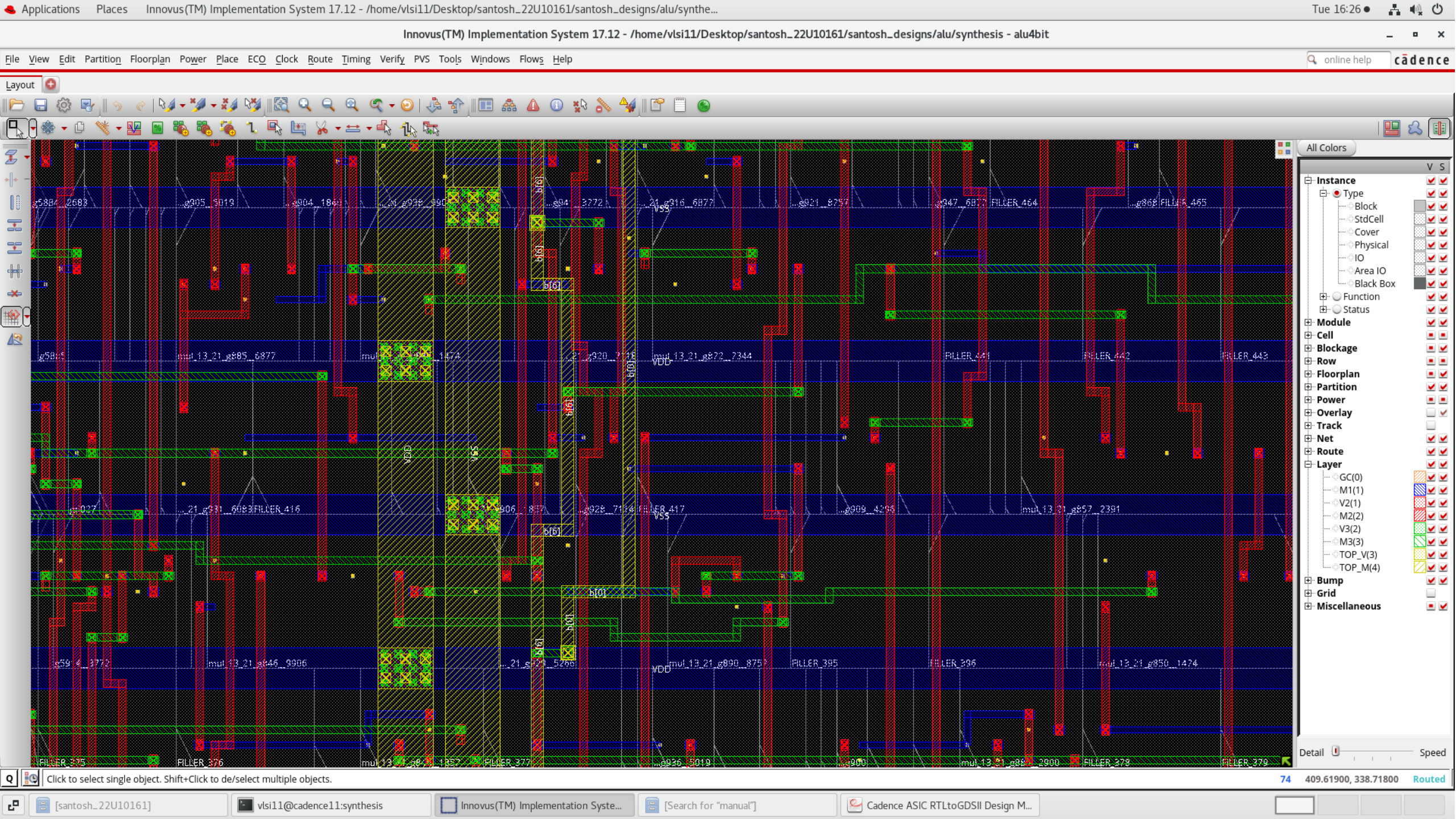
FILLER_N_1
FILLER_N_2
FILLER_N_3
FILLER_N_4
FILLER_N_5
FILLER_W_5
FILLER_W_4
FILLER_W_3
FILLER_W_2
FILLER_W_1
FILLER_W_0
FILLER_E_5
FILLER_E_4
FILLER_E_3
FILLER_E_2
FILLER_E_1
FILLER_E_0
VDD
VSS
out2
out1
out0
out3
Click to select single object. Shift+Click to de/select multiple objects.
74
350.53400, 490.84200
Routed
[santosh_22U10161]
vlsi11@cadence11:synthesis
Innovus(TM) Implementation Syste...
[Search for "manual"]
Cadence ASIC RTLtoGDSII Design M...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Innovus(TM) Implementation System 17.12 - /home/vlsi11/Desktop/santosh_22U10161/santosh_designs/alu/synthesis - alu4bit
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
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M2(2)
V3(2)
M3(3)
TOP_V(3)
TOP_M(4)
Bump
Grid
Miscellaneous
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
74
409.61900, 338.71800
Routed
[santosh_22U10161]
vlsi11@cadence11:synthesis
Innovus(TM) Implementation Syste...
[Search for "manual"]
Cadence ASIC RTLtoGDSII Design M...