```
library ieee;
use ieee.std_logic_1164.all;

entity siirtorekisteri is
  port(CLK, DATAIN:in std_logic; Q: out std_logic_vector(0 to 3));
end siirtorekisteri;

architecture toiminta of siirtorekisteri is
begin
  process(CLK)
  variable apu, talle: std_logic_vector(0 to Q'length-1);
  begin
    talle:=apu;
    if (CLK='1' and CLK'event) then
      for i in 0 to Q'length-2 loop
        apu(i+1):=talle(i);
      end loop;
      apu(0):= DATAIN;
    end if;
    Q<=apu;
  end process;
end toiminta;
```