

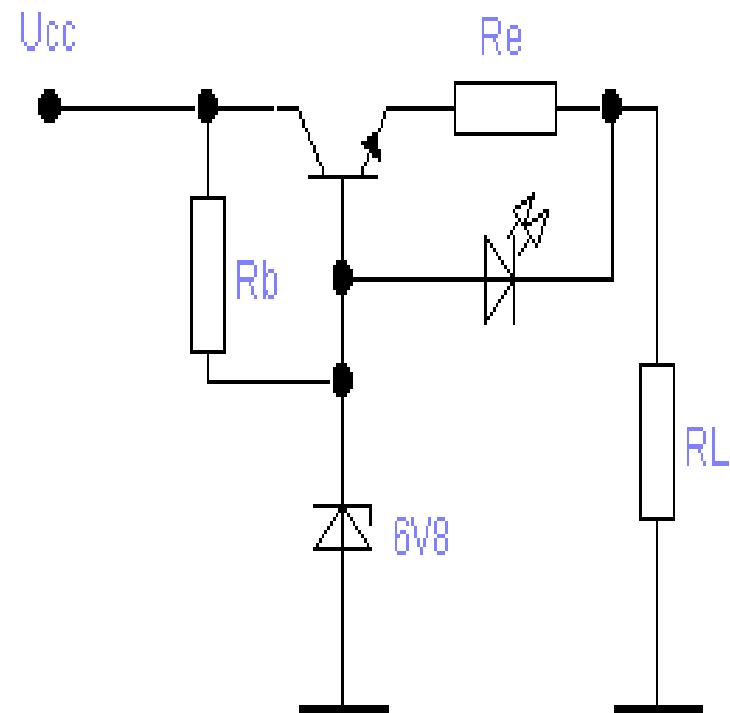
Regulators

- Regulators are needed to make DC voltage smooth enough
- We can build up a regulator by using discrete components or we can use integrated regulators

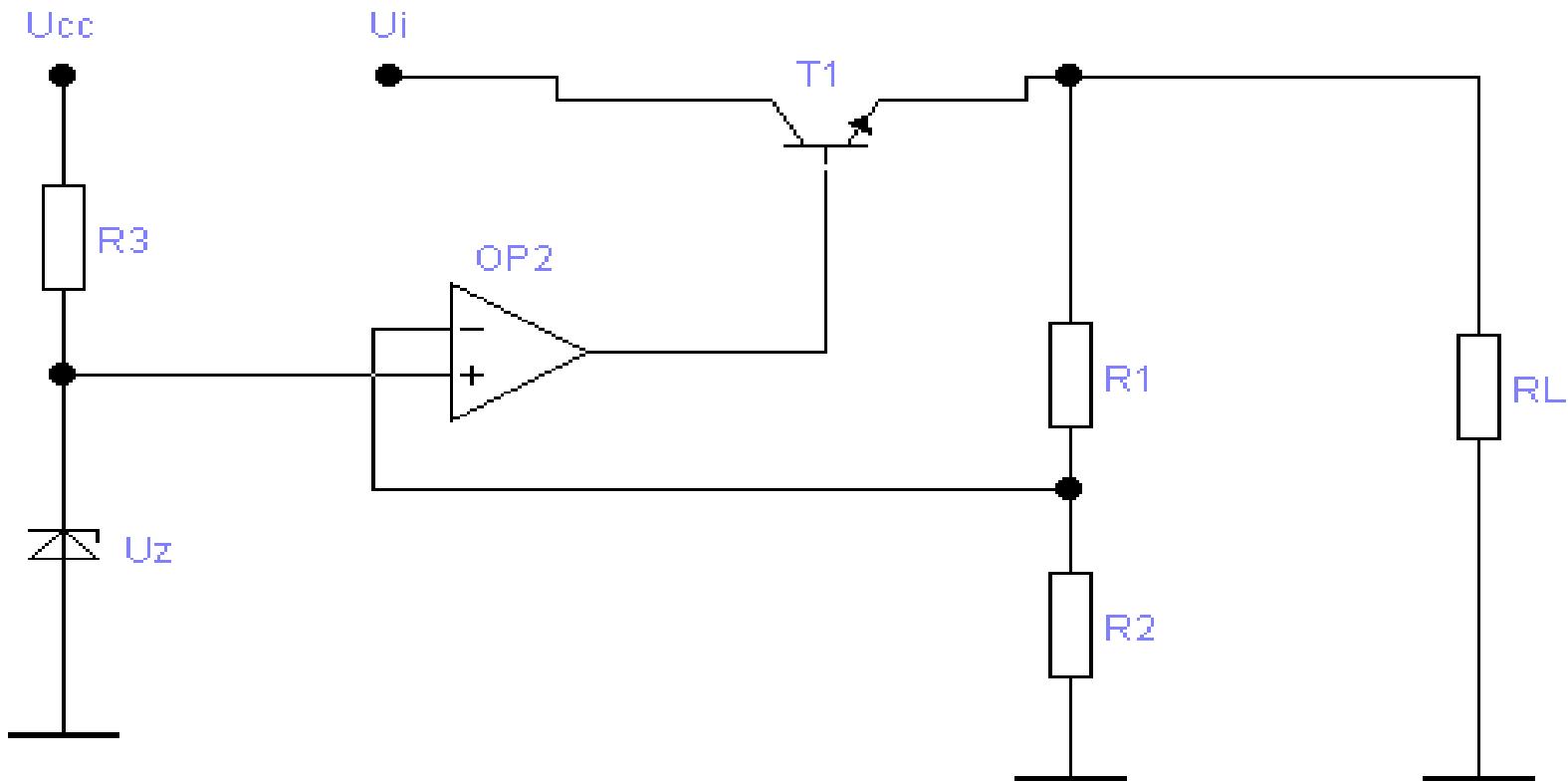


Simple Regulator

- Zener defines the base voltage
- “Constant” drop across BE junction of the transistor sets the voltage across the load resistance
- LED and the emitter resistance together with BE junction form a current delimiter



Discrete Regulators



Integrated Regulators

LM7805, LM7812,...

LM7905, LM7912,..

LM317

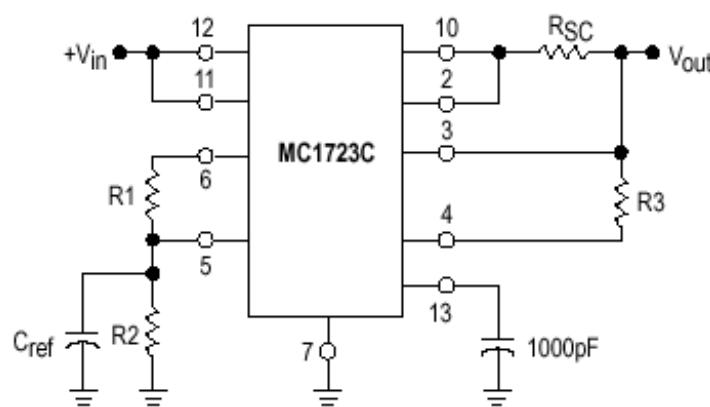
LM337

LM723



Typical 723 applications

Figure 16. Typical Connection for $2 < V_O < 7$

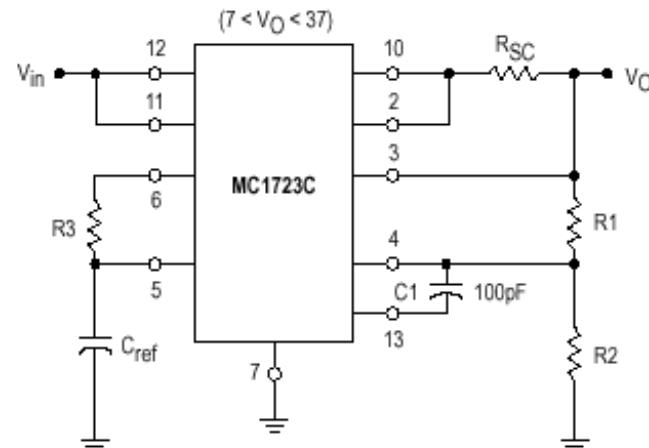


$$V_O = 7 \left[\frac{R_2}{R_1 + R_2} \right] \quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}} \text{ at } T_J = +25^\circ\text{C}$$

For best results $10 \text{ k} < R_1 + R_2 < 100 \text{ k}$

For minimum drift $R_3 = R_1 R_2$

Figure 2. Typical Circuit Connection



$$V_O = 7 \left(\frac{R_1 + R_2}{R_2} \right) \quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}} \text{ at } T_J = +25^\circ\text{C}$$

For best results $10 \text{ k} < R_2 < 100 \text{ k}$

For minimum drift $R_3 = R_1 || R_2$

<http://www.crownhill.co.uk/mlm723.pdf>



Switching Regulators

In the regulators the DC voltage is changed as a AC voltage
and after the level change the voltage is filtered again =>
it's possible to get a better efficiency than in traditional
regulators

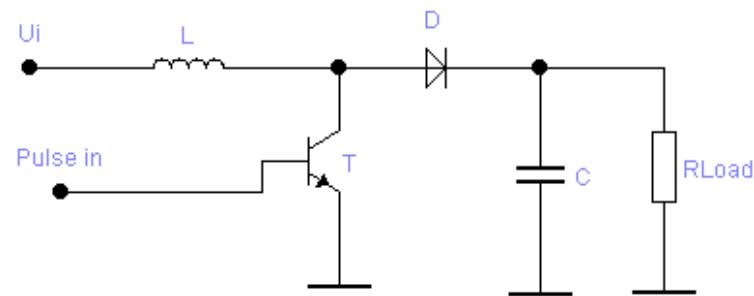
Switching frequencies are usually bout in 100 kHz range

There are also integrated switching regulators available on the
market

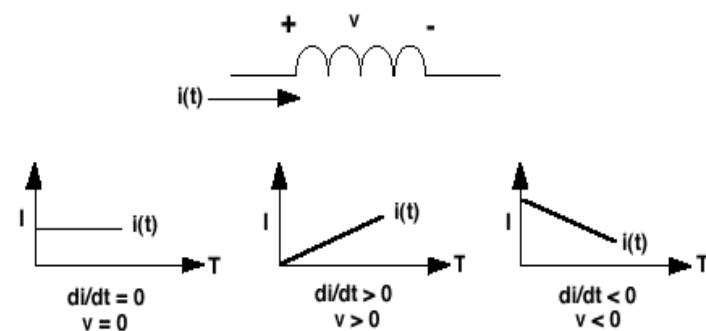


Step-Up Switching Regulator

- During the high pulse transistor T conducts and a voltage increases across the inductor L. Load current is taken from the capacitor C



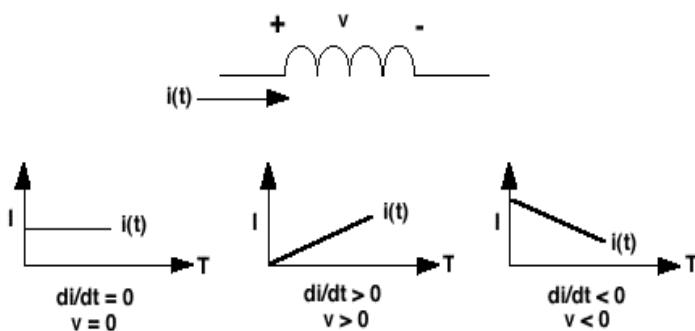
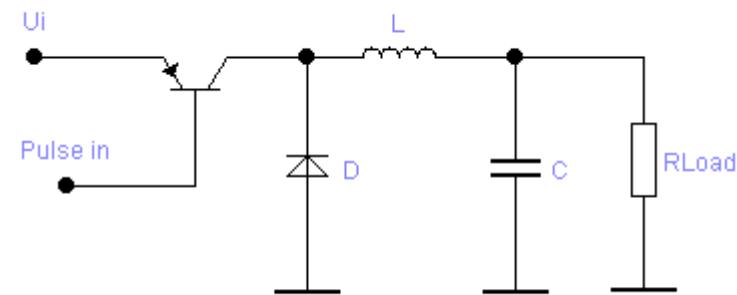
- During the low pulse the energy of the inductor L charges the capacitor C



Step-Down Switching Regulator

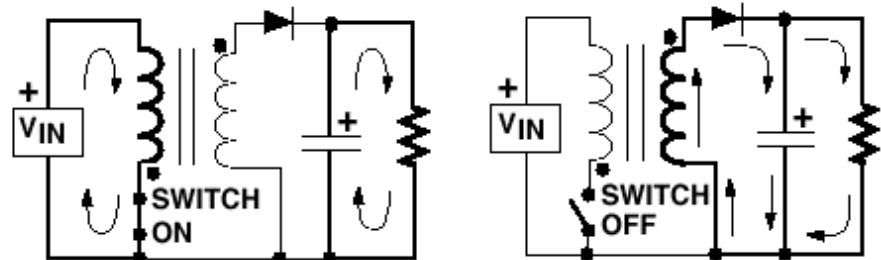
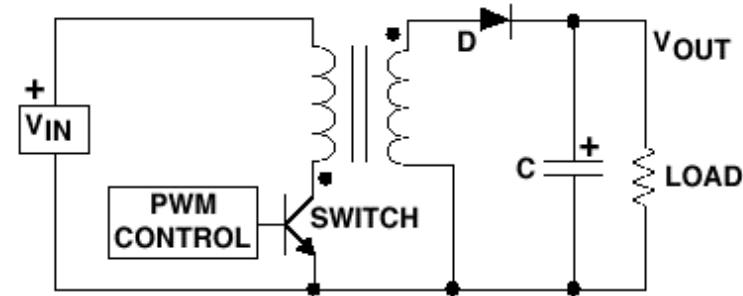
During the low pulse the transistor T conducts and L and C are charged

During the high pulse the diode conducts L gives energy for the discharging of the capacitor C

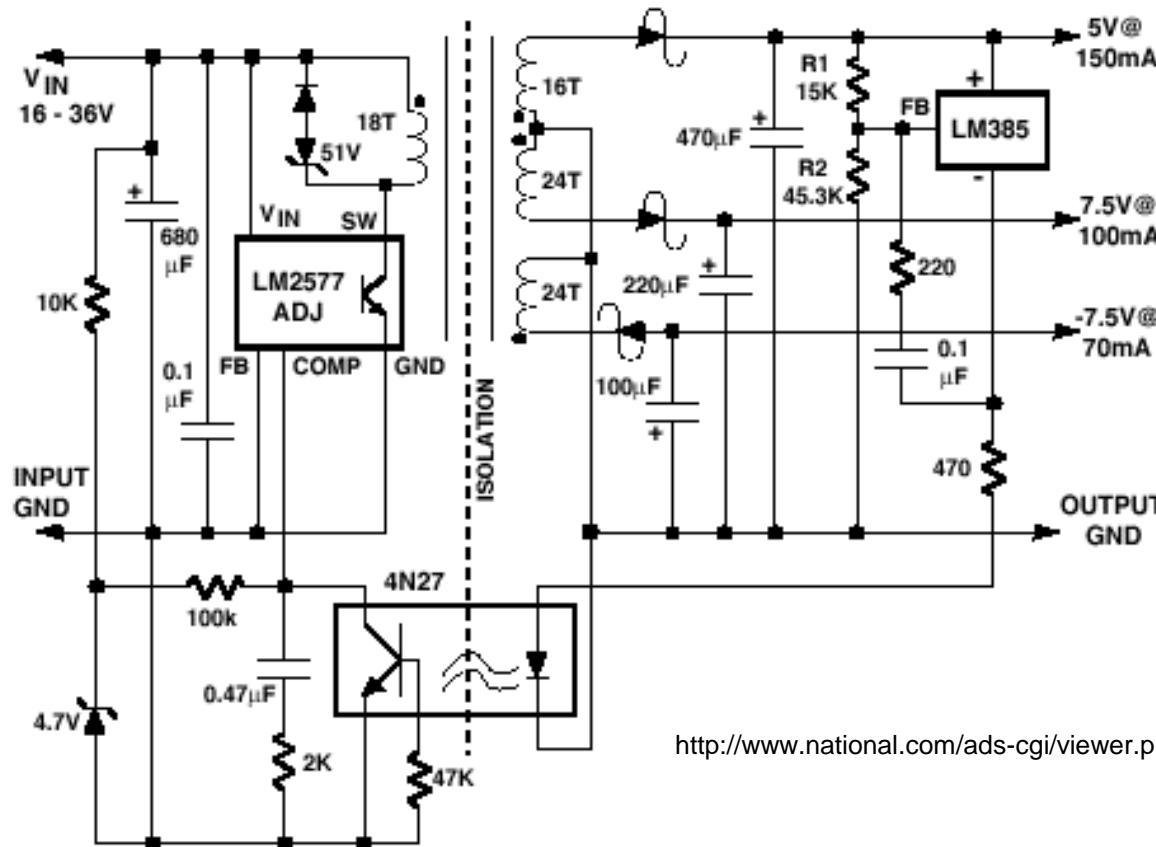


Flyback Regulator

- Most versatile architecture
- Popular in systems where high efficiency and several output voltages are needed
- Used for example in battery-powered systems



Three-output Flyback Regulator



<http://www.national.com/ads-cgi/viewer.pl/appinfo/power/files/f5.pdf>



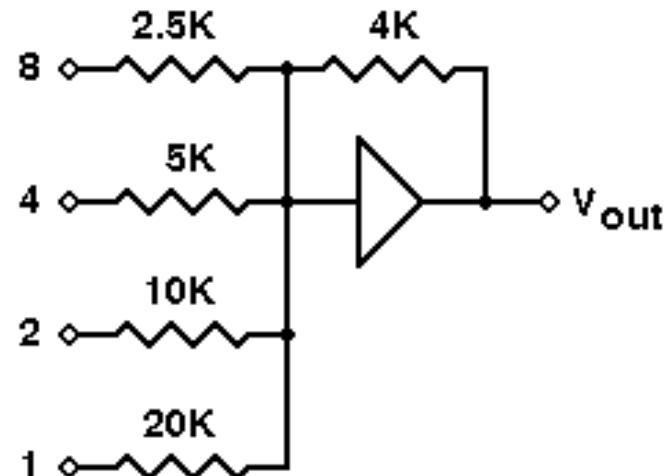
DA and AD Converters

- DA and AD converters are used to change analog responses to digital (and vice versa)
- World is analog, but the things are easier to handle in digital form. That's why converters are key components in several systems
- There are several different converter architectures
- More often converters are integrated as a part of microprocessor



BCD-weighted DA Converter

- Converts the applied BCD number to a matching (inverted) output voltage
- The digits 1, 2, 4, and 8 refer to the relative weights assigned to each input. Thus, 1 is the LSB of the input binary number and 8 is the MSB

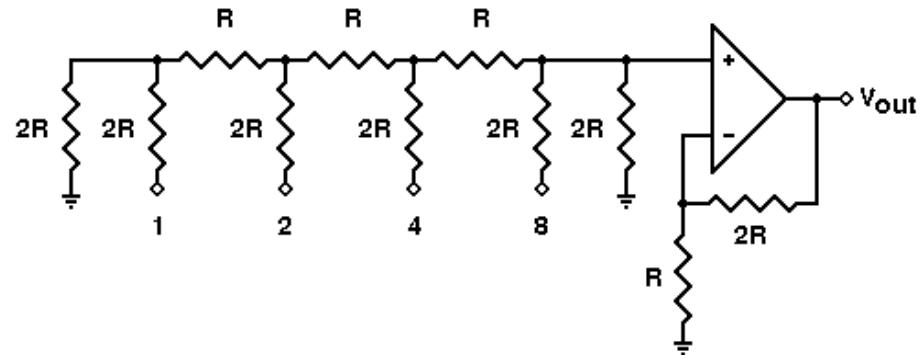


R/2R Ladder in DA Converter

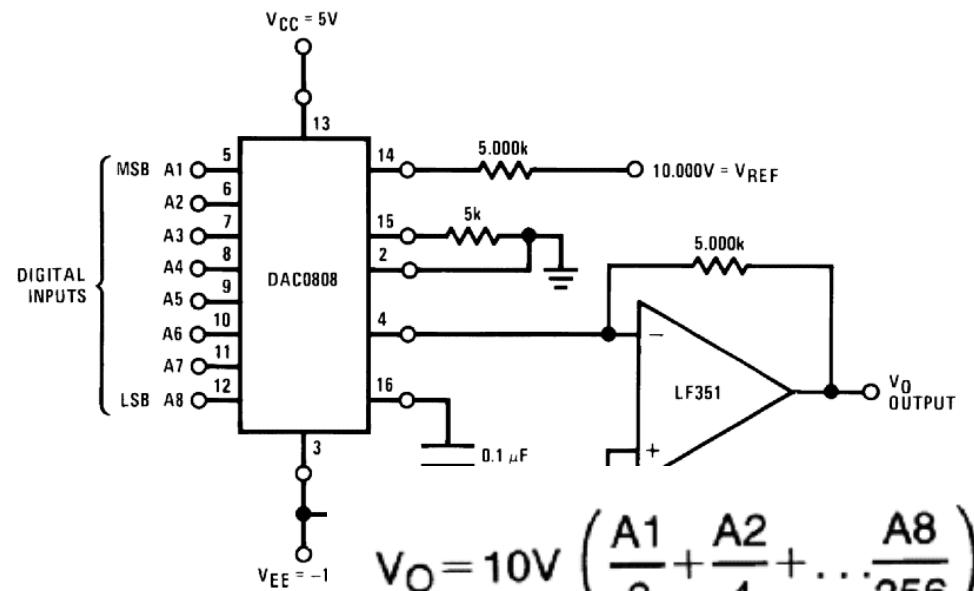
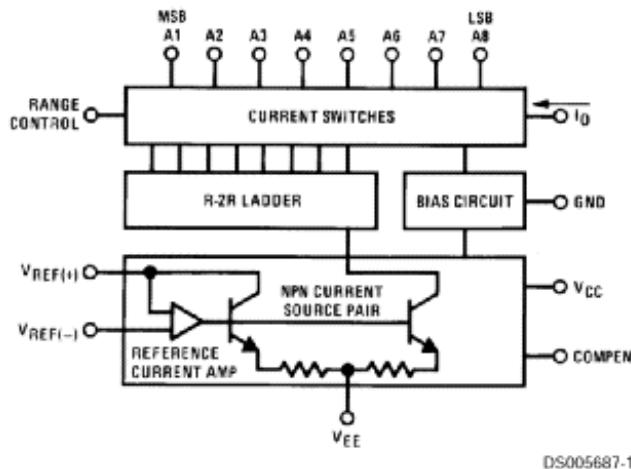
It's rather typical that the inputs (1-8) are driven by CMOS gates

Only two values of precision resistance are needed, in a resistance ratio of 2:1

The MSB is 8 and the LSB is 1

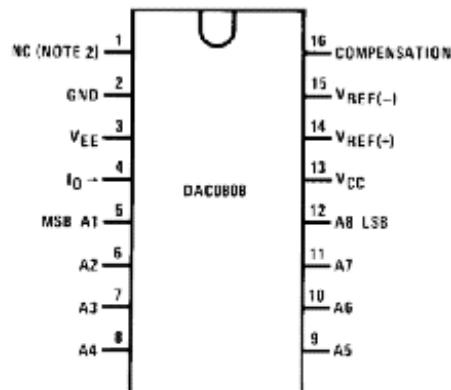


Commercial Example. DAC0808



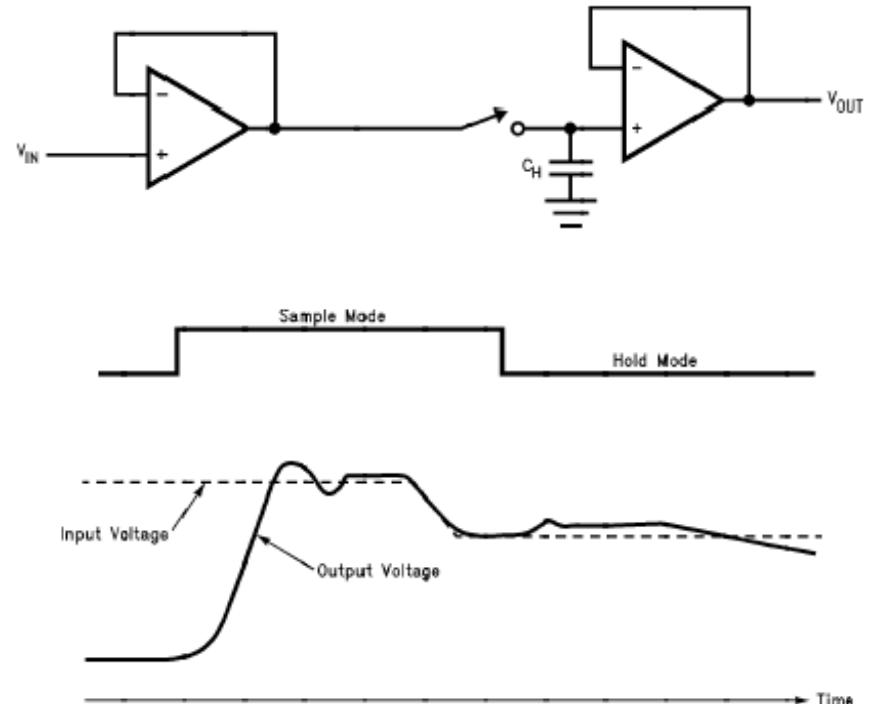
$$V_O = 10V \left(\frac{A_1}{2} + \frac{A_2}{4} + \dots + \frac{A_8}{256} \right)$$

Dual-In-Line Package



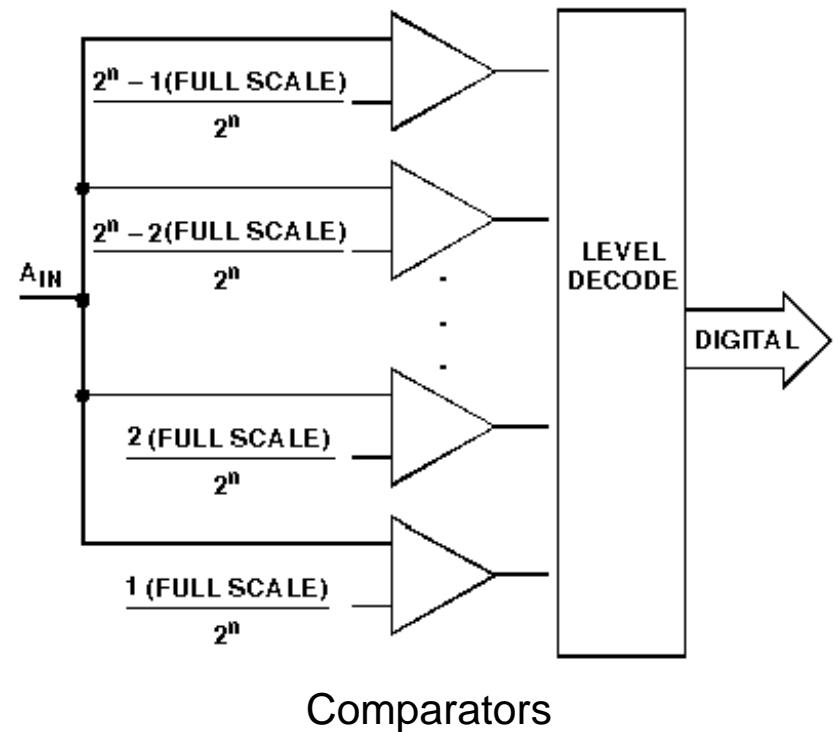
Sample and Hold, a Part of ADC

- During the sample period the capacitor is charged
- During the hold period the capacitor keeps the charged value so that the converter has stable voltage for the conversion



Flash AD Converter

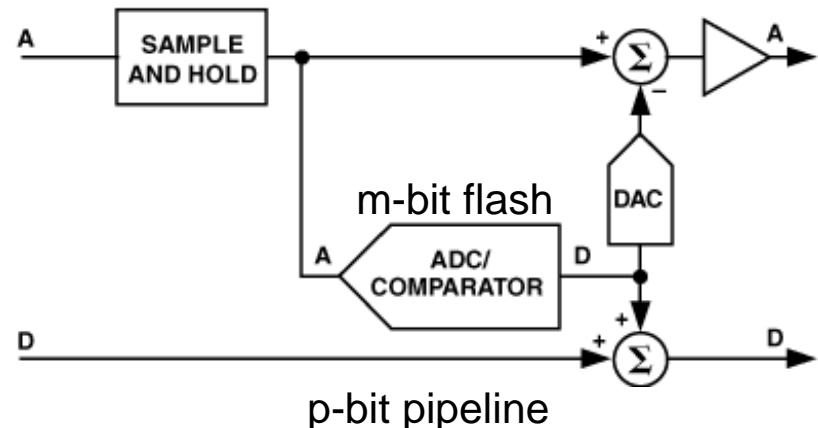
- Flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle
- Requires many comparators
- For example, a 4-bit ADC requires 15 comparators, an 8-bit ADC requires 255 comparators, and a 16-bit ADC would require 65,535 comparators



Comparators

Pipelined Flash Converter

- High-speed ADC with a resolution of $n = p * m$ bits using $p * (2^m - 1)$ comparators
- In practice, however, a few additional bits are generated to provide for error correction
- For example, a 2-stage pipelined converter with (total) 8-bit resolution requires 30 comparators

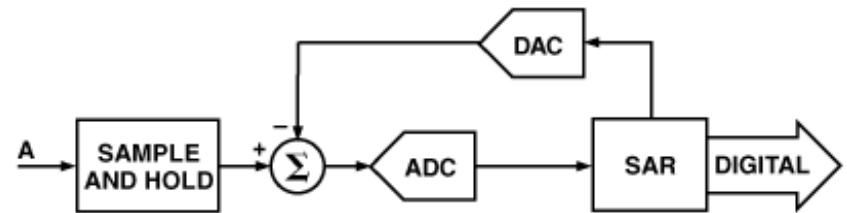


A pipelined converter divides the conversion task into several consecutive stages. First the sample and hold circuit of the first stage acquires the signal. The m -bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an m -bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution.



SAR-based AD converter

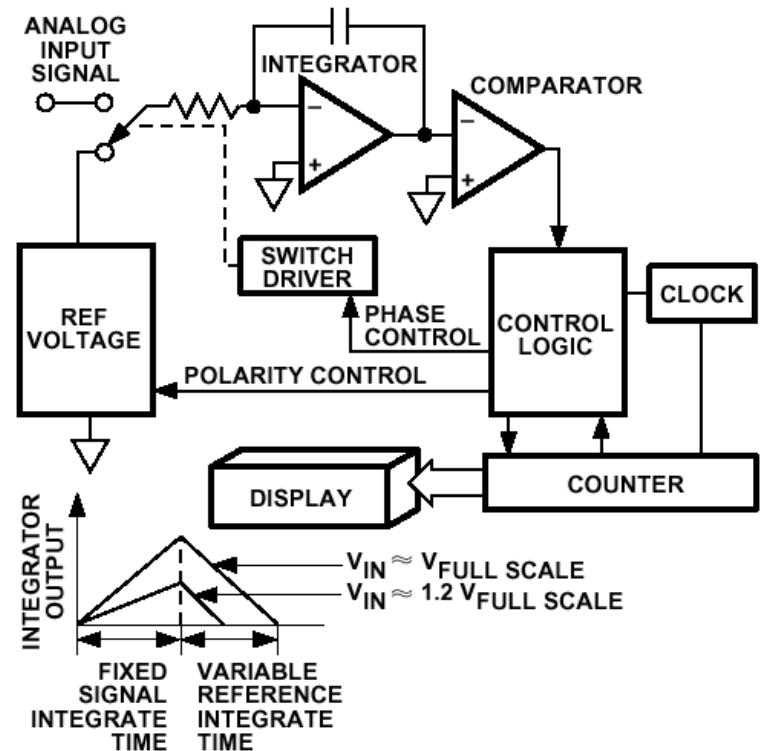
- The SAR converter works like an old-fashioned balance scale
- Requires n comparison cycles to achieve n -bit resolution



This first weight represents the most significant bit (MSB). If the unknown quantity is larger, the $\frac{1}{2}$ -scale weight is retained; if the unknown quantity is smaller, it is removed. This series of steps is repeated n times, using successively smaller weights in binary progression (e.g., $1/4$, $1/8$, $1/16$, $1/32$, ... $1/2^n$ of full scale) until the desired resolution, n , is attained.

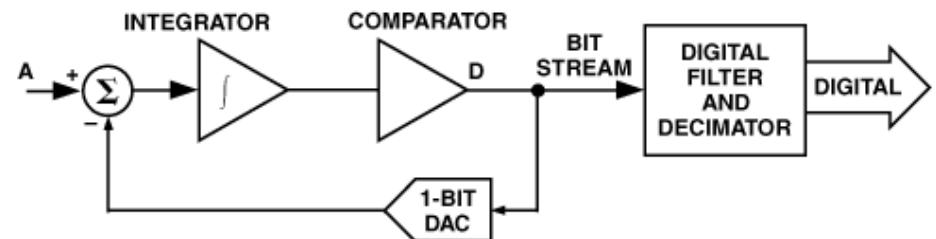
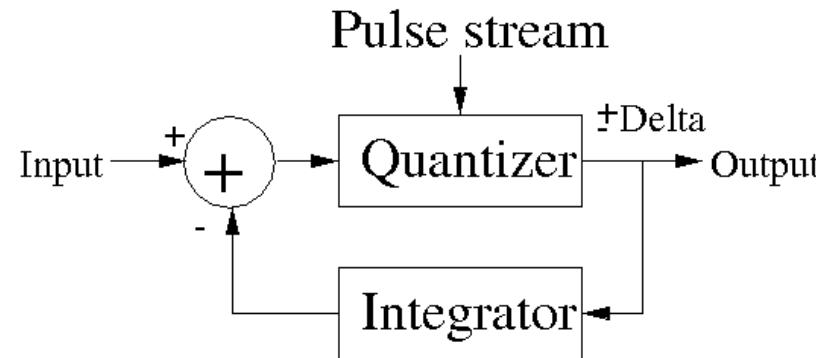
Dual Slope AD Converter

- Input signal is integrated for a fixed time period. After that an opposite polarity constant reference voltage is integrated until output voltage returns to zero. During that time pulses are counted and the output of counter is the conversion result.

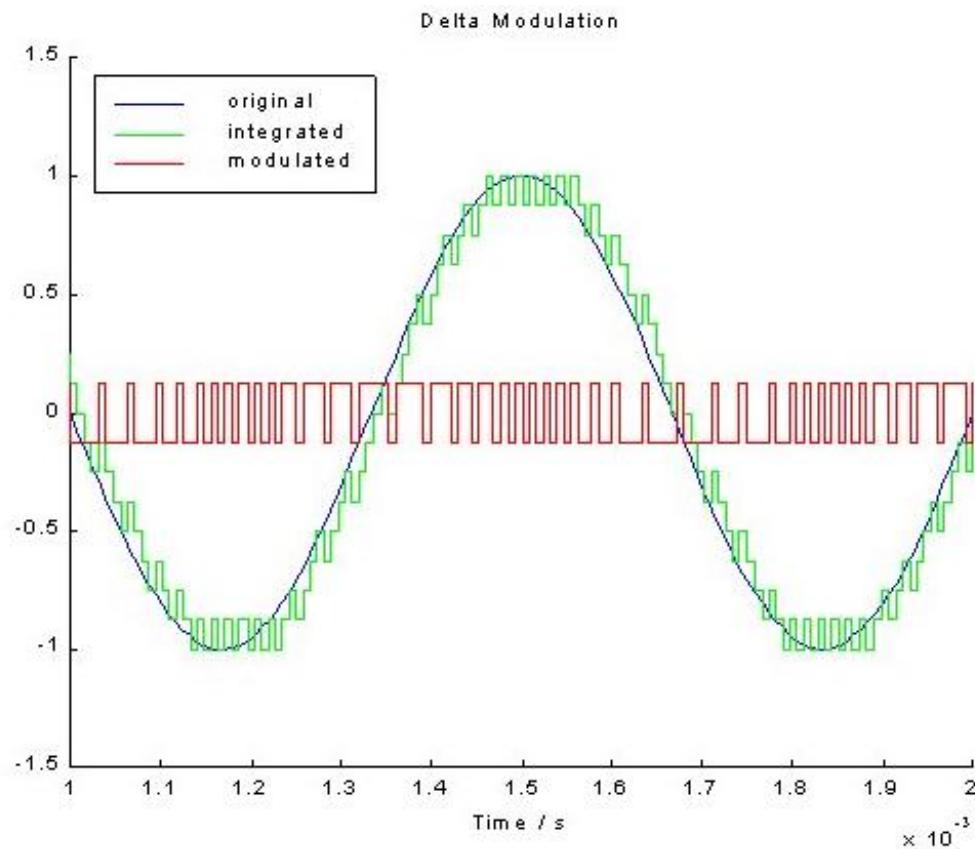


1 Bit Converters

- The input signal is compared to the integrated output pulses and the delta (difference) signal is applied to the quantizer. The quantizer generates a positive pulse when the difference signal is negative, and a negative pulse when the difference signal is positive. This difference signal moves the integrator step by step closer to the present value input, tracking the derivative of the input signal

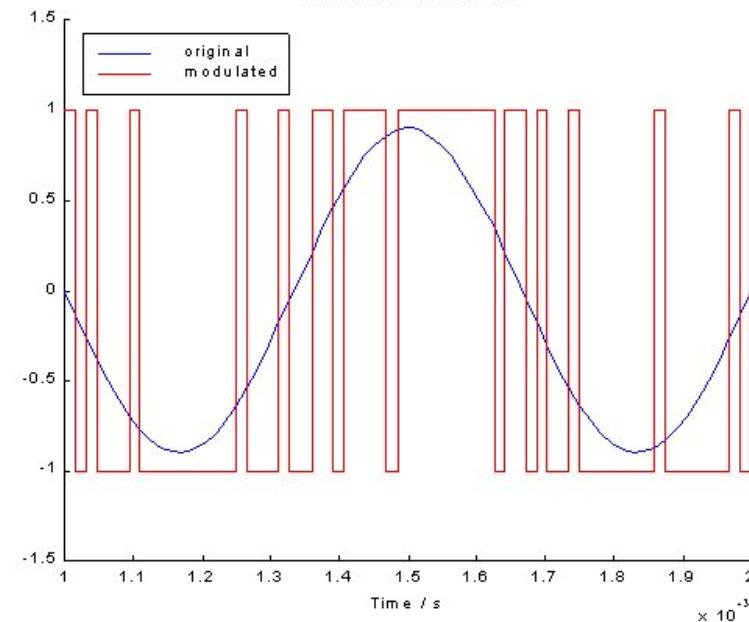
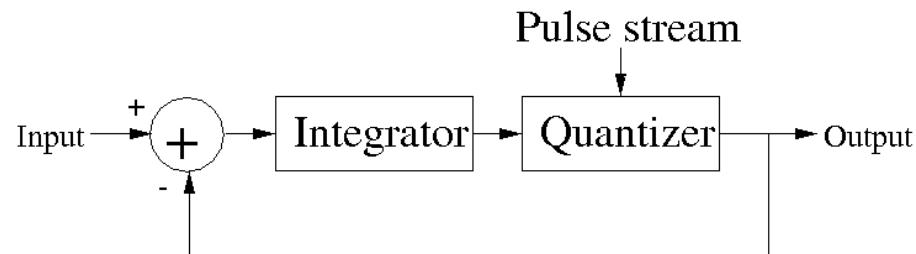


Oversampling and Modulation

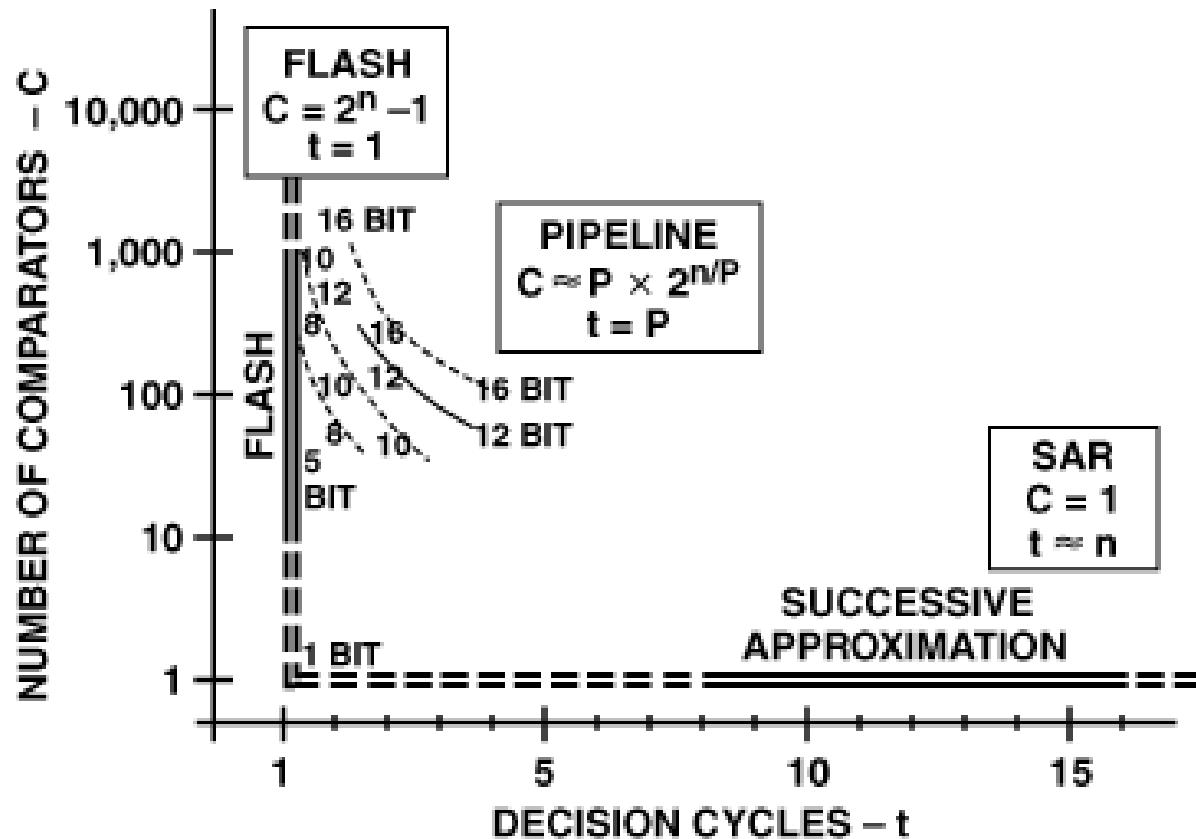


Sigma-Delta Converter

- Sigma-delta systems quantize the delta (difference) between the current signal and the sigma (sum) of the previous difference. An integrator is placed at the input to the quantizer; signal amplitude is constant with increasing frequency; thus SDM is also known as pulse density modulation (PDM).



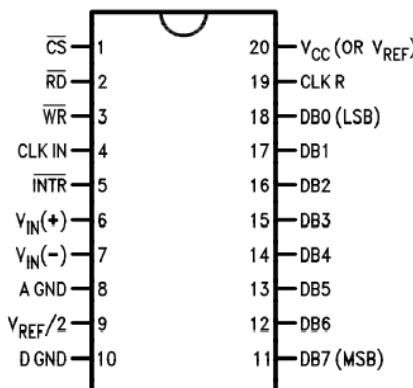
Number of Comparators Versus Clock Cycles



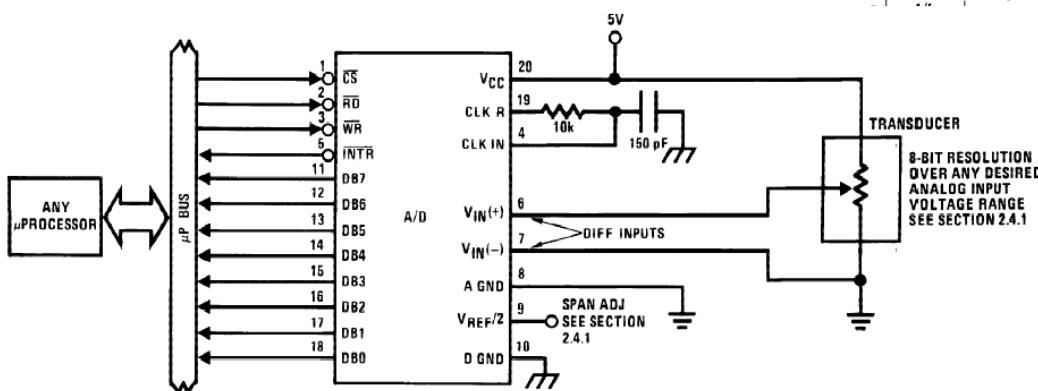
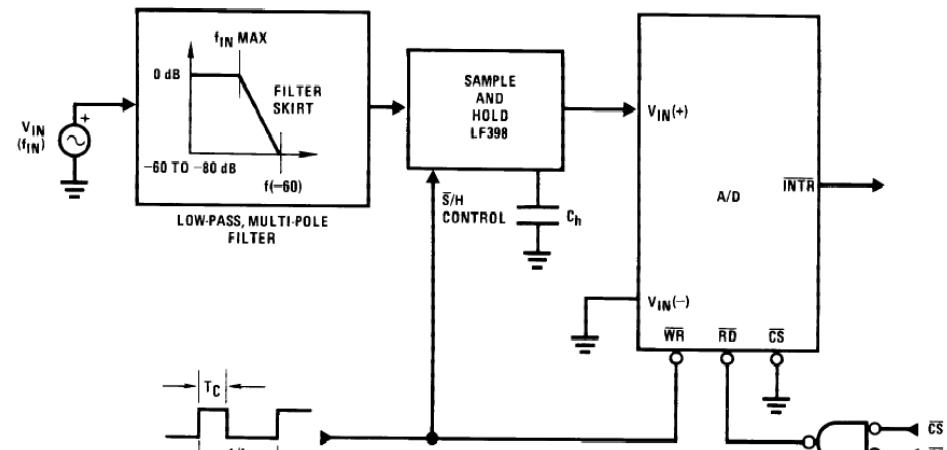
STUDY MATERIAL

Commercial Example, ADC0804

ADC080X
Dual-In-Line and Small Outline (SO) Packages



Sampling an AC Input Signal



<http://www.national.com/ds/AD/ADC0801.pdf>



Oscillators

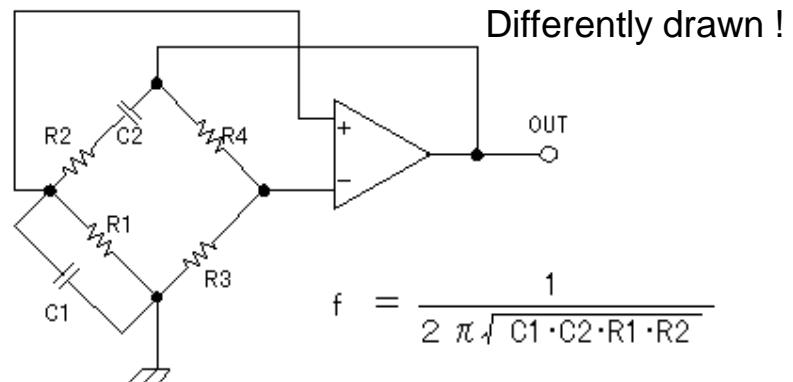
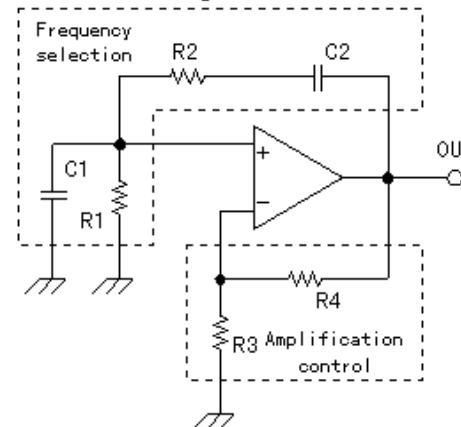
- Oscillator is a circuit that generates repetitive signal (sinusoidal, pulse, triangle, saw tooth,...)
- Important part of electronics (microprocessors, other sequential circuits, phase-locked loops, receivers, transmitters,...)
- Oscillator is so called astable multivibrator



STUDY MATERIAL

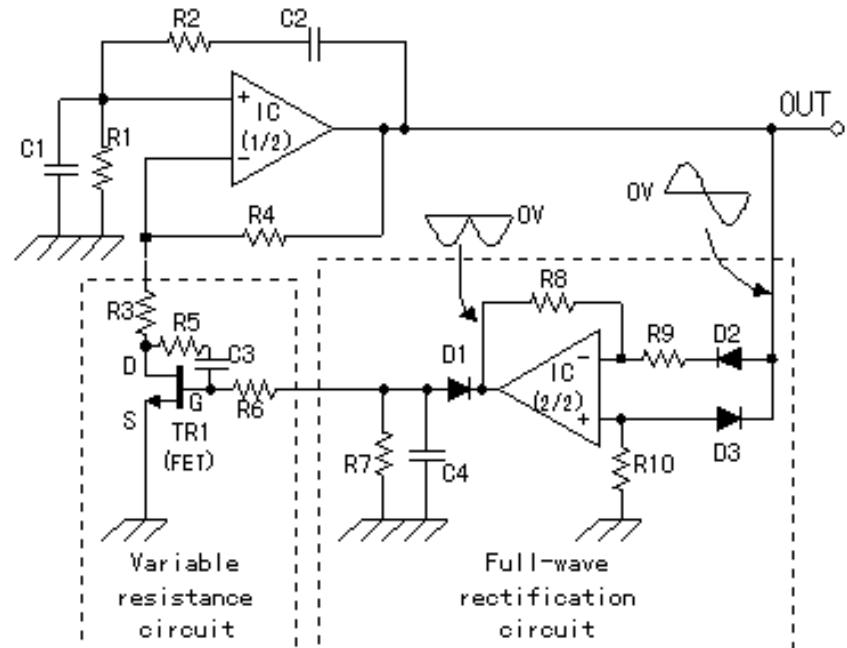
Wien Bridge Oscillator (Sine Wave)

- Oscillation starts when gain (amplification) is 3 (or a little bit more)
- $A_u = (1 + R_4/R_3) = 3$. It means that the condition of $R_4 = 2 \times R_3$ is necessary
- $u_+ = u_0 Z(R_1, C_1) / [Z(R_1, C_1) + Z(R_2, C_2)]$,
 $f = 1/[2\pi RC]$, if $R = R_1 = R_2$ and $C = C_1 = C_2$, and so
 $u_+/u_0 = 1/3$



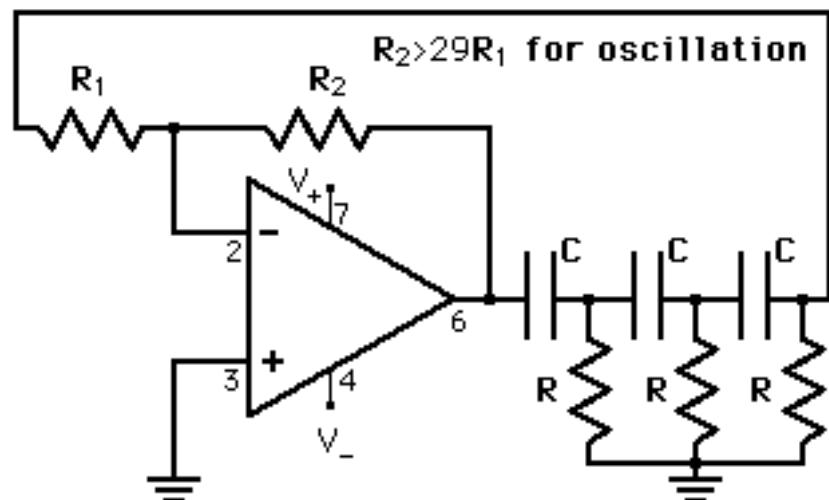
Wien Bridge Oscillator with Amplitude Control

- The negative voltage which is gained by the gate of TR1 becomes high when the output signal of IC(1/2) increases. Then, the resistance value between the drain and the source of TR1, too, increases. The gain of IC(1/2) falls when the resistance value of $(R_3 + R_{TR1})$ becomes high.
- R5 and C3 improve the frequency characteristic of TR1



Phase-Shift Oscillator

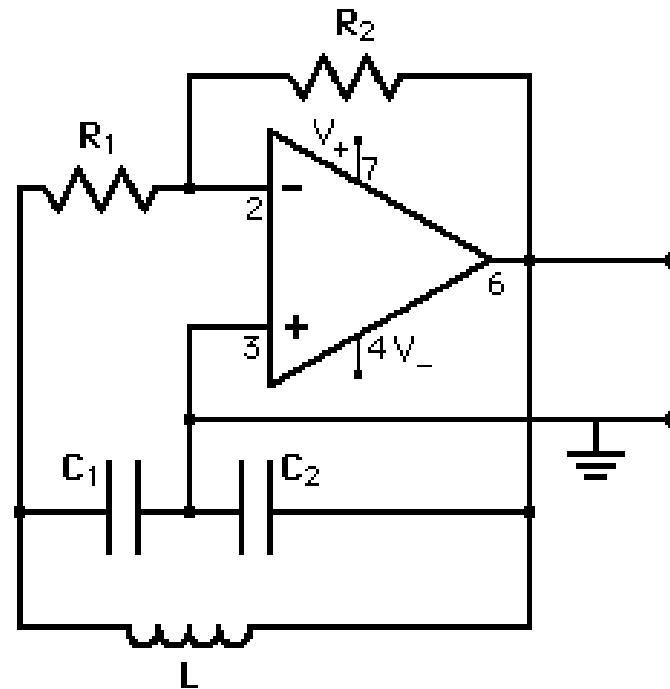
- The phase shift oscillator produces positive feedback by using an inverting amplifier and adding another 180° of phase shift with the three high-pass filter circuits. It produces this 180° phase shift for only one frequency at which the feedback fraction $B=1/29$.



$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{6}RC}$$

Colpitts Oscillator

- The Colpitts oscillator achieves positive feedback by using an inverting amplifier plus the 180° phase shift across a parallel resonant circuit.



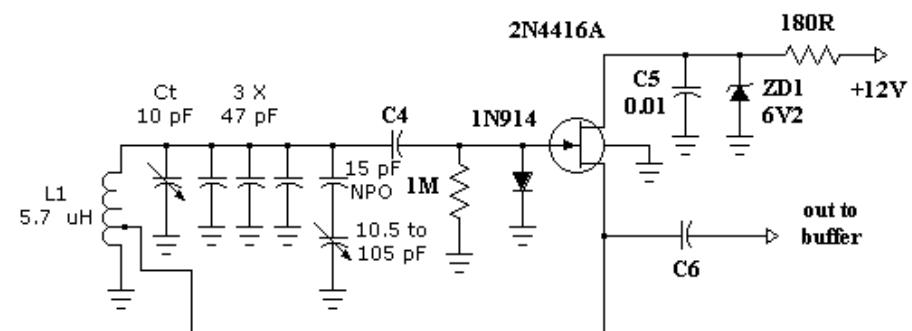
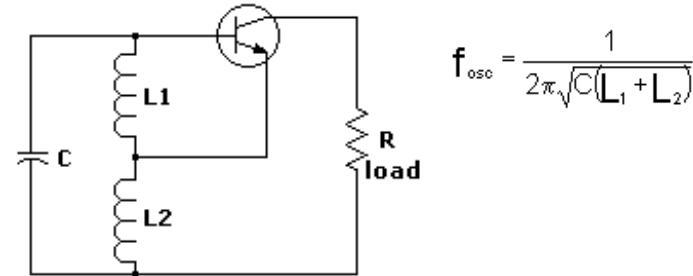
$$\omega_0 = \frac{1}{\sqrt{\frac{LC_1C_2}{C_1 + C_2}}}$$

$$C_{eq} = \frac{C_1C_2}{C_1 + C_2}$$



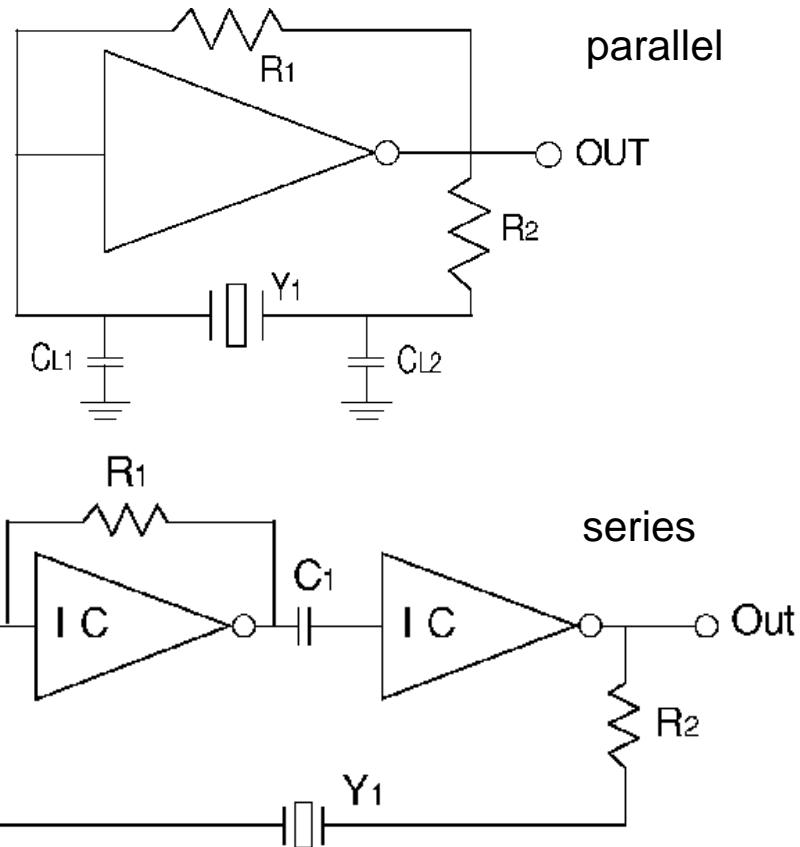
Hartley Oscillator

- The Hartley oscillator achieves positive feedback by using an inverting amplifier plus the 180° phase shift across a parallel resonant circuit



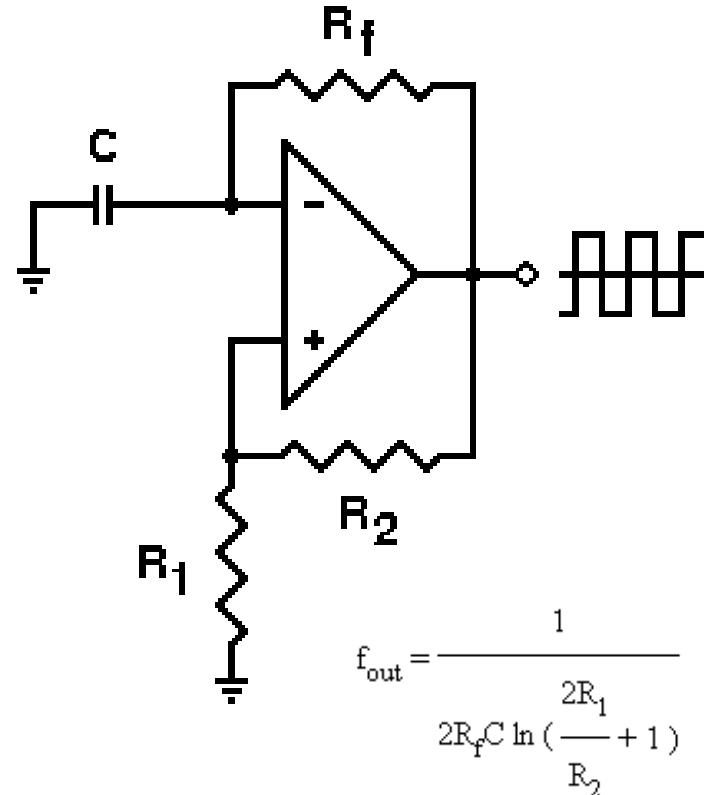
Crystal Oscillator

- A parallel resonant oscillator circuit uses a crystal unit which is designed to operate with a specified value of load capacitance. This will result in a crystal frequency which is higher than the series resonant frequency
- A series resonant oscillator circuit uses a crystal which is designed to operate at its natural series resonant frequency. In such a circuit, there will be no capacitors in the feedback loop



OPAMP-based Square-Wave Generator

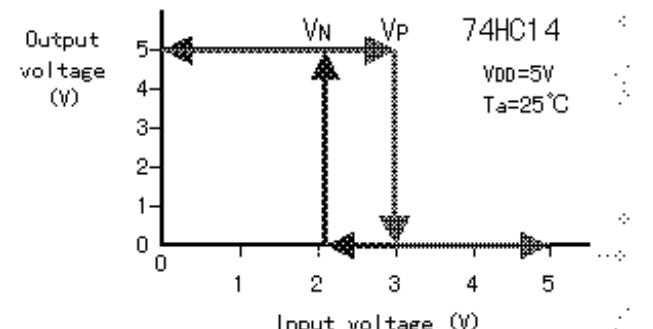
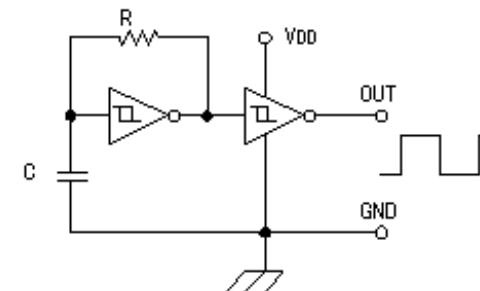
- We assume it starts at $-U_{cc}$ volts, then the voltage at the "+" input will be set equal to $-U_{cc}R_1/(R_1 + R_2)$. This then becomes the reference voltage and the output will remain unchanged until the "-" input becomes more negative than this value. C is gradually charging towards $-U_{cc}$ through resistor R_f . Since C is charging towards $-U_{cc}$, but the reference voltage at the "+" input is necessarily smaller than $-U_{cc}$ limit, eventually the capacitor will charge to a voltage that exceeds the reference voltage. When that happens, the circuit will immediately change state.



STUDY MATERIAL

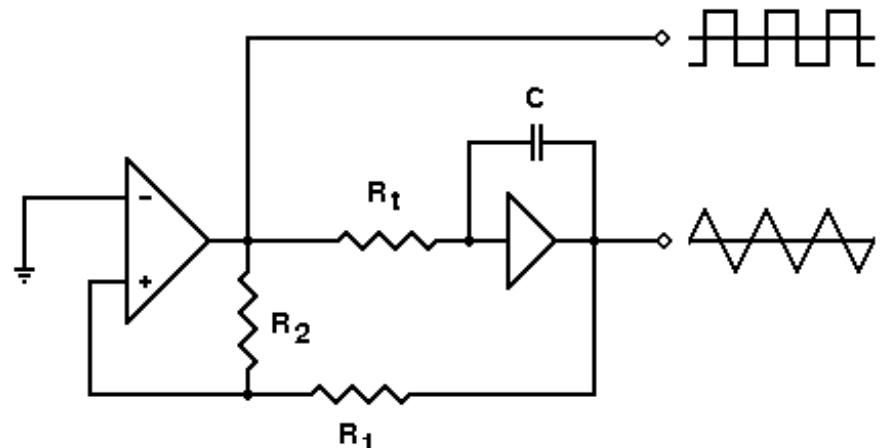
Pulse Oscillator Based on Logic Gate

- The capacitor is charged and discharged via the resistor R.
- The hysteresis voltage defines the estimate formula for the frequency together with resistor and capacitance values
- Estimate of frequency $f=1/RC$
- R should be less than 5k



Triangle Wave Generator

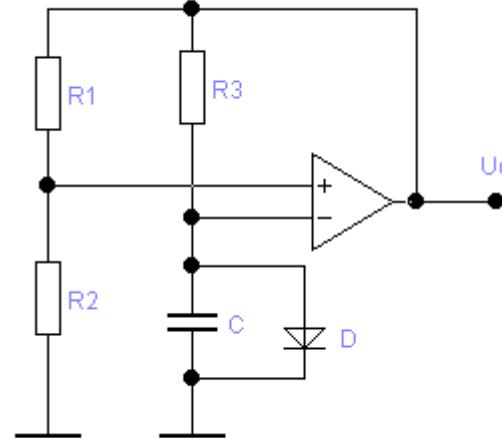
- In the circuit to the right, we use a separate integrator to generate a ramp voltage from the generated square wave. As a result, we can get both waveforms from a single circuit.
- Integrator inverts as well as integrating, so it will produce a negative-going ramp for a positive input voltage



$$f_{\text{out}} = \frac{1}{4R_tC} \left(\frac{R_2}{R_1} \right)$$

Monostable circuit

- Let's assume that U_o is U_{cc} . C starts charge but diode limits the “-” terminal voltage (u_-).
- R_1 and R_2 set “+” terminal voltage (u_+)
- If the circuit is designed so that $u_+ > u_-$ the output stays U_{cc} . After that if set short negative pulse in the (+) terminal, we will see longer negative pulse at the output terminal



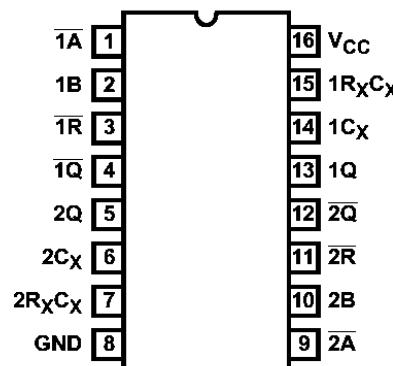
STUDY MATERIAL

Commercial Monostable Circuit

CD74HC123, CD74HCT123, CD74HC423, CD74HCT423

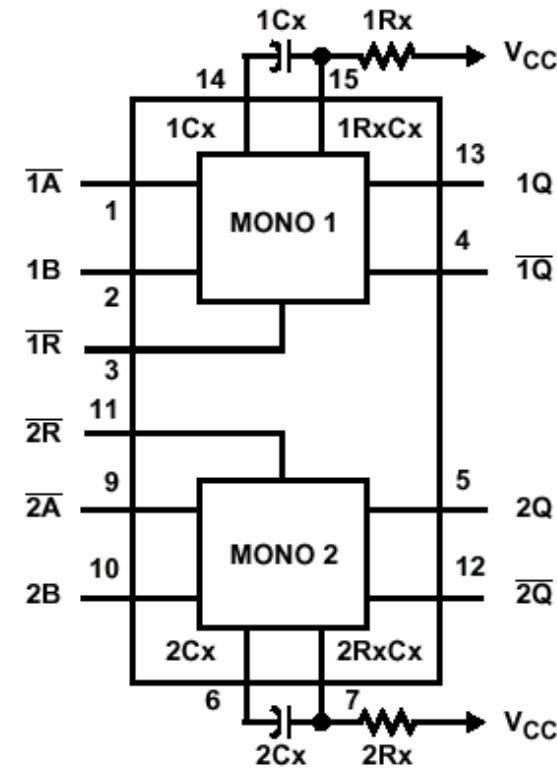
(PDIP, SOIC)

TOP VIEW



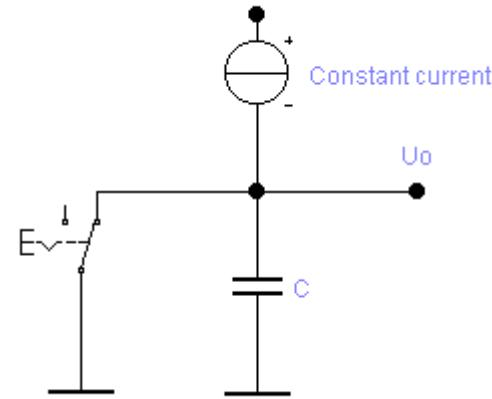
TRUTH TABLE

INPUTS			OUTPUTS	
\bar{A}	B	\bar{R}	Q	\bar{Q}
CD74HC/HCT123				
H	X	H	L	H
X	L	H	L	H
L	\uparrow	H	$\uparrow\!\!\!\downarrow$	$\uparrow\!\!\!\downarrow$
\downarrow	H	H	$\uparrow\!\!\!\downarrow$	$\uparrow\!\!\!\downarrow$
X	X	L	L	H
L	H	\uparrow	$\uparrow\!\!\!\downarrow$	$\uparrow\!\!\!\downarrow$



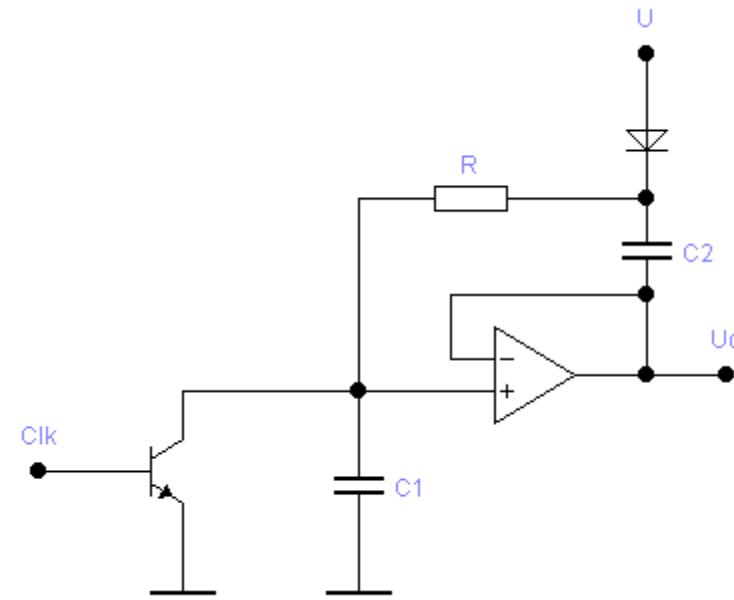
Principle of Ramp Signal Generation

- Clock controls the switch.
- Switch controls the charging of the capacitor
- When the switch is closed C is discharged. ($U_o=0$)
- When the switch is open C is charged with constant current and ramp voltage can be seen at the output



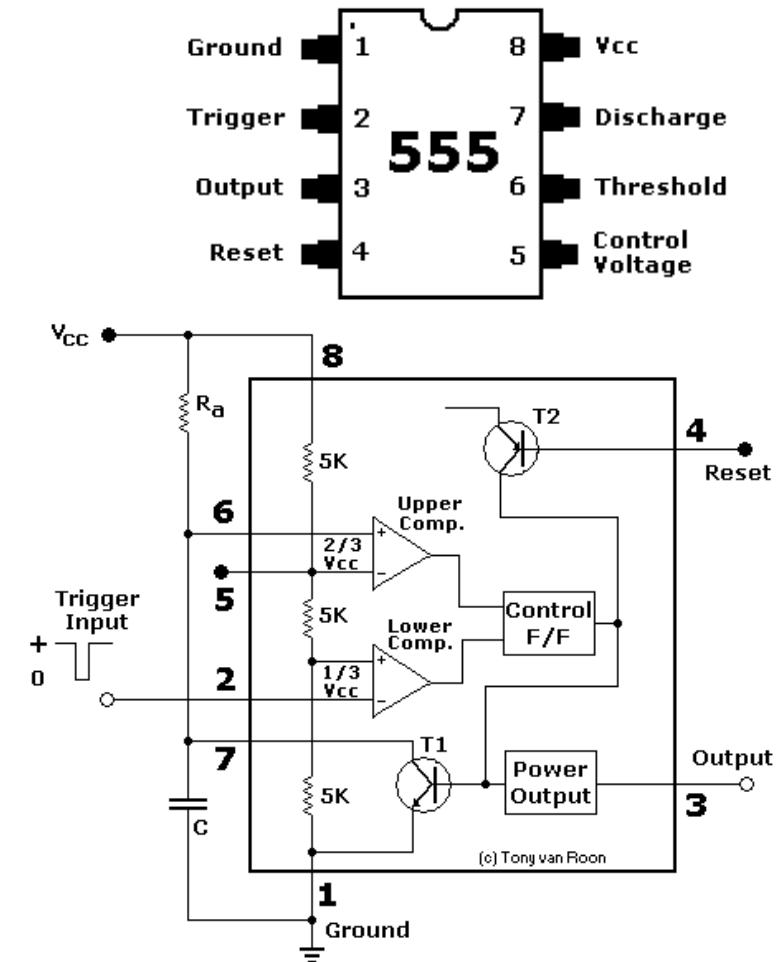
Simple Sweep Circuit

- Transistor acts as a switch that controls the charging of capacitor
- C2 is charged via diode
- Because $u_+ = u_-$, it means that voltage across R (and C2) is constant ($C_2 \gg C_1$)
- Constant current charges C1 and ramp pulse is generated



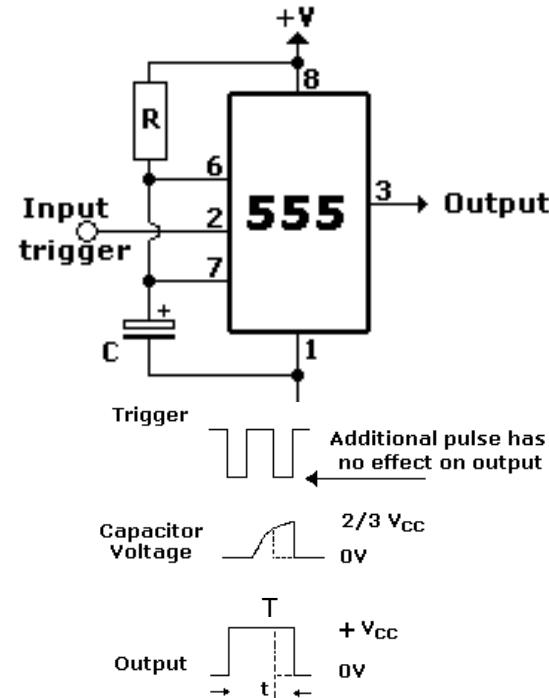
555 Timer Circuit

- 5k resistances form a fixed voltage division from the supply
- Comparators can be used for setting the reference levels in different applications (pin 6 and 2)



555 As a Monostable

- When a negative-going trigger pulse is applied to the trigger input, the threshold on the lower comparator is exceeded. The lower comparator, therefore, sets the flip-flop
- As soon as the charge on the capacitor equal 2/3 of the supply voltage, the upper comparator triggers and resets the control flip-flop

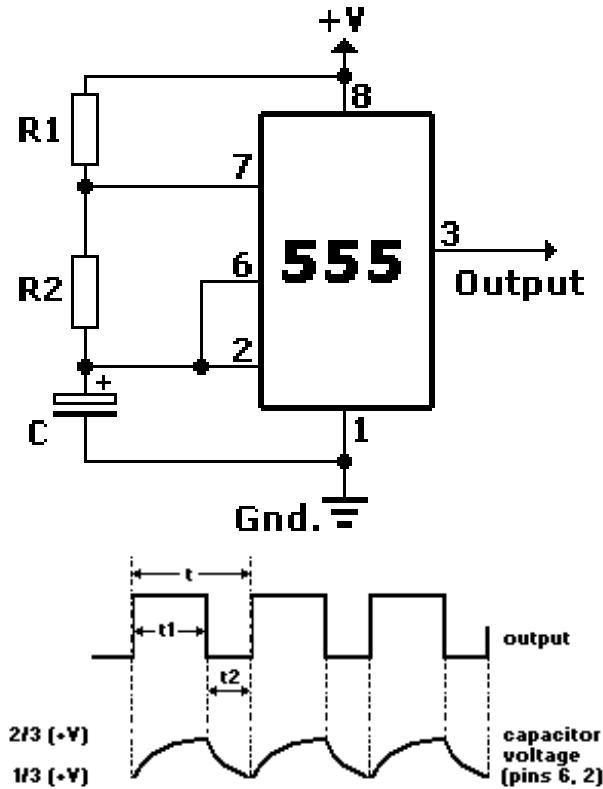


$$T = 1.1 \times R \times C$$



555 As an Oscillator

- The capacitor charges toward the supply voltage through the two resistors, R1 and R2.
- As the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset
- Discharging starts until 1/3 supply voltage reached
- Again charging and so on



$$t_1 = .693(R_1+R_2)C$$

$$t_2 = .693 \times R_2 \times C$$



Logic Families

- Bipolar: S, LS, AS, ALS, F, ECL
- CMOS: 4000, HC, AC, AHC
- Combined: BiCMOS



Markings of Logic Gates

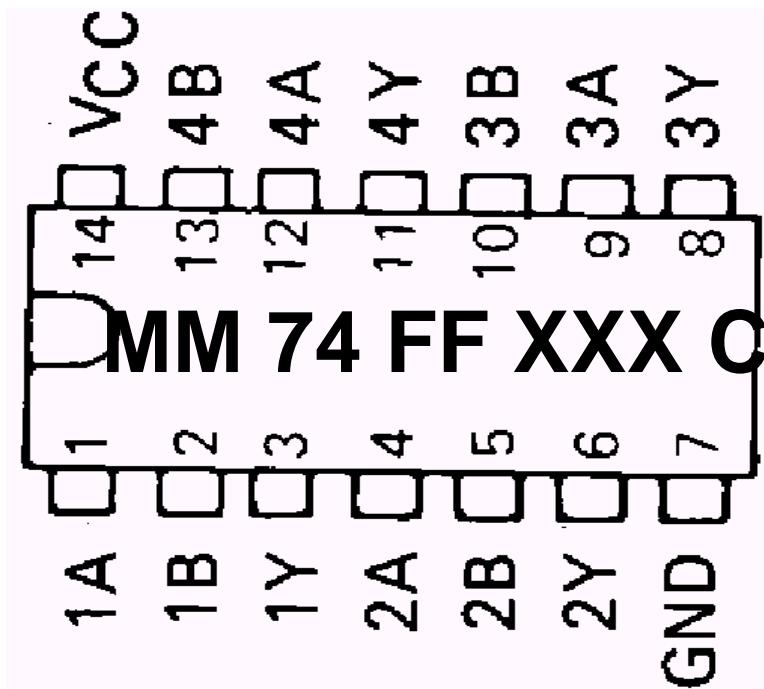
MM=Manufacturer, **SN**=Texas Instruments,...

74 or **54**, 74=commercial, 54=military

FF=Family, **HC**=High-Speed CMOS,
LS=Low-power Schottky, **LV**=Low Voltage,...

XXX=Circuit type, **00**=NAND,
138=Decoder (3/8),...

C=Capsule, **N**=DIL, **D**=SOIC,...



Key Parameters

U_{OH} , Voltage Output High

U_{OL} , Voltage Output Low

U_{IH} , Voltage Input High

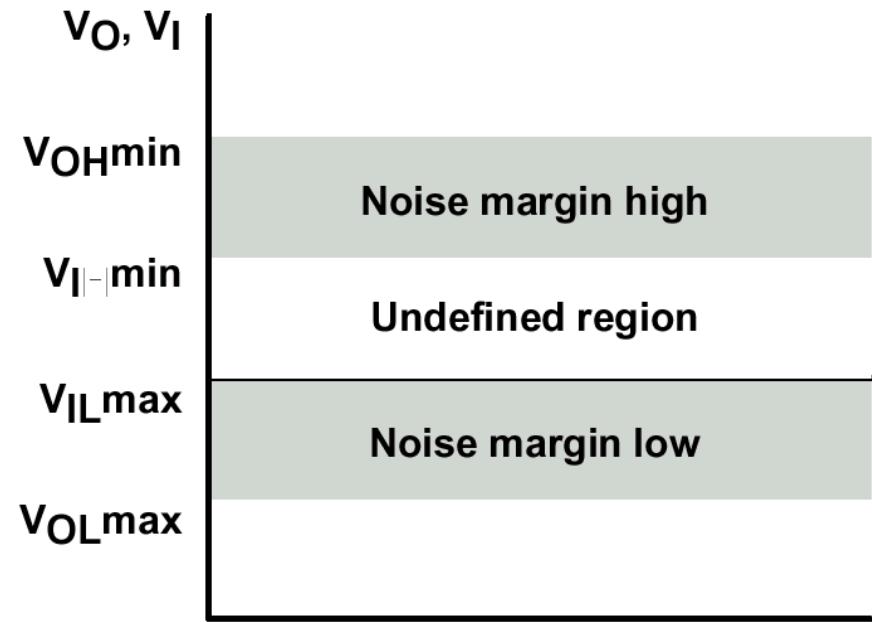
U_{IL} , Voltage Input Low

I_{OH} , Current Output High

I_{OL} , Current Output Low

I_{IH} , Current Input High

I_{IL} , Current Input Low



Noise Margin

Key Parameters of Some Logic Families

Parameter	LS	HC	ABT	Unit
VOH (min)	2.4	4.5	2.5	V
VOL (max)	0.4	0.5	0.5	V
VIH (min)	2	3.5	2	V
VIL(max)	0.8	1.5	0.8	V
IOH(max)	0.4	25.0	15	mA
IOL(max)	16	25.0	20	mA
IIH(max)	40	1	1	µA
IIL(max)	1600	1	1	µA



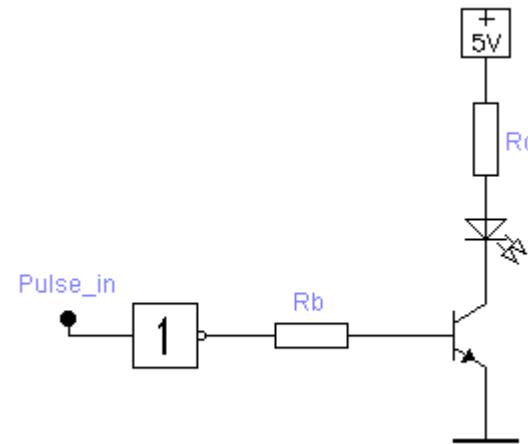
Comparison of Logic Families

Typical Commercial Parameter (0°C to +70°C)	Logic Families												
	TTL				CMOS					ECL			
	LS	ALS	ABT	FAST	MG	HC	FACT	LVC	LCX	10H	100K	ECL in PS(3)	E-Lite
Speed													
Gate Prop Delay (ns)	9	7	2.7	3	65	8	5	3.3	3.5	1	0.75	0.33	0.22
Flip-Flop Toggle Rate (MHz)	33	45	200	125	4	45	160	200	200	330	400	1,000	2800
Output Edge Rate (ns)	6	3	3	2	50	4	2	3.7	3.6	1	0.7	0.5	0.25
Power Consumption Per Gate (mW)													
Quiescent	5	1.2	0.005	12.5	0.0006	0.003	0.0001	0.003	1E-04	25	50	25	73
Operating (1 MHz)	5	1.2	1.0	12.5	0.04	0.6	0.6	0.8	0.3	25	50	25	73
Supply Voltage (V)	+4.5 to +5.5	+4.5 to +5.5	+4.5 to +5.5	+4.5 to +5.5	+3 to +18	+2 to +6	+1.2 to +3.6	+2 to +3.6	+2 to +6	-4.5 to -5.5	-4.2 to -4.8	-4.2 to -5.5	-4.2 to -5.5
Output Drive (mA)	8	8	32/64	20	1	4	24	24	24	50 ohm load	50 ohm load	50 ohm load	50 ohm load



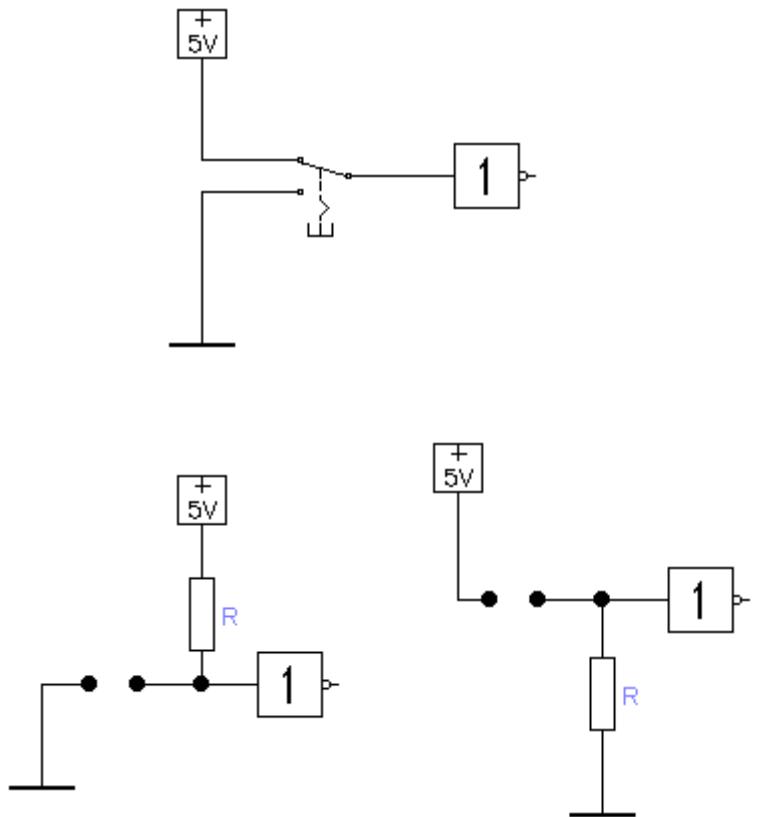
Parameters, a Part of Design

- R_c limits the pulse current
- R_b limits the base current
- Minimum value for R_b results from the maximum loading of the gate.
Maximum value for R_b results from the fact that transistor must be saturated all possible current values of the transistor



Switch Interfacing

- If a switch has only two connections or if are using a jumper for setting the state pull-up or pull-down resistance is needed.



Fanout

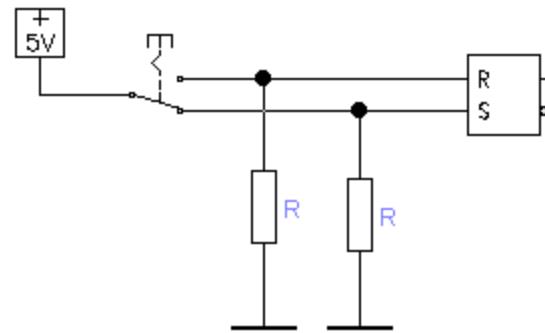
- Fanout describes gates capability to drive other similar (or different) gates

Case	Low-state		High-state		Overall
	Ratio	Fanout	Ratio	Fanout	Fanout
74LS driving 74LS	$\frac{8\text{mA}}{0.4\text{mA}}$	20	$\frac{400\mu\text{A}}{20\mu\text{A}}$	20	20
74LS driving 74S	$\frac{8\text{mA}}{2\text{mA}}$	4	$\frac{400\mu\text{A}}{50\mu\text{A}}$	8	4



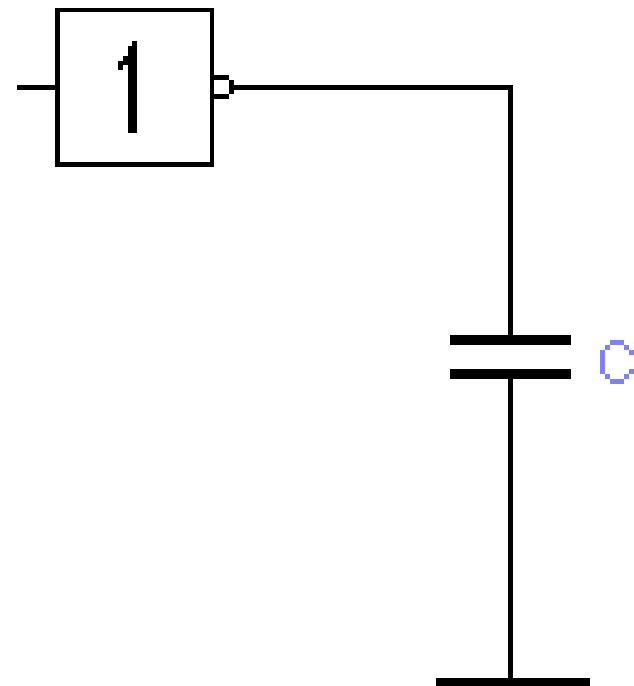
Contact Bouncing

- In some cases the contact bounce of switches can cause unwanted effects in the system. For example a RS flip-flop can be applied the elimination of contact bouncing



Capacitive Loads

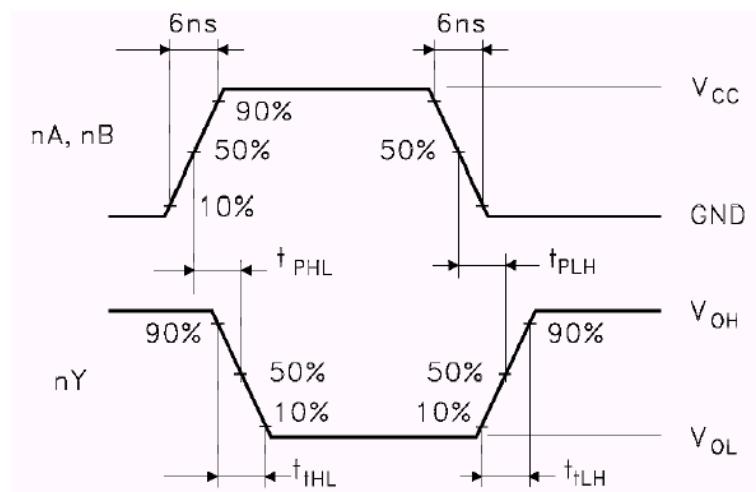
- The speed of the circuit depends mainly on the technology
- Usually fast technology needs more power
- Capacitive loads increase rising and falling times of signal



STUDY MATERIAL

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH} t_{THL}$	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{PLH} t_{PHL}$	Propagation Delay Time	2.0			27	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	



Some LS00 Time Parameters

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 280 \Omega$, $C_L = 15 \text{ pF}$	3	4.5	ns	
t_{PHL}				3	5	ns	
t_{PLH}		Y	$R_L = 280 \Omega$, $C_L = 50 \text{ pF}$	4.5		ns	
t_{PHL}				5		ns	

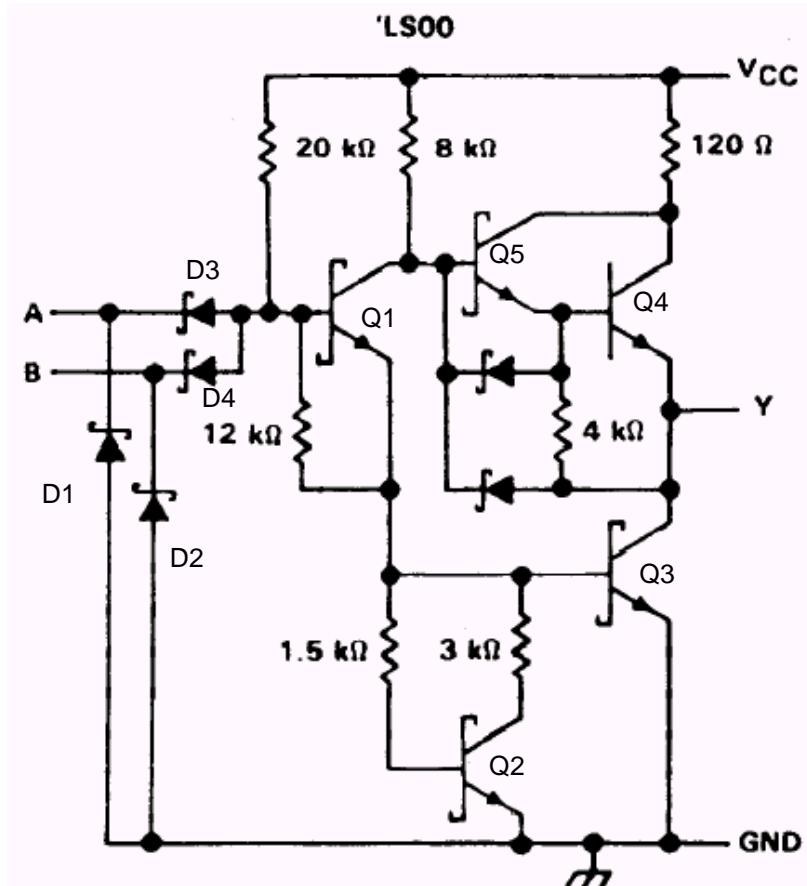
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$	9	15	ns	
t_{PHL}				10	15	ns	



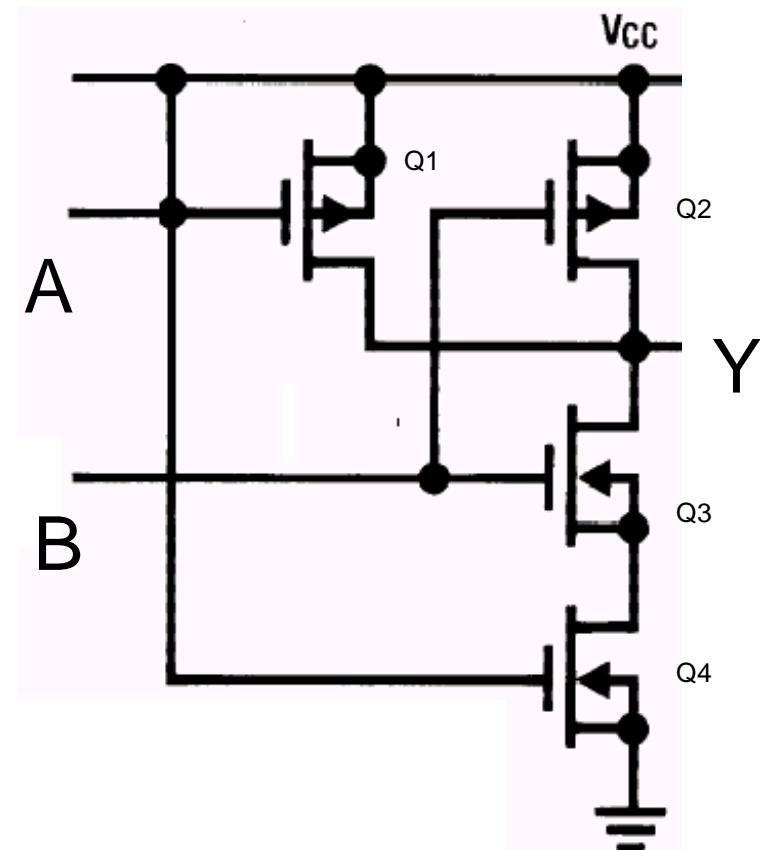
The Internal Structure of LS-TTL Gate

- Inputs are protected by diodes
- If either D3 or D4 conducts, the chain of Q1 and Q2 doesn't open. So it means that Q3 doesn't conduct and Y is HIGH
- If both inputs are in the high state, the chain of Q1 and Q2 conducts. So also Q3 conducts and Y is LOW.
- At HIGH state only Q5 conducts at small current levels, if more current is needed, also Q4 opens

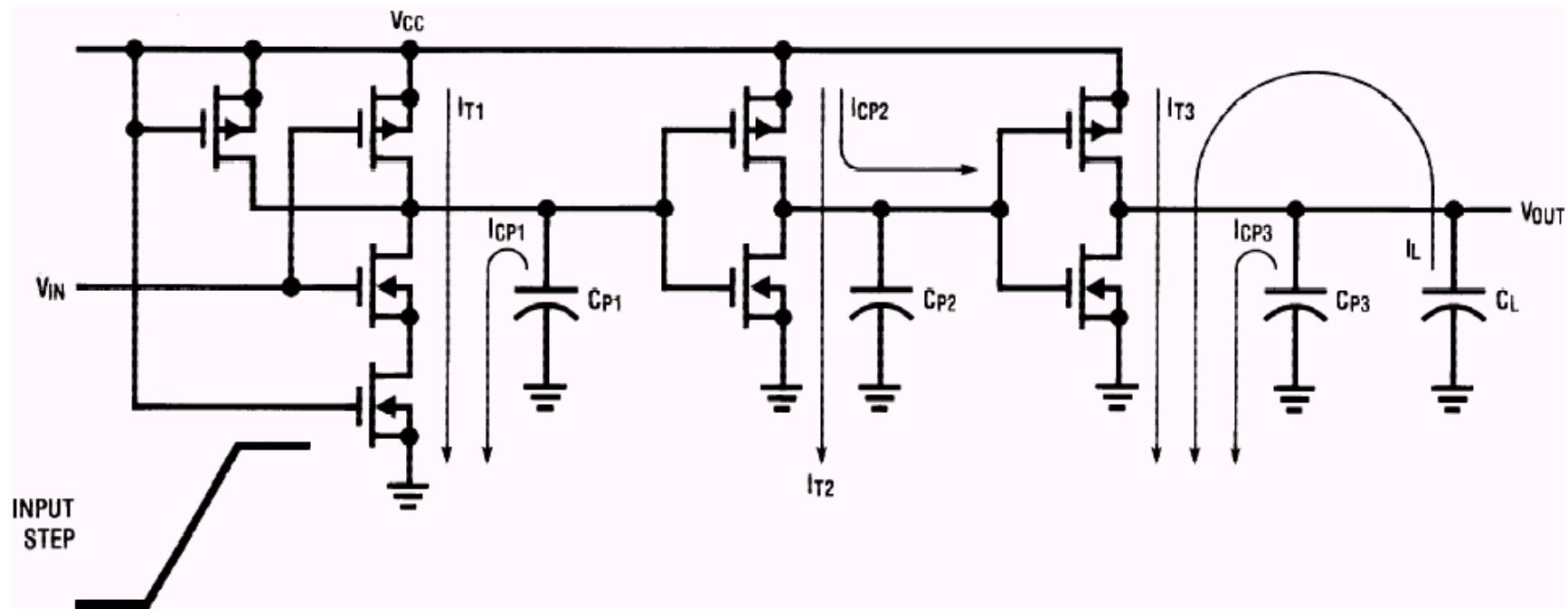


Internal Structure of High-Speed CMOS Gate

- If A and B both are in the HIGH state Q3 and Q4 conduct and the output is LOW
- In all other cases Q1 or Q2 conduct (or both) and the output is HIGH. In these cases the chain of Q3 and Q4 is not open.



Currents in CMOS Gate



Matching

- At high frequencies impedance level of the transmission path plays an important role if want to avoid the distortion of the signal
- Long transmission lines on the PCB board shall be terminated in order to avoid reflections
- Output impedance of transmitter=Characteristic impedance=Input impedance of receiver (Optimum matching)



STUDY MATERIAL

When Matching is Needed ?

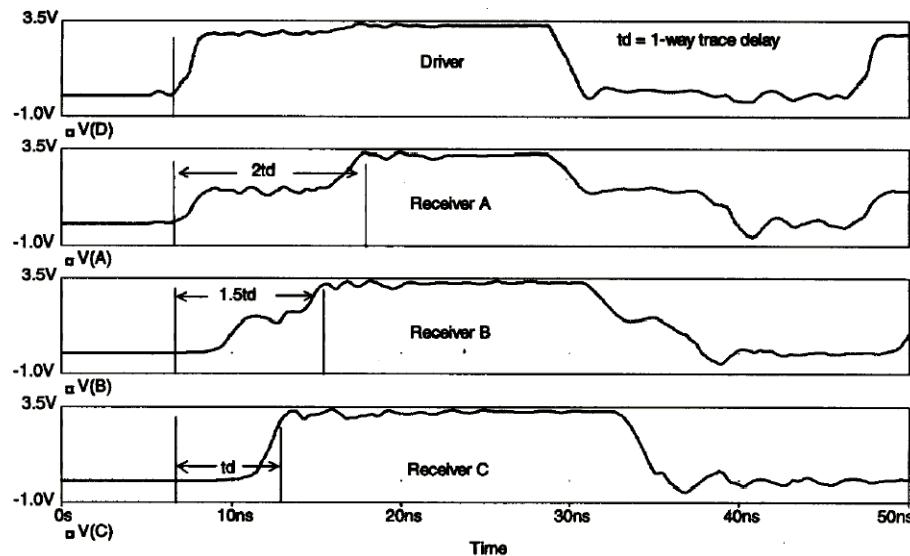
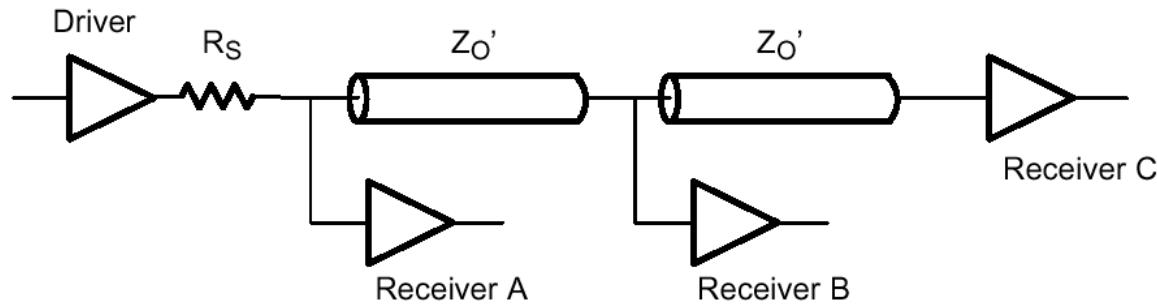
**Maximum trace length in inches with
15pF loading**

Family	tr ns	tf ns	100 Ω	70 Ω	50 Ω	35 Ω	25 Ω
HC	2.9	2.9	18.1	12.7	9.1	6.3	4.5
AHC	2.1	1.6	10.0	7.0	5.0	3.5	2.5
AC	1.2	1.7	7.5	5.3	3.8	2.6	1.9
ALS	2.7	1.7	10.6	7.4	5.3	3.7	2.7
FAST	4.0	1.4	8.8	6.1	4.4	3.1	2.2
ABT	0.9	1.2	5.6	3.9	2.8	2.0	1.4
LVT	0.8	0.6	3.8	2.6	1.9	1.3	0.9
ALVT	0.8	0.7	4.4	3.1	2.2	1.5	1.1
LVC	1.8	1.8	11.3	7.9	5.6	3.9	2.8
LV	2.9	2.9	18.1	12.7	9.1	6.3	4.5
ALVC	1.2	1.1	6.9	4.8	3.4	2.4	1.7

As you can see, using faster edge families even with relatively short traces still requires consideration of transmission line effects.

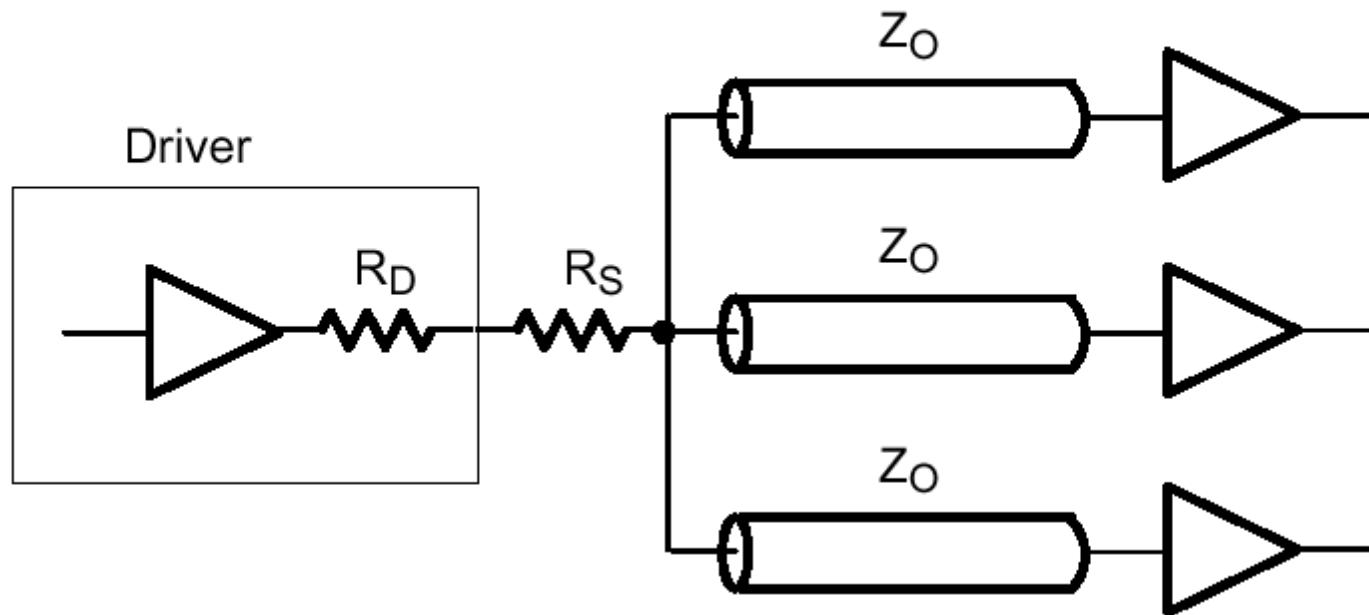


Source Termination

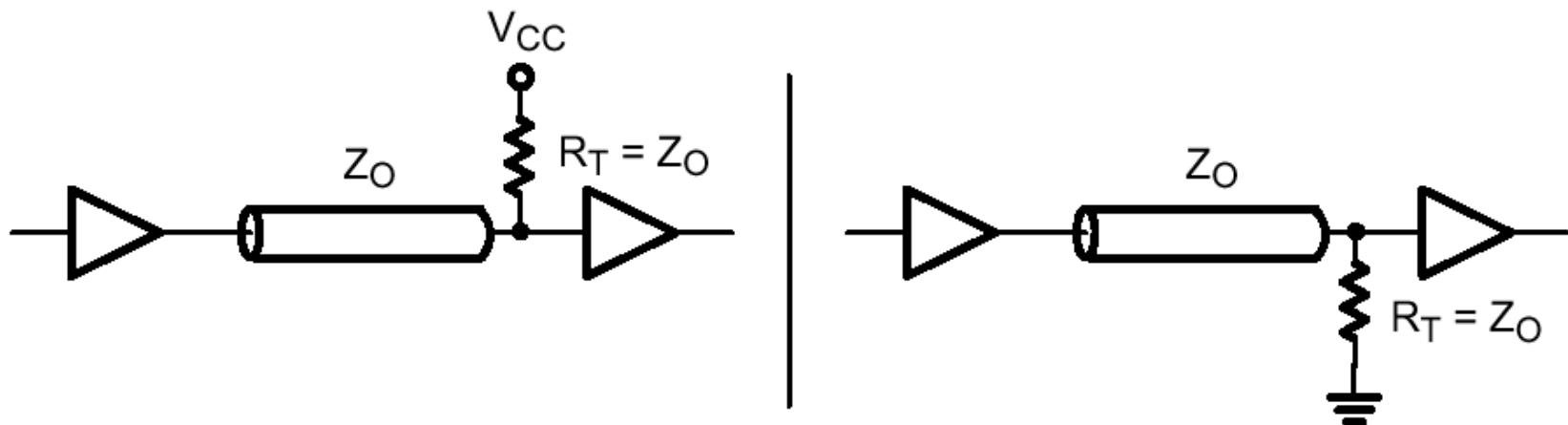


Equal Delay Branches

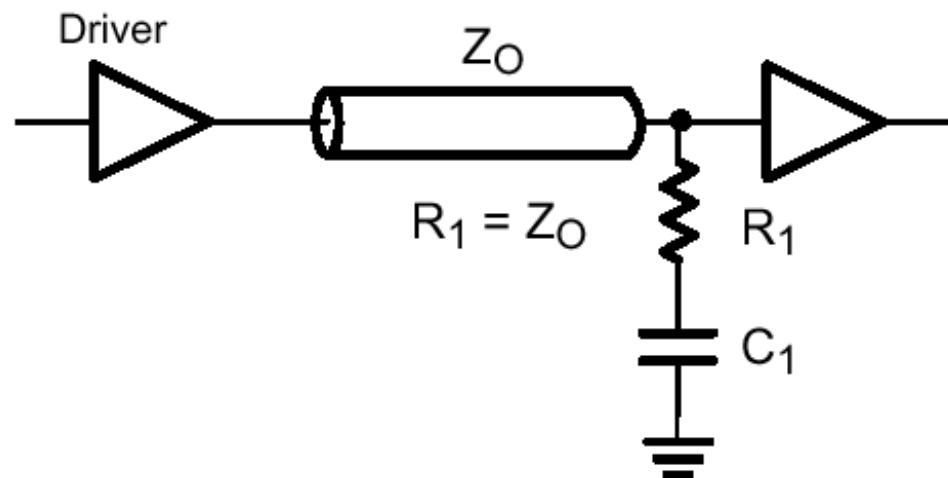
$$R_S = Z_0/3 - R_D$$



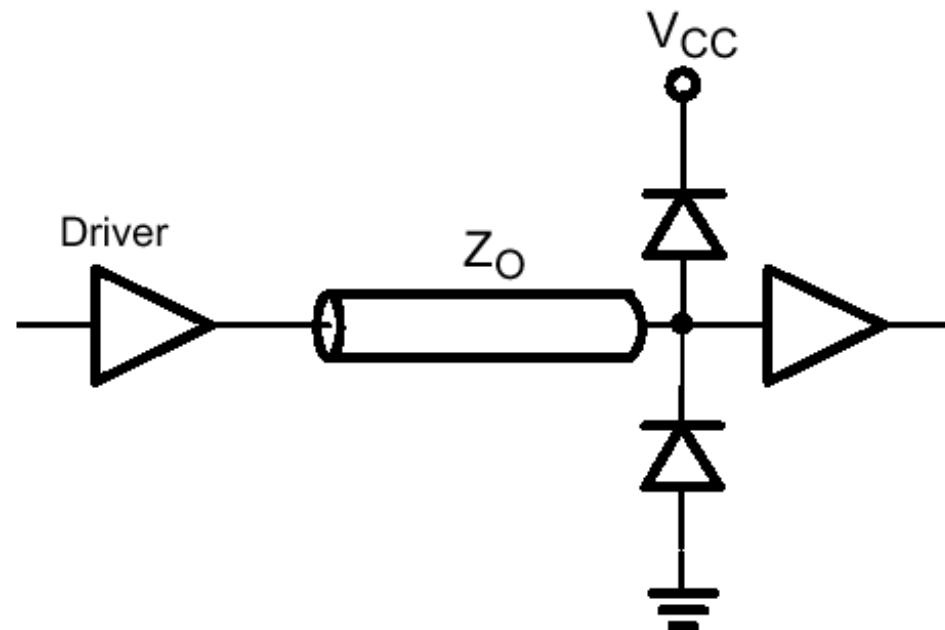
Parallel Terminations



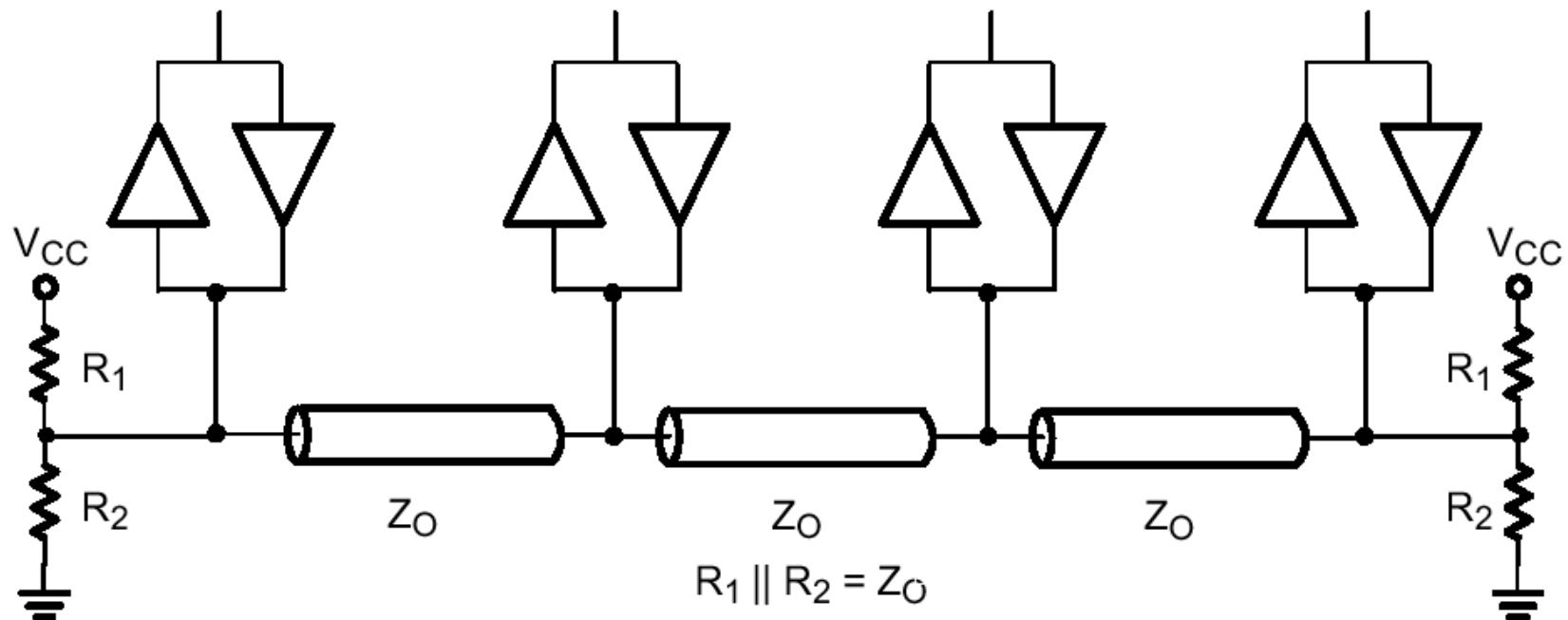
AC Termination



Diode Clamp Termination



Bus Termination



IC Fabrication Steps

- Wafer preparation
- Oxidation
- Diffusion
- Ion implantation
- Chemical vapour deposition
- Metallisation
- Photolithography
- Packaging



Wafer Preparation

- Starting material is high purity silicon which is grown as a single cylinder-shaped crystal ingot
- Crystal is sawed to produce wafers ($400\text{-}600\mu\text{m}$ thick)
- Wafer properties can be controlled during the growth (impurities, crystal orientation and especially resistivity)
- Heavily doped (+), lightly doped (-)



Oxidation

- Silicon reacts with oxygen to form SiO_2
- To speed reaction the temperature is raised to 1000-1200 °C
- The thermally grown oxide layer has excellent electrical insulation properties
- Oxide layer is used to protect certain areas of wafer during the manufacturing as well as to form integrated capacitors



Diffusion

- In fabrication impurity atoms are added at high temperature (1000-1200 °C) in order to change the resistivity of silicon. It is very much like a drop of ink dispersed through a glass of water (but slower)
- When the wafer is cooled impurities are in their position
- N-type dopants are phosphorus and arsenic
- P-type dopant is boron



Ion Implantation

- Another method to get impurities into silicon
- Impurity ions are accelerated by an electric field
- Because ion implantation can be electrically controlled, it is much more accurate than diffusion
- Repeatability is also better than in diffusion



Chemical Vapour Deposition

- Gases or vapours are chemically reacted leading the formation of a solid on a substrate
- For instance if silane gas and oxygen are mixed above , silicon dioxide deposits as a solid on the silicon
- The oxide layer formed is not as good as thermally grown
- Silane gas alone =>silicon layer
- Silane + high temp (1000 °C) =>crystalline silicon
(is called epitaxial layer)



Metallisation

- Deposition of interconnect the various components of the integrated circuits
- Diodes, transistors, capacitors, etc.
- Metal used in interconnections is usually aluminium, but also copper is used nowadays



Photolithography

- The surface geometry of components are defined photographically
- Silicon is coated with a photosensitive layer (photoresist). When exposed to light through a pattern, the photoresist become softened. The exposed layer can be removed by using a chemical developer
- In high resolution process UV light or an electron beam is needed for exposition



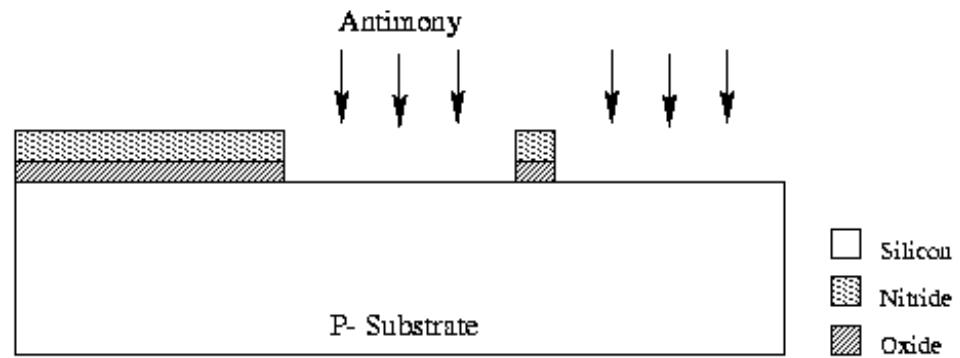
Packaging

- After process steps a silicon wafer can contain hundreds of finished circuits
- Before packaging circuits are tested in wafer form and bad circuits are marked
- The circuits are separated are good circuits are mounted in packages
- Fine gold wires are used for bonding (package to circuit interconnection)
- Sealing of a package

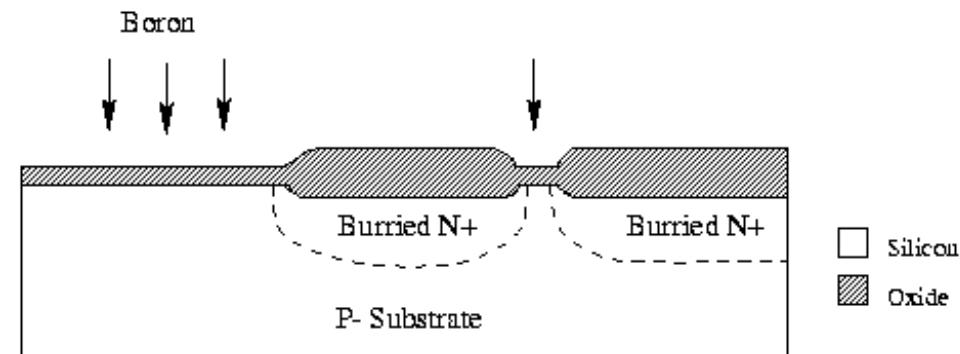


BiCMOS Example Process

- Antimony Implantation

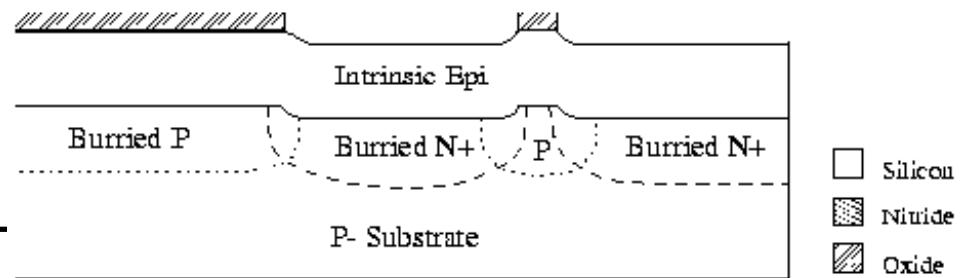
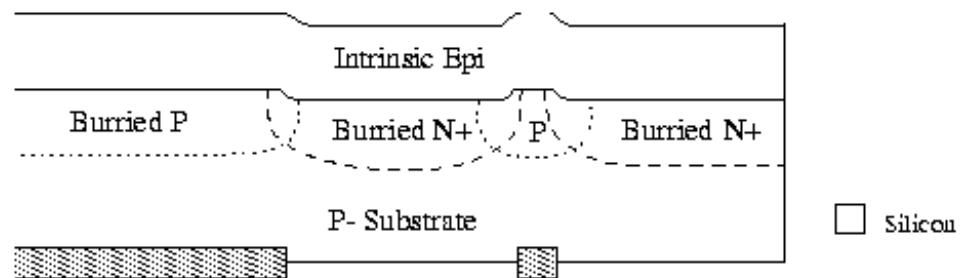


- Oxide grown and nitride removed



BiCMOS Example Process, continued

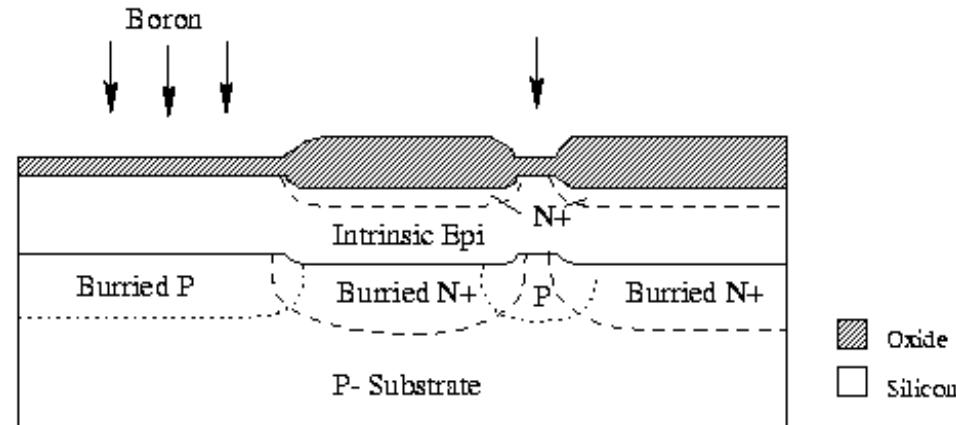
- All oxide removed and intrinsic layer grown



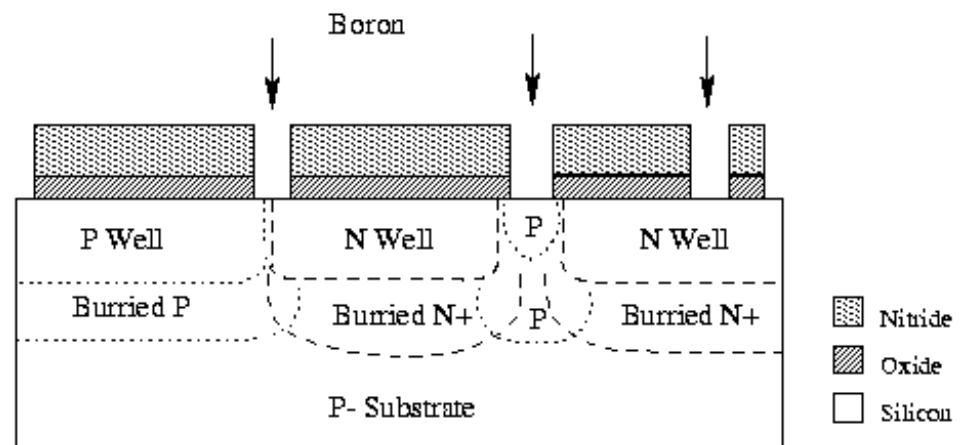
- Nitride protection done and N- regions opened

BiCMOS Example Process, continued

- N-type dopant implanted and oxide layer added

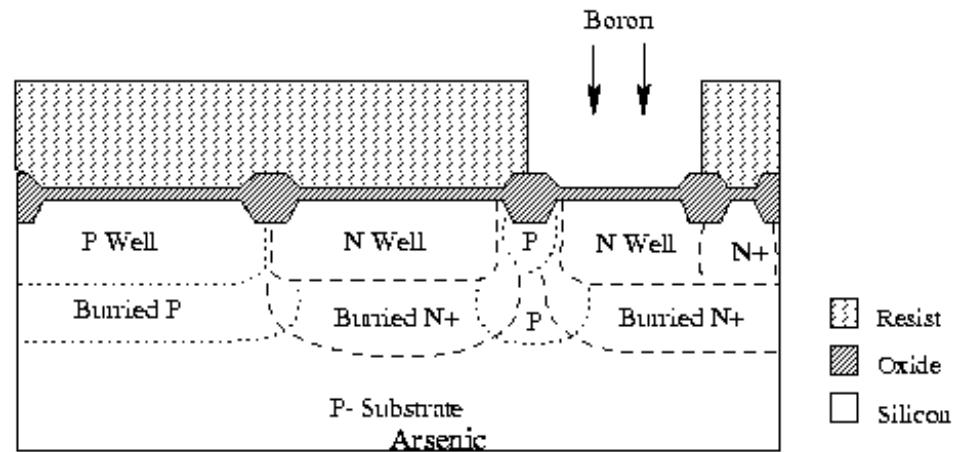
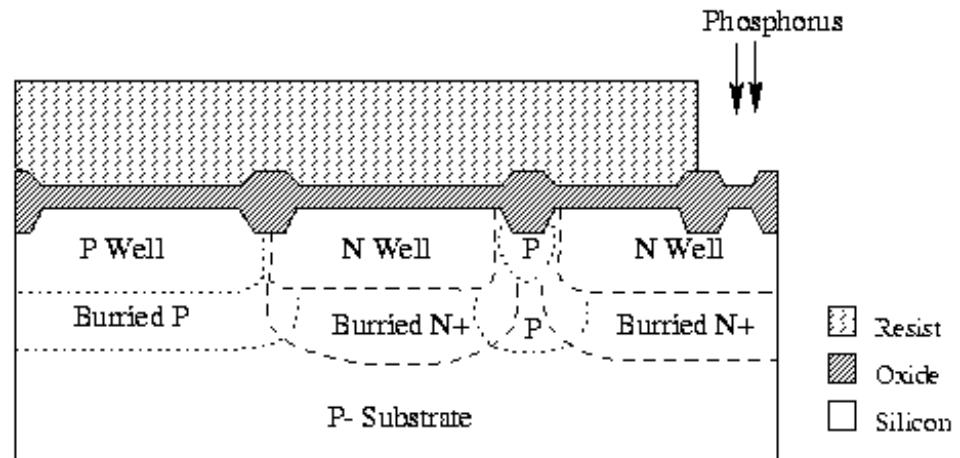


- Wells fabricated, oxide grown, isolation areas etched



BiCMOS Example Process, continued

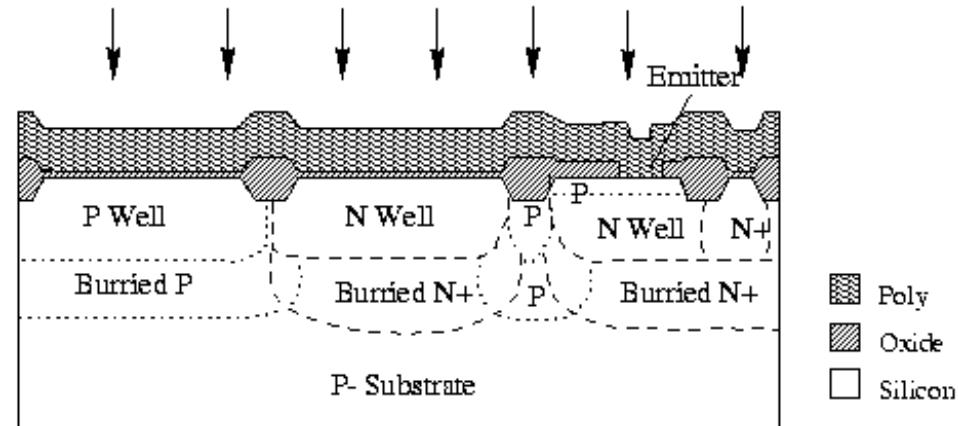
- Nitride masks removed and subcollector (N^+) pattern for implanting



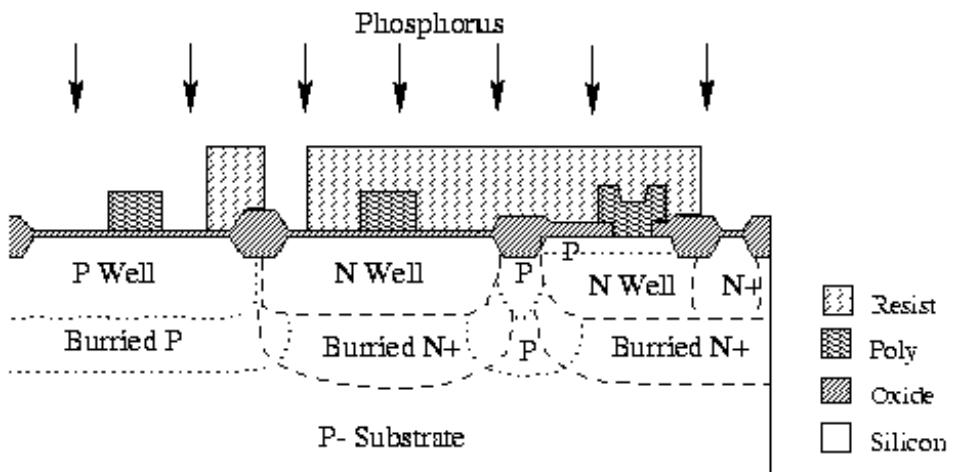
- Base region opened for implanting

BiCMOS Example Process, continued

- Emitter window patterned and opened as well as polysilicon layer deposited

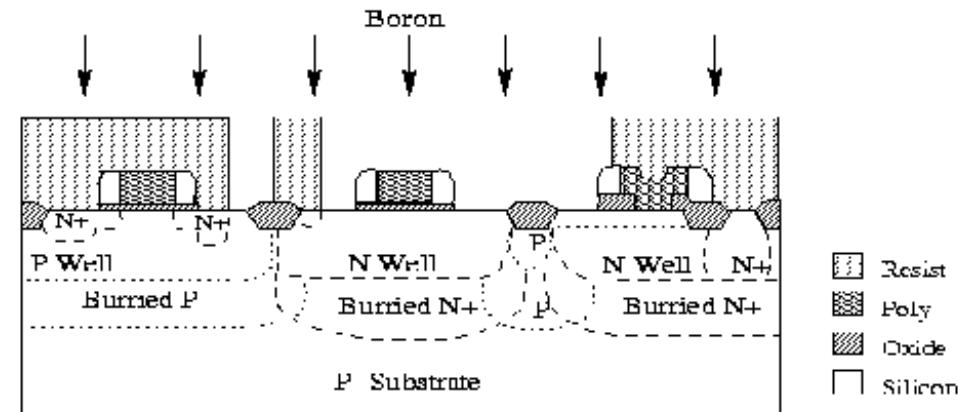
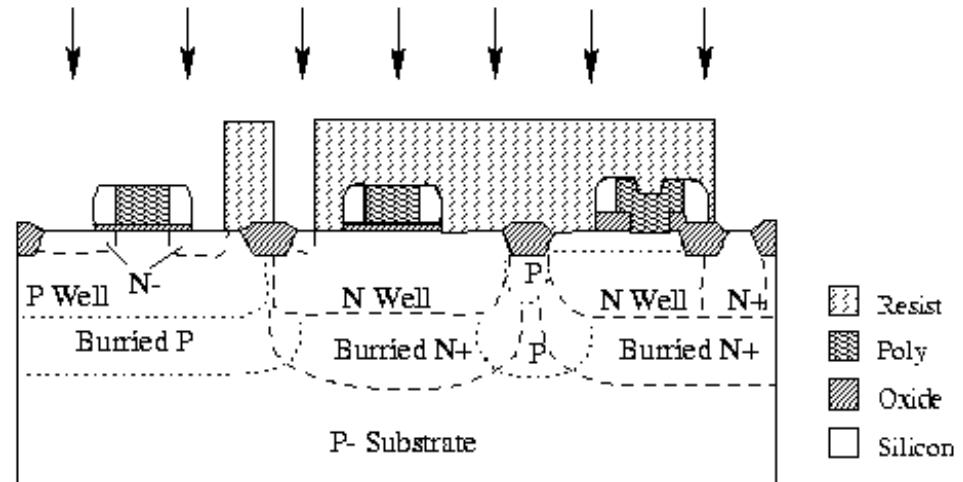


- CMOS patterned and phosphorus implanted



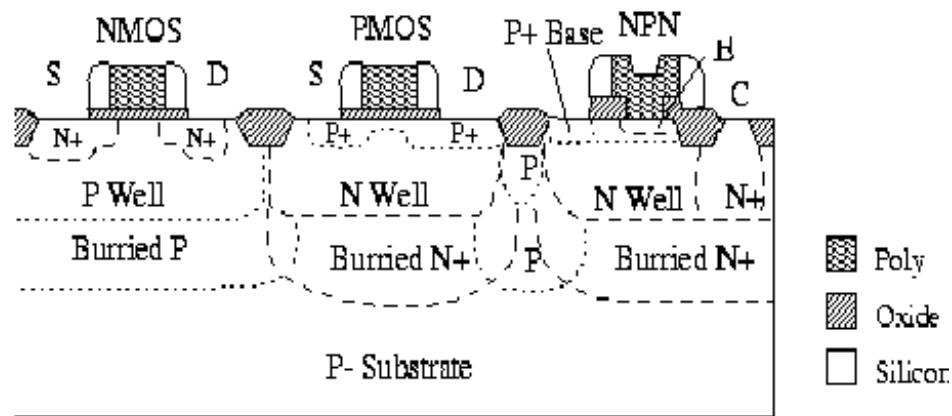
BiCMOS Example Process, continued

- Source-drain regions are heavily doped by phosphorus and boron



BiCMOS Example Process, continued

- Device cross-section of BiCMOS process after fabrication of the active areas. The source-drain anneal is optimised to emitter outdiffusion conditions. Afterwards the structure is scheduled for a double-level interconnect process.



SOI

- Silicon-On-Insulator (SOI) is a semiconductor fabrication technique developed by IBM that uses pure crystal silicon and silicon oxide for integrated circuits (ICs) and microchips. An SOI microchip processing speed is often 30% faster than today's complementary metal-oxide semiconductor (CMOS)-based chips and power consumption is reduced 80%, which makes them ideal for mobile devices. SOI chips also reduce the soft error rate, which is data corruption caused by cosmic rays and natural radioactive background signals.
- SOI is based on Separation by Implantation of Oxygen (SIMOX). SIMOX involves the direct injection of purified oxygen into the silicon wafer at an extremely high temperature. The oxygen bonds with the silicon and forms thin layers of silicon oxide. This layer of silicon oxide film is perfect enough that it bonds with the pure crystal silicon layer.



Copper Process

- Copper has lower resistivity, and ultimately lower resistance, than aluminum
- The advantage of copper interconnect is its inherently lower resistivity, which minimises power supply drop throughout the device. In a 0.18-micron, six-layer metal process, the top two layers deploy copper interconnect. These two layers are used to route clock lines to minimise both clock skew and I/O skew, leading to optimised performance once again



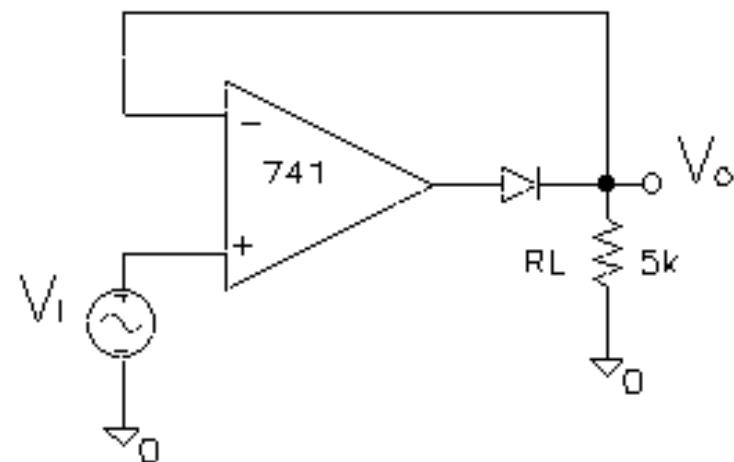
Active Rectifiers

- Active rectifiers are used in the applications, where accurate rectifiers are needed.
- For example in voltage meters accurate rectifiers are needed
- In power supplies the rectifier accuracy is not the key issue

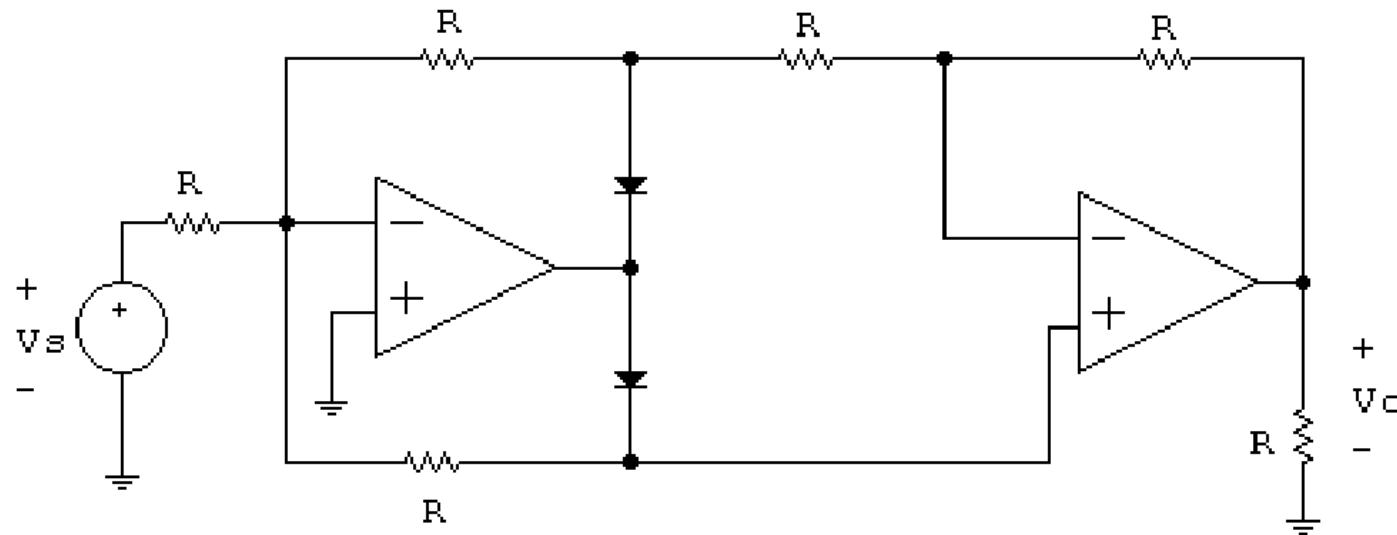


Simple Precision Half-Wave Rectifier

- Operates similarly than normal diode
- Forward voltage reduces by the factor $1/A$, $A=\text{open-loop gain of an operational amplifier}$

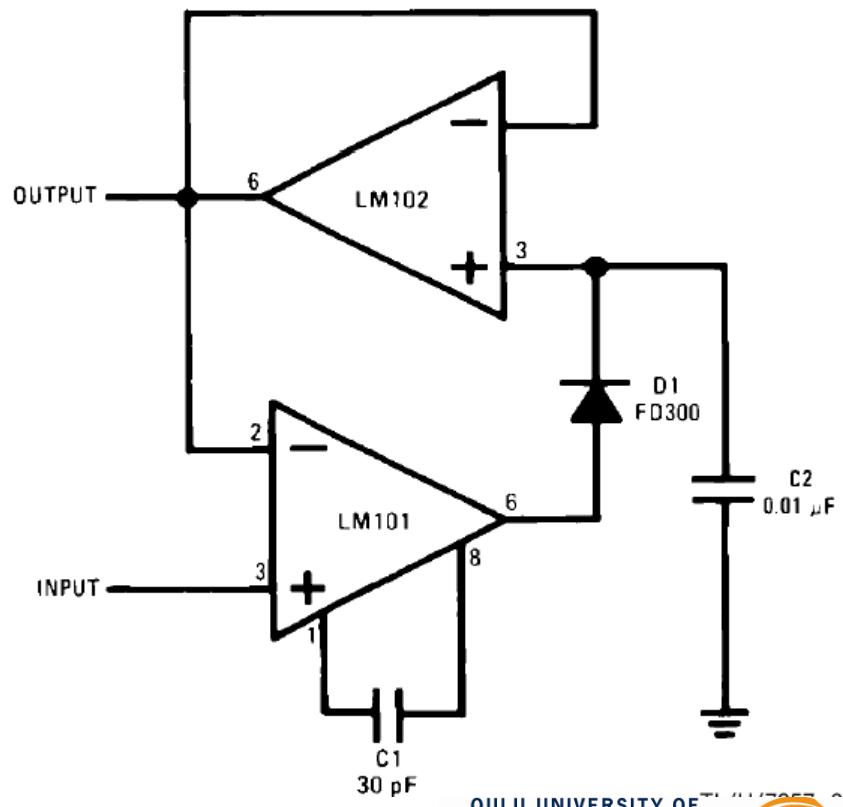


Precision Full-Wave Rectifier



Active Peak Detector

- A peak value is stored in the capacitor and there are not a current path for discharging the capacitor
- FET-input operational amplifier is preferred as an output buffer



Cooling of Components

- Both the performance reliability and life expectancy of electronic equipment are inversely related to the component temperature of the equipment. The relationship between the reliability and the operating temperature of a typical silicon semi-conductor device shows that a reduction in the temperature corresponds to an exponential increase in the reliability and life expectancy of the device. Therefore, long life and reliable performance of a component may be achieved by effectively controlling the device operating temperature within the limits set by the device design engineers.
- Heat sinks are devices that enhance heat dissipation from a hot surface, usually the case of a heat generating component, to a cooler ambient, usually air.



Selection of a Heat Sink

T_a=Air temperature

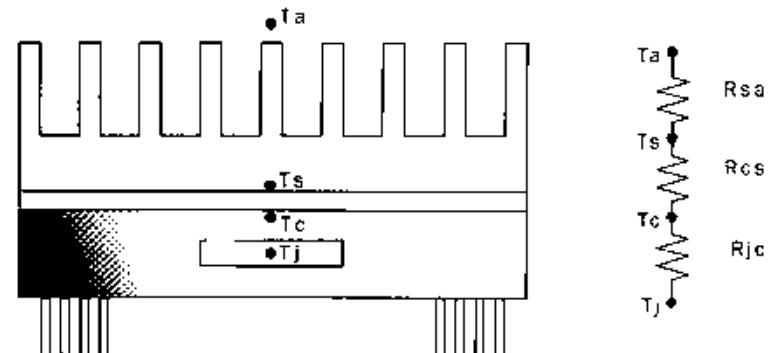
T_s=Sink temperature

T_c=Capsule temperature

T_j=Junction temperature

R_{sa}, R_{cs}, R_{jc}=Thermal resistances

$$T_a + P(R_{jc} + R_{cs} + R_{sa}) = T_j$$



Some Thermal Resistances, Rcs

Material	Conductivity W/in °C	Thickness inches	Resistance in ² °C/W
There-O-Link Thermal Compound	0.010	0.002	0.19
High Performance Thermal Compound	0.030	0.002	0.07
Kon-Dux	0.030	0.005	0.17
A-Dux	0.008	0.004	0.48
1070 Ther-A-Grip	0.014	0.006	0.43
1050 Ther-A-Grip	0.009	0.005	0.57
1080 Ther-A-Grip	0.010	0.002	0.21
1081 Ther-A-Grip	0.019	0.005	0.26
A-Phi 220 @ 20psi	0.074	0.020	0.27
1897 in Sil-8	0.010	0.008	0.81
1898 in Sil-8	0.008	0.006	0.78

Table 1: Thermal properties of interface materials¹

