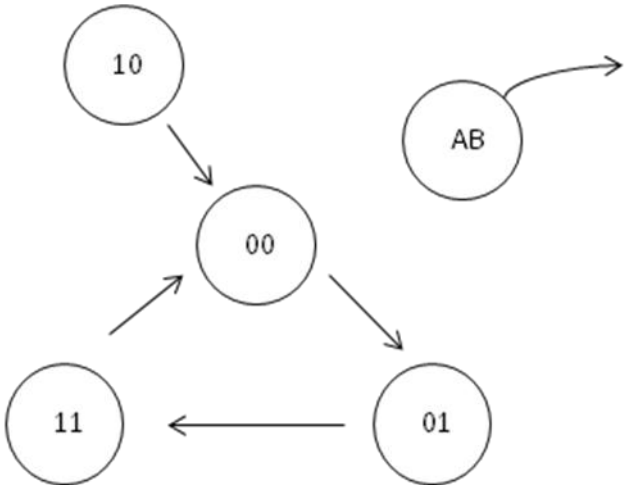
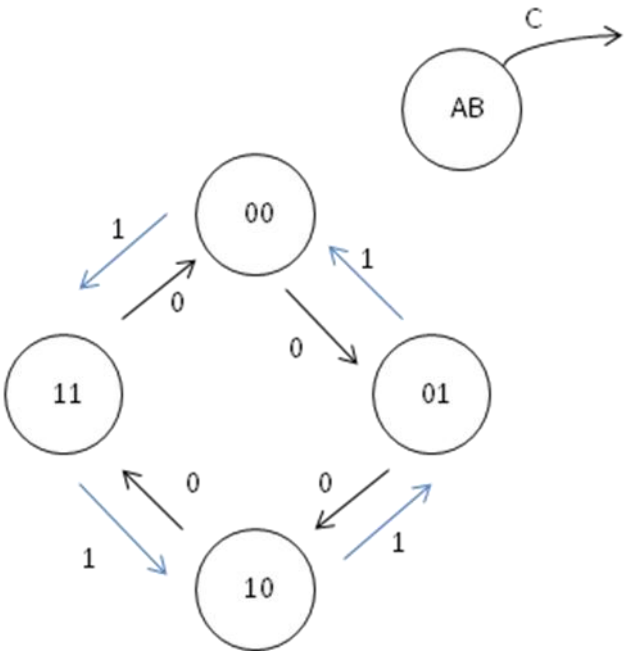
Exercise 5

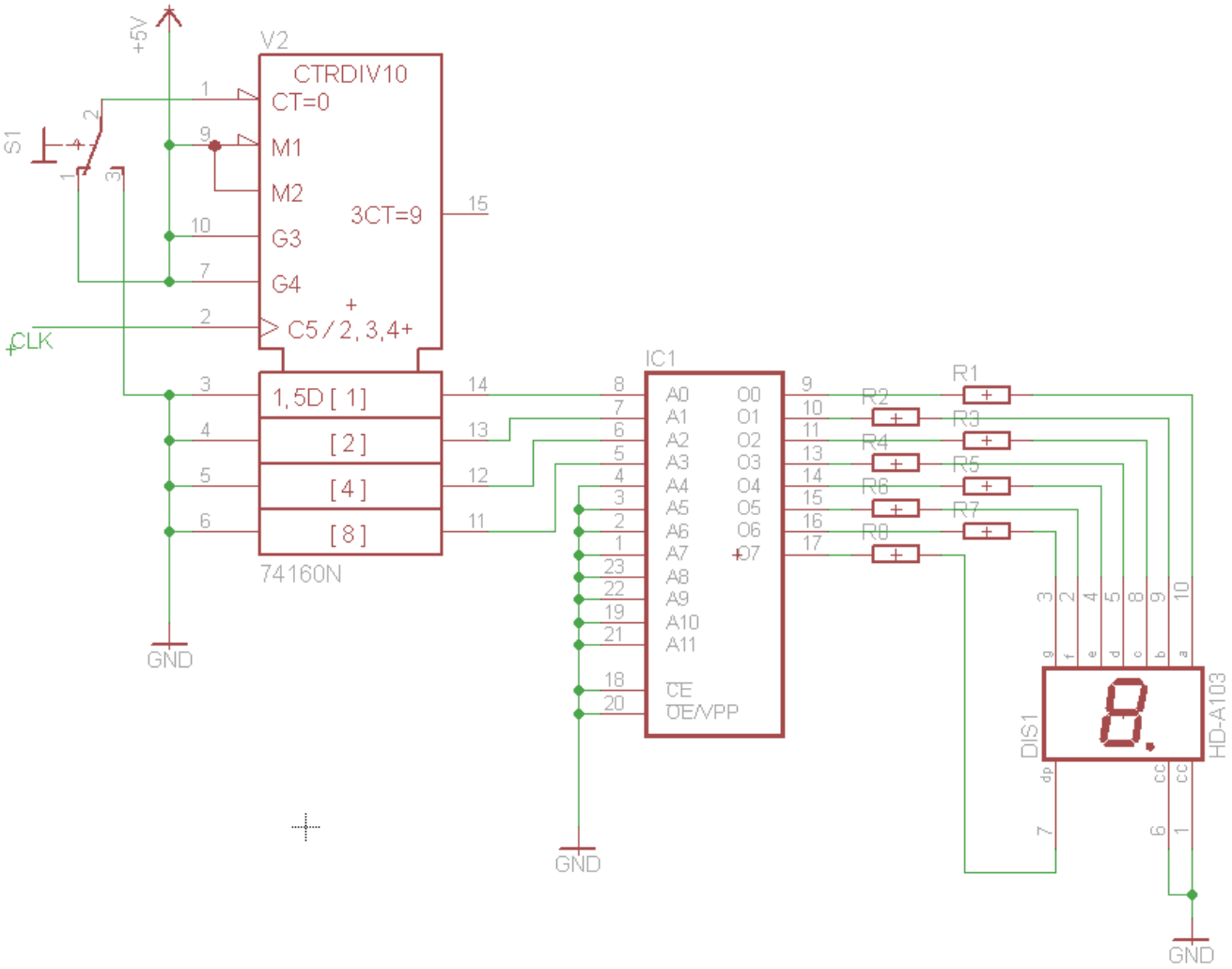
1. Design a sequential circuit that satisfies the following state diagram.
    a. By using D flip flops.
    b. By using JK flip flops.



2. Design a sequential circuit that satisfies the following state diagram.
    a. By using D flip flops.
    b. By using JK flip flops.



3. In the figure there is an EPROM based sequential circuit that monitors it's state on the 7 segment display. Define the EPROM data so that monitoring is working as intended. Decimal point is not shown.



INTERNAL CIRCUIT DIAGRAM