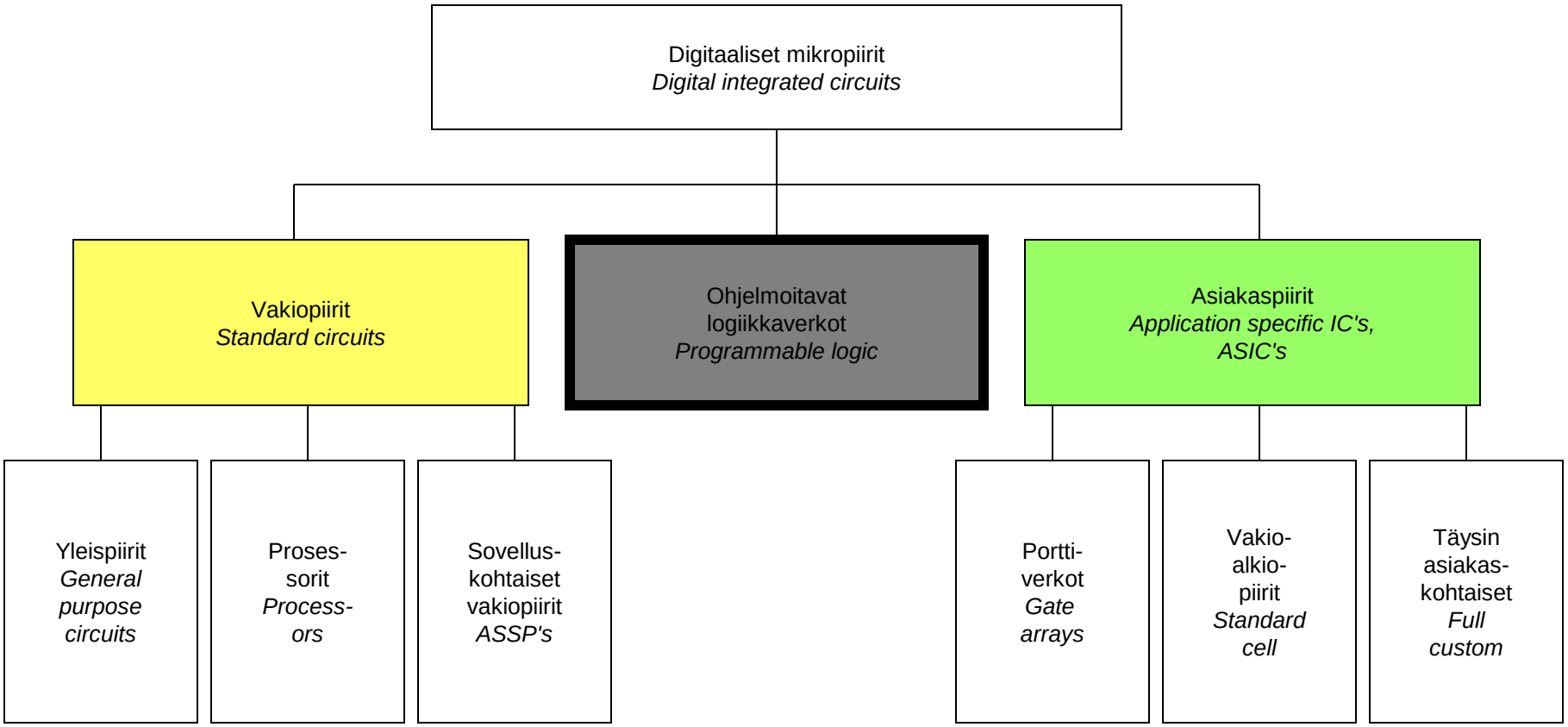
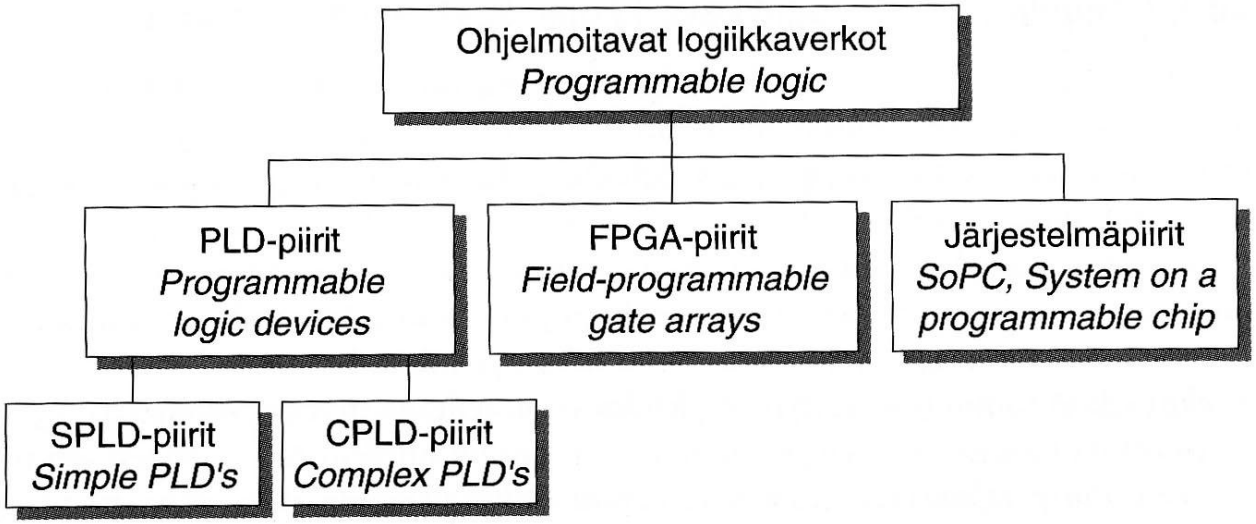
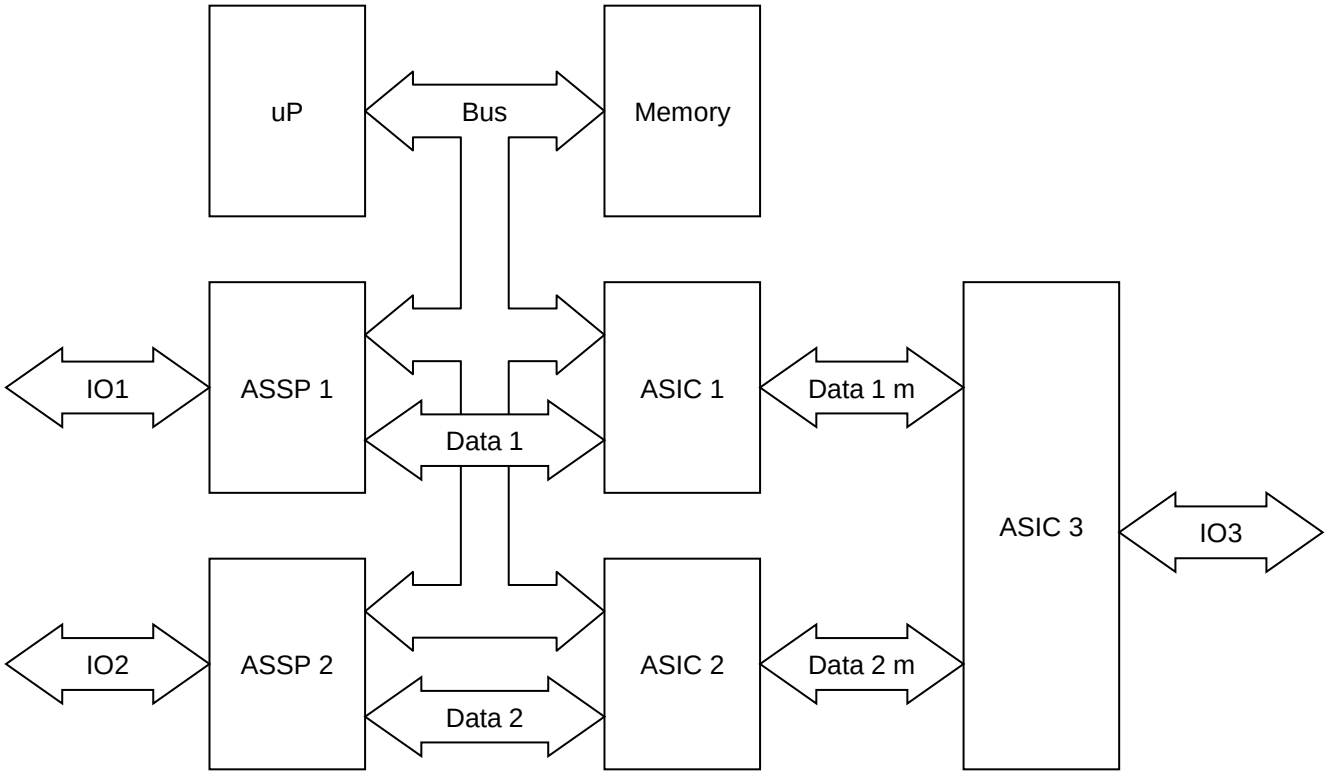
Integrated Digital Electronics



Programmable Logic Arrays



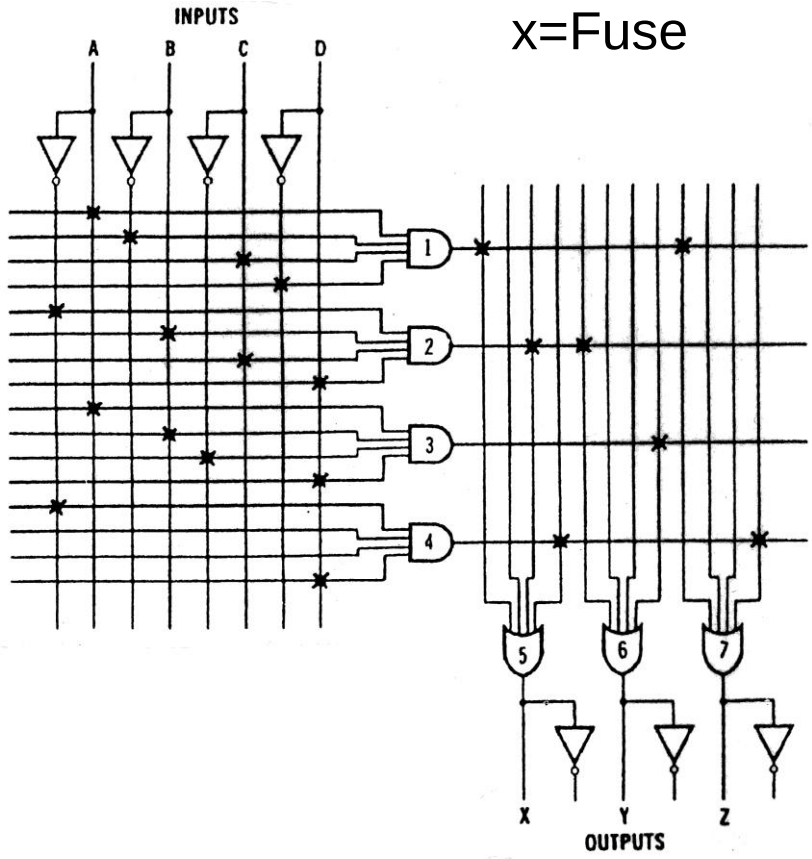
Example Architecture of Digital Design



PLA Programming

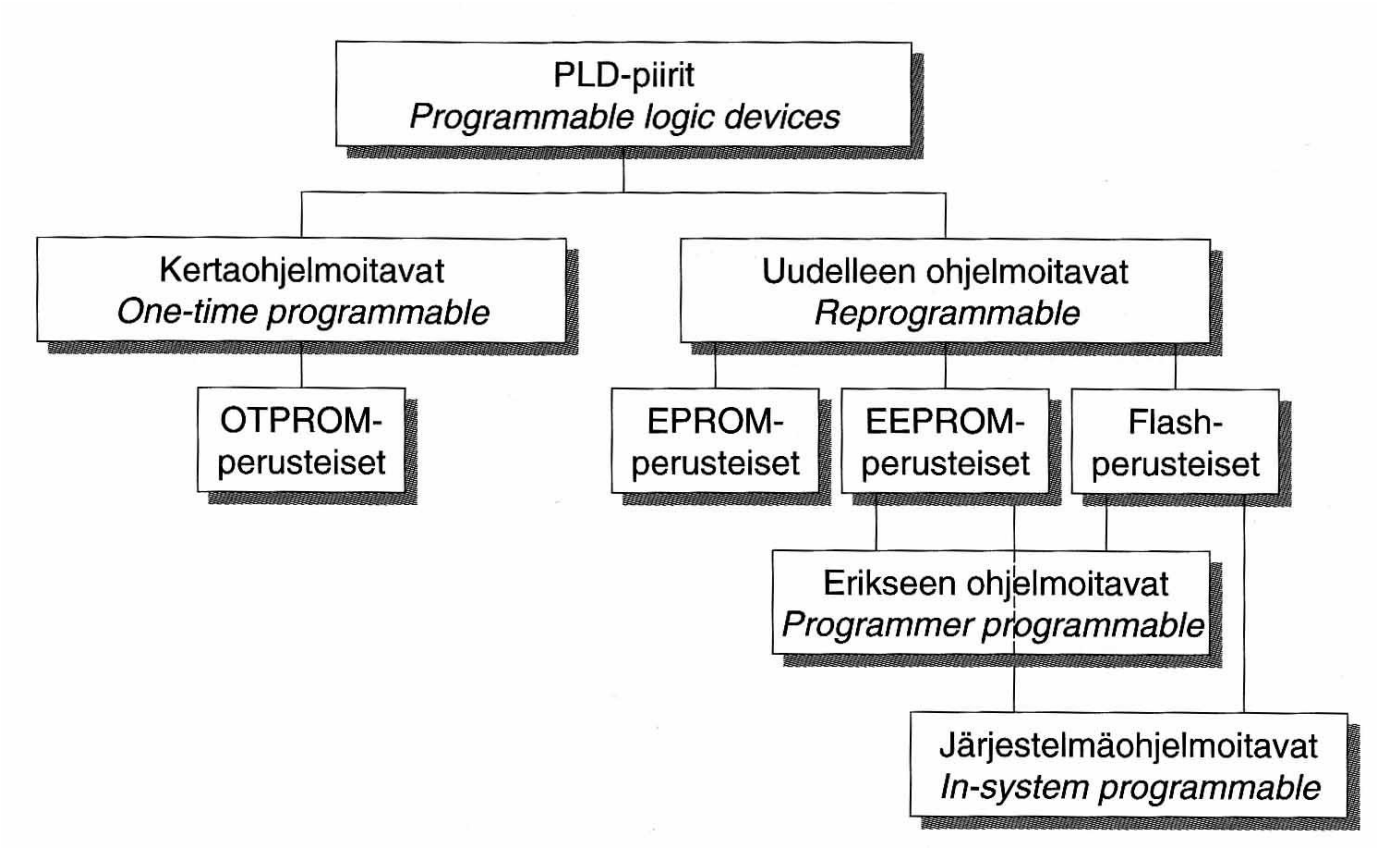
x=Fuse

AND



OR

PLD Programming Architectures



Typical Development Environment

VHDL

- VHDL=Very High Speed Integrated Circuit Hardware Description Language
- The development of VHDL was originally initiated by Ministry of Defense in USA in 1981
- VHDL is specified especially to design circuits at the behavioral and the gate leve
- VHDL is
  - based on a public standard
  - design-system independent
  - technology independent

VHDL Example

```
library ieee;
use ieee.std_logic_1164.all;
entity oor is
    port( A, B: in std_logic; Y: out std_logic);
end oor;

architecture functionality of oor is
begin
   process (A,B)
   begin
      Y<=A or B;
   end process;
end functionality;
```


STUDY MATERIAL

Second VHDL Example

```
library ieee;
use ieee.std_logic_1164.all;  --take std logic in use

entity ls374 is      --entity with port definitions for ls374
   port (CLK, OC: in std_logic; D:in Std_logic_vector (0 to 7);
   Q: out std_logic_vector (0 to 7));
end ls374;

architecture functionality_of_ls374 of ls374 is  --architecture desription for ls374
begin
   process (CLK, OC)
      variable result: std_logic_vector (0 to 7) ;
   begin
      if (OC='1') then Q<="ZZZZZZZZ";
      else  Q<=result;
      end if;
      if (CLK='1' and CLK'event) then result:=D;
      end if;
   end process;
end functionality_of_ls374;
```


An Example of FPGA Development Tools

- QUARTUSII, Web Edition for Altera Products

http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html