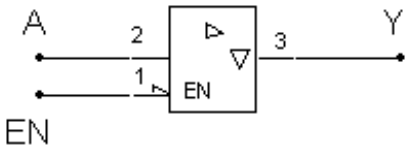
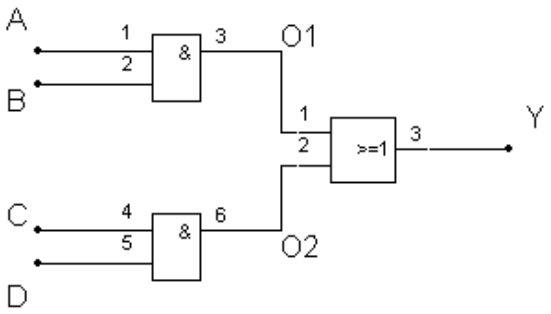
Exercise 10

1. Make a VHDL description of the gate below. Simulate and test.



2. Do the following tasks.
    a. Make a VHDL description of dff. Simulate and test.
    b. Change the VHDL description of the dff so that you write a function (find_r_edge) to find the rising edge of a signal. This function is then called in the main VHDL description of the dff.
    c. Write a procedure including all the features of the dff. Then write the main VHDL description (main_dff) so that you call the just written procedure

3. Write the VHDL description for the following circuits. Write codes for the gates at first and then connect gates by using VHDL signals.



4. Make a VHDL description of the following circuits. Simulate and test.