```
library ieee;
use ieee.std_logic_1164.all;

entity iso_andi is
		port(A1, B1, C1, D1:in std_logic; Y1: out std_logic);
end iso_andi;


architecture toiminta of iso_andi is
		signal apu1, apu2: std_logic;
		component andi
				port (A, B: in std_logic; Y: out std_logic);
		end component;

begin
		X0: andi port map (A1, B1, apu1);
-- tai X0: andi port map (A=>A1, B=>B1, Y=>apu1);
		X1: andi port map (C1, D1, apu2);
		X2: andi port map (apu1, apu2, Y1);
end toiminta;
```