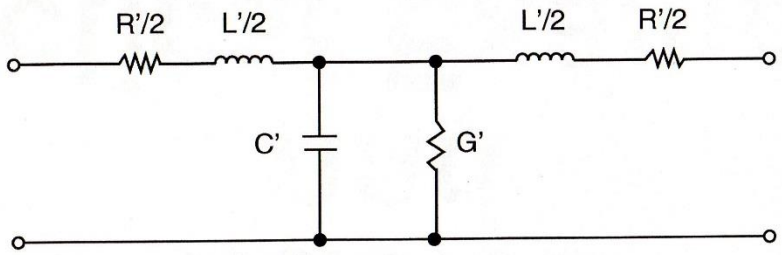
CIRCUIT DIAGRAM OF A TRANSMISSION LINE

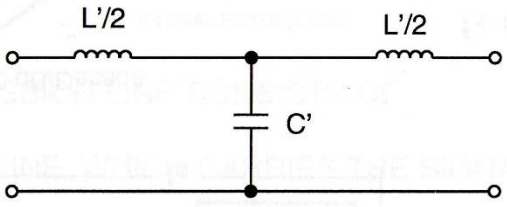


L'	CHARACTERISTIC INDUCTANCE PER UNIT LENGTH	nH/cm
C'	CHARACTERISTIC CAPACITANCE PER UNIT LENGTH	pF/cm
R'	CHARACTERISTIC RESISTANCE PER UNIT LENGTH	Ω/cm
G'	CHARACTERISTIC CONDUCTANCE PER UNIT LENGTH	S/cm

LINE IMPEDANCE $\vec{Zo} = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$

LOSS-FREE TRANSMISSION LINES

ON PRINTED CIRCUIT BOARDS IN DIGITAL SYSTEMS THE LOSSES OF THE LINE CAN BE NEGLECTED:



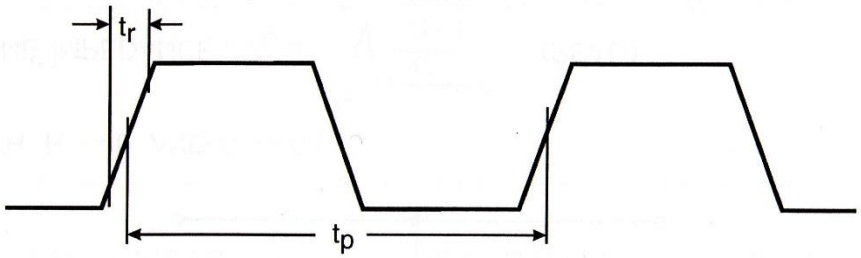
WITH $R' \rightarrow 0$ AND $G' \rightarrow 0$:

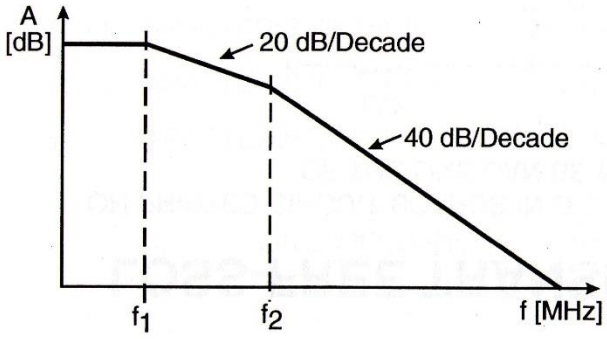
LINE IMPEDANCE : $Z_0 = \sqrt{\frac{L'}{C'}}$ (REAL!)

PROPAGATION TIME $T = \sqrt{L' \times C'}$

CUT-OFF FREQUENCY: $fo = \frac{1}{2\pi\sqrt{L' \times C'}}$ WITH $L', C' \rightarrow 0 \Rightarrow f_g = \infty$

FREQUENCY SPECTRUM OF DIGITAL SIGNALS

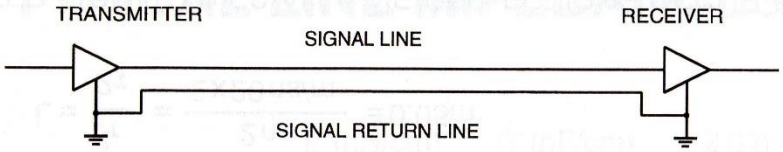




$$f_1 = \frac{1}{t_p}$$

$$f_2 = \frac{1}{\pi \times t_r}$$

TRANSMISSION LINE



A TRANSMISSION LINE CONSISTS OF

- A SIGNAL LINE, WHICH CARRIES THE SIGNAL CURRENT

- A SIGNAL RETURN LINE (MOSTLY GND) WHICH CARRIES A RETURN CURRENT OF THE SAME MAGNITUDE.

ANY DC INTERCONNECT BETWEEN THE GND TERMINALS OF THE TWO CIRCUITS (e.g. SAFETY EARTH) WILL NOT PROVIDE A SIGNAL RETURN PATH ACCORDING TO THE TRANSMISSION LINE THEORY.

THE AREA BETWEEN THE SIGNAL LINE AND THE RETURN LINES DETERMINES THE CAPABILITY OF THE CIRCUIT TO RADIATE RF AND ALSO ITS IMMUNITY AGAINST EMI.

TRANSMISSION LINE THEORY

RULE OF THUMB:

THE TRANSMISSION LINE THEORY HAS TO BE APPLIED WHEN THE RISE TIME OF THE SIGNAL IS SHORTER THAN TWICE THE PROPAGATION TIME.

EXAMPLE 1: TWISTED PAIR CABLE; $\tau = 5$ ns/m ; $t_r = 2$ ns

$$L = \frac{t_r}{2\tau} = \frac{2\,\text{ns}}{2 \times 5\,\text{ns/m}} = 0.2\,\text{m}$$

EXAMPLE 2: BUS LINE; $\tau = 20$ ns/m ; $t_r = 2$ ns

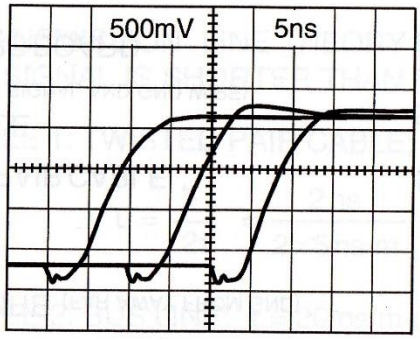
$$L = \frac{t_r}{2\tau} = \frac{2\,\text{ns}}{2 \times 20\,\text{ns/m}} = 0.05\text{m}$$

WITH SHORTER SIGNAL LINES ALL LINE REFLECTIONS OCCUR DURING THE RISE/FALL TIME OF THE SIGNAL. IN THIS CASE IT IS ALLOWED TO USE THE SIMPLIFIED CAPACITIVE LOAD LINE MODEL.

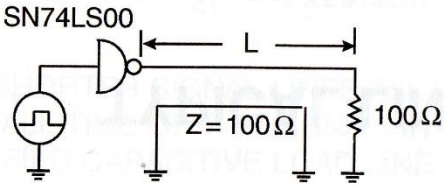
TYPICAL LINE IMPEDANCES

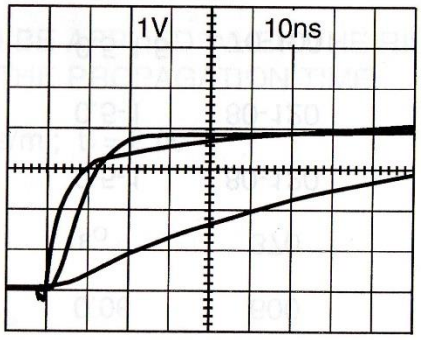
	L' (nH/cm)	C' (pF/cm)	Z (Ω)	τ (ns/m)
SINGLE WIRE (FAR AWAY FROM GND)	20	0.06	600	~4
SPACE	μ_o	ε_o	370	3,3
TWISTED PAIR CABLE	5-10	0.5-1	80-120	5
FLAT CABLE (ALTERNATING SIGNAL AND GND WIRE)	5-10	0.5-1	80-120	5
WIRE ON PC BOARD	5-10	0.5-1.5	70-100	~5
COAX CABLE	2,5	1.0	50	5
BUS LINE	5-10	10-30	20-40	10-20

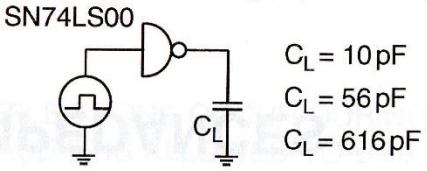
WAVEFORMS
WITH TRANSMISSION LINE AND CAPACITIVE LOAD



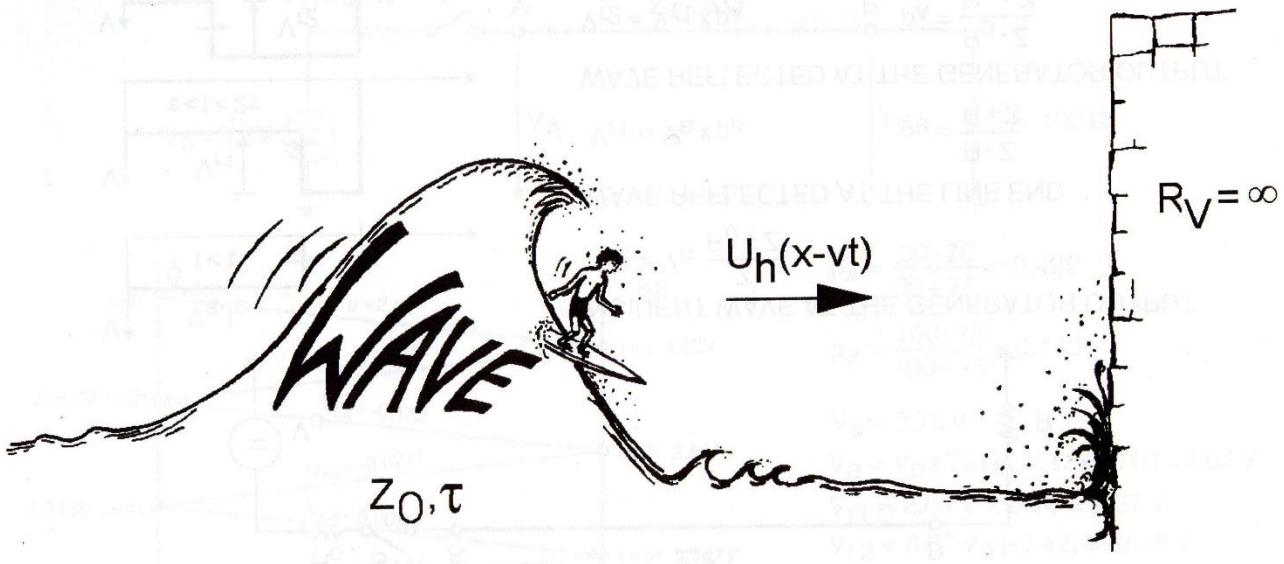
L=0m (~10pF) L=1m (~56pF) L=11m (~616pF)



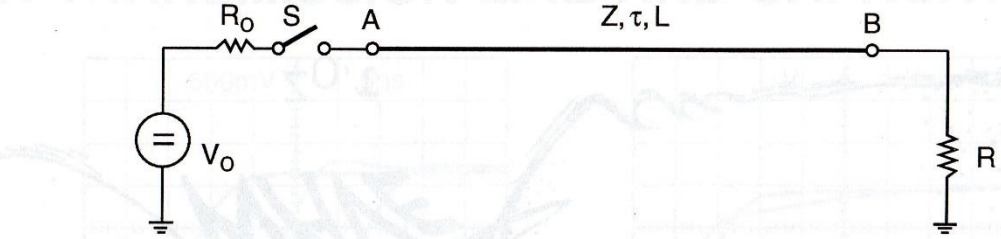


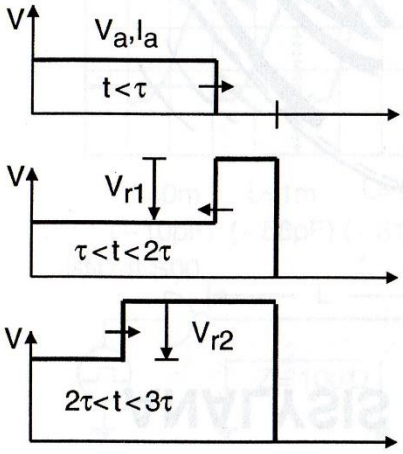


ANALYSIS OF LINE REFLECTIONS



WAVEFORMS CAUSED BY LINE REFLECTIONS





INCIDENT WAVE AT THE GENERATOR OUTPUT

$$V_a = V_o \frac{Z}{R_o + Z}$$

WAVE REFLECTED AT THE LINE END

$$V_{r1} = V_a \times \rho_B \qquad \rho_B = \frac{R - Z}{R + Z}$$

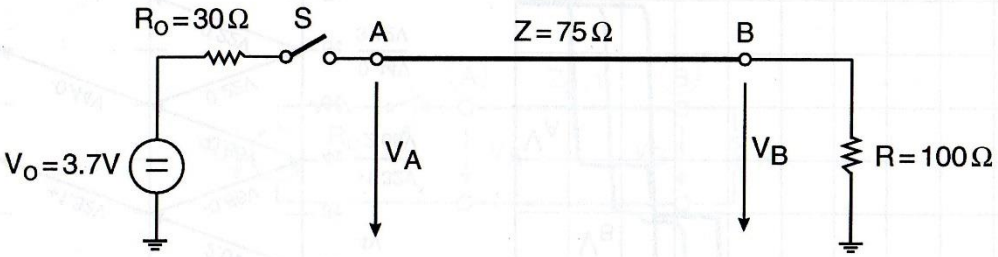
WAVE REFLECTED AT THE GENERATOR OUTPUT

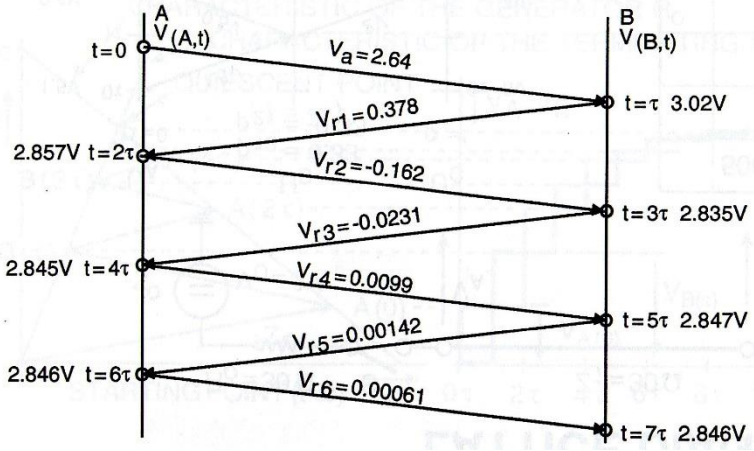
$$V_{r2} = V_{r1} \times \rho_A \qquad \rho_A = \frac{R_o - Z}{R_o + Z}$$

QUIESCENT STATE

$$V_\infty = V_o \frac{R}{R_o + R}$$

LATTICE DIAGRAM





$$\rho_A = \frac{30 - 75}{30 + 75} = -0.429$$

$$\rho_B = \frac{100 - 75}{100 + 75} = 0.143$$

$V_o = 3.70\,V$

$V_a = V_o \times 75\,\Omega / (75\,\Omega + 30\,\Omega) = 2.64$

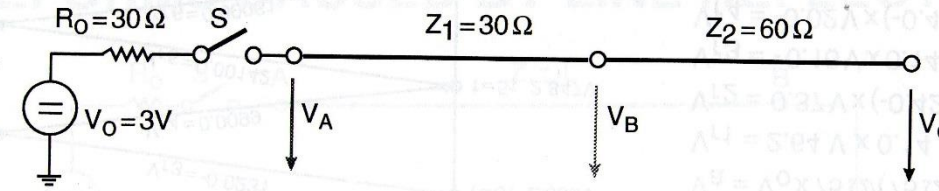
$V_{r1} = 2.64\,V \times 0.14 = 0.37\,V$

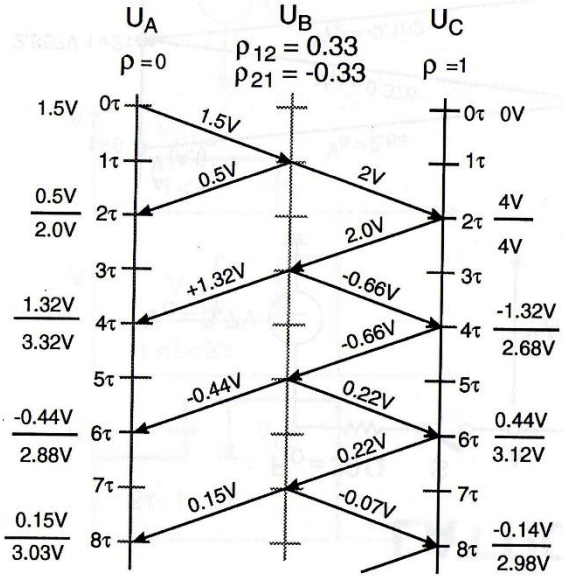
$V_{r2} = 0.37\,V \times (-0.42) = -0.16\,V$

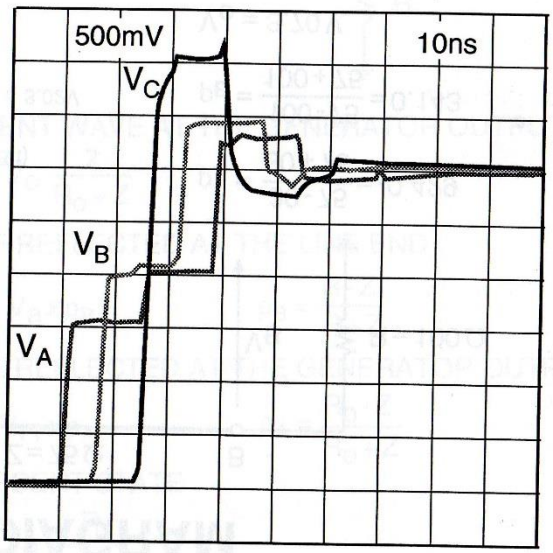
$V_{r3} = -0.16\,V \times 0.14 = -0.02\,V$

$V_{r4} = -0.02\,V \times (-0.42) = 0.009\,V$

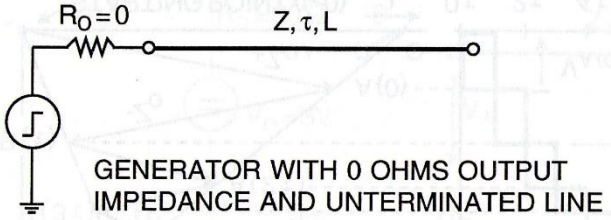
LATTICE DIAGRAM

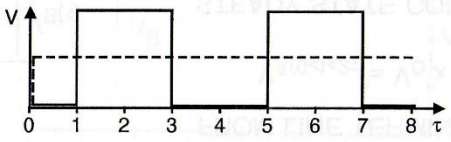


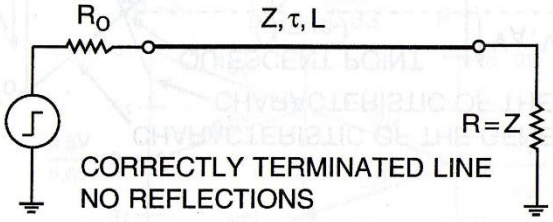


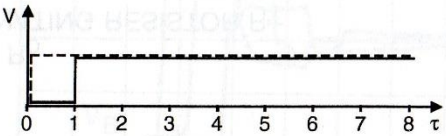


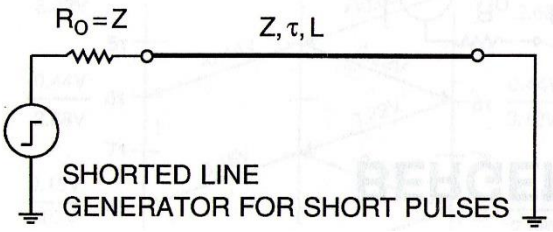
LINE REFLECTIONS - SPECIAL CASES

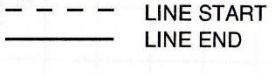


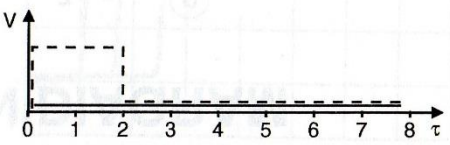




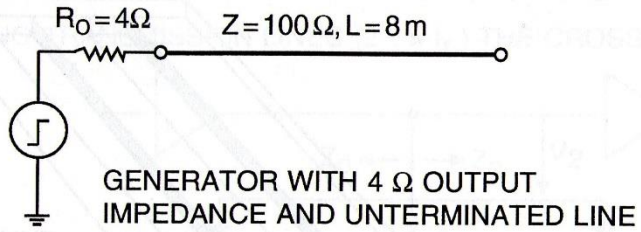




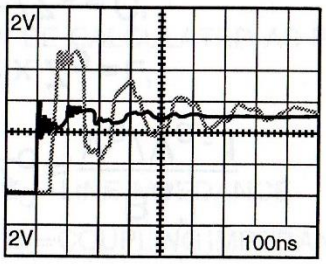


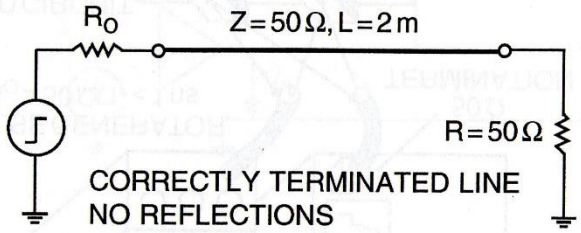


LINE REFLECTIONS - SPECIAL CASES

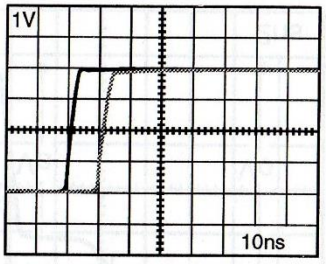


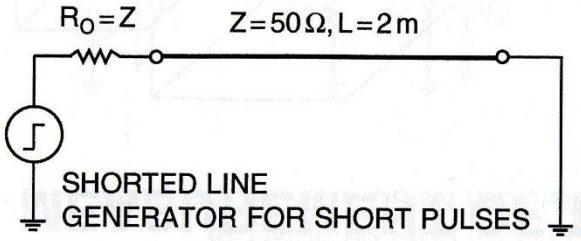
GENERATOR WITH 4 Ω OUTPUT
IMPEDANCE AND UNTERMINATED LINE



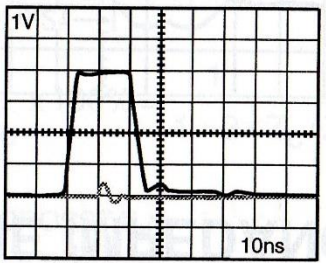


CORRECTLY TERMINATED LINE
NO REFLECTIONS

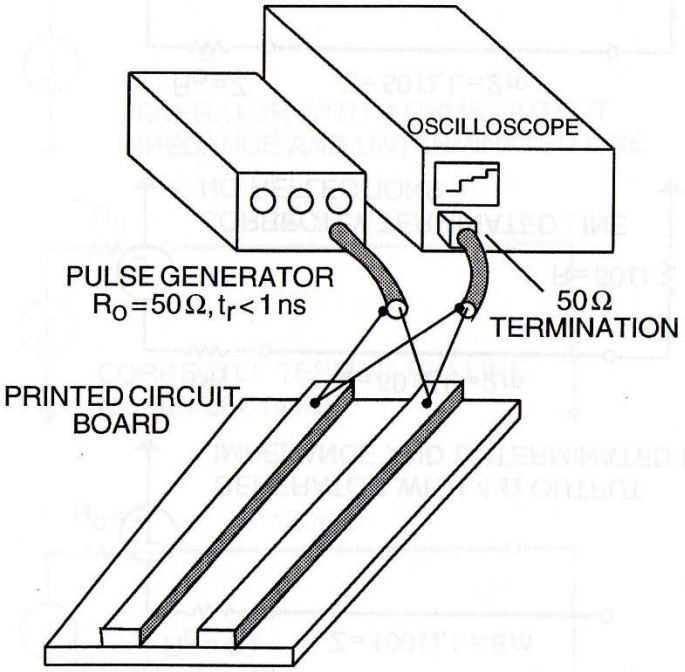


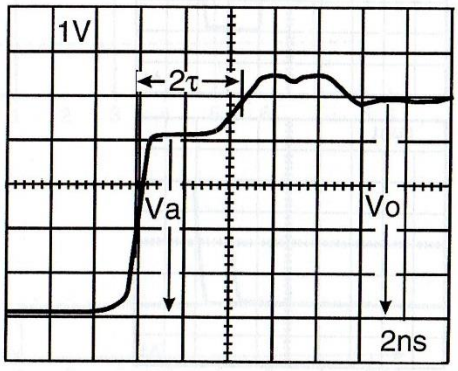


SHORTED LINE
GENERATOR FOR SHORT PULSES



MEASUREMENT OF THE LINE IMPEDANCE





$$Z_O = \frac{R_O{}^{*)}}{V_O/V_a - 1}$$

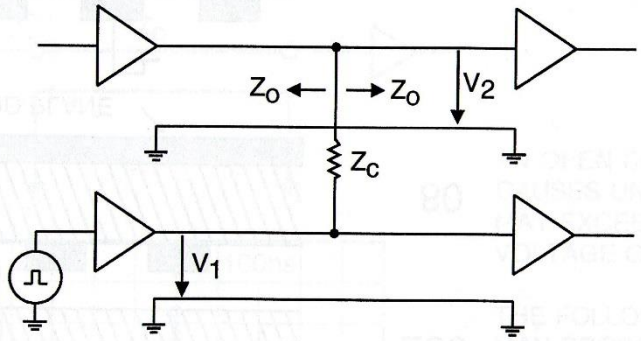
$$\tau \times Z_O = L'$$

$$\tau / Z_O = C'$$

*) NOTE: R_o = 50 Ω // 50 Ω = 25 Ω

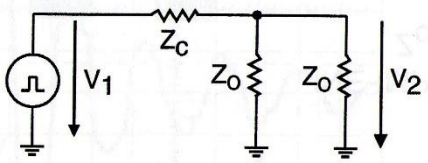
CROSSTALK

ON LONG TRANSMISSION LINES ($2\tau > t_r$) THE CROSSTALK CAN BE CALCULATED AS FOLLOWS:



Z_O = LINE IMPEDANCE

Z_C = COUPLING IMPEDANCE



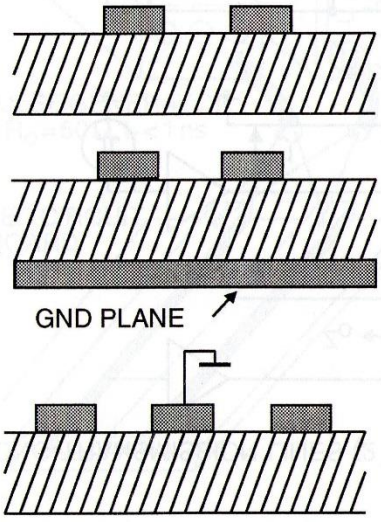
CROSSTALK:

$$C = \frac{V_2}{V_1} \times 100\%$$

$$= \frac{0.5\,Z_O}{0.5\,Z_O + Z_C} \times 100\% = \frac{1}{1 + 2 \times Z_C / Z_O} \times 100\%$$

NOTE: AT THE END OF AN UNTERMINATED LINE CROSSTALK IS TWICE AS HIGH (REFLECTION FACTOR ρ = 1) !

CROSSTALK ON PRINTED CIRCUIT BOARDS (TYPICAL VALUES)



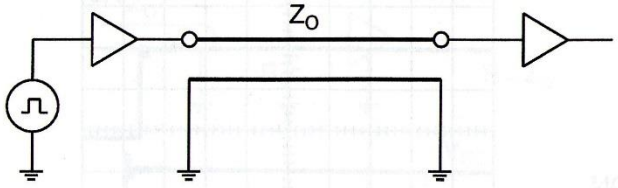
LINE IMPEDANCE Z_O [Ω]	COUPLING IMPEDANCE Z_C [Ω]	CROSSTALK [%]
200	100	50
80	125	25
100	400	11

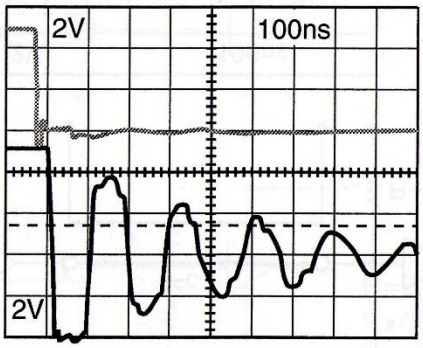
Note: line width = line distance

EH8919/02/018/00/E

LINE REFLECTIONS

OPEN CIRCUIT

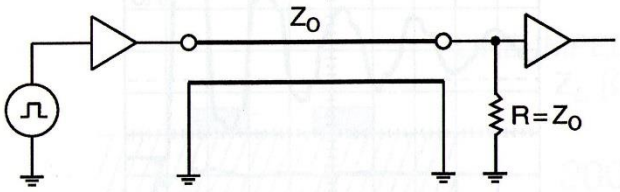


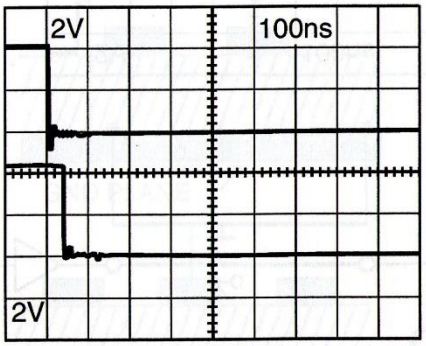


AN OPEN CIRCUIT AT THE LINE END CAUSES UNDER- AND OVERSHOOTS WHICH MAY EXCEED THE MAXIMUM RATED INPUT VOLTAGE OF THE RECEIVING CIRCUIT.

THE FOLLOWING OVER- AND UNDERSHOOTS MAY CROSS THE THRESHOLD VOLTAGE OF THE RECEIVER SEVERAL TIMES AND MAY GENERATE SYSTEM ERRORS.

LINE REFLECTIONS
TERMINATED LINE

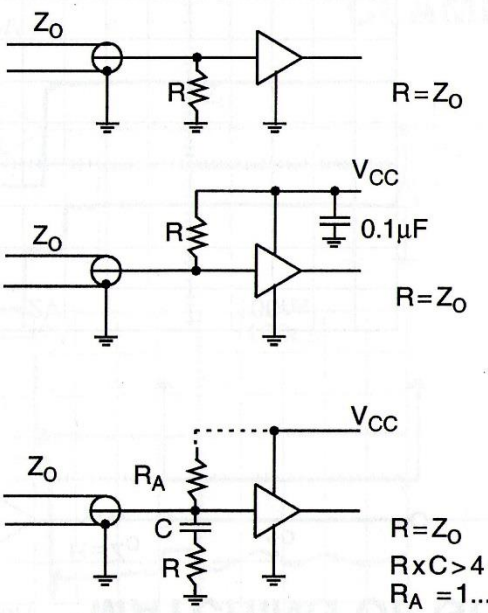


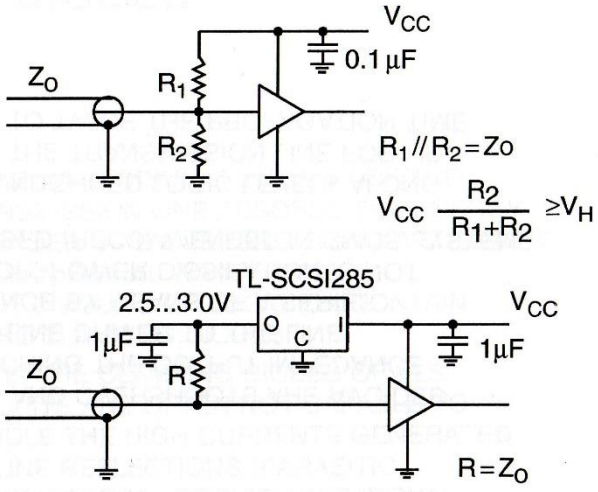


LINE REFLECTIONS ARE ELIMINATED BY A CORRECT LINE TERMINATION.
A MISMATCH UP TO 50% IS ACCEPTABLE.

NOTE: - INCREASED POWER DISSIPATION
- HIGH DRIVE CAPABILITY REQUIRED.

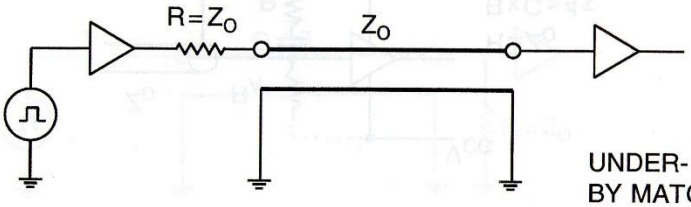
LINE TERMINATION CIRCUITS

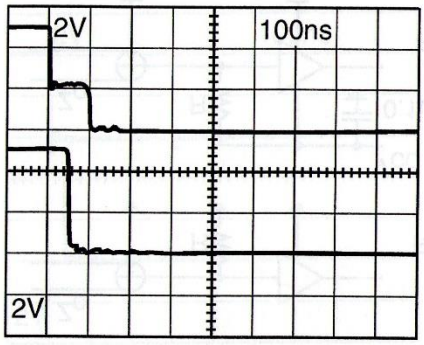




MISMATCH OF 50%...100% ACCEPTABLE
(WITH LOW IMPEDANCE BUS LINES
UP TO 400%).

LINE REFLECTIONS
MATCHING OF GENERATOR IMPEDANCE

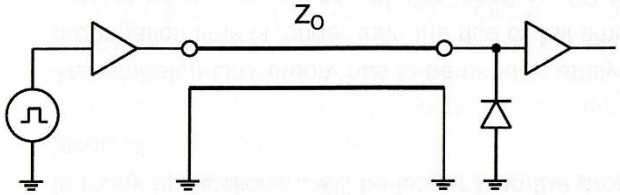


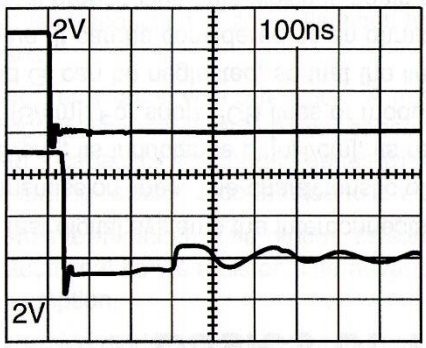


UNDER- AND OVERSHOOTS ARE AVOIDED BY MATCHING THE OUTPUT IMPEDANCE OF THE LINE DRIVER TO THE LINE IMPEDANCE BY MEANS OF A SERIES RESISTOR. POWER DISSIPATION IS NOT INCREASED (RECOMMENDED IN CMOS SYSTEMS).

NOTE: UNDEFINED LOGIC LEVELS ALONG THE TRANSMISSION LINE FOR UP TO TWICE THE PROPAGATION TIME.

LINE REFLECTIONS
CLAMPING DIODES





CLAMPING DIODES AT THE END OF THE TRANSMISSION LINE ABSORBE THE ENERGY OF UNDER- AND OVERSHOOTS AND ENSURE A CLEAN SIGNAL WAVEFORM.
INPUT CIRCUITS OF LOGIC IC's CONTAIN THESE CLAMPING DIODES.

NOTE: THE CLAMPING DIODES OF VLSI CIRCUITS ARE OFTEN NOT CAPABLE TO HANDLE THE HIGH CURRENTS GENERATED BY LINE REFLECTIONS (PARASITIC TRANSISTORS!) . PROVIDE ADDITIONAL SCHOTTKY CLAMPING DIODES!