```
library ieee;
use ieee.std_logic_1164.all;  --take std logic in use

entity ls163 is      --entity with port definitions for ls163
  port (CLK, CLR, ENT, ENP, LOAD: in std_logic; D:in Std_logic_vector (3 downto 0);
  RCO: out std_logic; Q: out std_logic_vector (3 downto 0));
end ls163;

architecture operation of ls163 is  --architecture desription for ls163
function increment_counter (input: std_logic_vector) return std_logic_vector is
  variable result: std_logic_vector (3 downto 0):=input;
  variable carry: std_logic:='1';
  begin
    for index in 0 to 3 loop
       result(index):= result(index) xor carry;  --bitwise incrementing
       carry:=input(index) and carry;
       exit when carry='0';
    end loop;
  return result;
end increment_counter;

begin
  process (CLK)
    variable result: std_logic_vector (3 downto 0) ;
  begin
    if CLK='1' and CLK'event then
       if CLR='0' then result:="0000";
       elsif LOAD='0' then result:=D;
       elsif ENT='1' and ENP='1' then result:=increment_counter(result);
       end if;
    end if;
    Q<=result;
    if result="1111" then RCO<='1';
    else RCO<='0';
    end if;
  end process;
end operation;
```