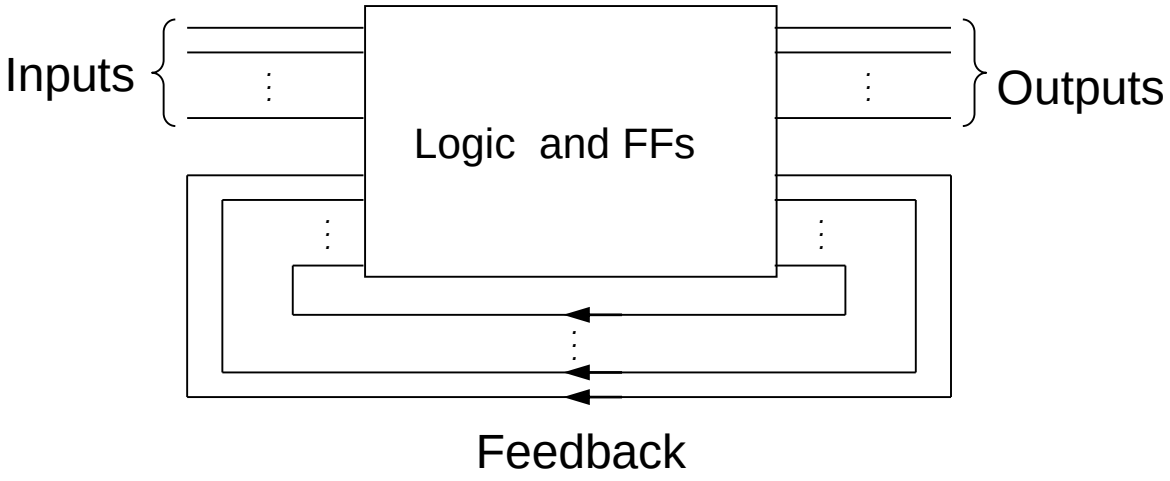
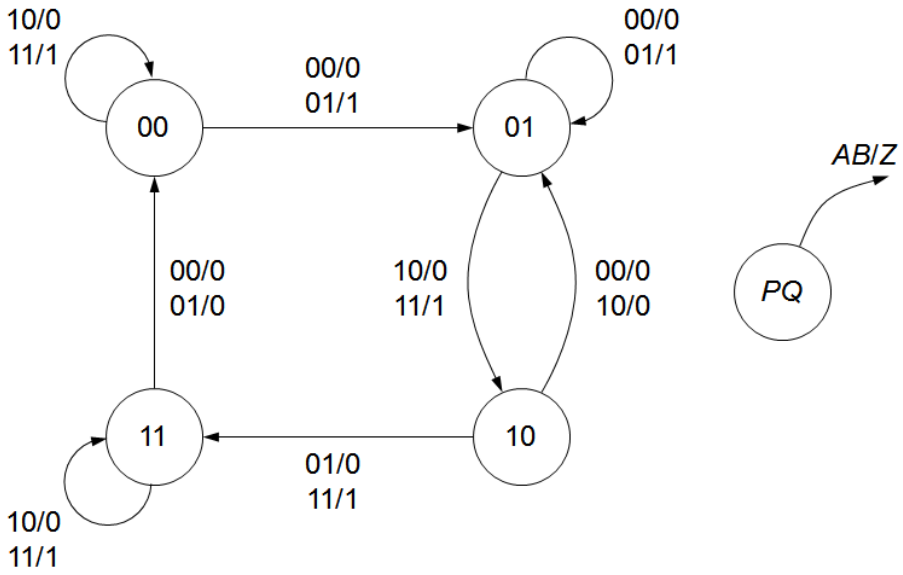
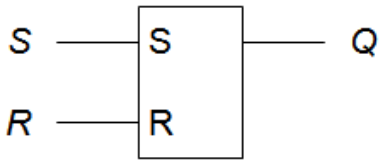
Sequential Logic



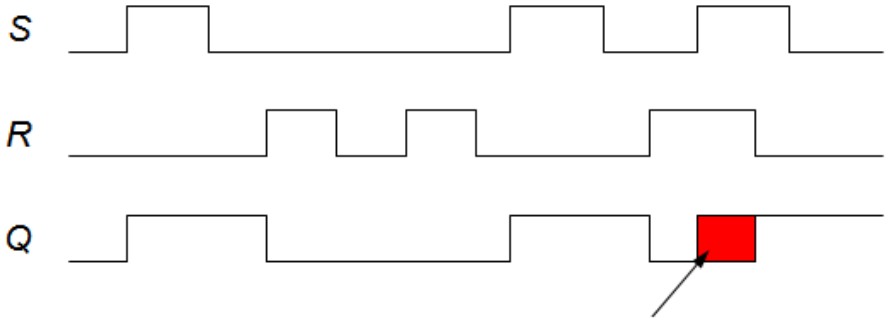
State Diagram



S R Flip Flop

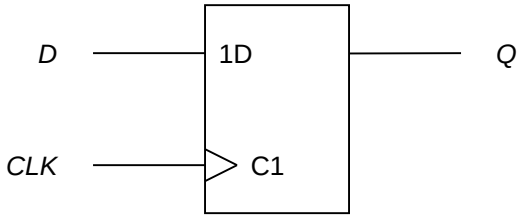


S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	X

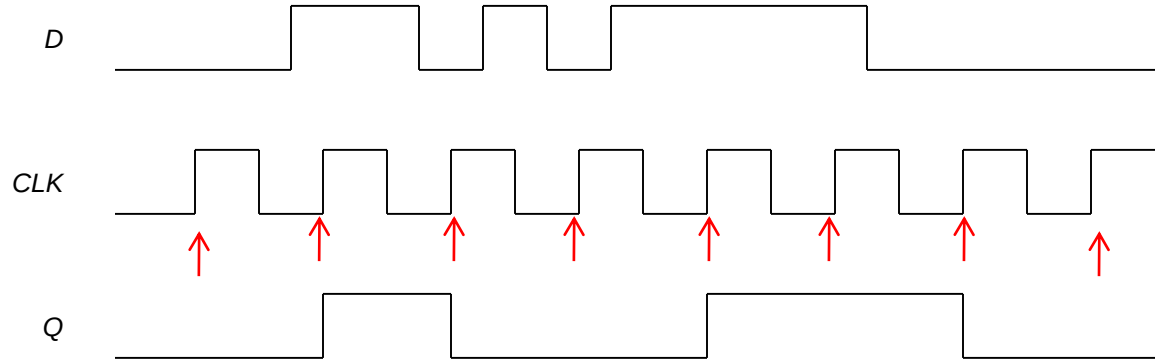


Undefined state

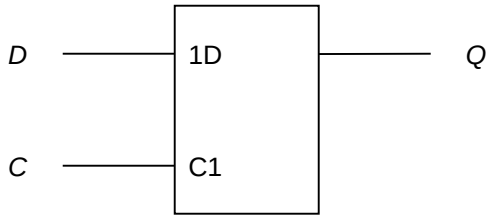
D Flip Flop



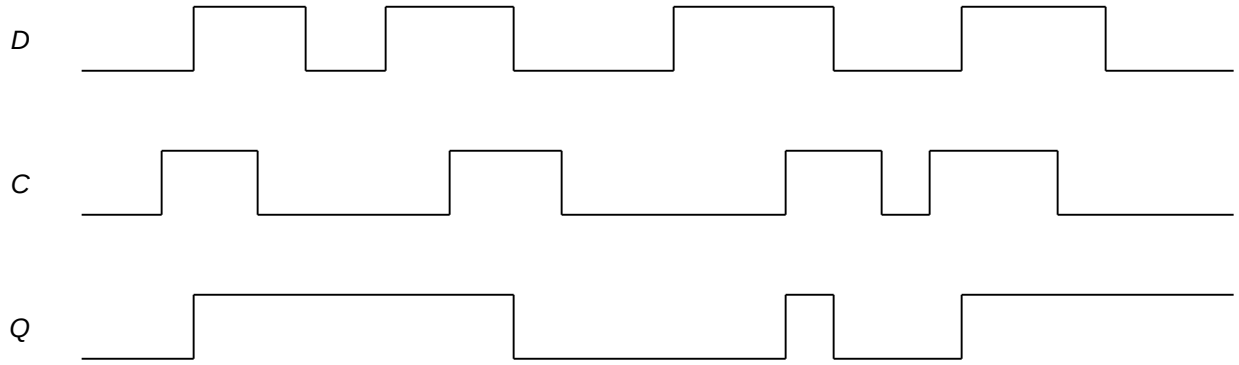
D	Q(t +1)
0	0
1	1



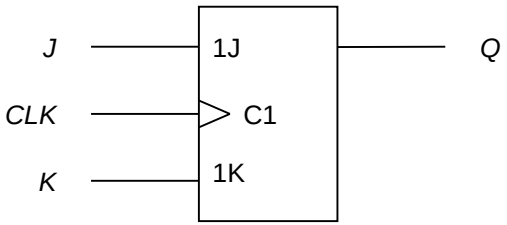
D Latch



C	D	Q(t +1)
0	X	Q(t)
1	0	0
1	1	1

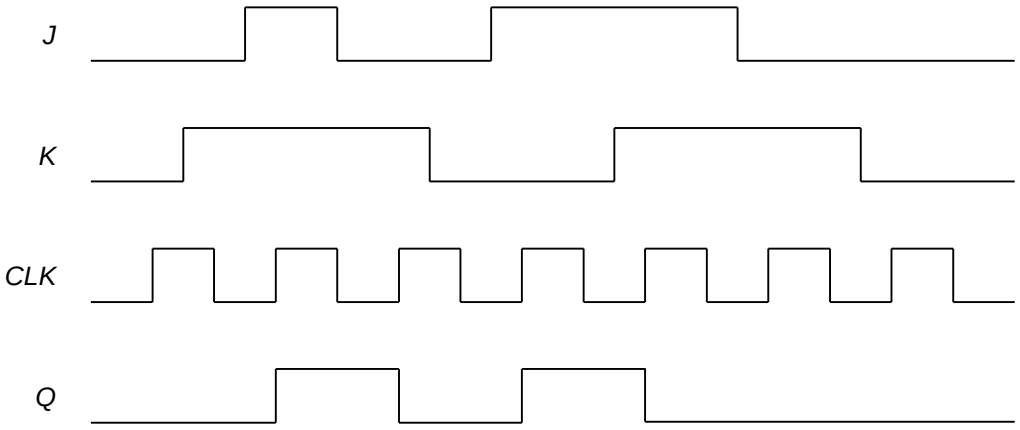


JK Flip Flop

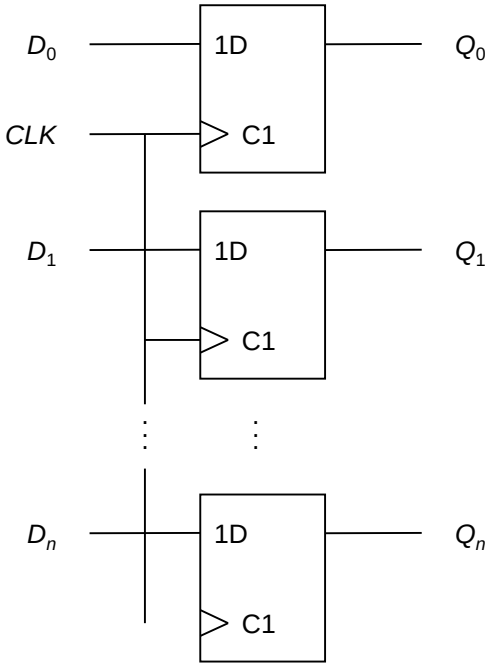


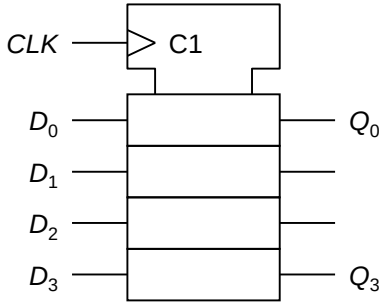
J	K	Q(t +1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

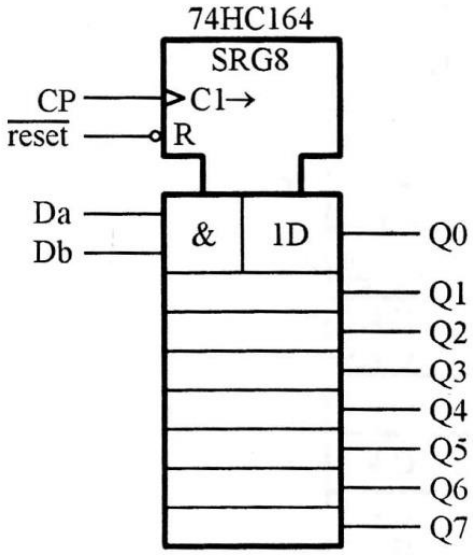


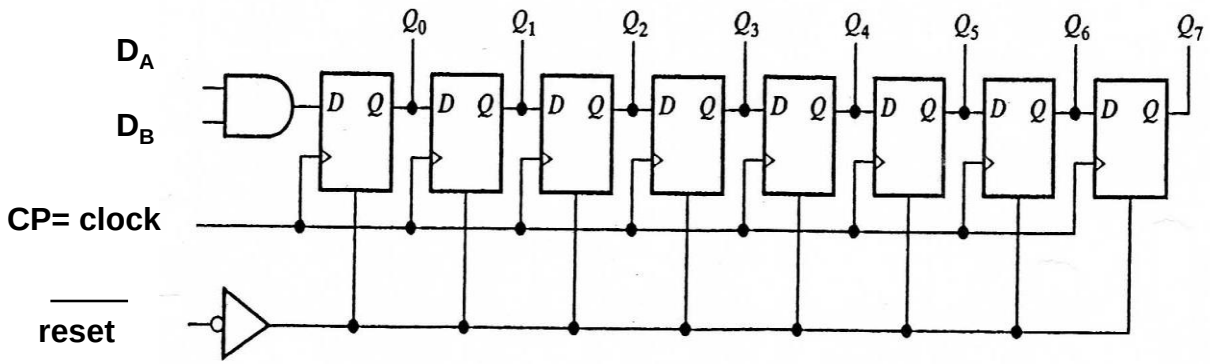
PIPO Register



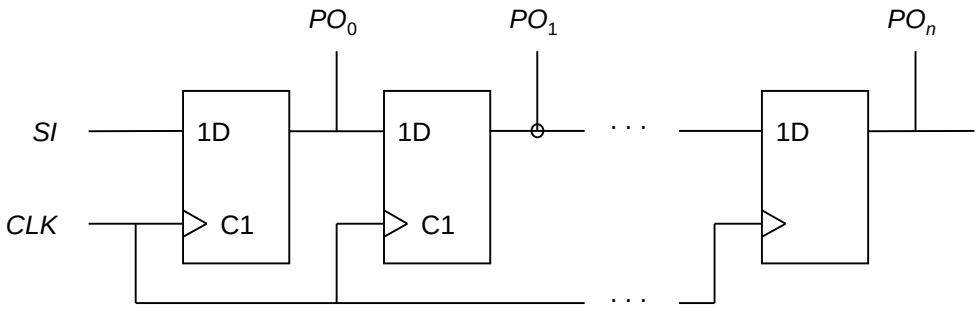


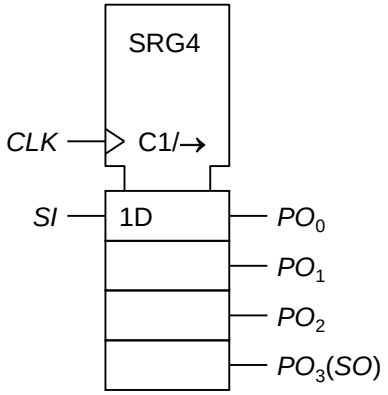
SIPO Register



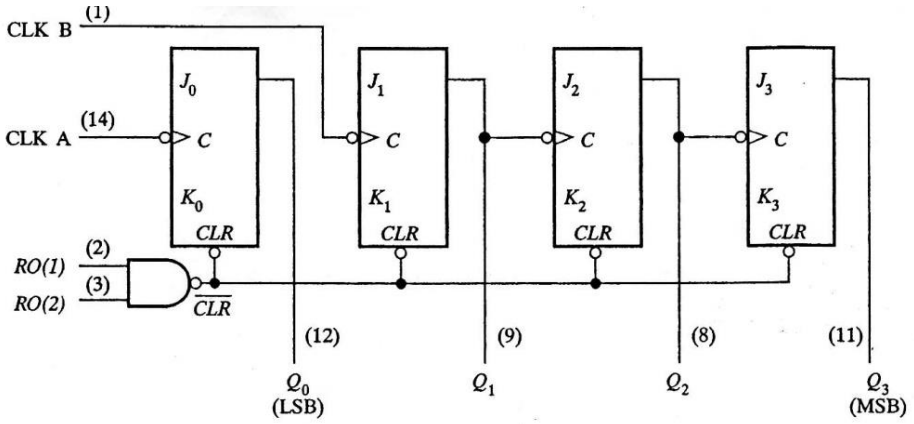


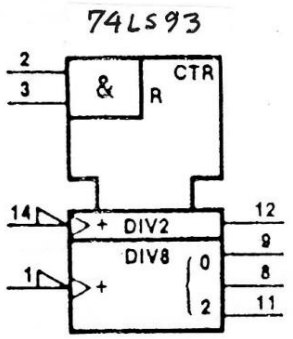
SIPO Register





Counter

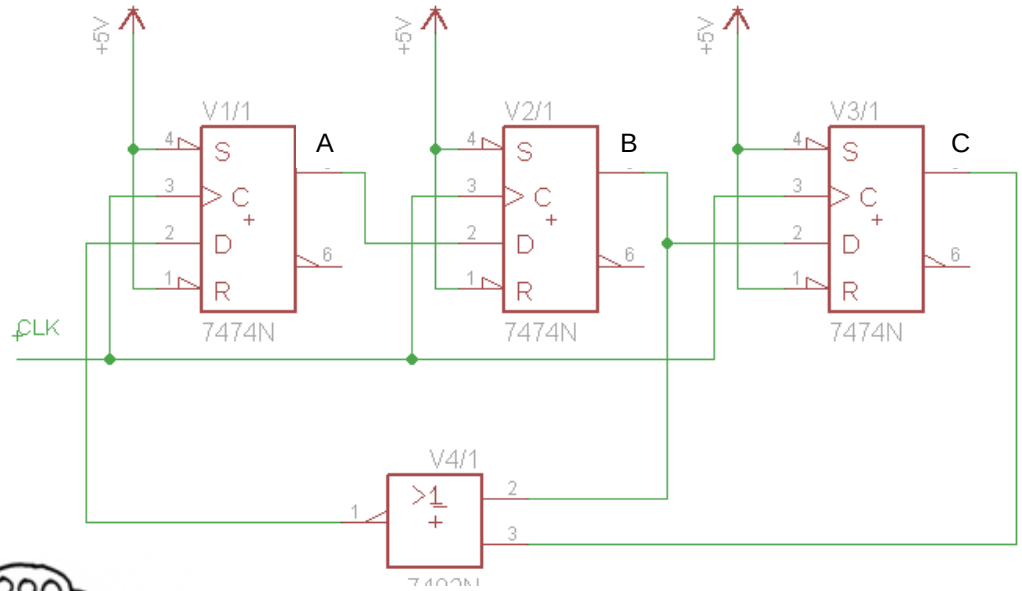


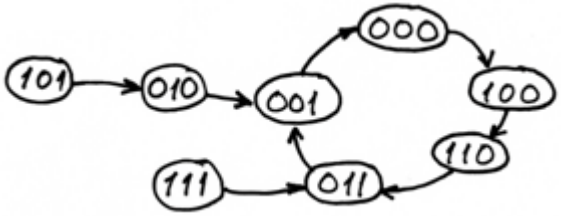


The 74LS93A 4-bit binary counter logic diagram. (Pin numbers are in parentheses, and all J and K inputs are internally connected HIGH.)

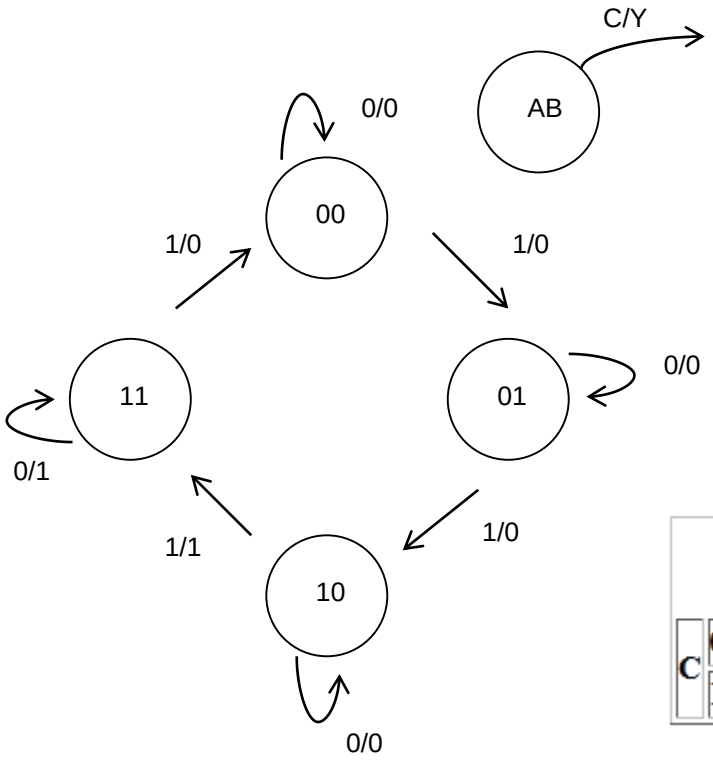
An Example, Find a State Diagram

Current			Next			Next State		
A	B	C	D_A	D_B	D_C	A	B	C
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1
0	1	1	0	0	1	0	0	1
1	0	0	1	1	0	1	1	0
1	0	1	0	1	0	0	1	0
1	1	0	0	1	1	0	1	1
1	1	1	0	1	1	0	1	1





An Example, Design a Circuit



Current st A	B	C	Next Da	Db	Next st A	B	Output Y
0	0	1	0	1	0	1	0
0	1	1	1	0	1	0	0
1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0
0	1	0	0	1	0	1	0
1	0	0	1	0	1	0	0
1	1	0	1	1	1	1	0

Karnaugh Map

C \ AB	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$$Da = A\overline{B} + A\overline{C} + \overline{A}BC$$

Karnaugh Map

C \ AB	00	01	11	10
0	0	1	1	0
1	1	0	0	1

$$Db = B\overline{C} + \overline{B}C$$

Example, Circuit Diagram of Design