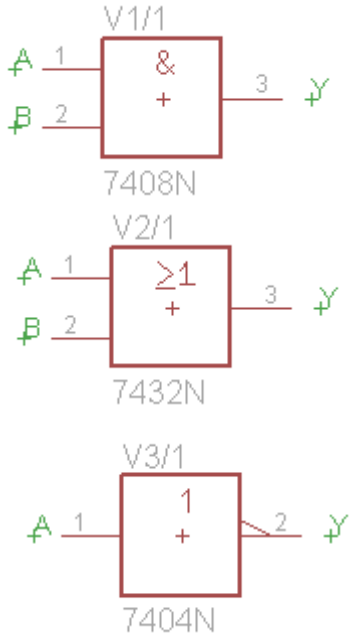
# Boolean Algebra

Basic operations

- AND (AB, A and B are Boolean variables)
- OR (A+B, A and B are Boolean variables)
- NOT (Ē, E is a Boolean variable)

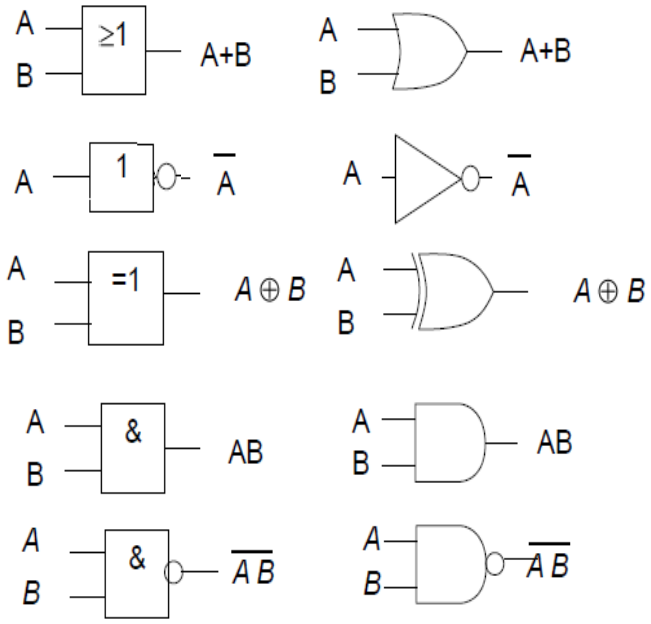



**Truth Table of Basic Operations**

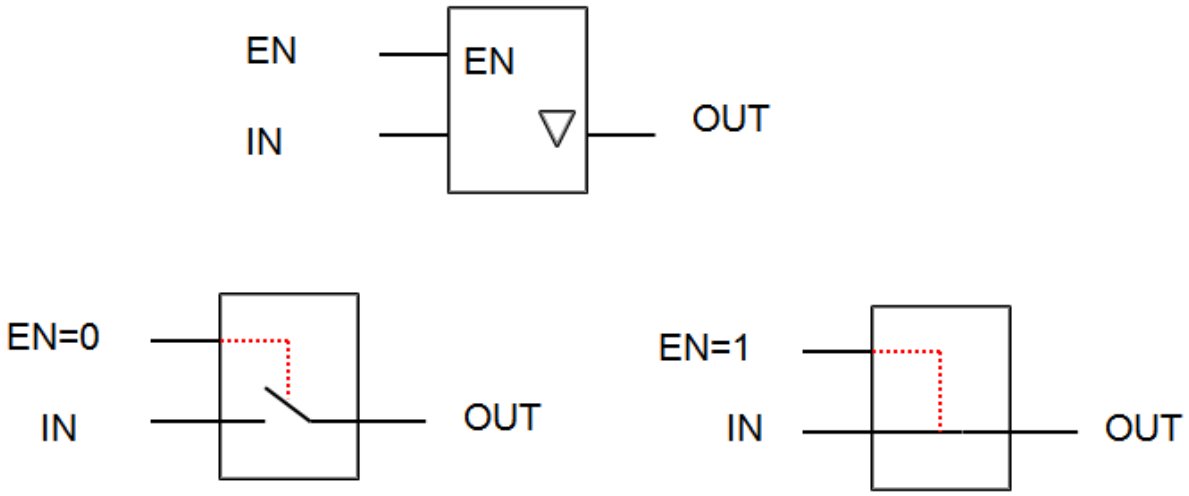
| AND | | | OR | | | NOT | |
|---|---|---|---|---|---|---|---|
| A | B | Y | A | B | Y | A | Y |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 1 | 1 | 1 | | |

# Some Basic Gates

- OR
- NOT
- XOR
- AND
- NAND



# Tri State Output



# Boolean Algebra Rules

$$A + 0 = A$$

$$A \cdot 1 = A$$

$$A + 1 = 1$$

$$A \cdot 0 = 0$$

$$A + A = A$$

$$A \cdot A = A$$

$$\overline{\overline{A}} = A$$

$$A + \overline{A} = 1$$

$$A \cdot \overline{A} = 0$$

$$A \cdot (\overline{A} + B) = A \cdot B$$

$$A + \overline{A} \cdot B = A + B$$

$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

http://en.wikipedia.org/wiki/Boolean_algebra

# Truth Table

- The truth table tells when a given function generates true (=1=H) output value and when false (=0=L) value

Example Truth Table

- 3 inputs (A, B, C)
- 1 output ( Y )

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

# Carnough Map

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Truth Table**

| A | B | C | F(ABC) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Karnaugh Map**

| | | AB | | | |
|---|---|---|---|---|---|
| | | 00 | 01 | 11 | 10 |
| C | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 1 | 0 | 0 |

$F(ABC) = \overline{A}\,B + \overline{A}\,C$

http://en.wikipedia.org/wiki/Karnaugh_map

http://www.ee.calpoly.edu/media/uploads/resources/KarnaughExplorer_1.html



# Carnough Map, 4x4

**Truth Table**

| A | B | C | D | F(ABCD) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Karnaugh Map**

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 0 | 1 |

$$F(ABCD) = B\,\overline{C} + \overline{B}\,C$$

**Truth Table**

| A | B | C | D | F(ABCD) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

**Karnaugh Map**

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 1 | 1 |

$$F(ABCD) = A\,\overline{D} + \overline{B}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D$$

# Logic Families

Logic family name is related to the transistor technology used inside the circuit (BJTs or MOSFETs or both)

- Bipolar: S, LS, AS, ALS, F, ECL,…
- CMOS: 4000, HC, AC, AHC,…
- Combined: BiCMOS

## Physical Components

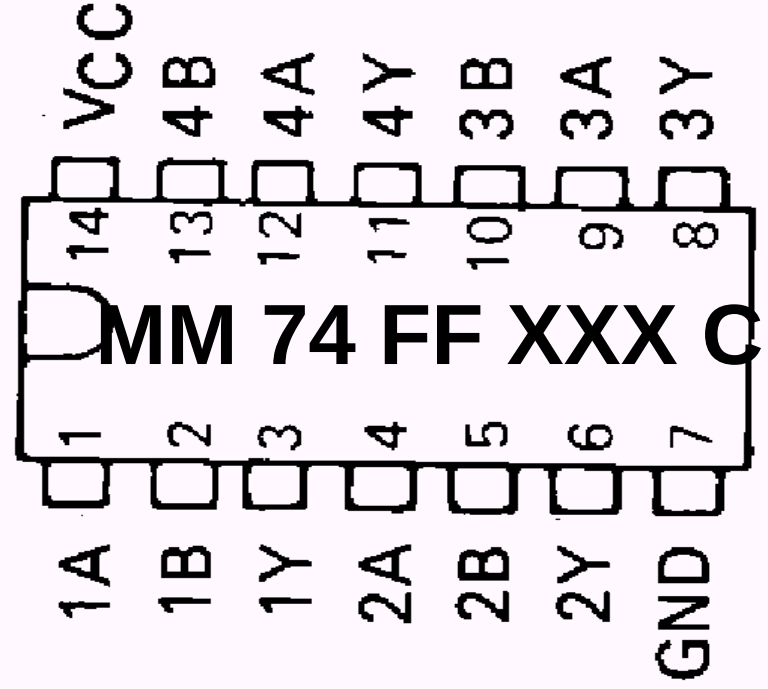
**MM**=Manufacturer, SN=Texas Instruments,…

**74** or **54**, 74=commercial, 54=military

**FF**=Family, HC=High-Speed CMOS, LS=Low-power Schottky, LV=Low Voltage,…

**XXX**=Circuit type, 00=NAND, 138=Decoder (3/8),…

**C**=Capsule, N=DIL, D=SOIC,...



# Key Electrical Parameters

$U_{OH}$, Voltage Output High

$U_{OL}$, Voltage Output Low

$U_{IH}$, Voltage Input High

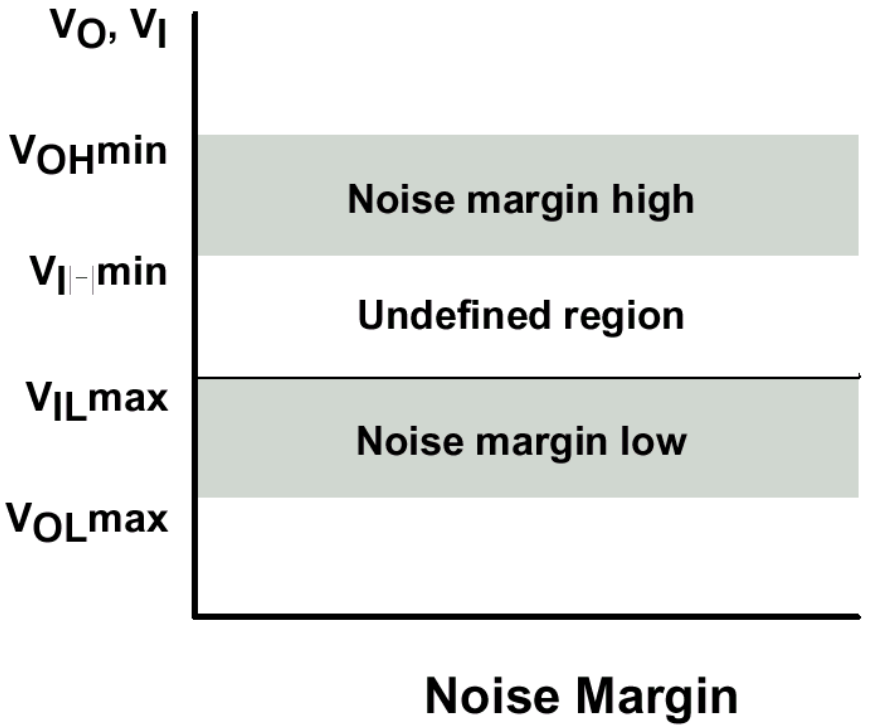
$U_{IL}$, Voltage Input Low

$I_{OH}$, Current Output High

$I_{OL}$, Current Output Low

$I_{IH}$, Current Input High

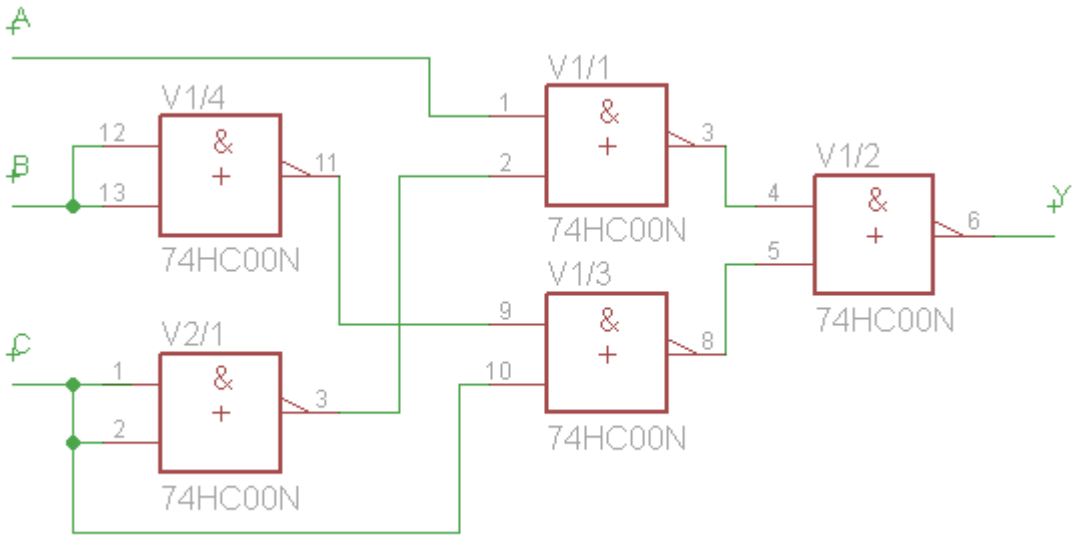
$I_{IL}$, Current Input Low



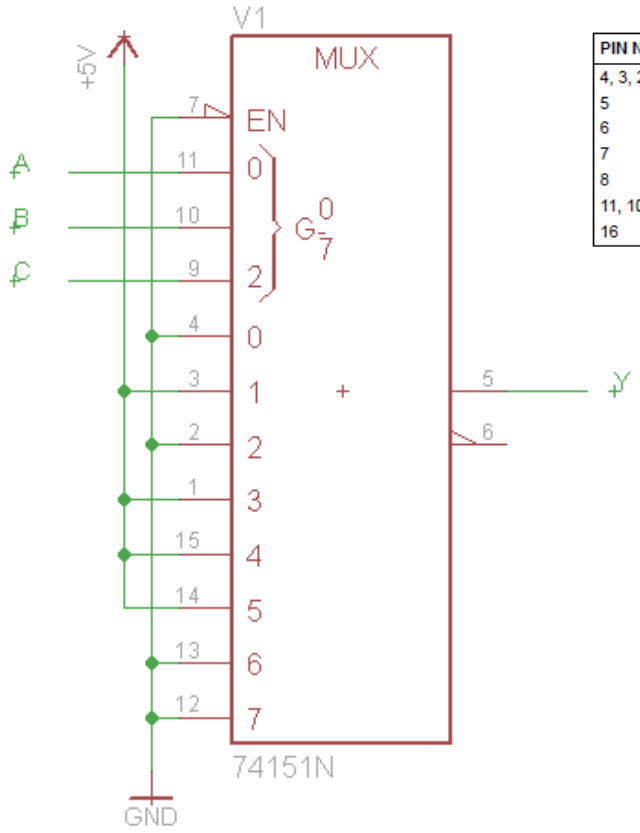
# Example Data of Some Logic Families

| Parameter | LS | HC | ABT | Unit |
|---|---|---|---|---|
| VOH (min) | 2.4 | 4.5 | 2.5 | V |
| VOL (max) | 0.4 | 0.5 | 0.5 | V |
| VIH (min) | 2 | 3.5 | 2 | V |
| VIL(max) | 0.8 | 1.5 | 0.8 | V |
| IOH(max) | 0.4 | 25.0 | 15 | mA |
| IOL(max) | 16 | 25.0 | 20 | mA |
| IIH(max) | 40 | 1 | 1 | μA |
| IIL(max) | 1600 | 1 | 1 | μA |

Example, Design with 2 input NANDs $Y = A\overline{C} + \overline{B}C$



# Example, Design with Mux, $Y = A\overline{C} + \overline{B}C$




| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 4, 3, 2, 1, 15, 14, 13, 12 | $I_0$ to $I_7$ | multiplexer inputs |
| 5 | Y | multiplexer output |
| 6 | $\overline{Y}$ | complementary multiplexer output |
| 7 | $\overline{E}$ | enable input (active LOW) |
| 8 | GND | ground (0 V) |
| 11, 10, 9 | $S_0$, $S_1$, $S_2$ | select inputs |
| 16 | $V_{CC}$ | positive supply voltage |

NCTION TABLE

| INPUTS | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | $S_2$ | $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $\overline{Y}$ | Y |
| H | X | X | X | X | X | X | X | X | X | X | X | H | L |
| L | L | L | L | L | X | X | X | X | X | X | X | H | L |
| L | L | L | L | H | X | X | X | X | X | X | X | L | H |
| L | L | L | H | X | L | X | X | X | X | X | X | H | L |
| L | L | L | H | H | X | X | X | X | X | X | X | L | H |
| L | L | H | L | X | X | L | X | X | X | X | X | H | L |
| L | L | H | L | X | X | H | X | X | X | X | X | L | H |
| L | L | H | H | X | X | X | L | X | X | X | X | H | L |
| L | L | H | H | X | X | X | H | X | X | X | X | L | H |
| L | H | L | L | X | X | X | X | L | X | X | X | H | L |
| L | H | L | L | X | X | X | X | H | X | X | X | L | H |
| L | H | L | H | X | X | X | X | X | L | X | X | H | L |
| L | H | L | H | X | X | X | X | X | H | X | X | L | H |
| L | H | H | L | X | X | X | X | X | X | L | X | H | L |
| L | H | H | L | X | X | X | X | X | X | H | X | L | H |
| L | H | H | H | X | X | X | X | X | X | X | L | H | L |
| L | H | H | H | X | X | X | X | X | X | X | H | L | H |

tes

H = HIGH voltage level
L = LOW voltage level
X = don't care.