CMOS Fabrication Process in Deep-Submicron (DSM) and Ultra Deep-Submicron (UDSM) Technology

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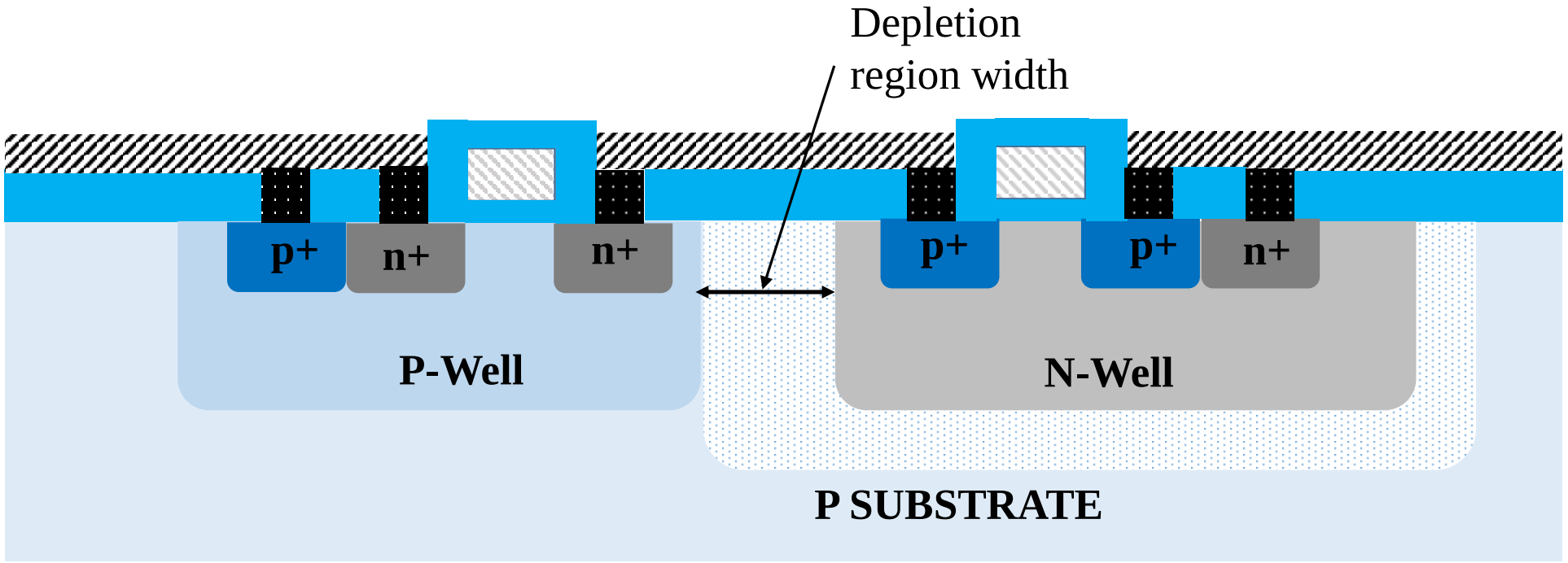
Disadvantage of the Submicron CMOS Process

Isolation of the Transistors:

- The use of reverse bias pn junctions to isolate transistors becomes impractical as the transistor sizes decrease.



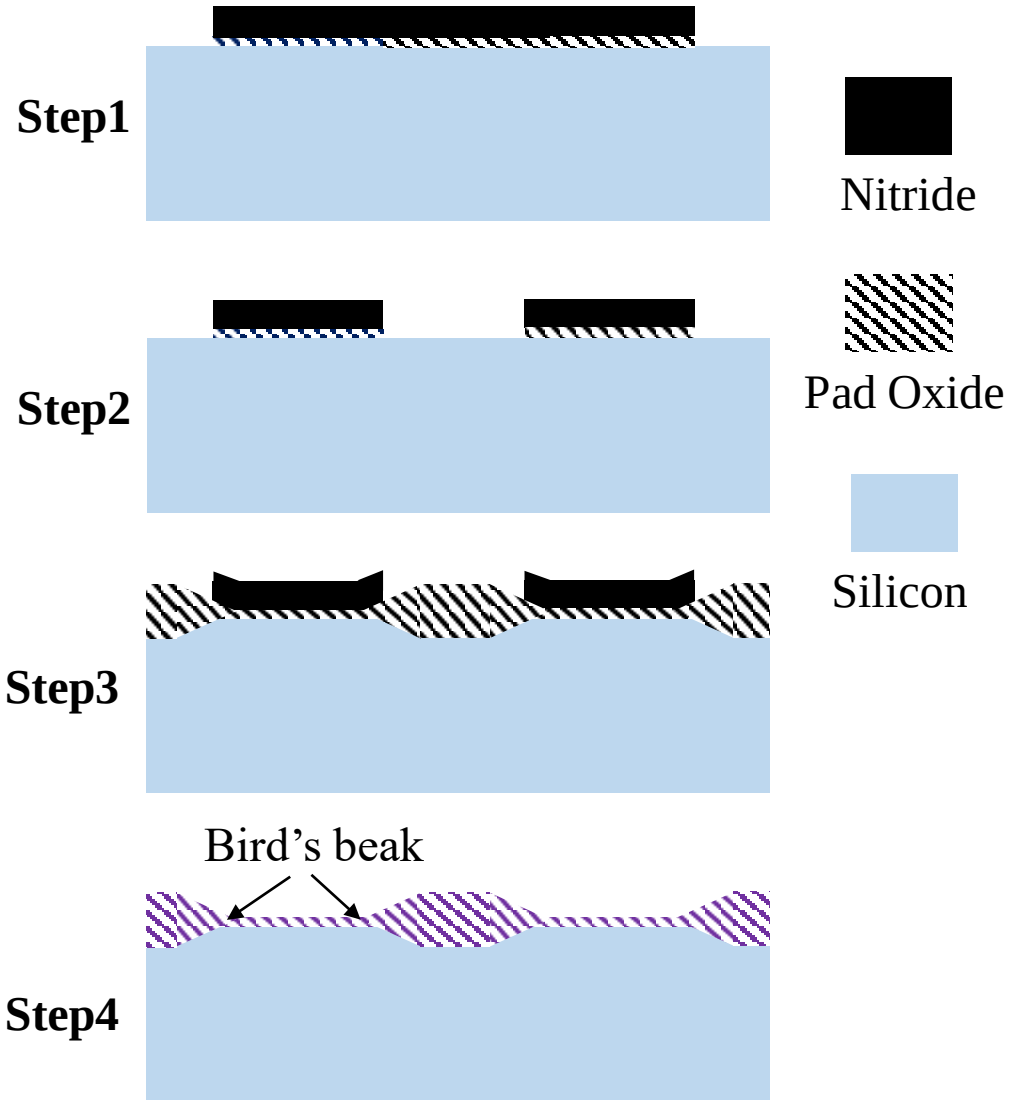
Local Oxidation of Silicon (LOCOS) Isolation Process

Local Oxidation of Silicon (LOCOS):

- Local Oxidation of Silicon is the traditional isolation technique used in submicron processes.

1) A very thin layer silicon dioxide is grown on the wafer, called as pad oxide. Then a layer of silicon nitride is deposited which is used as an oxide barrier.
2) Then photolithography is done to pattern and etch the nitride and pad oxide where the thick oxide will be grown
3) Then by thermal oxidation process thick oxide is grown in the exposed area.
4) The last step is the removal of the silicon nitride layer.

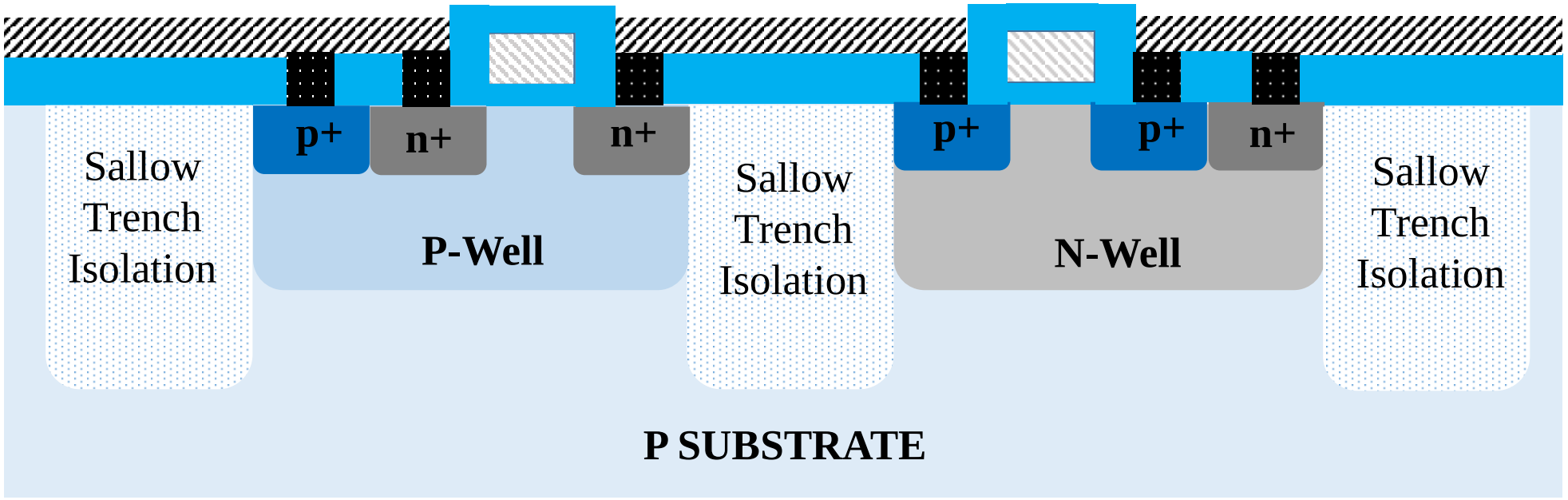
- The limitation of this technique is the bird's beak effect and the surface area which is lost to this encroachment.
- The advantages of LOCOS fabrication process is simple process flow and high oxide quality because the whole LOCOS structure is thermally grown.



Sallow Trench Isolation Technology

Use of Sallow Trench Isolation Technology:

- Shallow trench isolation (STI) allows closer spacing of transistors by eliminating the depletion region at the surface and Bird's beak effect due to LOCOS process.



Sallow Trench Isolation Process

Sallow Trench Isolation:

- Sallow Trench Isolation (STI) isolation process is the preferred isolation process for deep-submicron process because it completely avoids Bird's beak shape characteristics.

1) Cover the wafer with pad oxide and silicon nitride.
2) First etch nitride and pad oxide. Next, an anisotropic etch is made in the silicon to a depth of 0.4 to 0.5 microns.
3) Grow a thin thermal oxide layer on the trench walls.
4) A CVD dielectric film is used to fill the trench.
5) A chemical mechanical polishing (CMP) step is used to polish back the dielectric layer until the nitride is reached. The nitride acts like a CMP stop layer.
6) Densify the dielectric material at 900°C and strip the nitride and pad oxide.

- STI is more suitable for the increased density in a small area because it allows forming smaller isolation regions.
- The disadvantage is larger number of process steps.

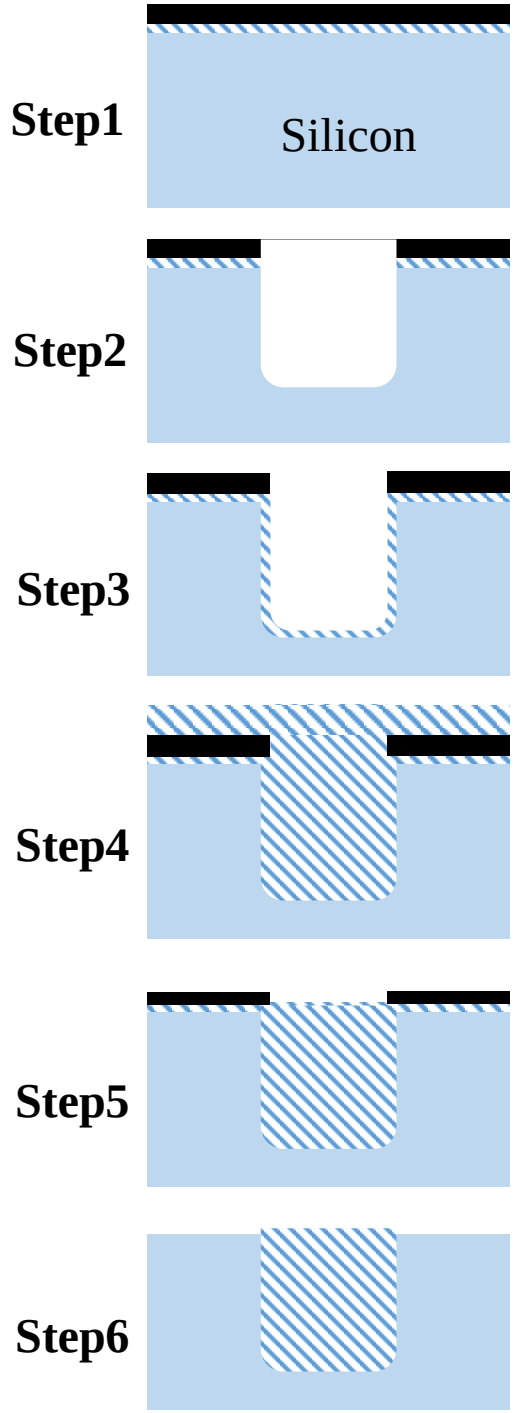


Illustration of a Deep Submicron (DSM) CMOS Technology

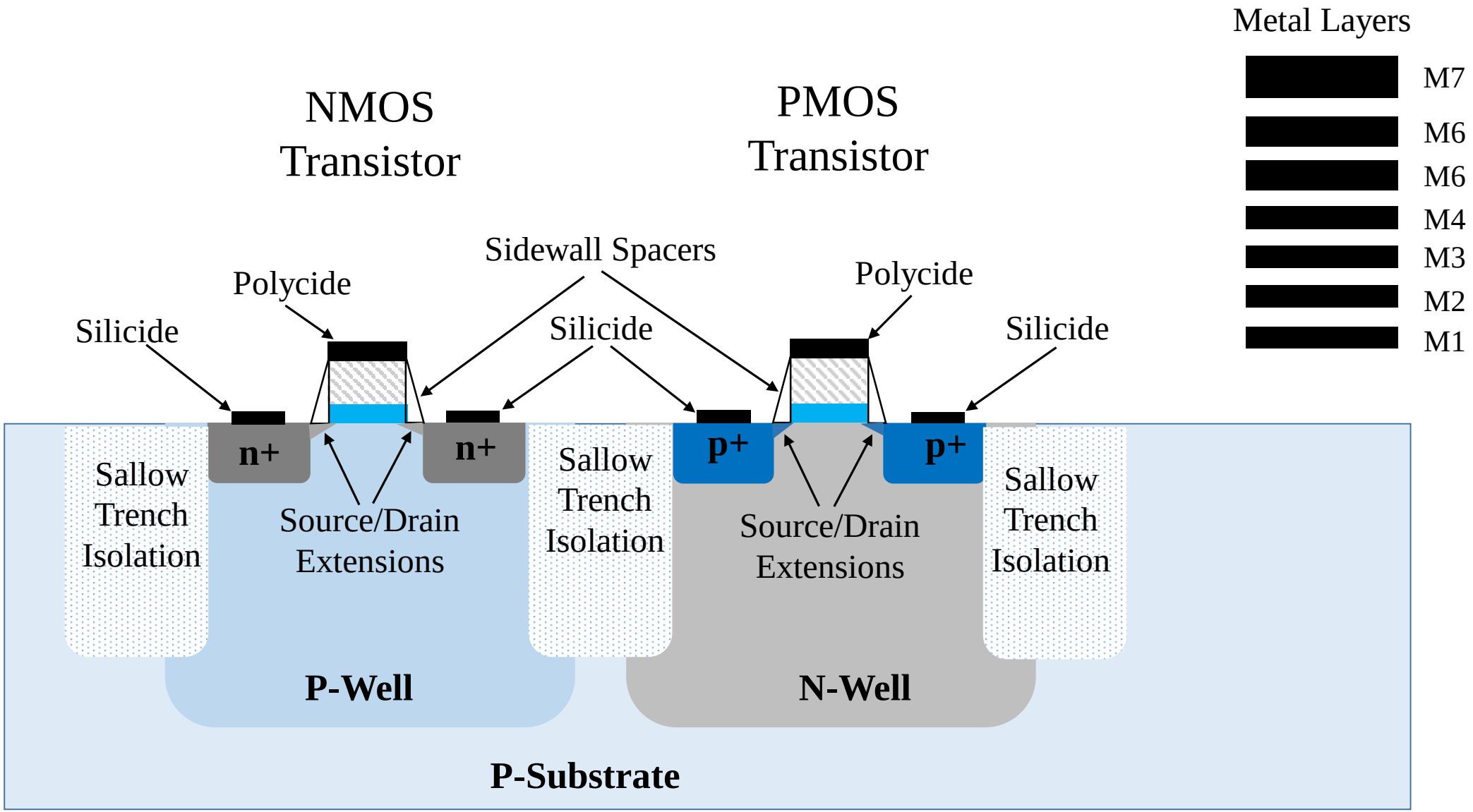
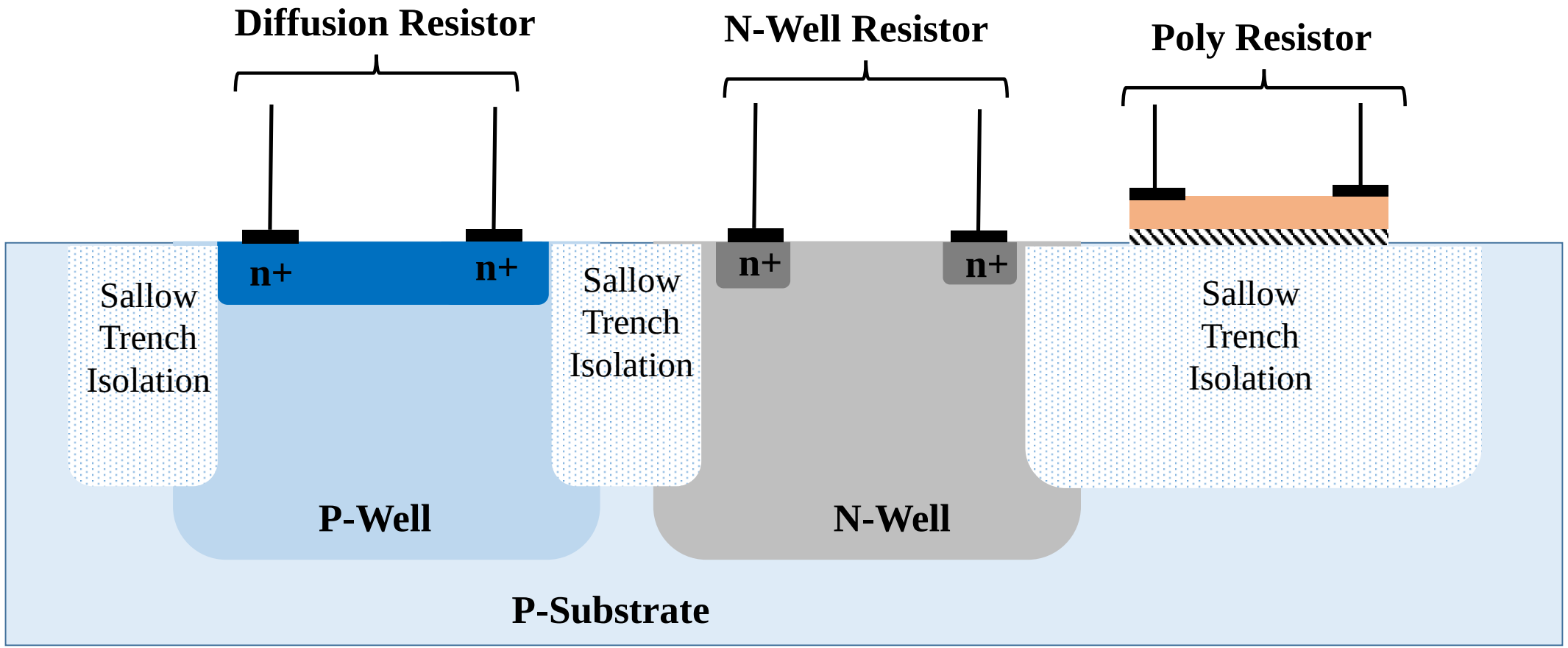


Illustration of a Deep Submicron (DSM) CMOS Technology

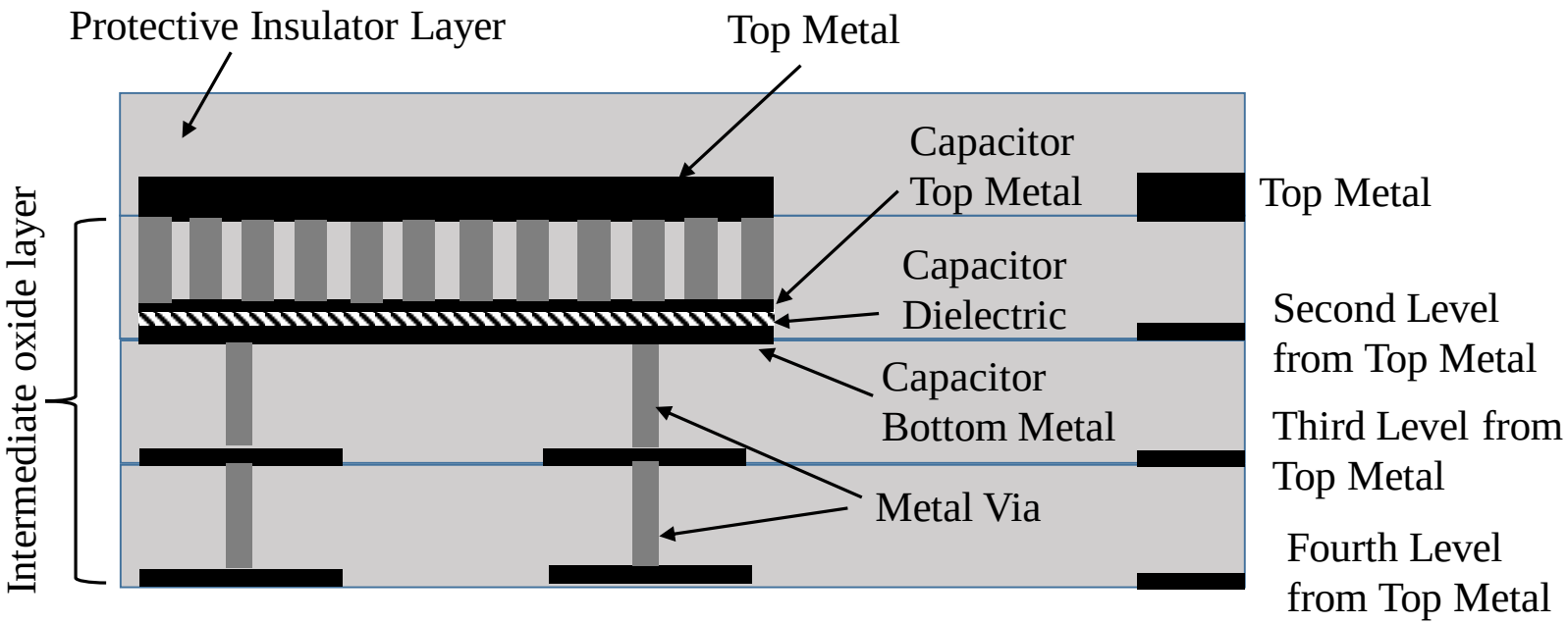
In addition to the NMOS and PMOS transistor, the DSM technology provides;

- A deep n-well that can be utilized to reduce substrate noise coupling.
- A MOS Varactor that can be used to make voltage controlled oscillators (VCOs).
- Different kind of resistors like,
  - Diffused and/or implanted resistors
  - Well resistors
  - Poly resistors
  - Metal Resistors
- At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

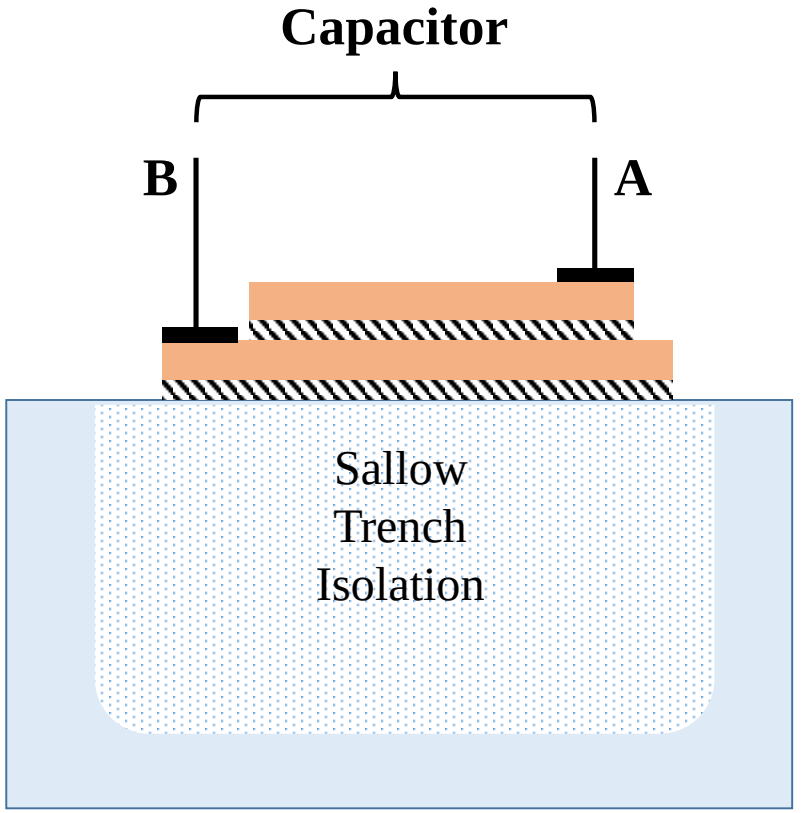
Different Types of Resistor in Deep Submicron (DSM) CMOS Technology



Different Types of Capacitor in Deep Submicron (DSM) CMOS Technology

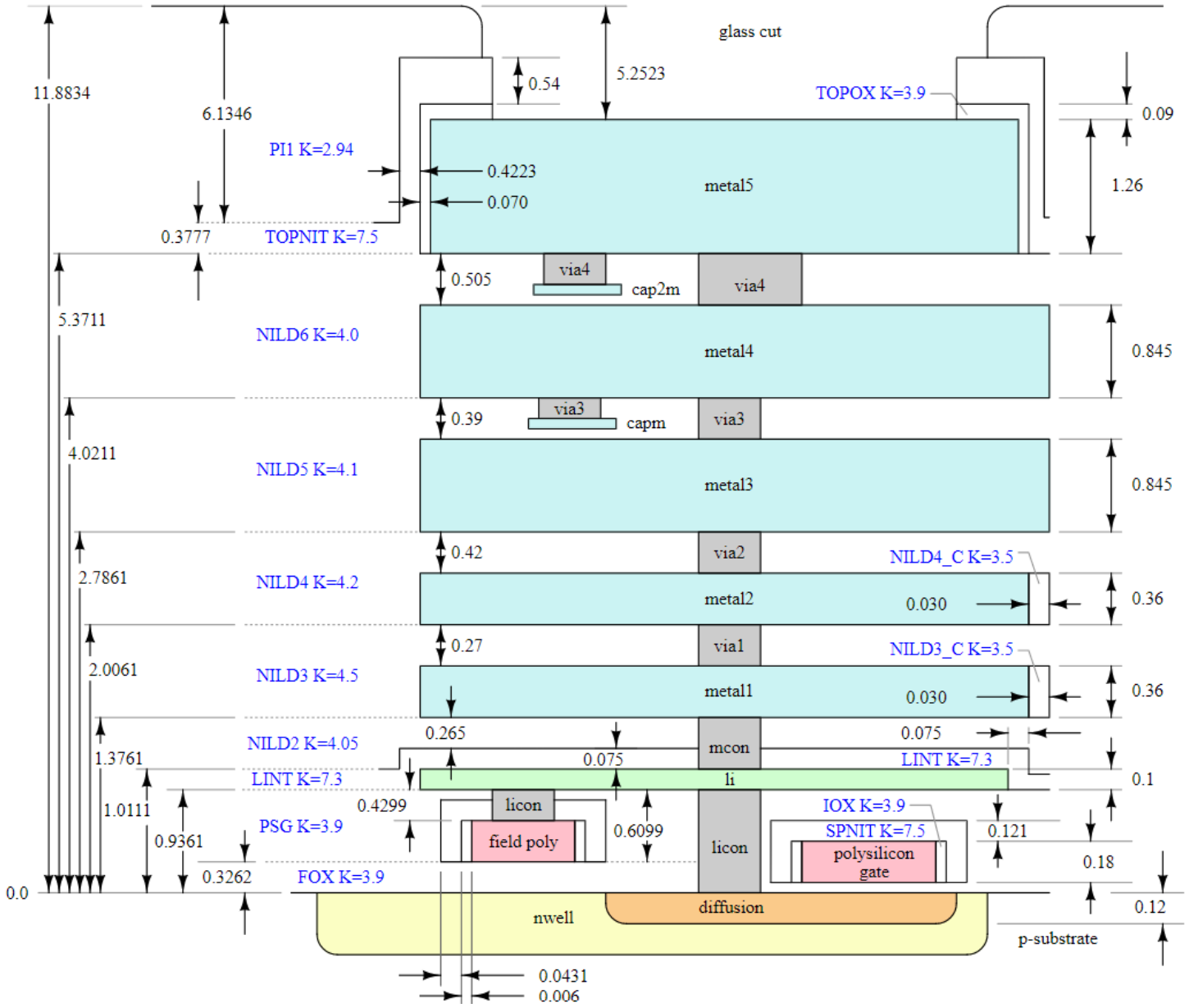


Metal-Insulator-Metal (MIM) Capacitor



Polysilicon-Polysilicon Capacitor

Example of a DSM Technology Process (SKY130)



Typical Deep Submicron (DSM) CMOS Fabrication Process

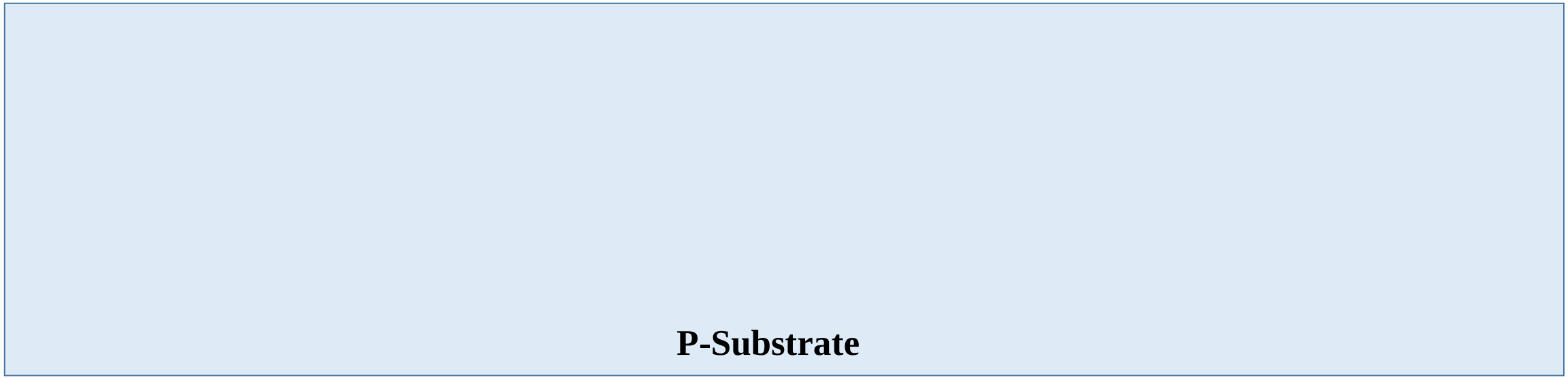
Major Fabrication Steps for a DSM CMOS Process

1) p and n wells
2) Shallow trench isolation
3) Threshold shift and anti-punch through implants
4) Thin oxide and gate polysilicon
5) Lightly doped drains and sources
6) Sidewall spacer
7) Heavily doped drains and sources
8) Siliciding (Salicide and Polycide)
9) Bottom metal, tungsten plugs, and oxide
10) Higher level metals, tungsten plugs/vias, and oxide
11) Top level metal, vias and protective oxide

Deep Submicron (DSM) CMOS Fabrication Process

Starting Material

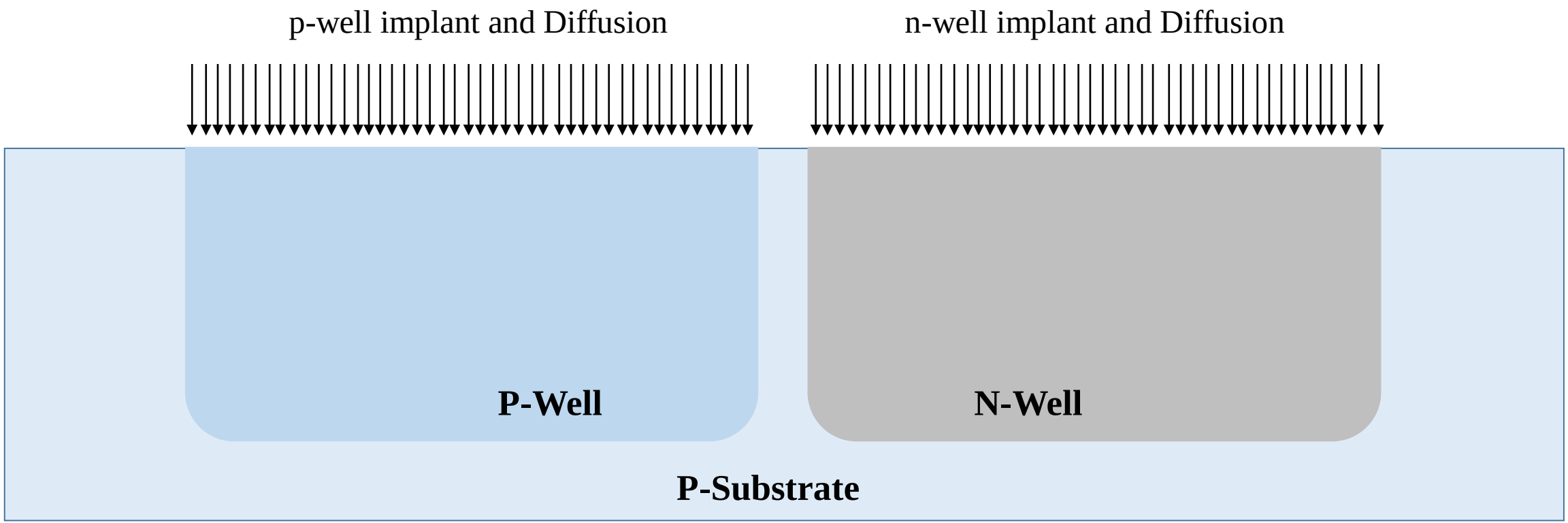
- The substrate should be highly doped to act like a good conductor.



Deep Submicron (DSM) CMOS Fabrication Process

Step-1: n and p-well Creation

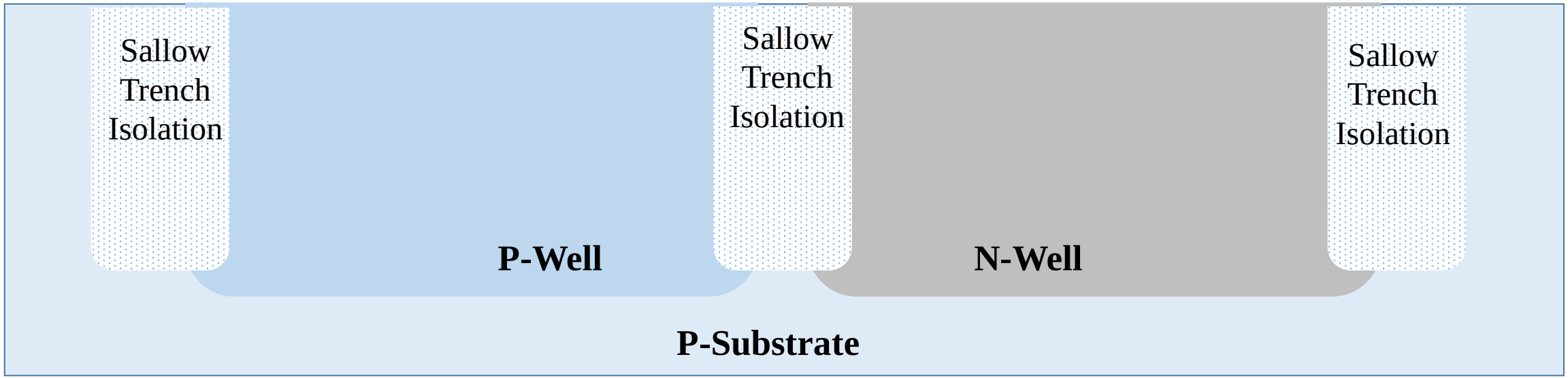
- These are the areas where the transistors will be fabricated - NMOS in the p-well and PMOS in the n-well.
- Done by implantation followed by a deep diffusion.



Deep Submicron (DSM) CMOS Fabrication Process

Step-2: Sallow Trench Isolation

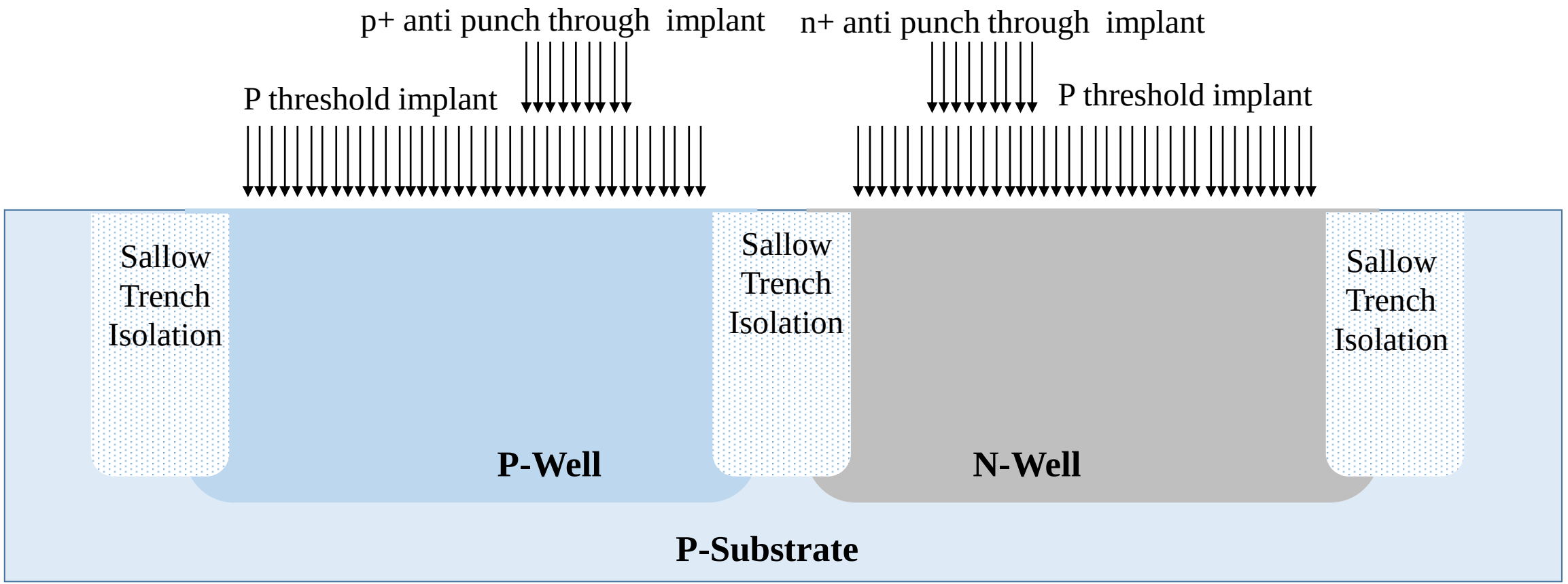
- The shallow trench isolation (STI) electrically isolates one region/transistor from another.



Deep Submicron (DSM) CMOS Fabrication Process

Step-3: Threshold Shift and Anti-Punch through Implants

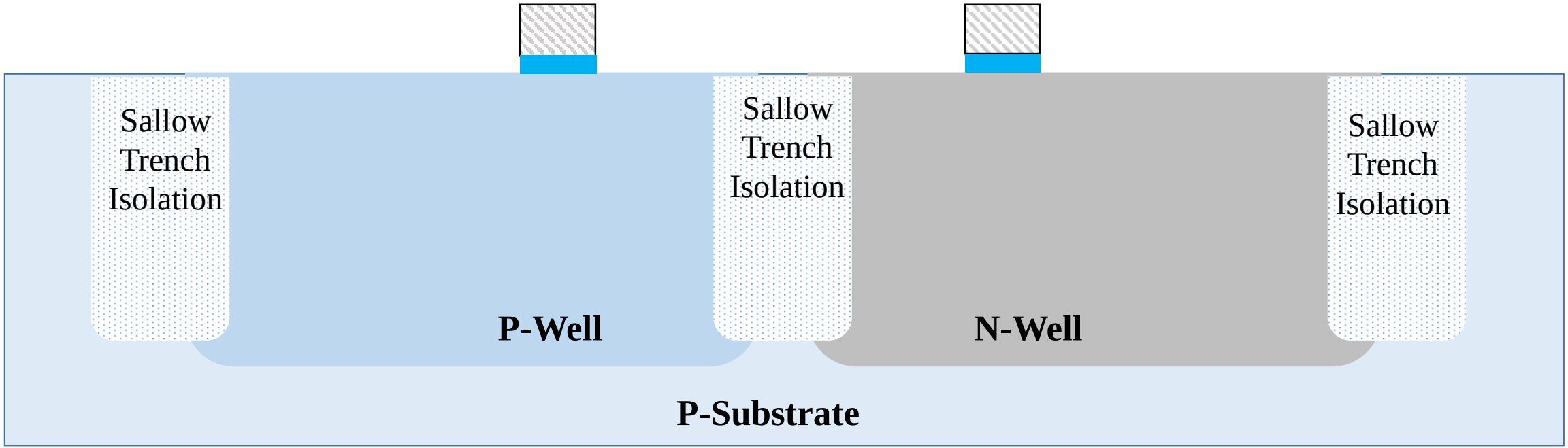
- The natural thresholds of the NMOS is about 0V and of the PMOS is about –1.2V. An p-implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.
- Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.



Deep Submicron (DSM) CMOS Fabrication Process

Step-4: Thin Oxide and Polysilicon Gate

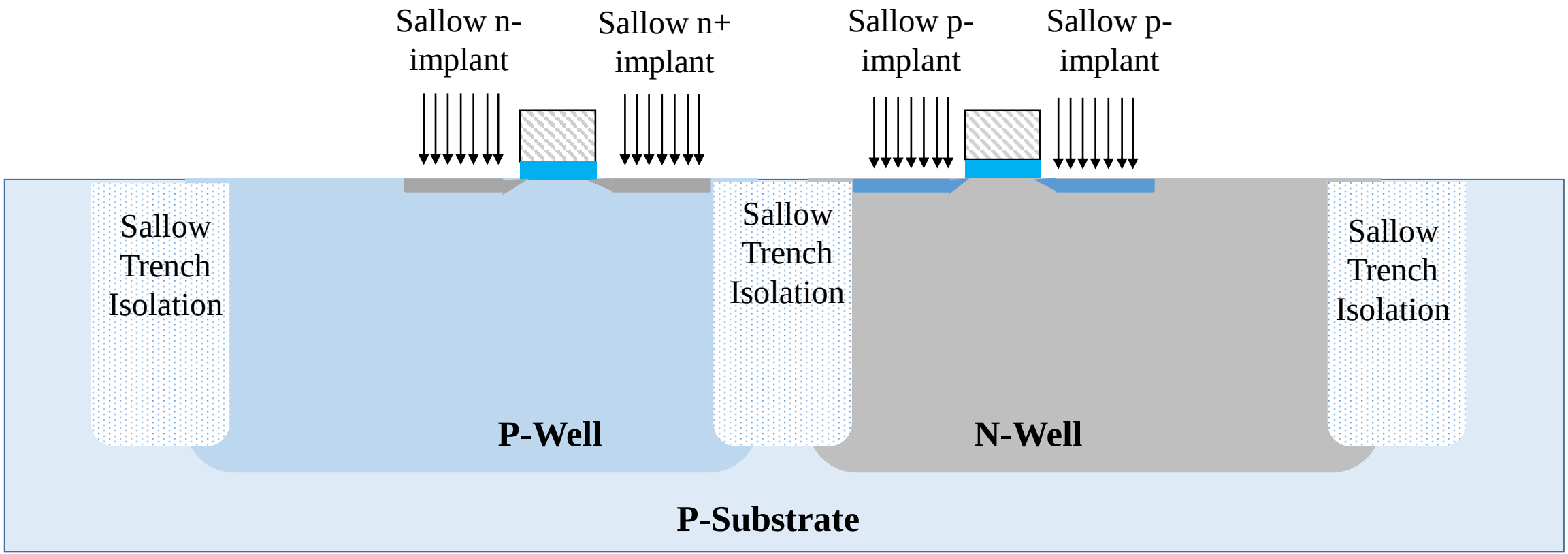
- A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.



Deep Submicron (DSM) CMOS Fabrication Process

Step-5: Lightly Doped Source and Drain

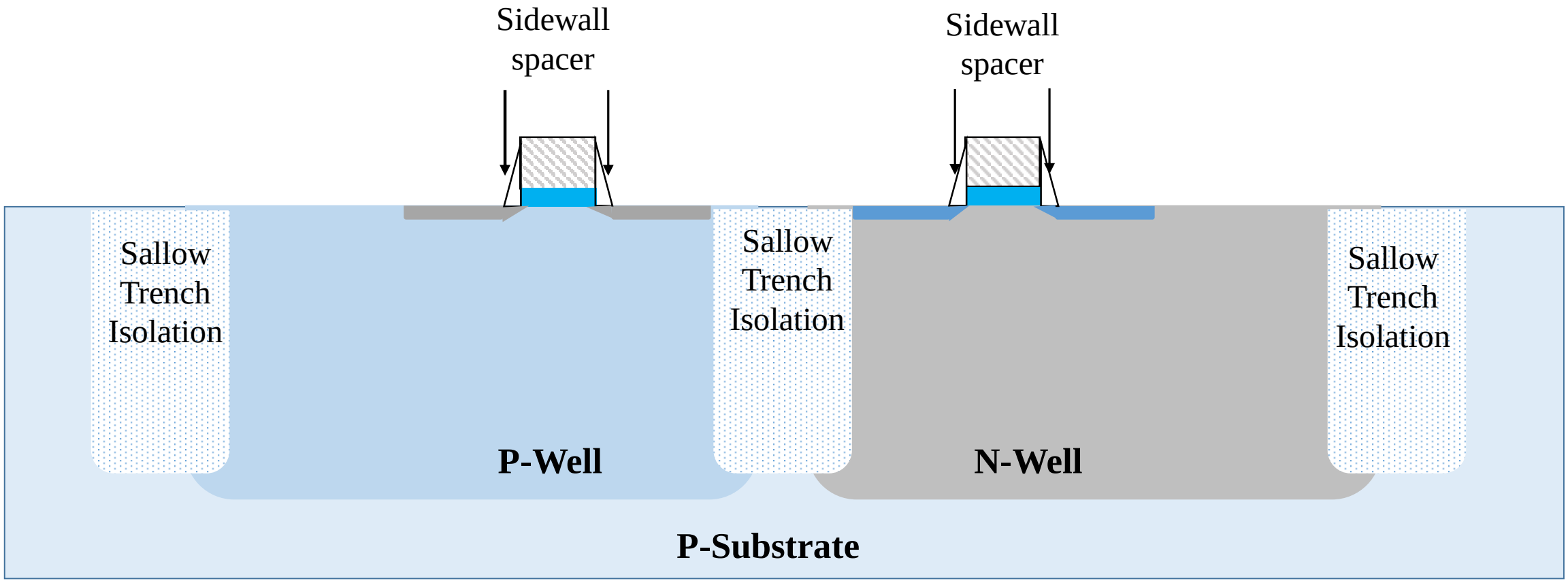
- A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.



Deep Submicron (DSM) CMOS Fabrication Process

Step-6: Sidewall Spacer

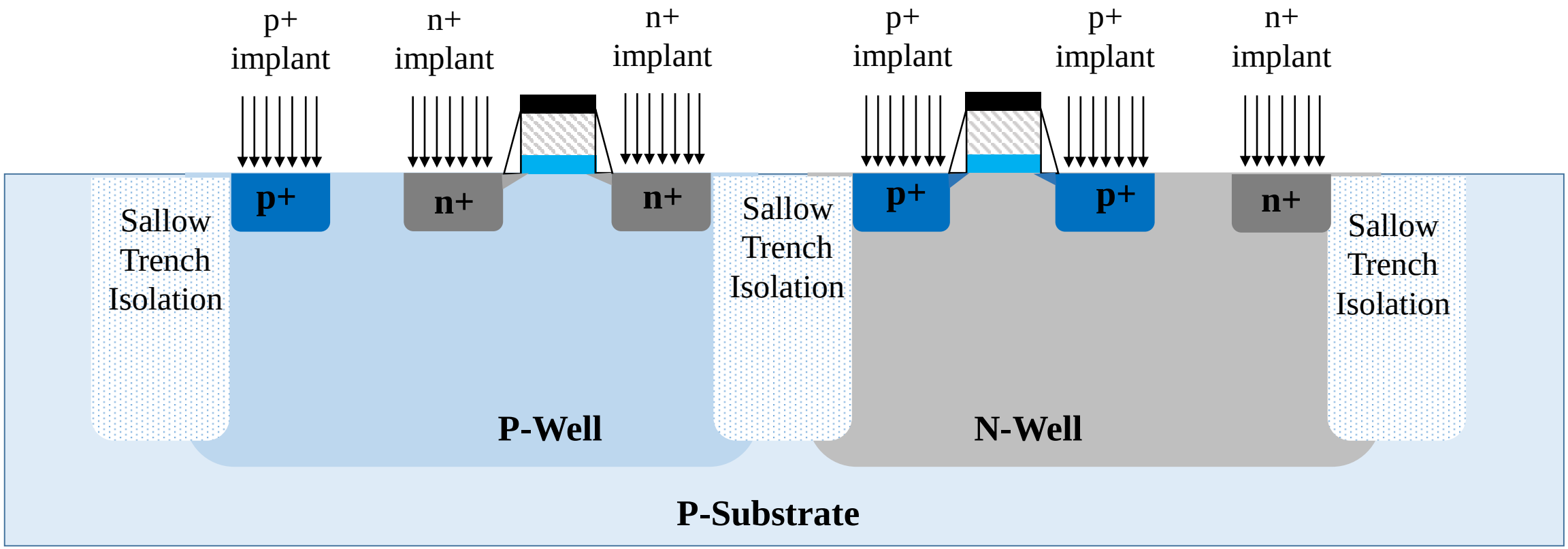
- A layer of dielectric is deposited on the surface and removed in such a way as to leave “sidewall spacers” next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.



Deep Submicron (DSM) CMOS Fabrication Process

Step-7: Implantation of Havily Doped Source and Drain

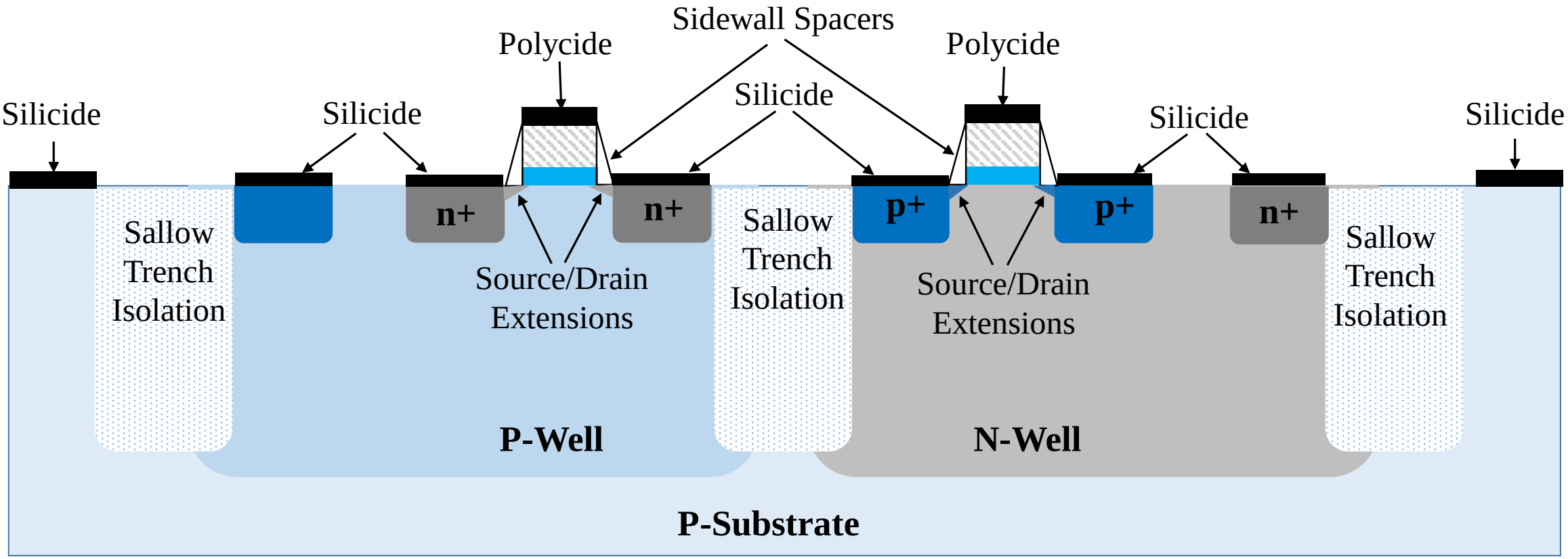
- Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.



Deep Submicron (DSM) CMOS Fabrication Process

Step-8: Siliciding (Salicide and Polyside)

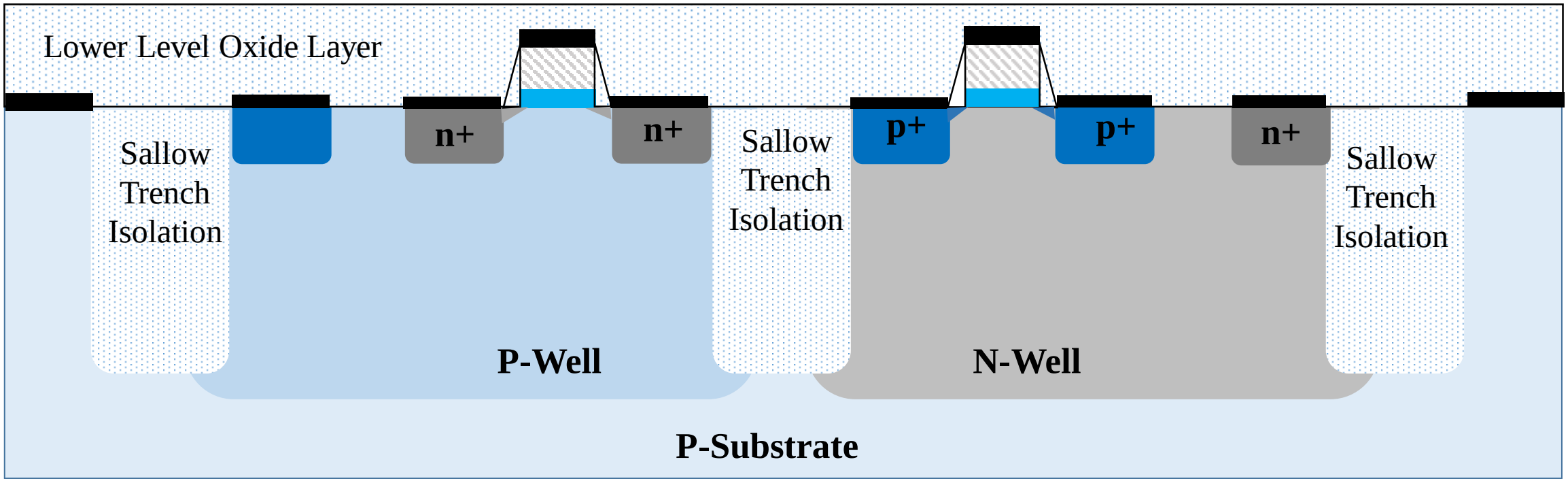
- This step reduces the resistance of the bulk diffusions and polysilicon and forms an ohmic contact with material on which it is deposited.



Deep Submicron (DSM) CMOS Fabrication Process

Step-9: Intermediate Oxide Layer

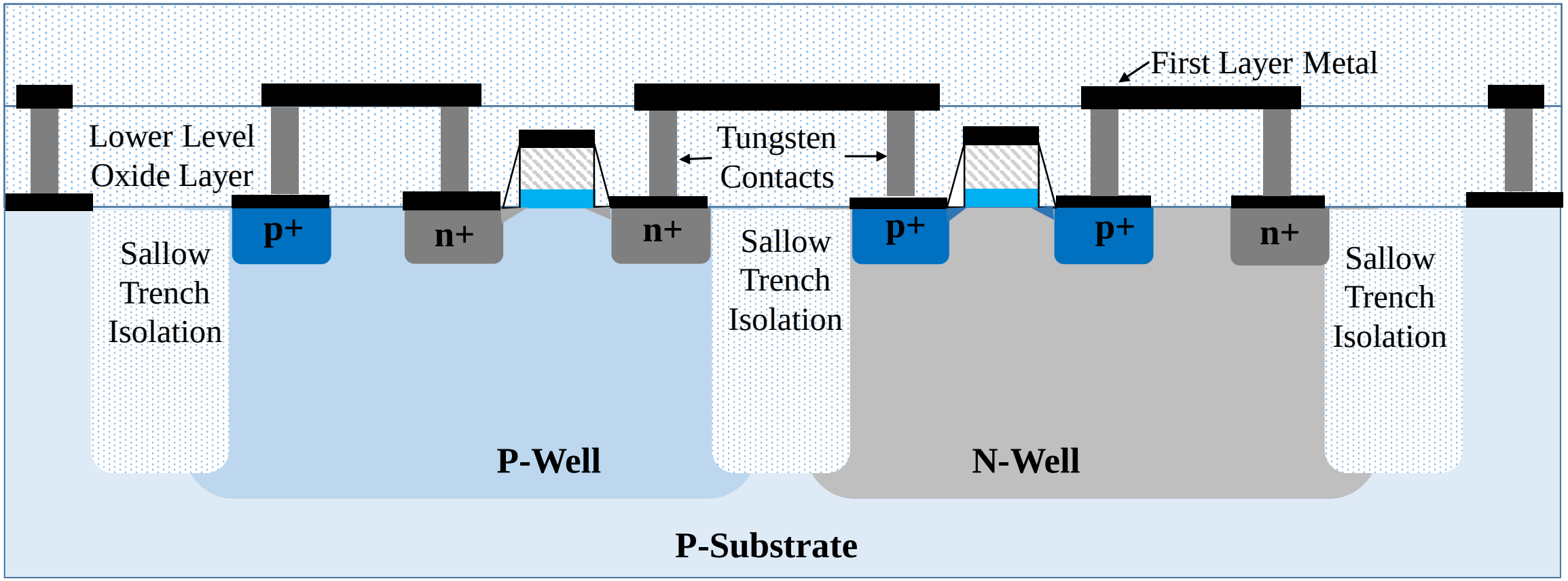
- An oxide layer is used to cover the transistors and to planarize the surface.



Deep Submicron (DSM) CMOS Fabrication Process

Step-10: First Level Metal

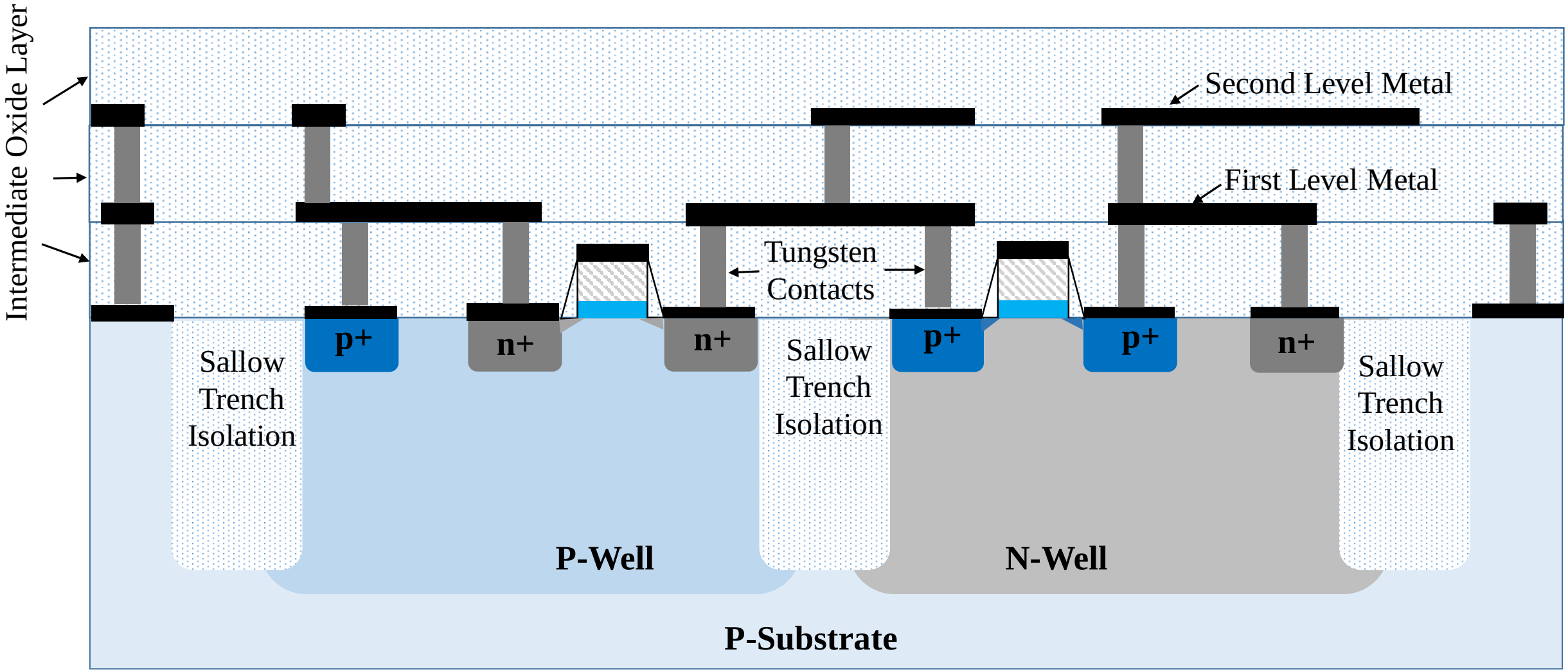
- Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.



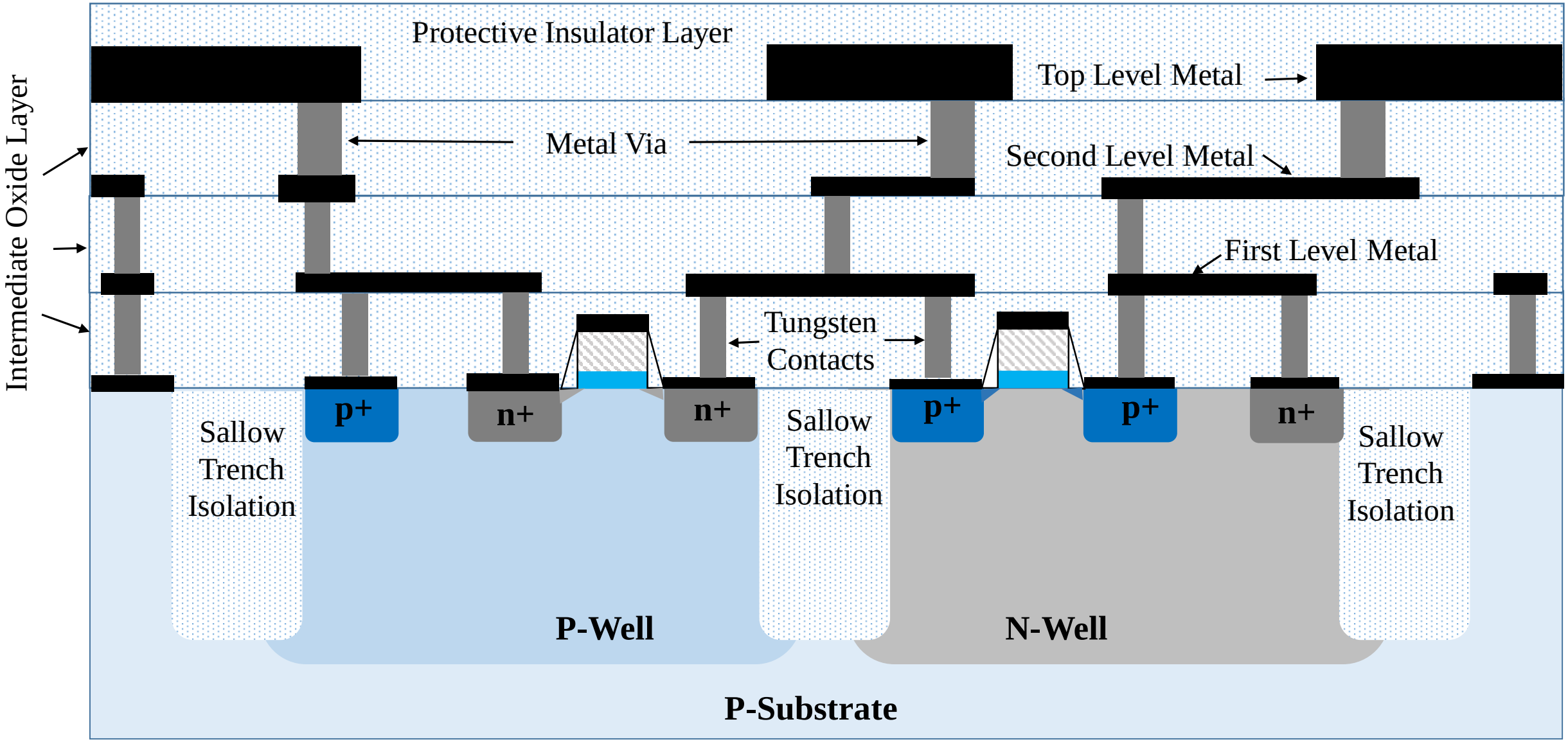
Deep Submicron (DSM) CMOS Fabrication Process

Step-11: Second Level Metal

- The previous step is repeated for the second-level metal.



Deep Submicron (DSM) CMOS Technology



Summary of Deep Submicron (DSM) CMOS Fabrication Process

- DSM technology typically has a minimum channel length between 0.35μm and 0.1μm
- DSM technology addresses the problem of excessive depletion region widths in junction isolation techniques by using shallow trench isolation
- DSM technology may have from 4 to 8 levels of metal
- Lightly doped drains and sources are a key aspect of DSM technology

Ultra Deep Submicron (UDSM) CMOS Technology

USDM Technology

- Lmin ≤ 0.1 microns
- Minimum feature size less than 100 nanometers
- Today's state of the art:
  - 22 nm drawn length
  - 5 nm lateral diffusion (12 nm gate length)
  - 1 nm transistor gate oxide
  - 8 layers of copper interconnect
- Specialized processing is used to increase drive capability and maintain low off currents

Ultra Deep Submicron (UDSM) CMOS Technology

Advantage of UDSM CMOS Technology

Digital Viewpoint:

- Improved Ion/Ioff
- Reduced gate capacitance
- Higher drive current capability
- Reduced interconnect density
- Reduction of active power

Analog Viewpoint:

- More levels of metal
- Higher cutoff frequency
- Higher capacitance density
- Reduced junction capacitance per trans-conductance
- More speed

Disadvantage of UDSM CMOS Technology

Analog Viewpoint:

- Reduction in power supply resulting in reduced headroom
- Gate leakage currents
- Reduced small signal intrinsic gain
- Increased nonlinearity
- Increased noise and poorer matching

Thank You