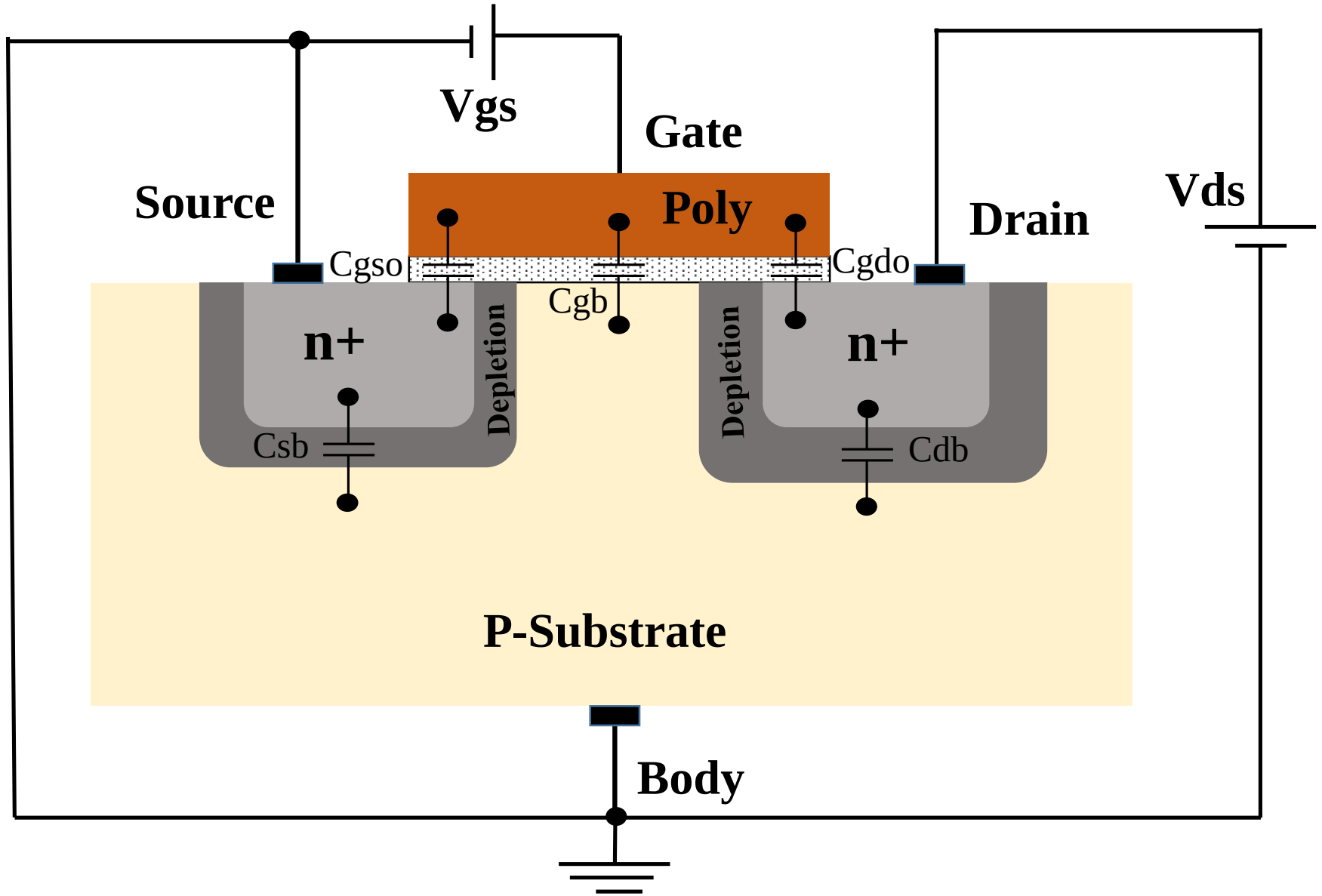
MOSFET Intrinsic Capacitances

Santunu Sarangi

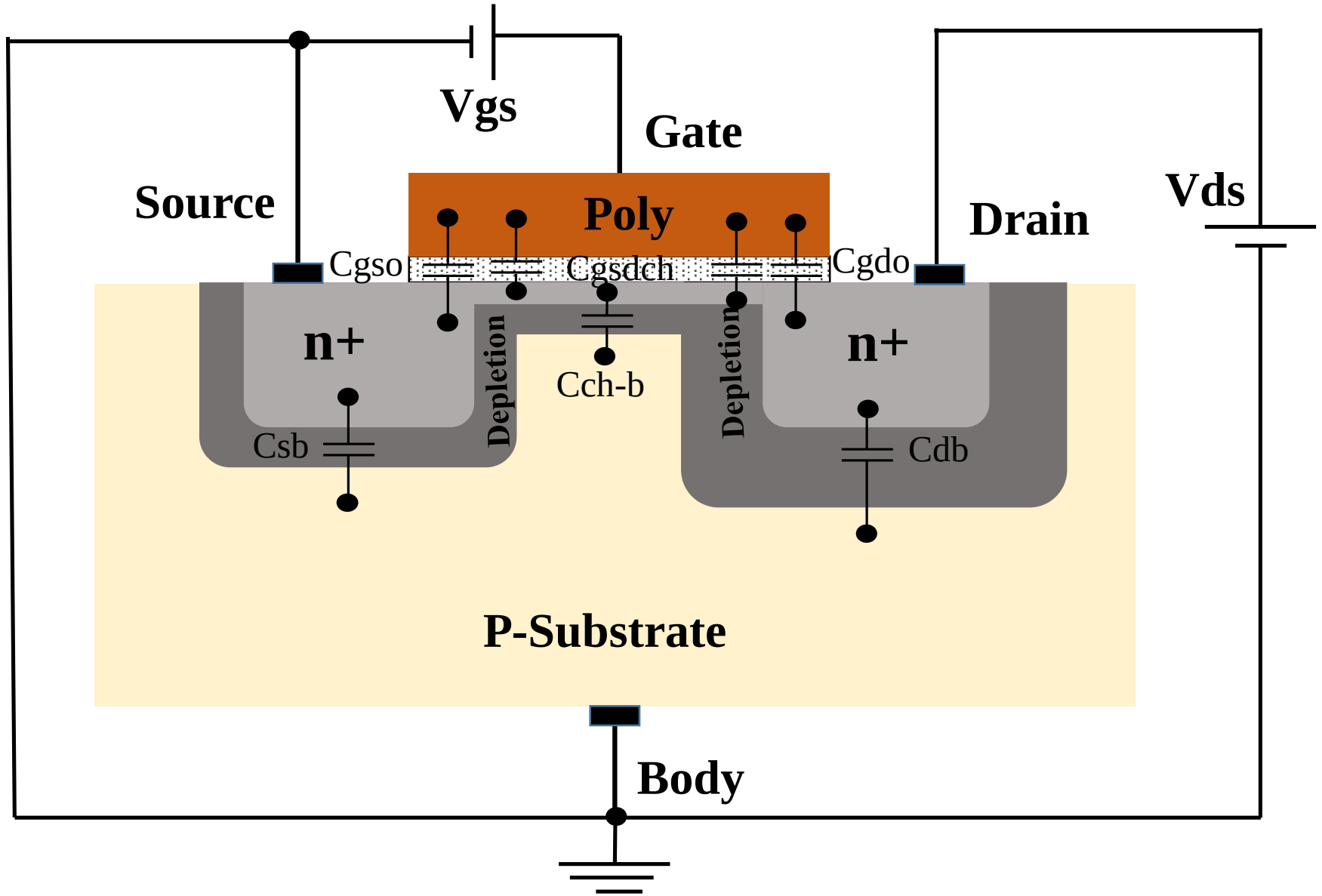
MOSFET Intrinsic Capacitance: Cutoff Region



Intrinsic Capacitance

- Cgso: gate-source overlap capacitance.
- Cgdo: gate-drain overlap capacitance.
- Cdb: drain-bulk reverse bias junction capacitance.
- Csb: source-bulk reverse bias junction capacitance.
- Cgb: gate-bulk oxide capacitance
- No channel relate capacitance because of no channel.

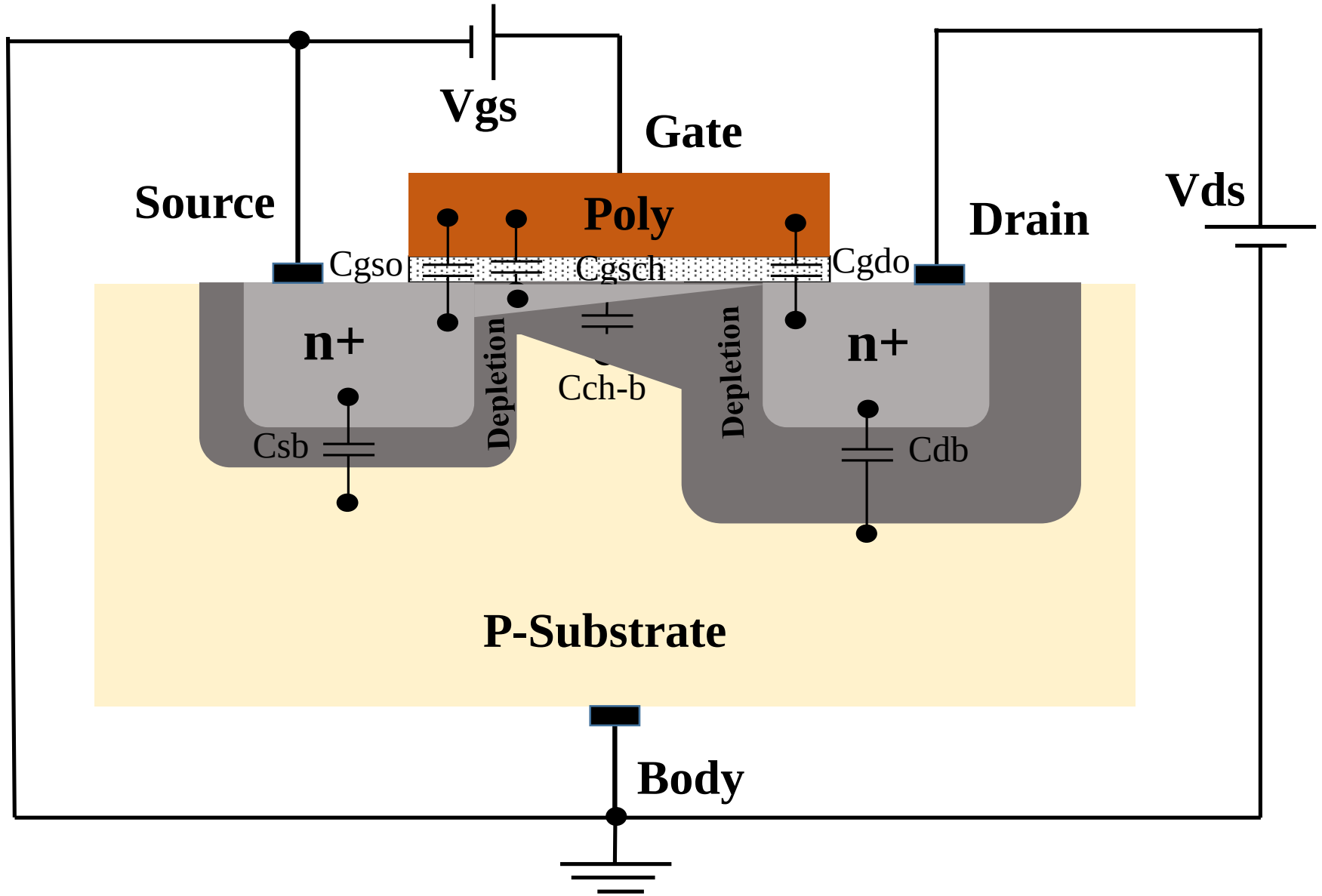
MOSFET Intrinsic Capacitance: Linear Region



Intrinsic Capacitance

- Cgso: gate-source overlap capacitance.
- Cgdo: gate-drain overlap capacitance.
- Cdb: drain-bulk reverse bias junction capacitance.
- Csb: source-bulk reverse bias junction capacitance.
- Cgsch: gate-channel oxide capacitance at source side.
- Cgdch: gate-channel oxide capacitance at source side.
- Cch-b: channel-bulk capacitance

MOSFET Intrinsic Capacitance: Saturatio Region



Intrinsic Capacitance

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- Cgsch: gate-channel oxide capacitance at source side.
- Cch-b: channel-bulk capacitance

MOSFET Intrinsic Capacitance Summary

1. Channel Capacitance

- Cutoff:
  - no channel capacitance
  - Only gate-to-bulk capacitance (High value)
- Linear:
  - Cgsch, Cgdch : Gate-to-channel at source side and gate-to-channel at drain side
  - Voltage dependent
  - $C_{gsch} = C_{gdch} = \frac{1}{2} C_{OX} W L_{eff}$
- Saturation:
  - Cgsch : Gate-to-channel at source side
  - No drain side capacitance because of pinch-off
  - $C_{gsch} = \frac{2}{3} C_{OX} W L_{eff}$

2. Junction Capacitance

- Bottom wall capacitance
  - Cdbbw: drain-to-bulk bottom wall capacitance
  - Csbbw: Source-to-bulk bottom wall capacitance
- Side wall capacitance
  - Cdbsw: drain-to-bulk side wall capacitance
  - Csbsw: Source-to-bulk side wall capacitance

3. Overlap Capacitance

- Cgso, Cgdo: Gate-to-source and Gate-to-drain overlap capacitance
- It is not depends on voltage
- $C_{gso} = C_{gdo} = C_{ox} W L_d$

Schematic Design, Circuit Simulation, Layout Design and Post-layout Simulation

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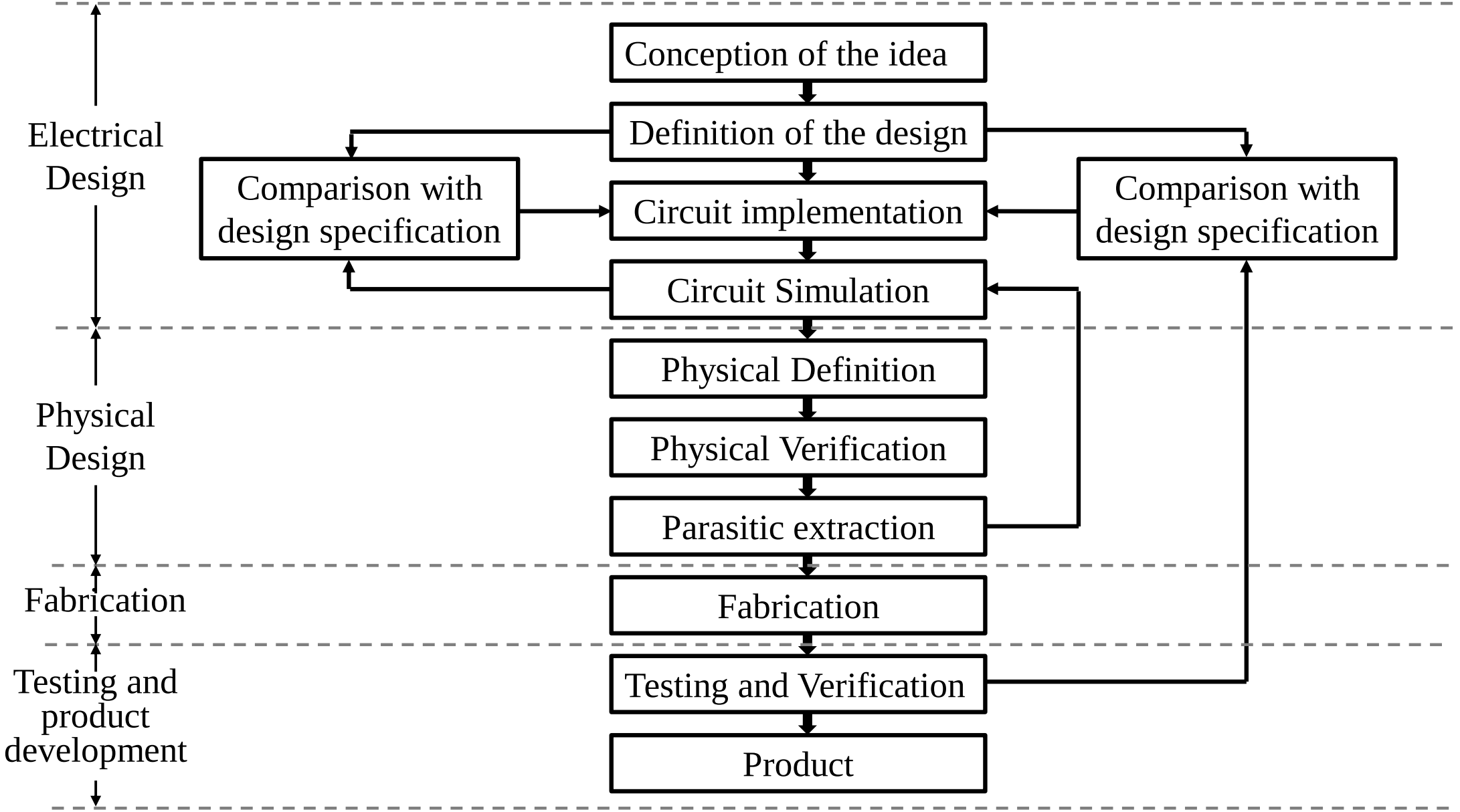
Custom IC Design Process



Custom IC Design Flow using Tools

Schematic Drawing Phase

Step-1: Schematic entry

Step-2: Symbol creation

Step-3: Create testbench for simulation

Circuit Simulation Phase

Step-4: Launch ADE-L

Step-5: Select simulation type;

- DC operating point sim.
- DC sweep simulation
- Transient Simulation
- AC simulation

Step-6: Plot waveforms and use calculators to plot for some predefined functions (rise time, fall time, delay, derivative, gain margin, phase margin etc)

Step-7: Do parametric simulation (vary two variable at a time)

Layout Design and Verification Phase

Step-8: Generate layout from schematic

Step-9: Place the components

Step-10: Routing between the components, supply and ground.

Step-11: Verify the layout with the design rule (DRC).

Step-12: Verify the layout with schematic (LVS)

Step-13: Extract the parasitic and create a schematic view of the that extracted netlist

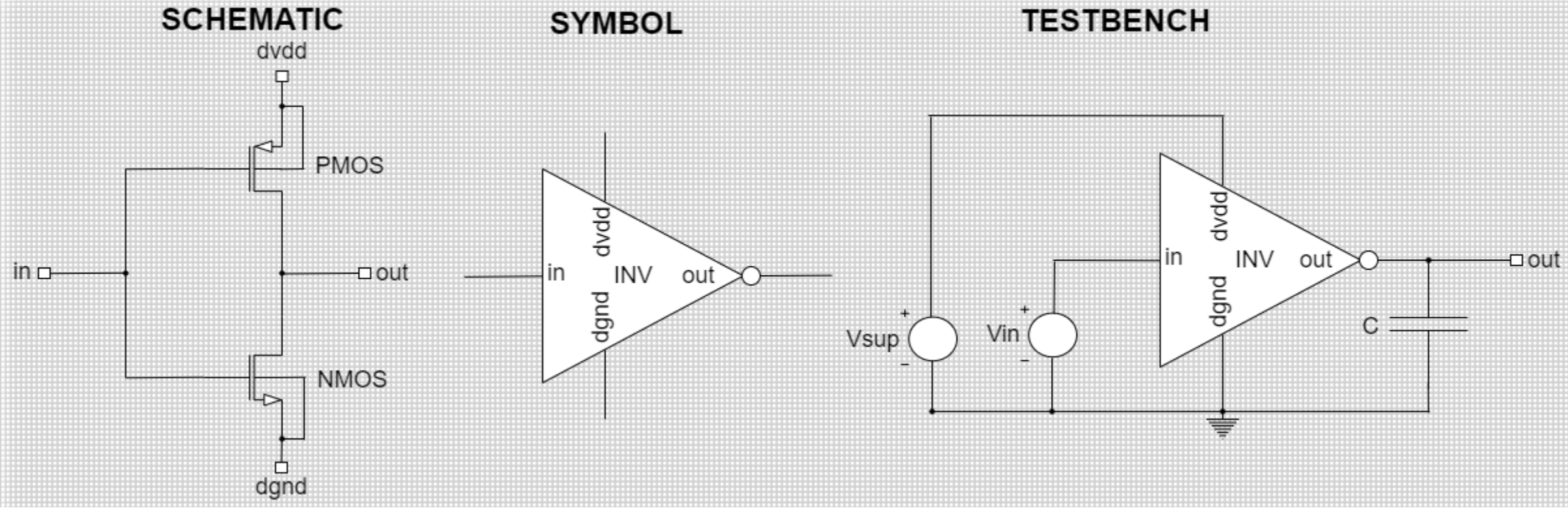
Post Layout Simulation Phase

Step-14: Create config view

Step-15: Do the simulation for both views and compare the result.

- Follow same process as you have done pre-layout simulation. Only difference is instead of schematic netlist you will use parasitic extracted netlist.

Custom IC Design Flow: Schematic Phase



Schematic

- Instantiate PMOS and NMOS, and change the W, L, F and M.
- Complete the connection using wires.
- Put input, output, vdd and gnd pins.

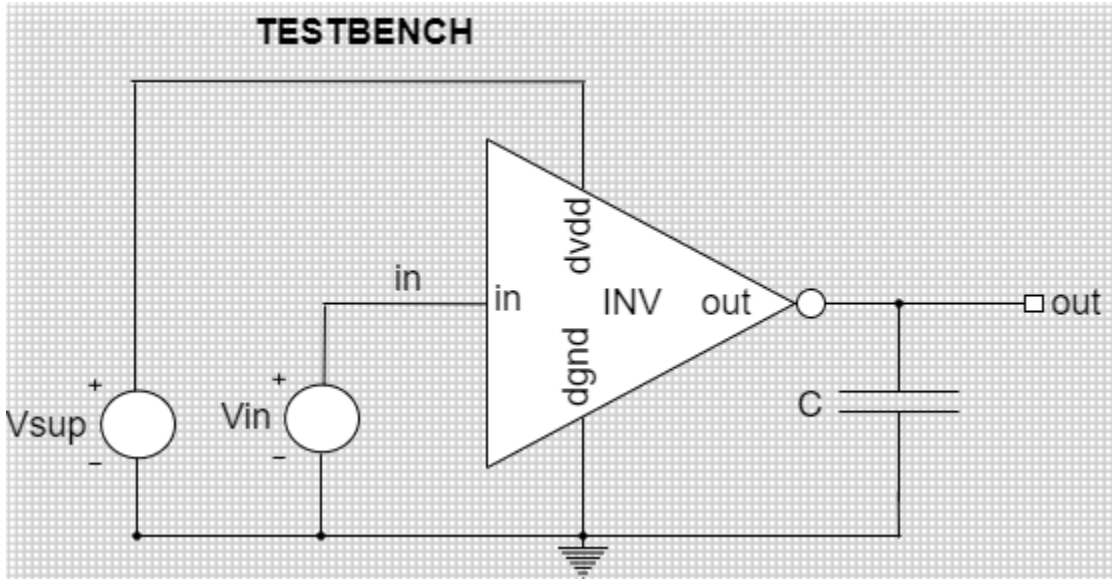
Symbol

- Create symbol view from schematic view.
- Modify the symbol shape and place the pin names in appropriate places.

Testbench

- Instantiate previously created symbol.
- Put the supply, ground and input sources.
- Modify the properties of the input source depends on the analysis type (OP, DC Sweep, Transient and AC)
- Connect the approximate output loads.

Custom IC Design Flow: Simulation Phase



Simulation Setup

- Launch ADE-L, choose the simulation type, copy the design variables, select the input and outputs nodes to be plotted.

Operating Point Simulation

- Vsup: Give the DC supply voltage
- Vin: Give a DC voltage (any voltage less than Vdd) and check all the node voltages.
- C: Capacitor value in pf range (ex:10-50pf)

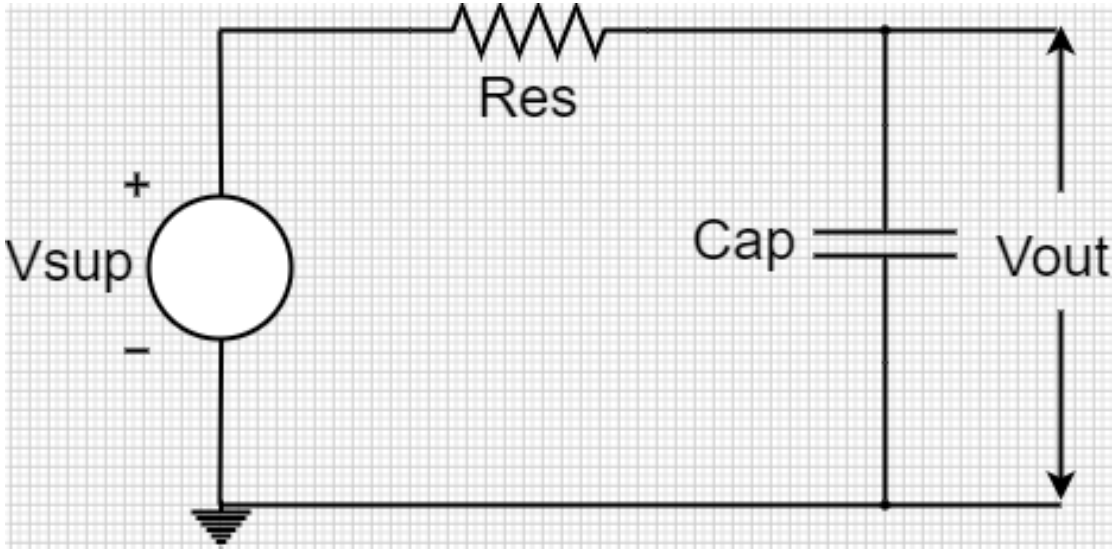
DC Sweep Simulation

- Vsup: Give the DC supply voltage
- Vin: Give a DC voltage (may be a variable name, which can be changed latter in ADE).
- C: Take a capacitor value in pf range (ex:10-50pf)
- Result: Plot the output curve. Also plot the current from the Vsup and understand the relation.

Transient Simulation

- Vsup: Give the DC supply voltage
- Vin: Set the initial voltage, final voltage, initial delay, rise time, fall time, pulse width and period, of the pulse input source,
- C: Take a capacitor value in pf range (ex:10-50pf)
- Result: Plot the output waveform and measure risetime, fall time and propagation delay manually.
- Same you can measure using calculator using ready-made functions.

Custom IC Design Flow: Simulation Phase (AC and Transient)



STEP Response (Transient)

- Vsup: Take a pulse source
- Give appropriate step input
- Do the transient analysis
- Result: measure the rise time or fall time, propagation delay and time constant
- Verify the result with manual calculation.

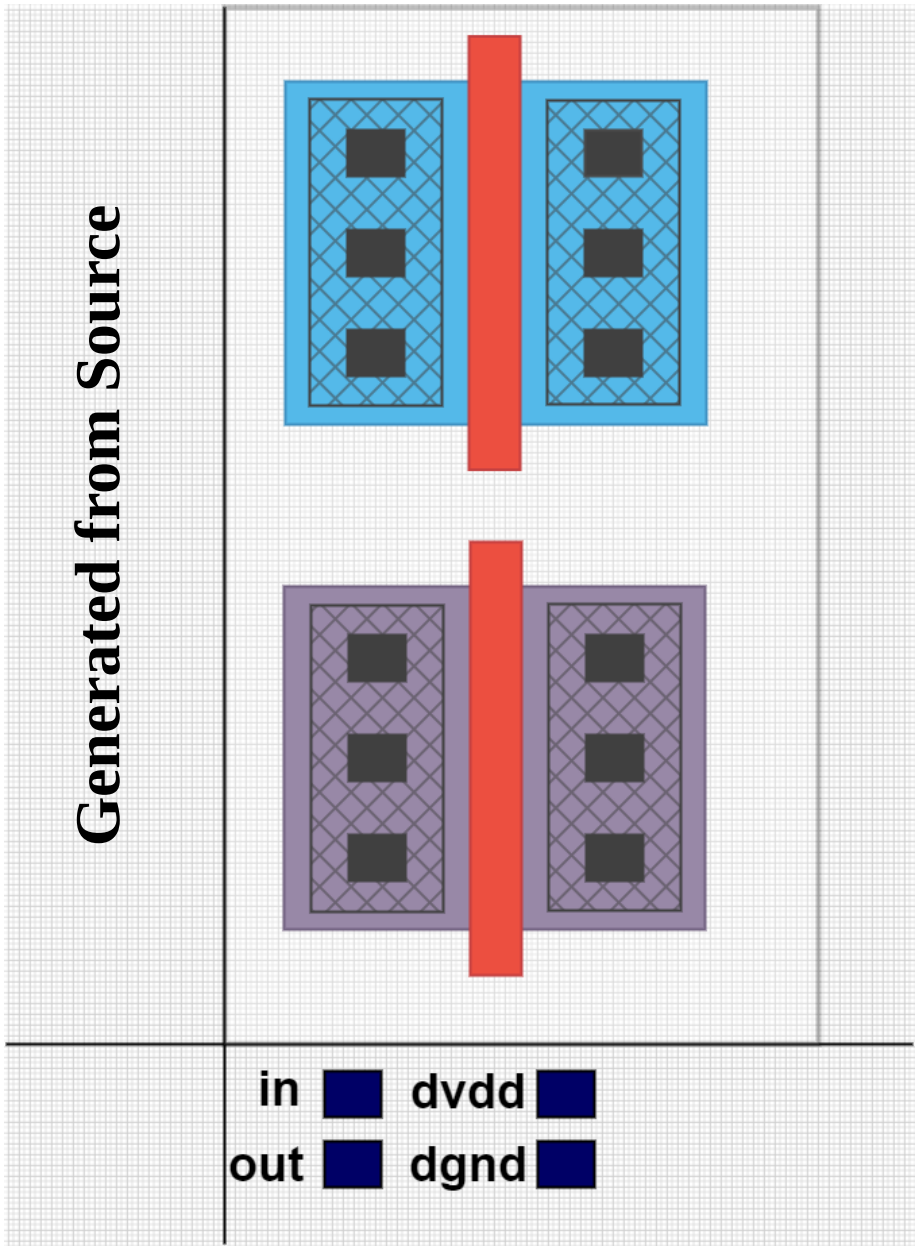
AC simulation

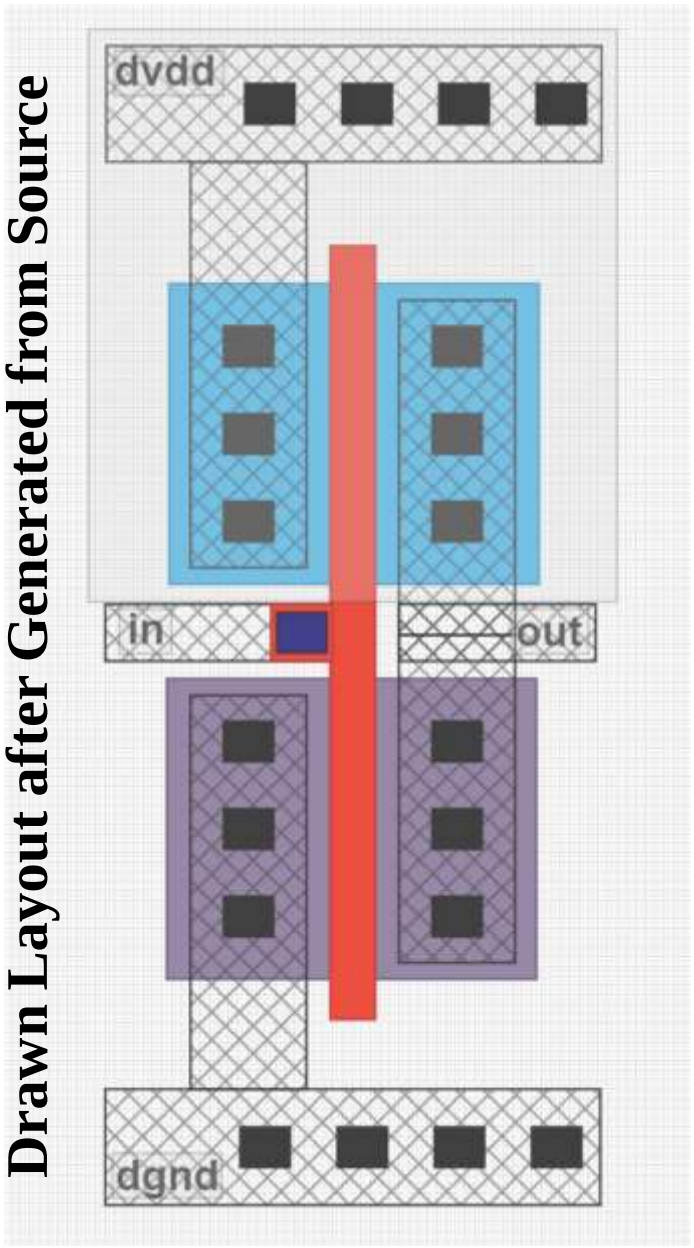
- Take a resistance of Kilo-Ohm range and Capacitance of Pico-Farad (pF) range.
- Vsup: Take a DC supply source
- Set the magnitude to 1 and phase to 0 Deg and give frequency range.
- Choose the analysis type AC in ADE window
- Run the simulation and plot the output wave form (Gain vs Freq.). Check 3dB frequency.

Sinusoidal Response (Transient)

- Vsup: Take a sinusoidal source and set the amplitude, frequency and phase.
- Run the transient simulation and plot the output wave form.
- Check the output waveform amplitude at different frequencies and find out the gain (Output/input).
- Compare the sinusoidal transient response result with the AC analysis result.

Custom IC Design Flow: Layout Phase (Generate from Source)





Layout Design

- Place all the P-Cell layouts and do the routing.
- Put the N-Well and diffusion contacts.
- Place the pins in appropriate nodes.

Layout Verification

- DRC: depending upon the tools (PVS or Calibre), do the DRC.
- LVS: Depending upon the tools (PVS or Calibre), do the LVS.

Parasitic Extraction

- PEX: depending upon the tools available (PVS-QRC or Calibre-PEX or Star-RC), do the parasitic extraction.

Simulation Practice: MOSFET Characterization

N-Channel MOSFET

1) Draw the schematic and testbench to characterize N-channel MOSFET
2) Simulate Ids-Vgs characteristics
3) Simulate Ids-Vgs Char. at different Vds
4) Simulate Ids-Vgs char. with body bias
5) Simulate Ids-Vds characteristics
6) Simulate Ids-Vds char. at different Vgs
7) Calculate Vt, λ, Kn and γ from the Ids-Vgs and Ids-Vds graph.
8) Do all the above simulations in different process corners (TT, SS, FF).
9) Do all the simulation in 3 different supply voltages (nominal, nominal + 10%, and nominal – 10%).
10) Do all the simulations in 3 different temperatures (-40, 27 and 125 Deg C)
11) Finally do all the simulations in best case (FF, +10%, -40) and worst case (SS, -10%, 125)

P-Channel MOSFET

1) Draw the schematic and testbench to characterize P-channel MOSFET
2) Simulate Isd-Vsg characteristics
3) Simulate Isd-Vsg Char. at different Vds
4) Simulate Isd-Vsg char. with body bias
5) Simulate Isd-Vsd characteristics
6) Simulate Isd-Vsd char. at different Vgs
7) Calculate Vt, λ, Kp and γ from the Isd-Vsg and Isd-Vsd graph.
8) Do all the above simulations in different process corners (TT, SS, FF).
9) Do all the simulation in 3 different supply voltages (nominal, nominal + 10%, and nominal – 10%).
10) Do all the simulations in 3 different temperatures (-40, 27 and 125 Deg C)
11) Finally do all the simulations in best case (FF, +10%, -40) and worst case (SS, -10%, 125)

Simulation Practice: RC Circuit and MOSFET-Capacitor Circuit

RC Circuit

1) Draw the step response of all the RC circuits provided in day-1 assignment.
2) Draw the pulsed response
3) Draw the sinusoidal response
4) Draw the ramp response
5) Do the AC analysis and plot the Bode plot and find the -3db frequency.
6) Do all the above simulations in different process corners (TT, SS, FF).
7) Do all the simulation in 3 different supply voltages (nominal, nominal + 10%, and nominal – 10%).
8) Do all the simulations in 3 different temperatures (-40, 27 and 125 Deg C)
9) Finally do all the simulations in best case (FF, +10%, -40) and worst case (SS, -10%, 125)

MOSFET with Capacitor

1) Draw the step response of MOSFET-Capacitor circuits and find out the region of operations of all the problems given in the day-6 assignment.
2) Draw the current through the MOSFET vs Time
3) Do all the above simulations in different process corners (TT, SS, FF).
4) Do all the simulation in 3 different supply voltages (nominal, nominal + 10%, and nominal – 10%).
5) Do all the simulations in 3 different temperatures (-40, 27 and 125 Deg C)
6) Finally do all the simulations in best case (FF, +10%, -40) and worst case (SS, -10%, 125)

Thank You