CMOS Inverter

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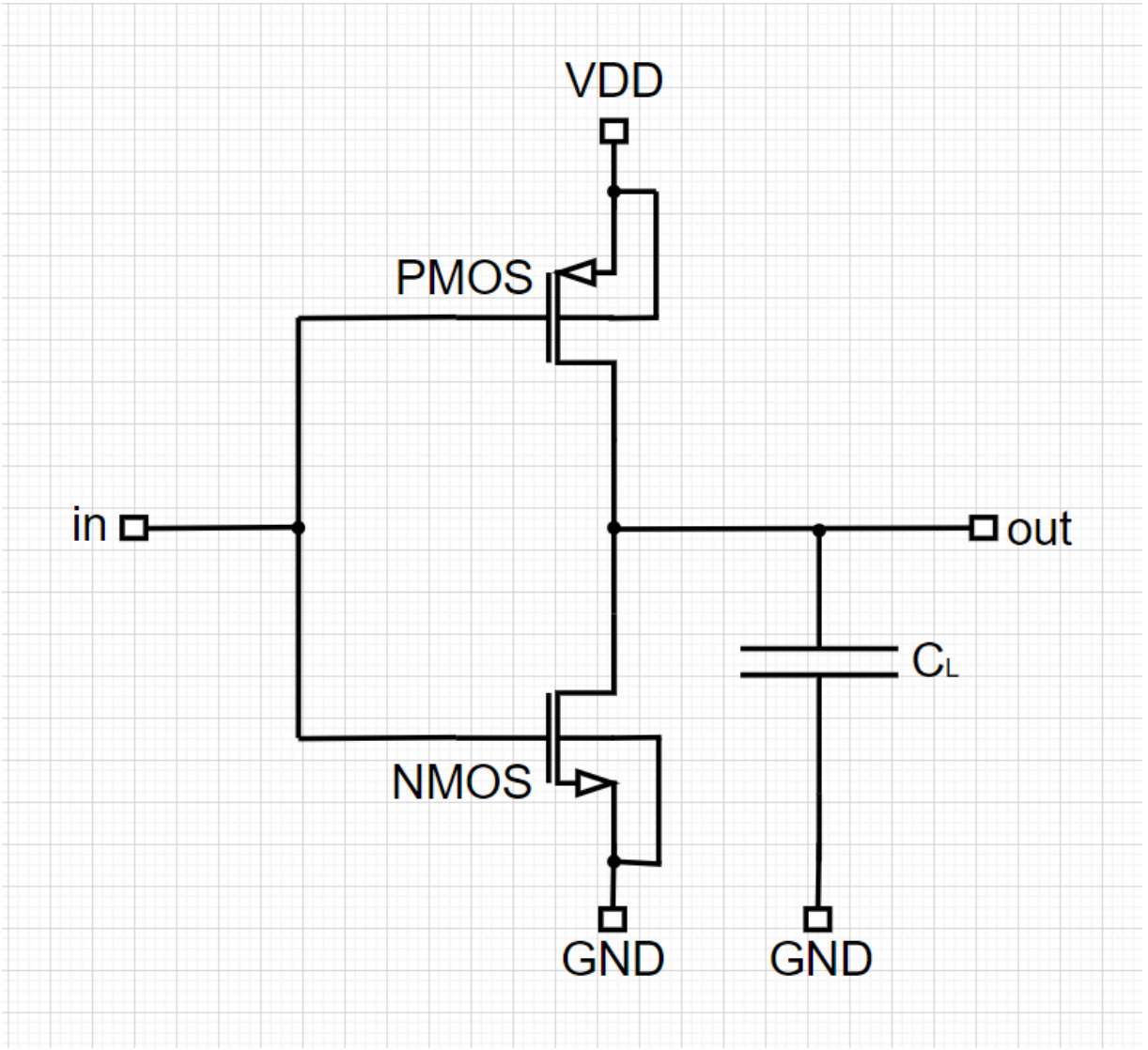
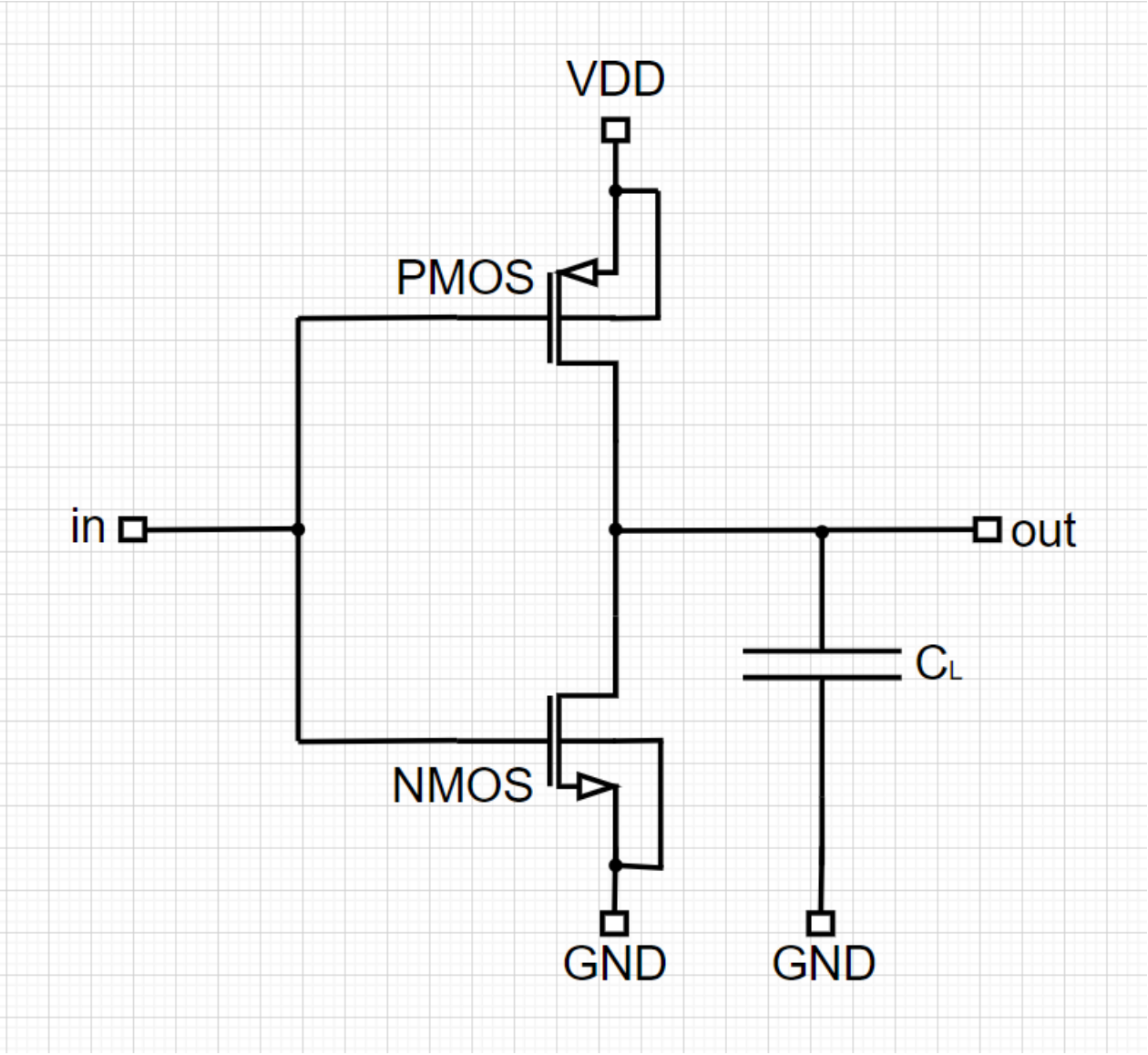
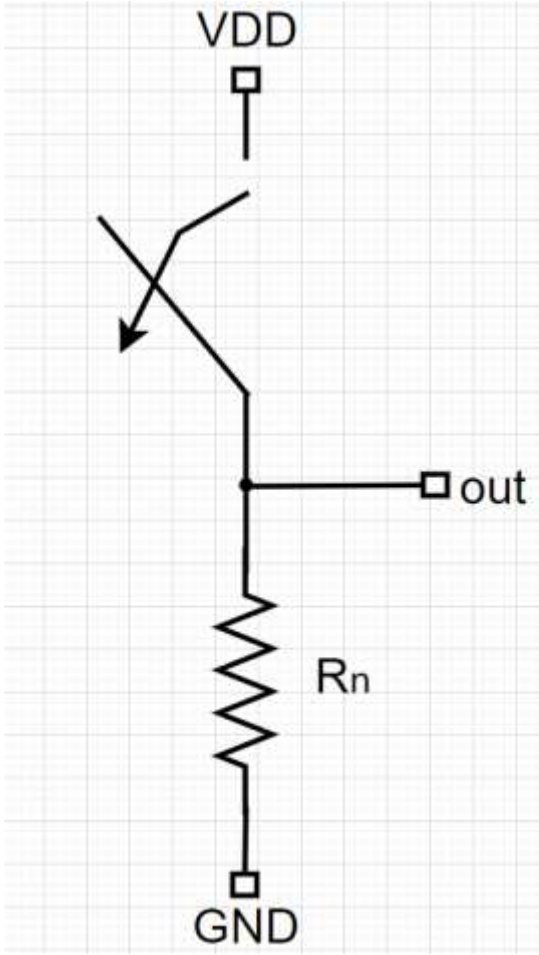
CMOS Inverter:

- The CMOS inverter is truly the nucleolus of all digital designs.
- CMOS inverter is the most popular at present, need some special attention to understand all about.
- We will analyze this gate with respect to different design matrices such as:
  - Cost: Expressed by the complexity and area
  - Integrity and robustness: Expressed by the static (steady-state) behavior.
  - Performance: Determined by the dynamic (or transient) response.
  - Energy Efficiency: Set by the energy and power consumption

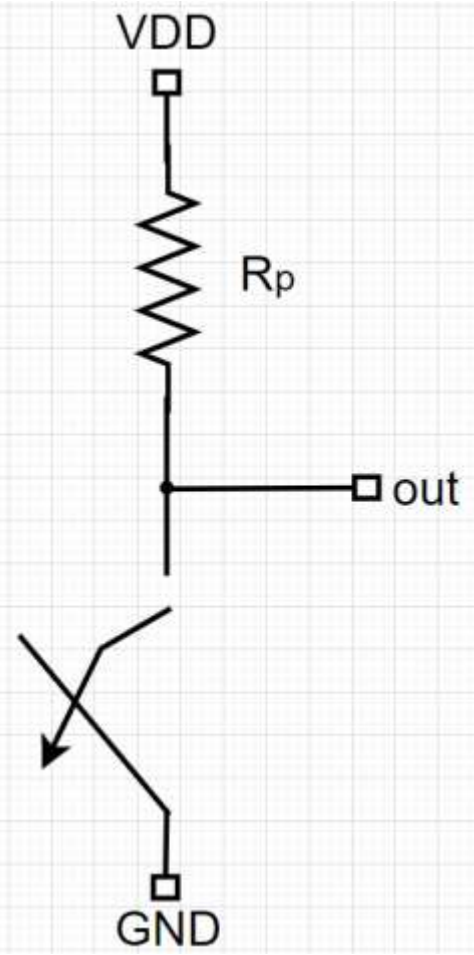


CMOS Inverter: Static Characteristics





Model for high input

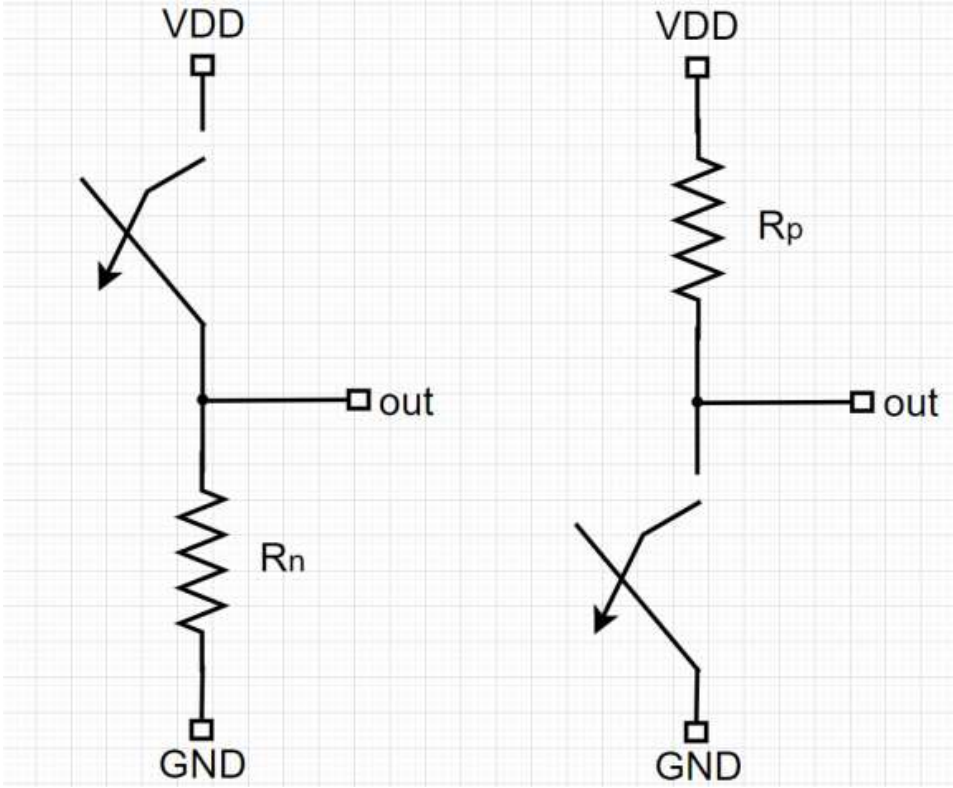


Model for low input

CMOS Inverter: Static Characteristics

Properties CMOS Inverter from Switched Level View:

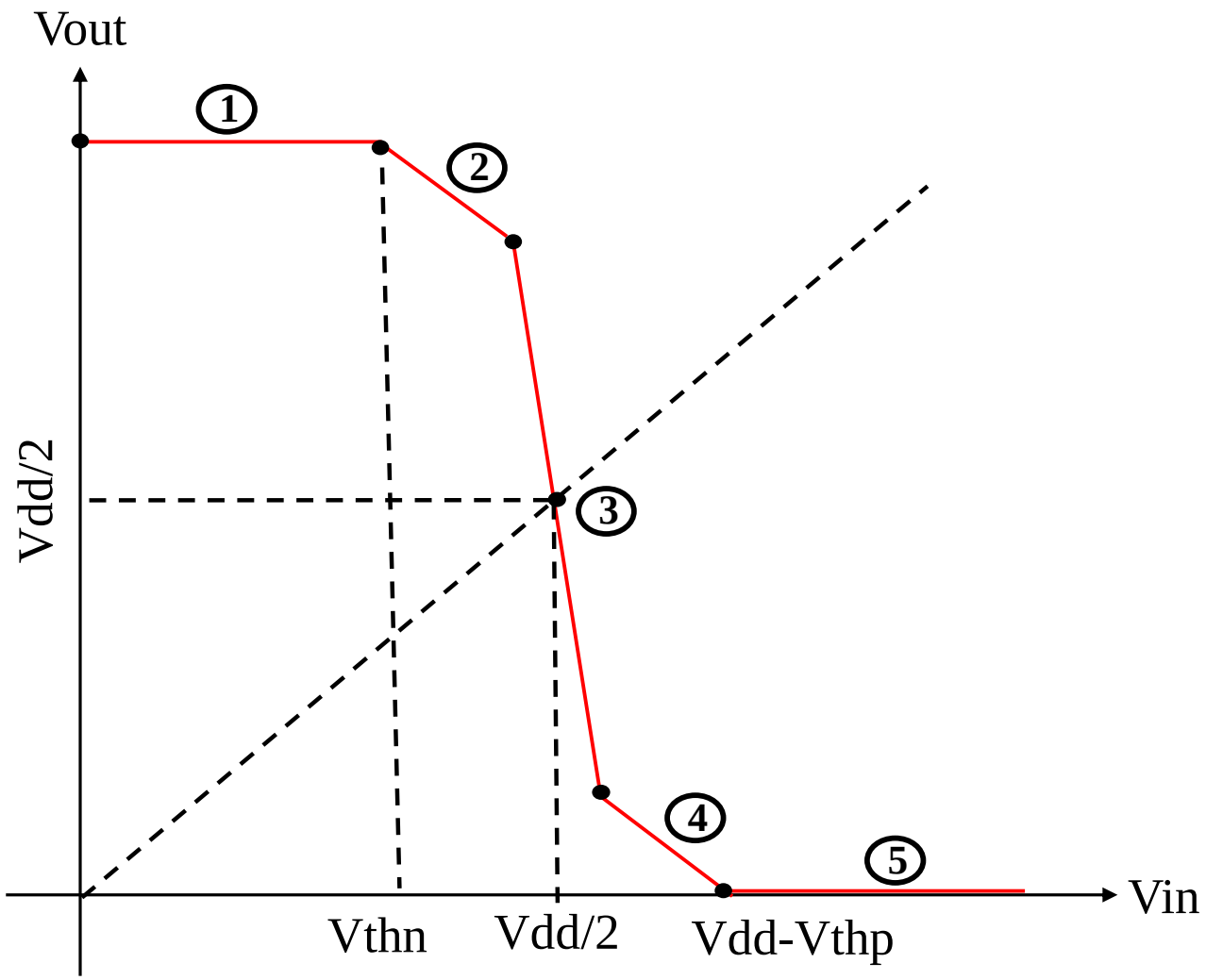
- Rail-to-rail swing: results high noise margin
- Logic levels are independent of device sizes (ratioless)
- In steady state there is always exist a path with a fine resistance between the output and either VDD or Ground. This results low output impedance and less sensitive to noise.
- Input impedance of the CMOS inverter is extremely high. Theoretically, a single inverter can drive infinite number of gates
- No direct path exit between supply and ground. Static power almost zero.



Model for high input

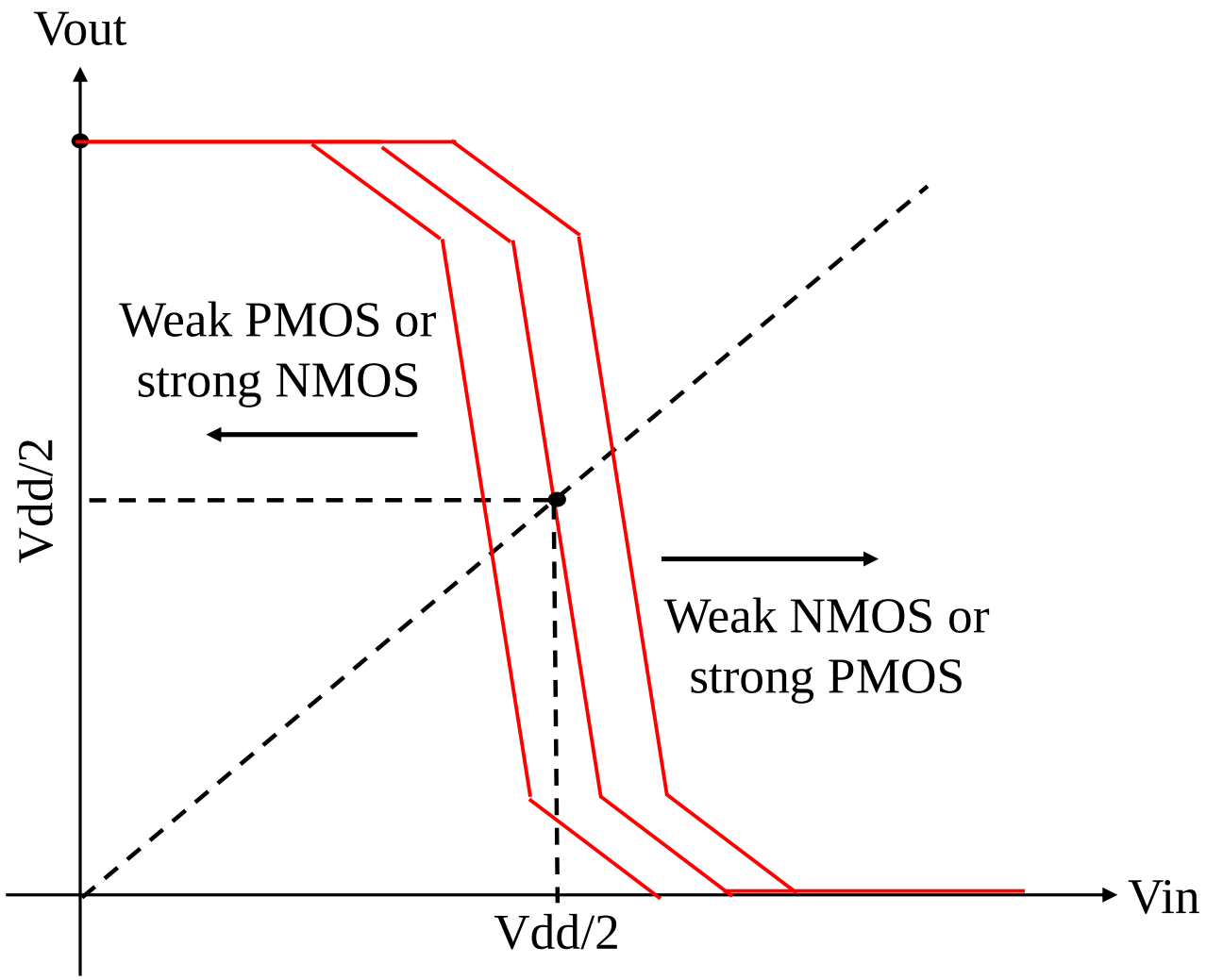
Model for low input

CMOS Inverter: Static Characteristics



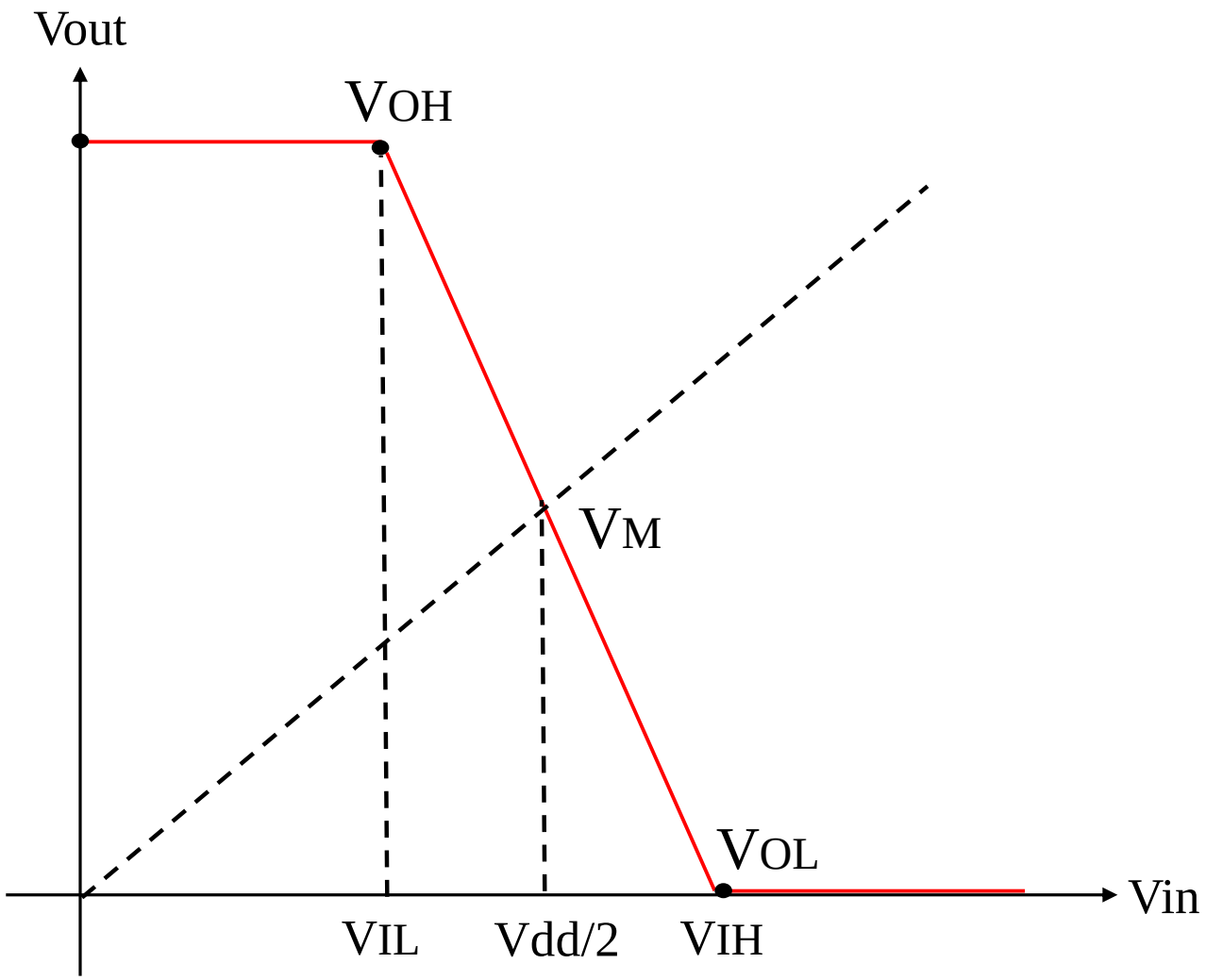
Regions	NMOS	PMOS
1	Cut-off	Linear
2	Saturation	Linear
3	Saturation	Saturation
4	Linear	Saturation
5	Linear	Cut-off

CMOS Inverter: MOSFET Strength Variation



NMOS	PMOS	Transition
Weak	Weak	Less Slope
Strong	Strong	More Slope
Weak	Strong	Right Shift
Strong	Weak	Left Shift

CMOS Inverter: Noise Margin

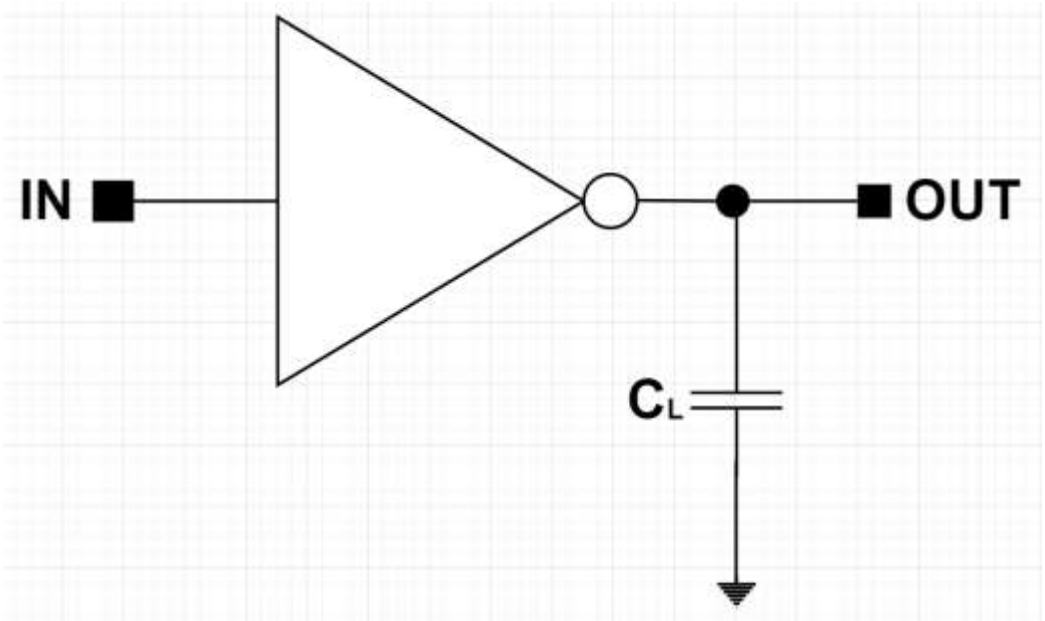


Noise Margin

- Transition Region: $V_{IH} - V_{IL}$
- $V_{IH} - V_{IL} = \left(\frac{V_{0L} - V_{OH}}{GAIN}\right) = -\frac{V_{DD}}{GAIN}$
- $V_{IH} = V_M + \frac{0 - V_M}{GAIN}$
- $V_{IL} = V_M - \frac{V_M - V_{DD}}{GAIN}$
- $NM_H = V_{DD} - V_{IH}$
- $NM_L = V_{IL}$

CMOS Inverter: Dynamic Behavior

- High performance CMOS circuit should have less propagation delay, less rise time and less fall time.
- Propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitance C_L through the PMOS and NMOS transistors respectively.
- If C_L increases;
  - Propagation delay (PD) increases
  - Output rise time (Trise) increases
  - Output fall time (Tfall) increases
- The above observation suggests that getting CL as small as possible is crucial to the realization to the high performance CMOS Circuits
- Need to understand the major components of the load capacitance.



CMOS Inverter: Dynamic Characteristics

Intrinsic Capacitance

- Cdbp, Cdbn : drain-bulk capacitance
- Cgdp, Cgdn: gate-drain overlap capacitance.

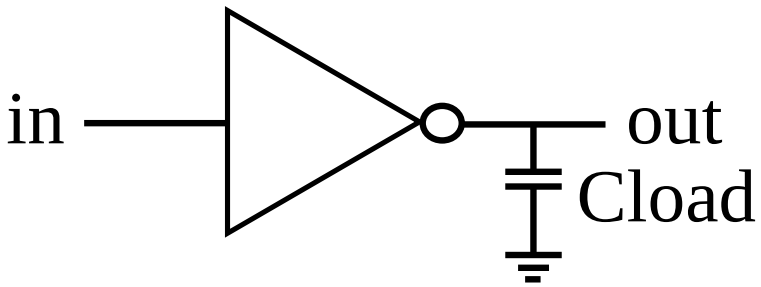
Wiring Capacitance

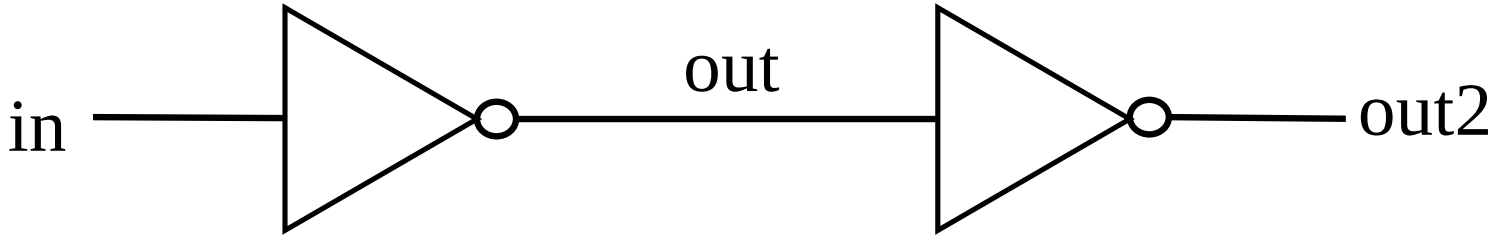
- Cw: Interconnect wiring capacitance

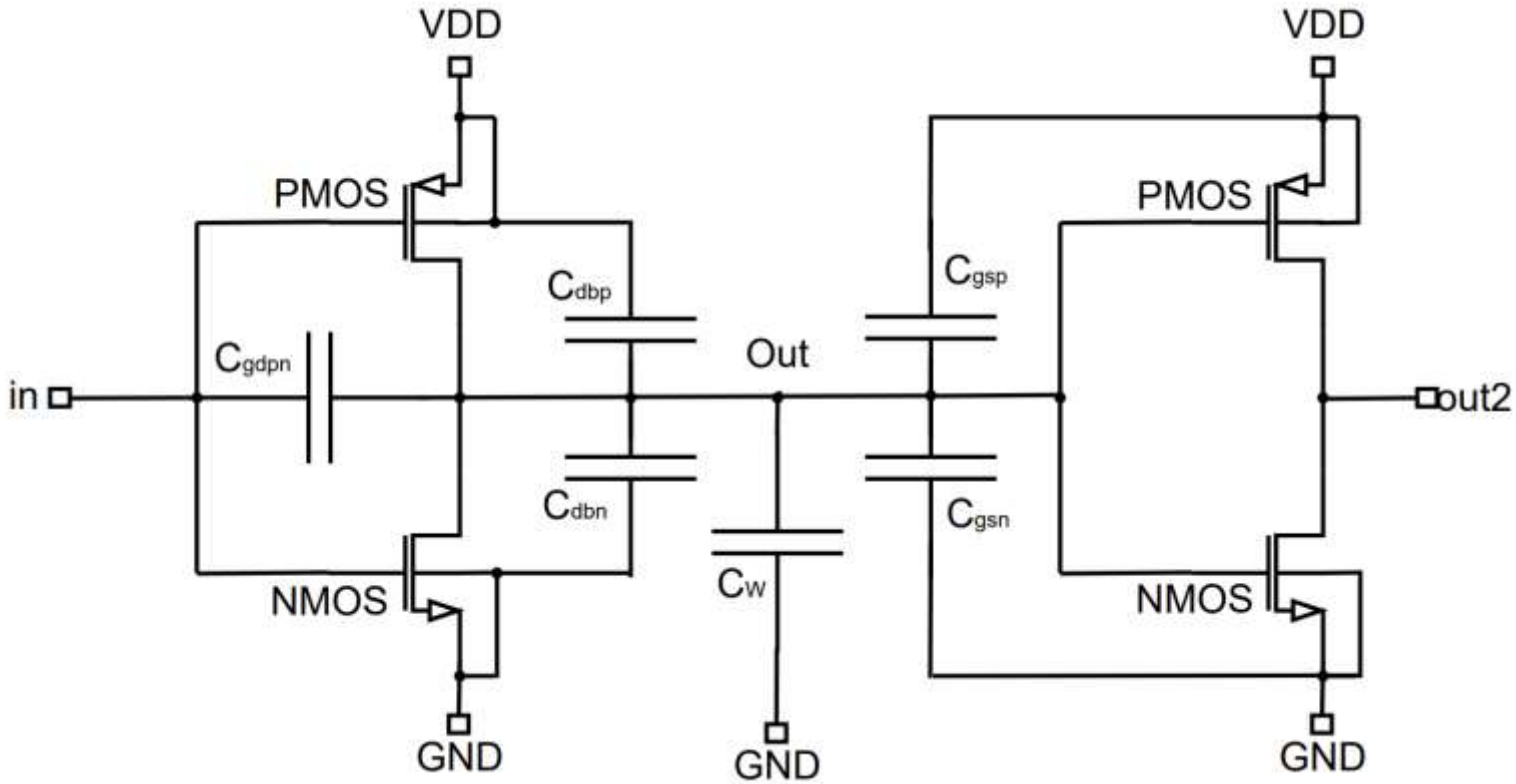
Fanout Capasitance

- Cgsp, Cgsn: source-bulk reverse bias junction capacitance.

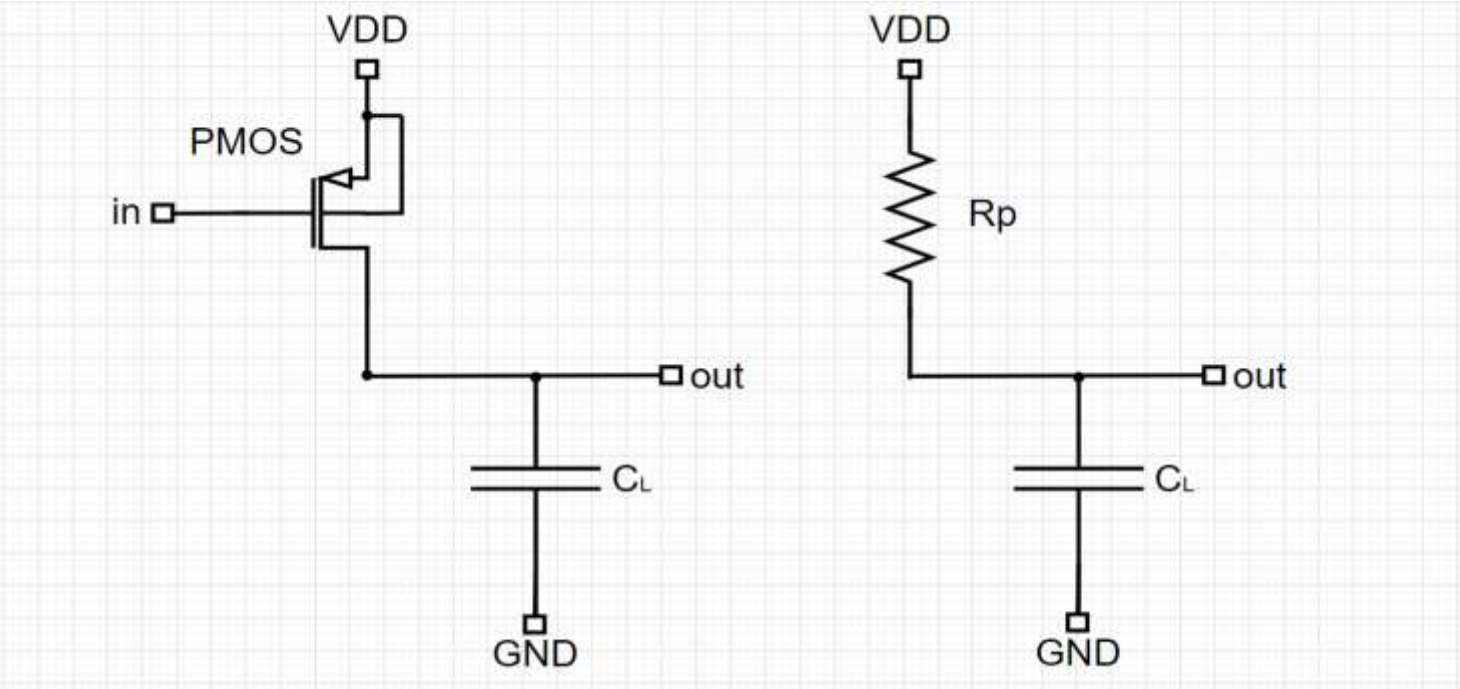
- **Cload = Cint + Cwiring + Cfanout**

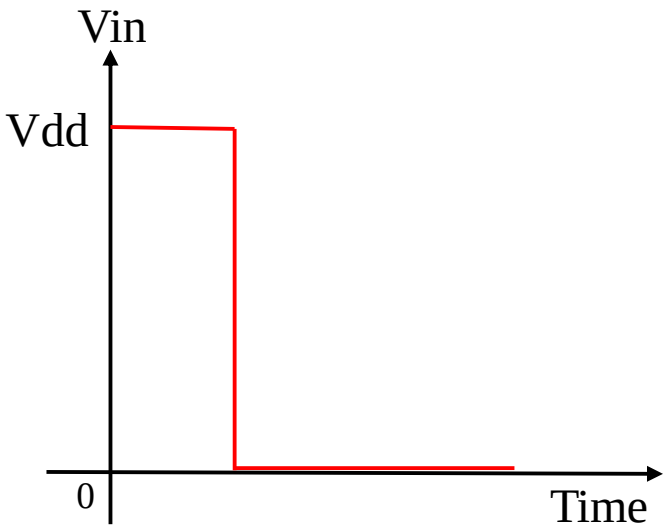


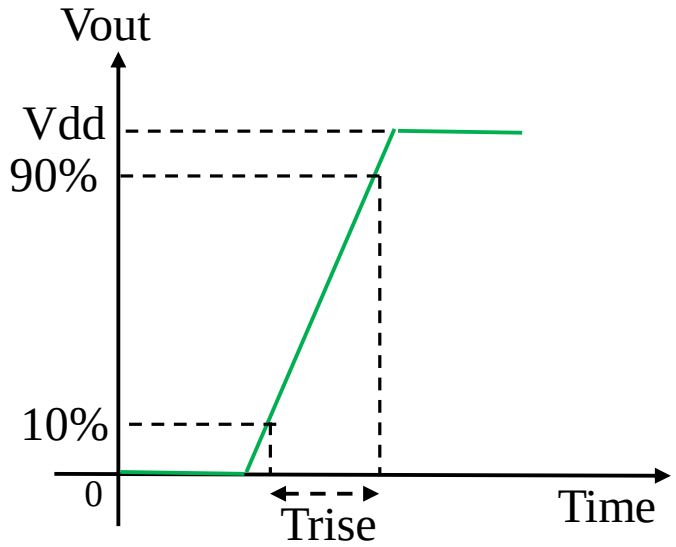




CMOS Inverter: Dynamic Characteristics



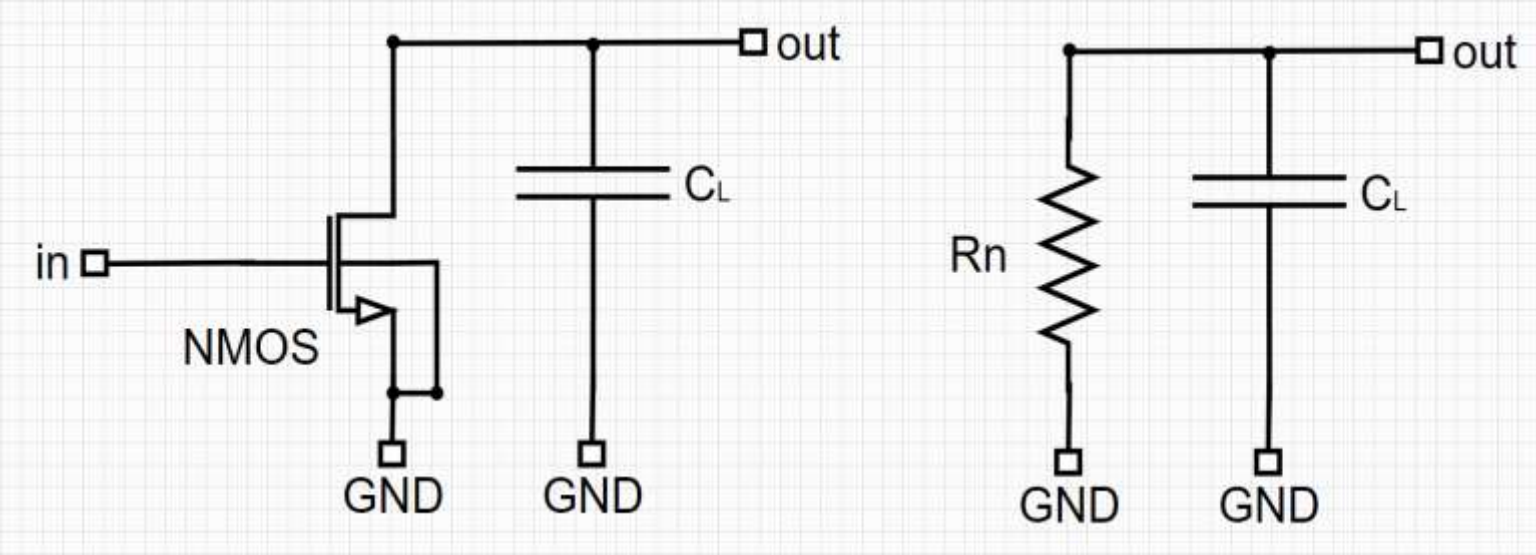




Rise Time

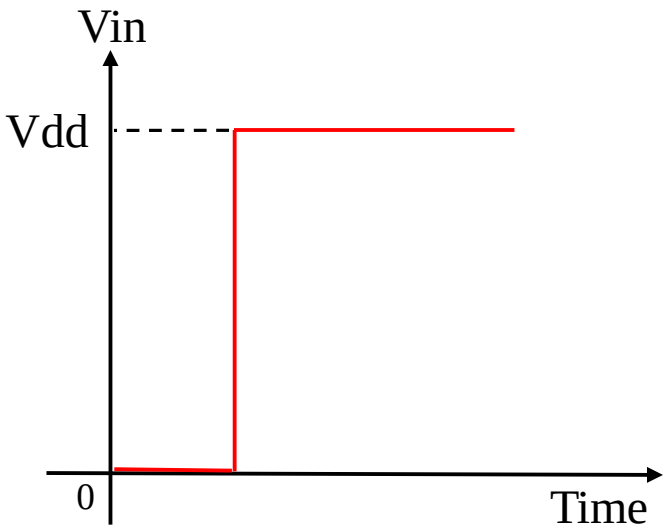
- The time required for the output voltage to rise from 10% to 90% of the supply voltage.

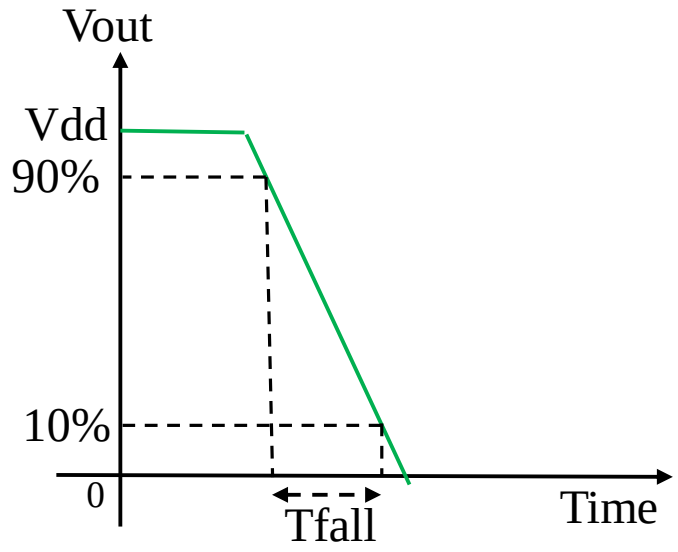
CMOS Inverter: Dynamic Characteristics



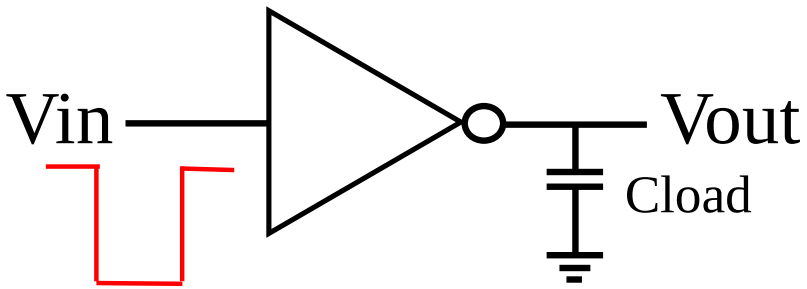
Fall Time:

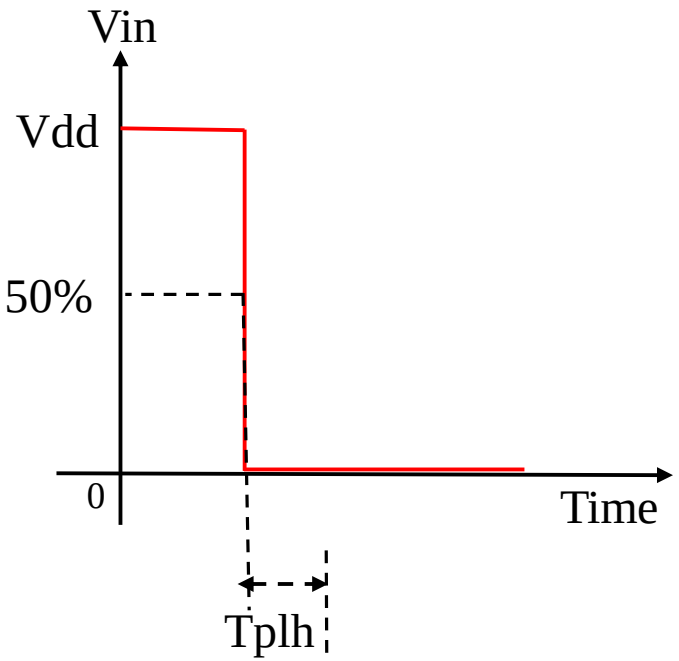
- The time required the output voltage to fall from 90% to 10% of the supply voltage.

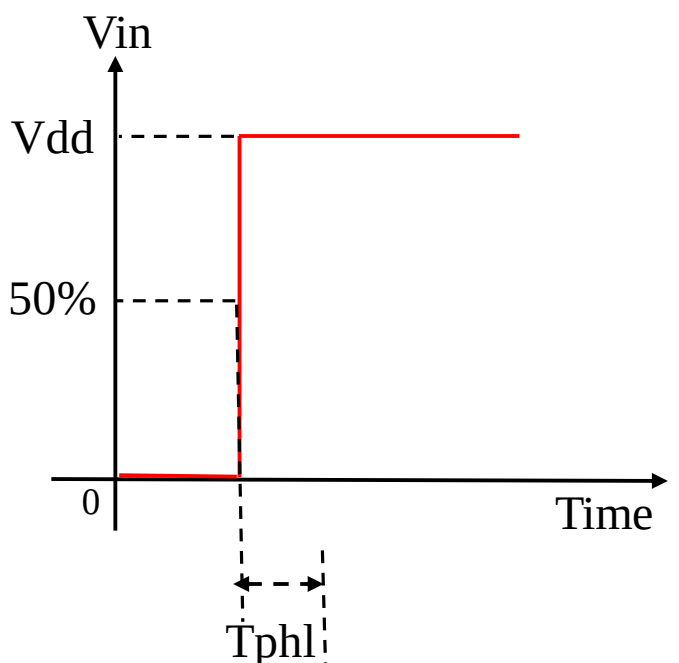




CMOS Inverter: Dynamic Characteristics

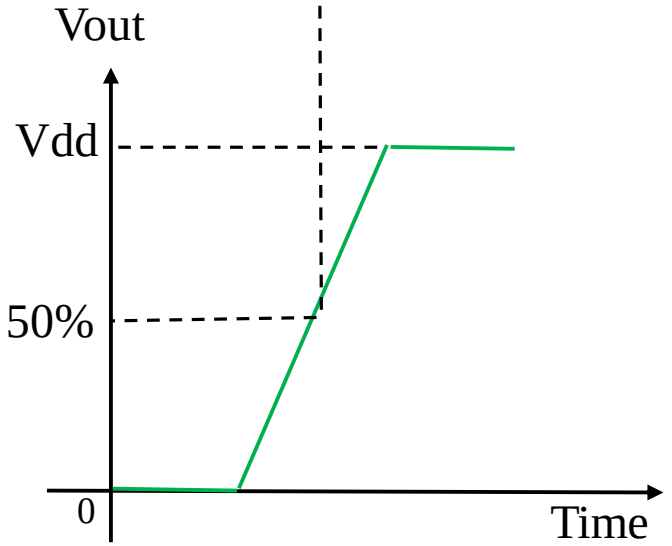


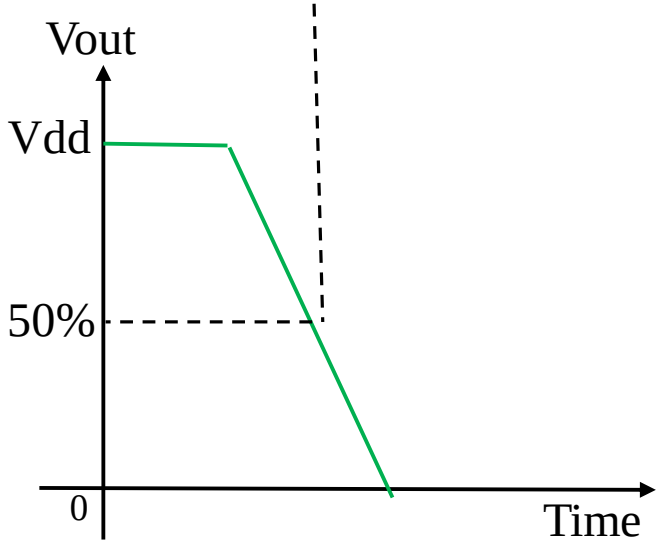




Propagation Delay (Tp):

- Input to output delay during the signal transition (at 50%)
- **Tplh:** Propagation delay at low to high transition at output.
- **Tphl:** Propagation delay at high to low transition at output.





CMOS Inverter: Propagation Delay Calculation

Propagation Delay (Tp):

- One way to compute propagation delay of the inverter is to integrate the capacitor charge (discharge) current.
- $t_p = \int_{V1}^{V2} \frac{C_L(V)}{I(V)} dV$

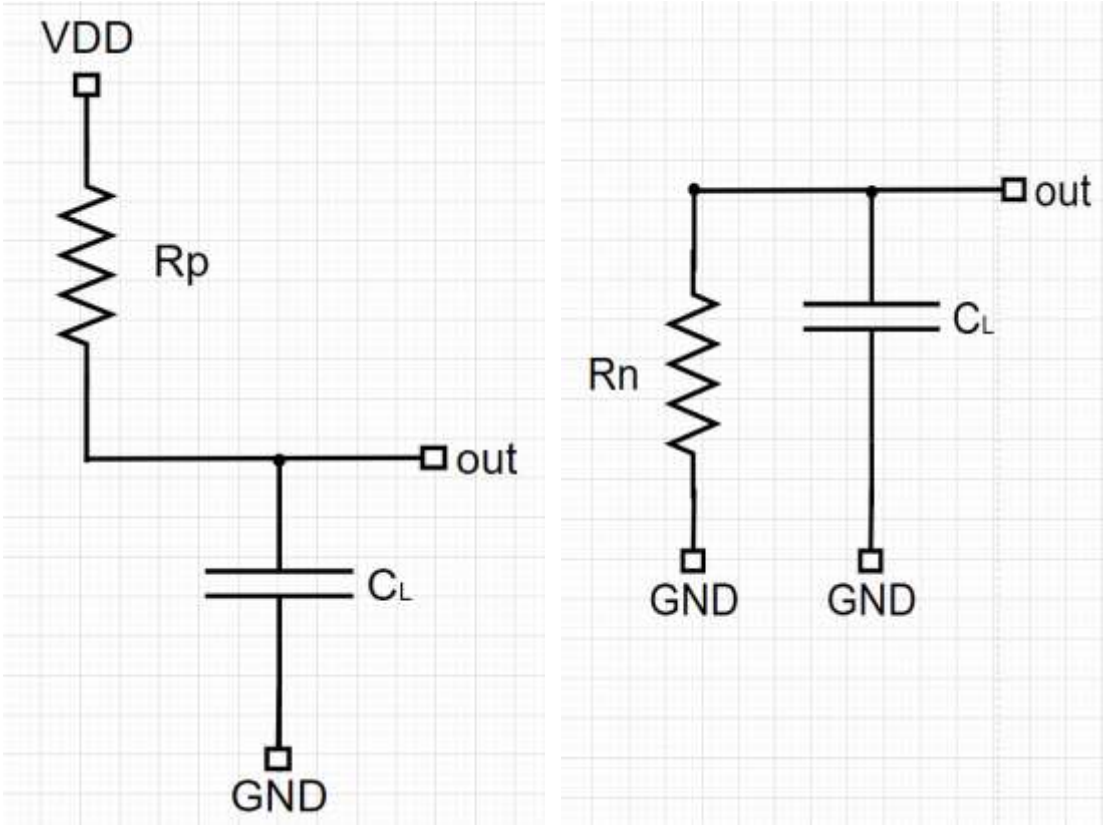
Where $i = Charge\ (discharge)\ current$

$V = Voltage\ over\ the\ capacitor$

$V1 = Initial\ voltage$

$V2 = Final\ voltage$

- Exact computation of above equation is difficult, as both $C_L(V)$ and $i(V)$ are non-linear functions of *V.*
- Deriving the propagation delay of the resulting circuit is now straight forward and is nothing more than the analysis of a first-order linear RC network



$t_{plh} = \ln(2) * R_P * C_L = 0.69\ R_P C_L$

Similarly, $t_{phl} = 0{,}69 R_P C_L$

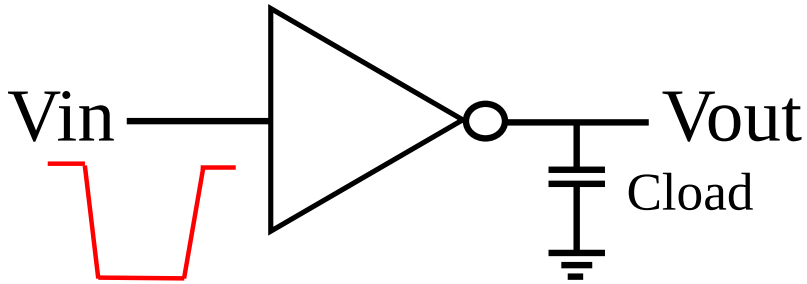
$t_p = \frac{t_{plh}+t_{phl}}{2} = 0.69 C_L \left(\frac{R_P+R_N}{2}\right)$

CMOS Inverter: Propagation Delay Summary

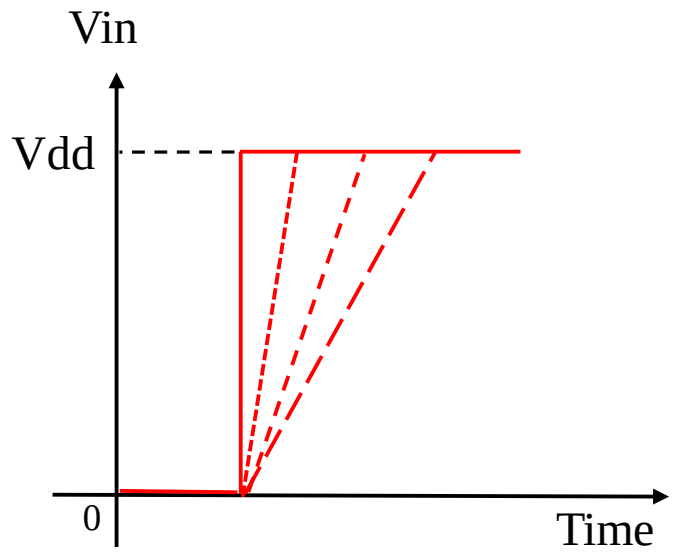
Propagation Delay (Tp) of a gate can be minimized in following ways

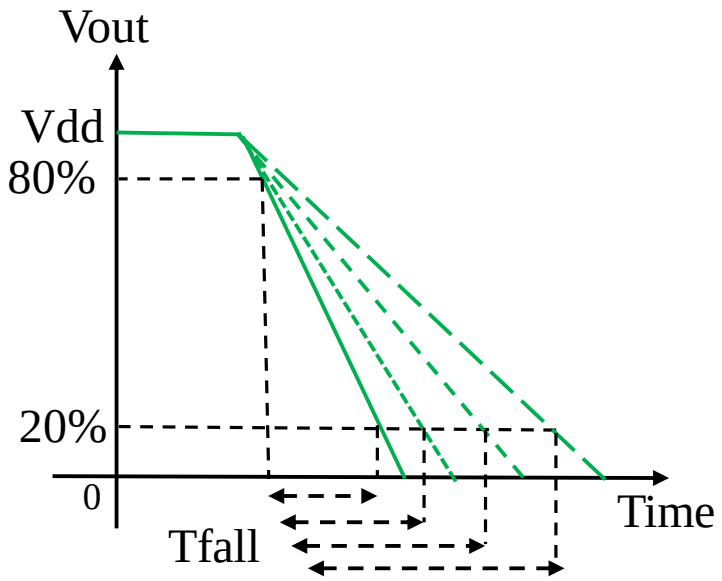
1. Reduce C_L
   - Internal diffusion capacitance
   - Interconnect capacitance
   - Fanout capacitance
2. Increase the $\frac{W}{L}$ ratio of transistors
   - This is most powerful and effective performance optimization tool in the hands of the designer.
   - Be careful, $\frac{W}{L}$ ratio proportional to C_L: once intrinsic capacitance starts dominating C_L increasing gate size does not longer help in reducing the delay.
     - Increase area (self loading)
     - Increase the fanout factor of the driving gate
3. Increase VDD
   - Delay of a gate can be modulated by modifying the supply voltage

CMOS Inverter: Delay Variation with Input Transition and Output Load



ns/pf	C1	C2	C3	C4	C5	C6
Tr1	Value	Value	Value	Value	Value	Value
Tr2	Value	Value	Value	Value	Value	Value
Tr3	Value	Value	Value	Value	Value	Value
Tr4	Value	Value	Value	Value	Value	Value
Tr5	Value	Value	Value	Value	Value	Value
Tr6	Value	Value	Value	Value	Value	Value

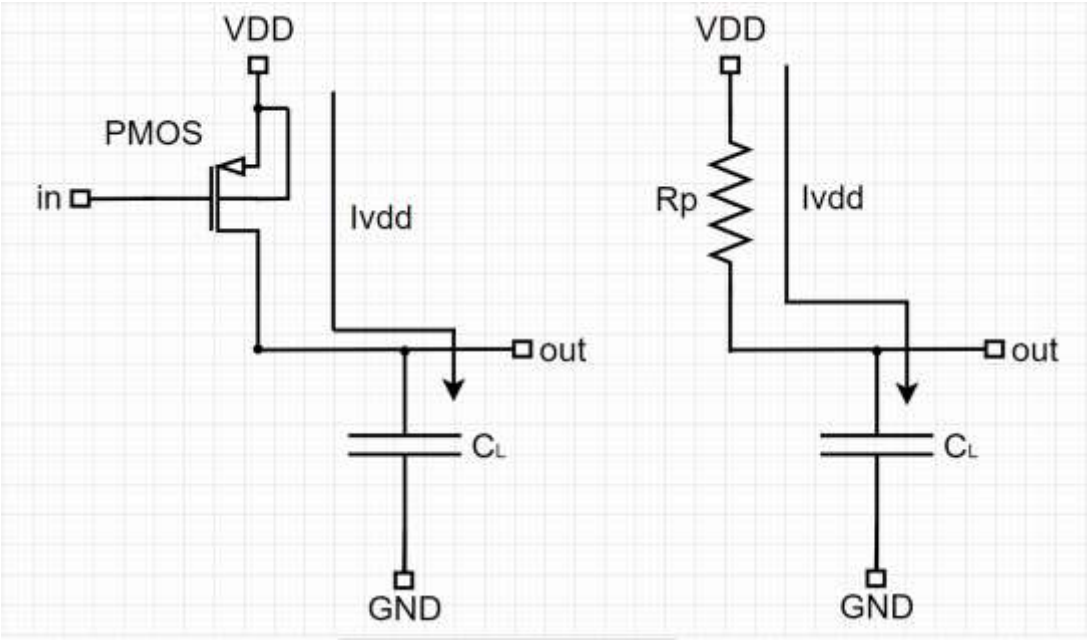




CMOS Inverter: Dynamic Power Consumption

Dynamic power dissipation due to charging and discharging of capacitance.

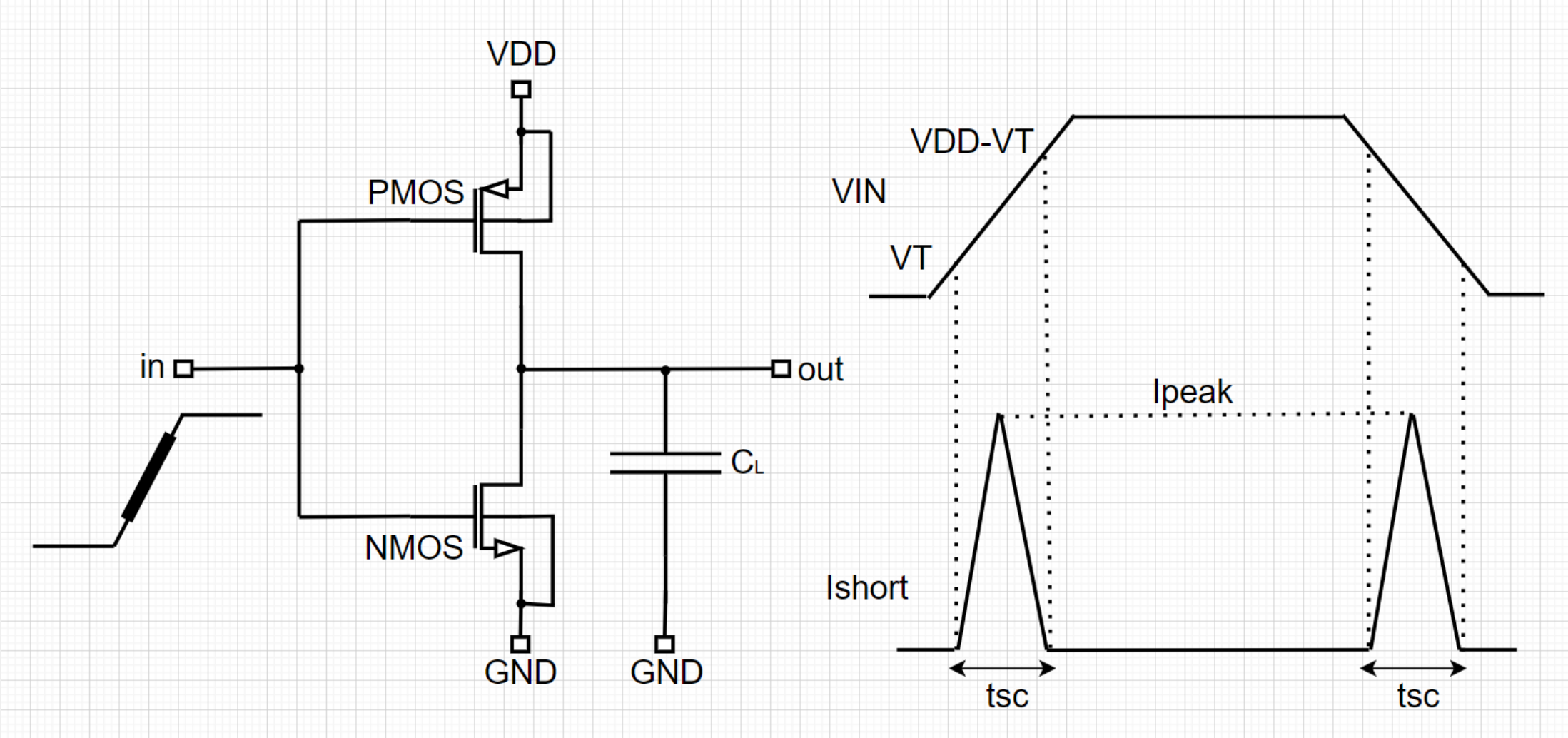
- Each time CL get charged through PMOS, its voltage rises from 0 to VDD.
- Due to this, certain amount of energy is drawn from the power supply.
- Part of this energy dissipated on the PMOS device while the remainder stored in load capacitor.
- During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS device.



- The values of the Energy E_{VDD} taken from the supply during the transition is;
- $E_{VDD} = \int_0^t i_{VDD}(t)\, V_{DD} dt = V_{DD} \int_0^t C_L \frac{dV_{OUT}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dV_{out} = C_L {V_{DD}}^2$
- Energy E_C stored on the capacitor at the end of the transition;
- $E_C = \int_0^t i_{VDD}(t)\, V_{out} dt = \int_0^t C_L \frac{dV_{OUT}}{dt} V_{out} dt = C_L \int_0^{V_{DD}} V_{out} dV_{out} = \frac{C_L {V_{DD}}^2}{2}$
- Only half of the energy supplied by the power source is stored on C_L. The other half has been dissipated in the PMOS transistor.

- If the gate is switched on and off f_{0-1} times per second, the power consumption equals;
- $P_{Dyn} = C_L {V_{DD}}^2 F_{0-1}$, Where F_{0-1} represents the energy consuming transitions.

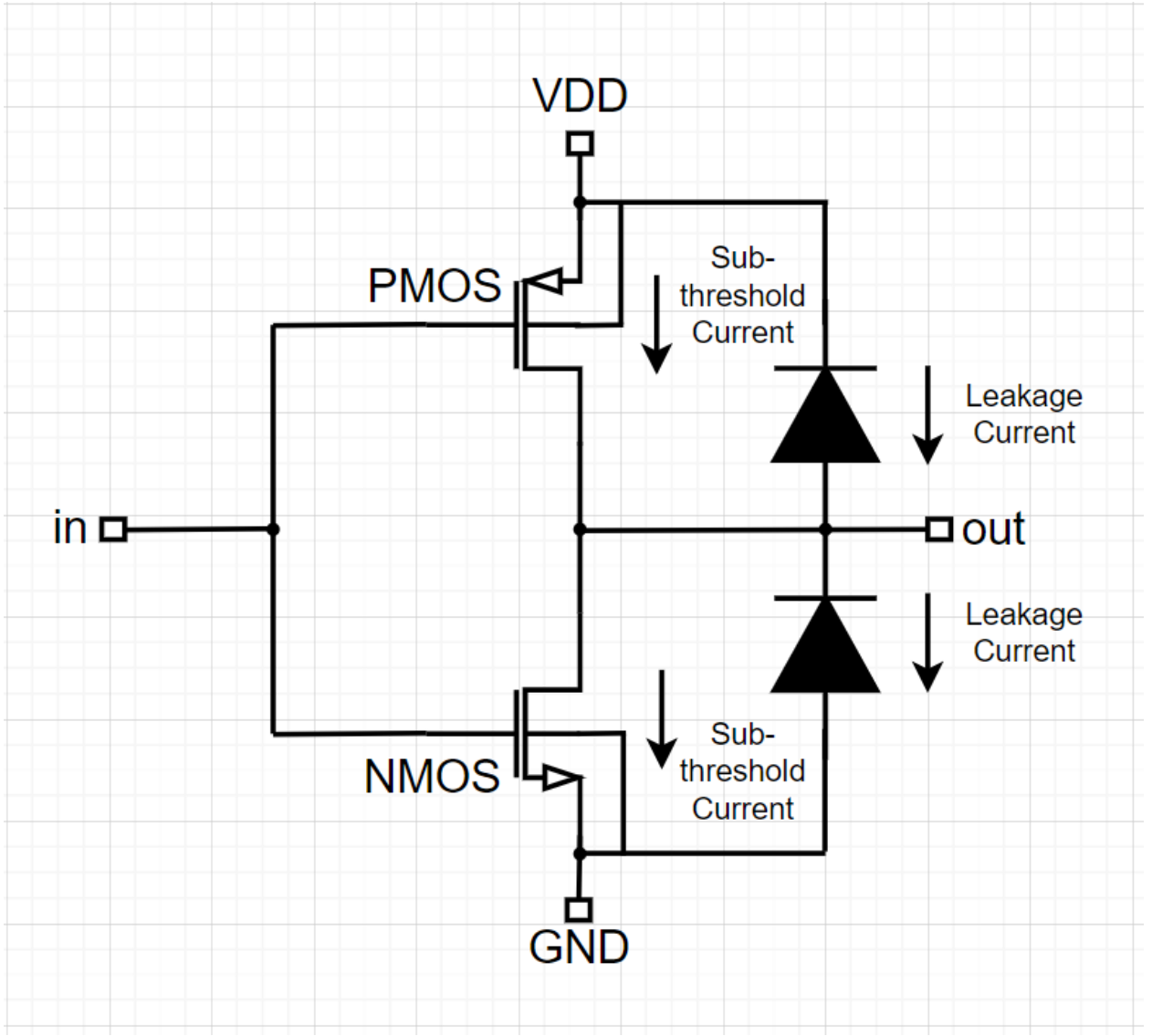
CMOS Inverter: Dissipation due to Direct Path Current



- Energy consume per switching period; $E_{dp} = V_{DD}\frac{i_{peak}}{2}t_{sc} + V_{DD}\frac{i_{peak}}{2}t_{sc} = V_{DD}i_{peak}t_{sc}$
- The average power consumption: $P_{dp} = V_{DD}i_{peak}t_{sc}f = C_{sc}{V_{DD}}^2 f$

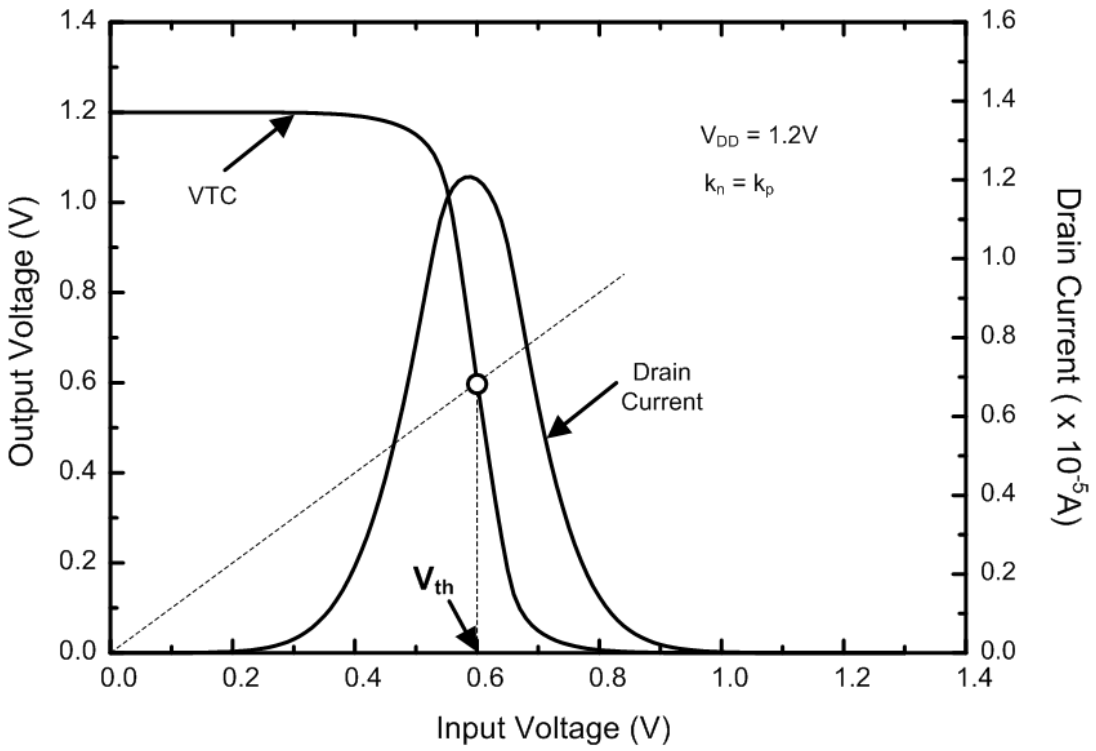
CMOS Inverter: Static Power Consumption

- The static or steady state power dissipation of a circuit is expressed as;
- $P_{stat.} = I_{stat.}V_{DD}$
- Ideally, $I_{stat.} = 0$ as the PMOS and NMOS devices are never on simultaneously in steady state operation.
- But a leakage current flowing through the reverse biased diode junctions of the transistor, located between source and drain and the substrate.
- In general the leakage currents are very small and can be ignored. However the junction currents are caused by thermally generated carriers.
- Sub-threshold Current: Drain-to-source current even when Vgs is smaller than the threshold voltage,



CMOS Inverter: Power Dissipation Summary

- The total power of the CMOS inverter is expressed as the sum of the its three components:
- $P_{Total} = P_{dyn} + P_{dp} + P_{stat.}$
- P_{dyn} = Dominant
- P_{dp} = Can be kept within bounds under the designers control
- $P_{stat.}$ = Ignorable but significant in sub-micron and deep sub-micron technologies.



Simulation Practice: CMOS Characterization

Static Characteristics

1) Draw the voltage transfer characteristic (VTC) curve
2) Draw the VTC curve for symmetrical inverter as well as asymmetrical inverter and check the difference.
3) For different strength of PMOS and NMOS draw the VTC curve and check the shifting od VTC to left or right.
4) Vary the supply voltage and observe the VTC curve
5) Vary the temperature and observe the VTC curve,
6) Draw the drain current thorough the inverter and calculate the static current.

Dynamic Characteristics

1) Do the transient analysis and measure the rise time, fall time and propagation delay.
2) Increase and decrease the device size and again do the same simulation and check the differences.
3) Calculate Tphl and Tplh for both symmetrical and asymmetrical inverter and check the difference.
4) Change the input transition slope and do the simulation and check the rise time, fall time and propagation delay.
5) Change the load capacitance and do the same.
6) From the calculator find the dynamic power consimption

Thank You