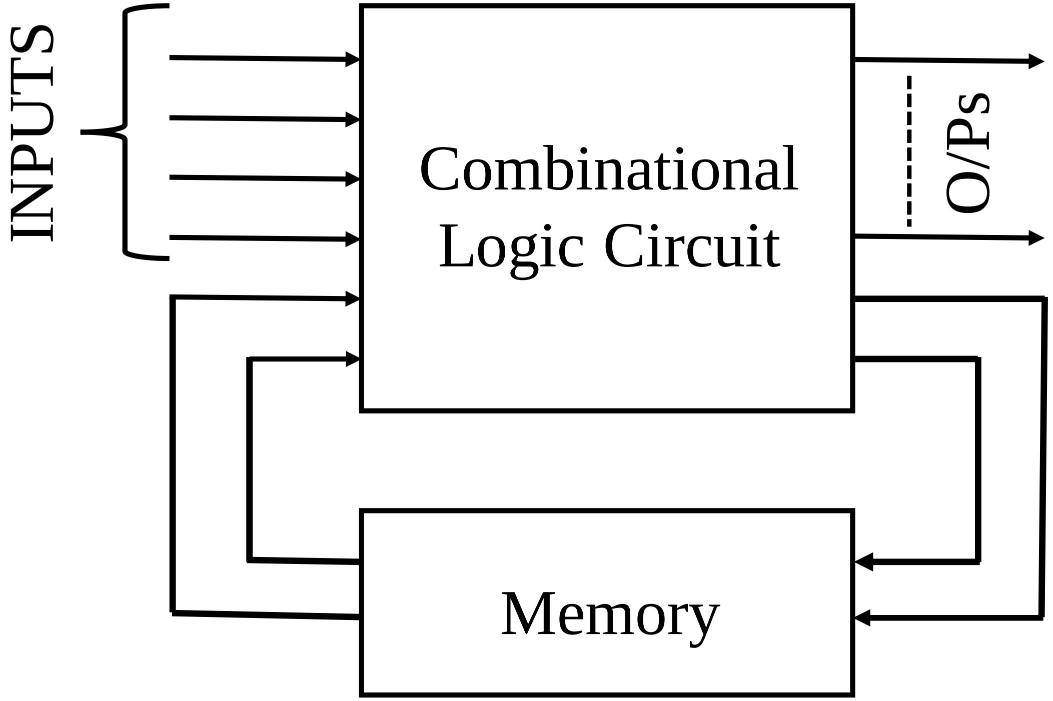
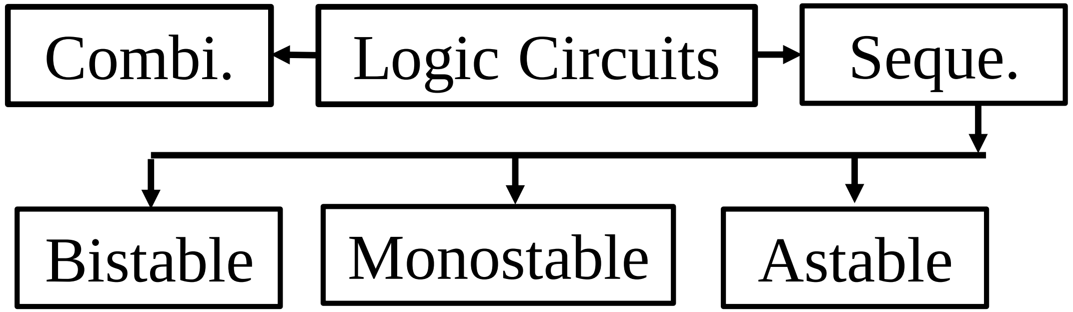
Sequential Digital Logic Circuits

Santunu Sarangi

Sequential Logic Circuit

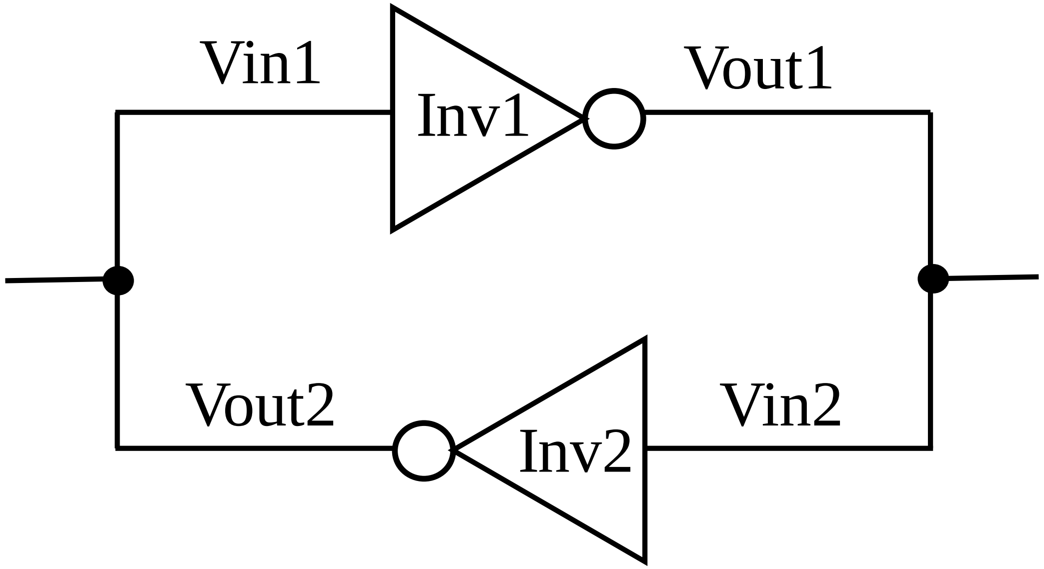
- In sequential logic circuits, the output of the circuit depends upon the current values of the inputs as well as previous input values.
- A sequential circuit remembers some of the past history of the system. It has memory.
- The critical components of sequential systems are the basic regenerative circuits, which can be classified into three main groups;
    - Bistable circuits
    - Monostable circuits
    - Astable circuits
- The bistable circuits are widely used: all the latches, flip-flops, registers and memory elements are made through bistable circuits

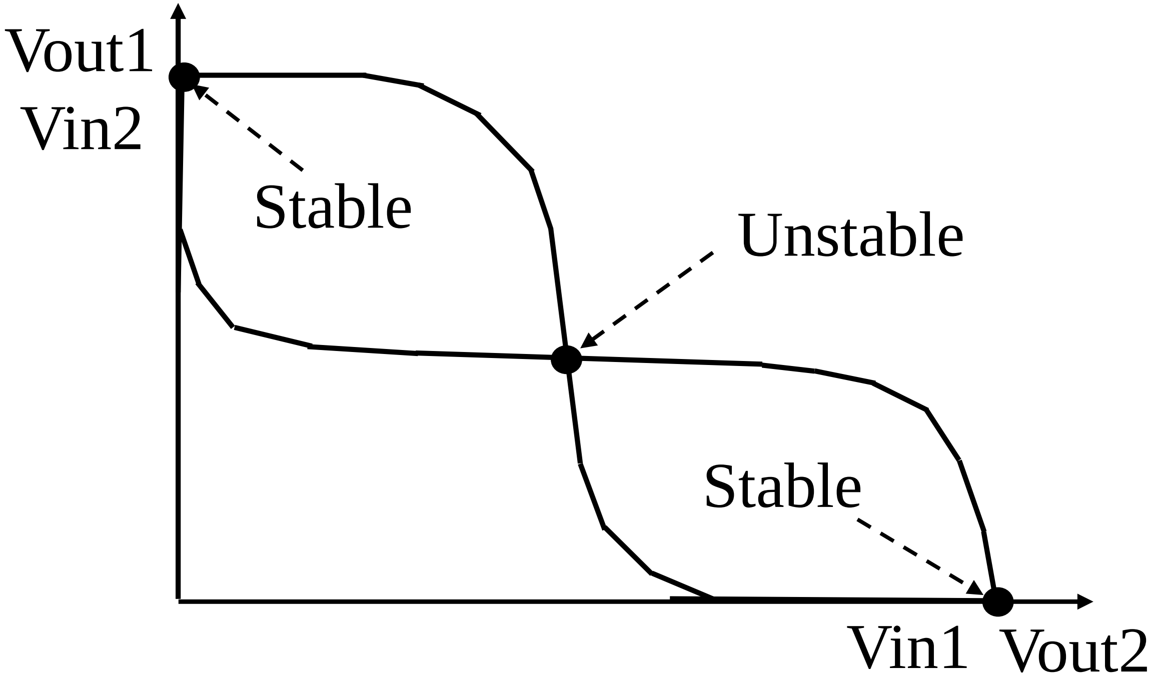




Electrical Behavior of Bistable Circuit

- Bistable circuit has three operating points.
  - 2 stable points
  - 1 unstable point
- If the circuit is initially operating at one of these two stable points, it will preserve this state unless it is forced externally to change its operating points.
- Gain at two stable points are less than 1.
- Gain at unstable point is larger than 1 in both the inverters. That means, a small perturbation at the input of any of the inverters will be amplified, causing the operating point to move to one of the stable operating points.
- Conclusion: The third point is unstable, so the circuit has two stable points, so it is called bistable circuit.

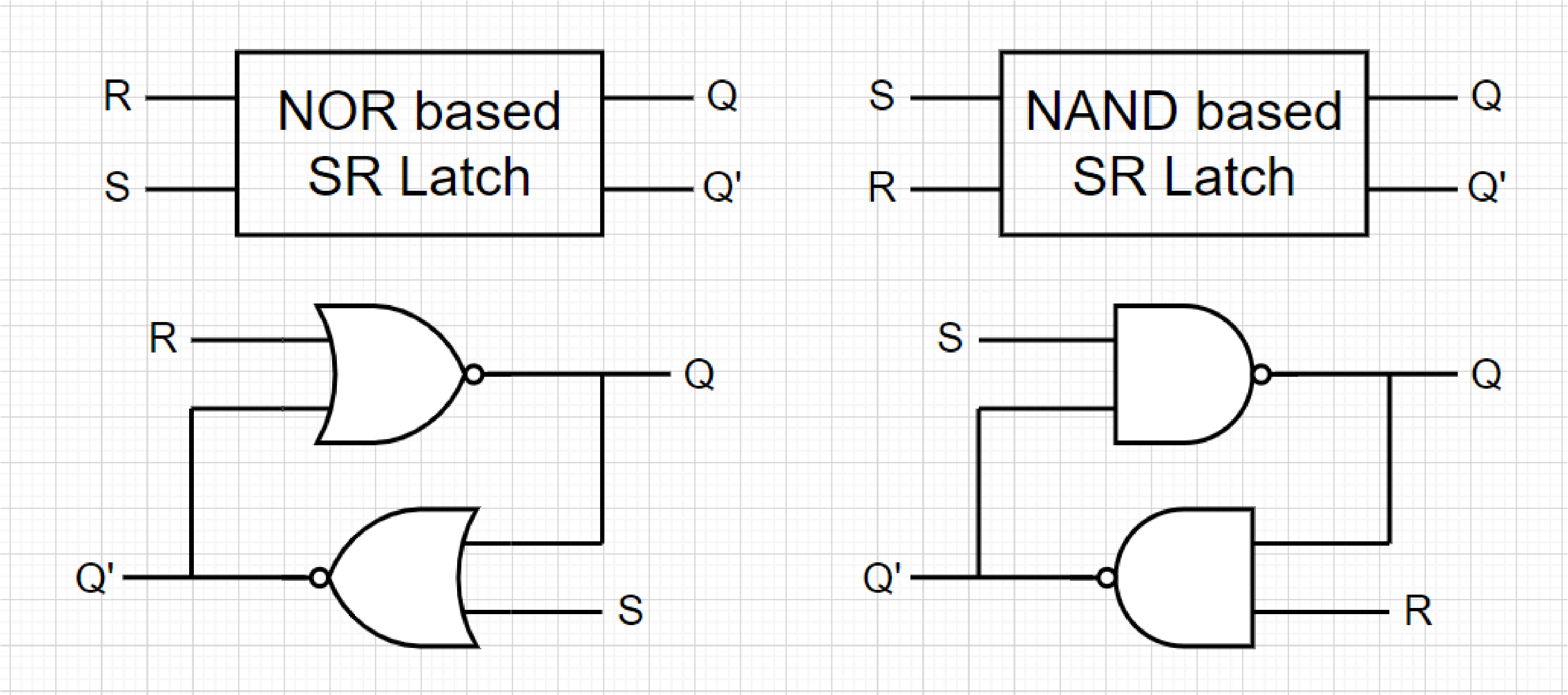




SR Latch

8 number of transistors required to implement.

Separate inputs (R, S) are there to control outputs (Q, Q’)



8 number of transistors required to implement.

Separate inputs (R, S) are there to control outputs (Q, Q’)

No clock or Enable input; Asynchronous

When S=R=1, output invalid

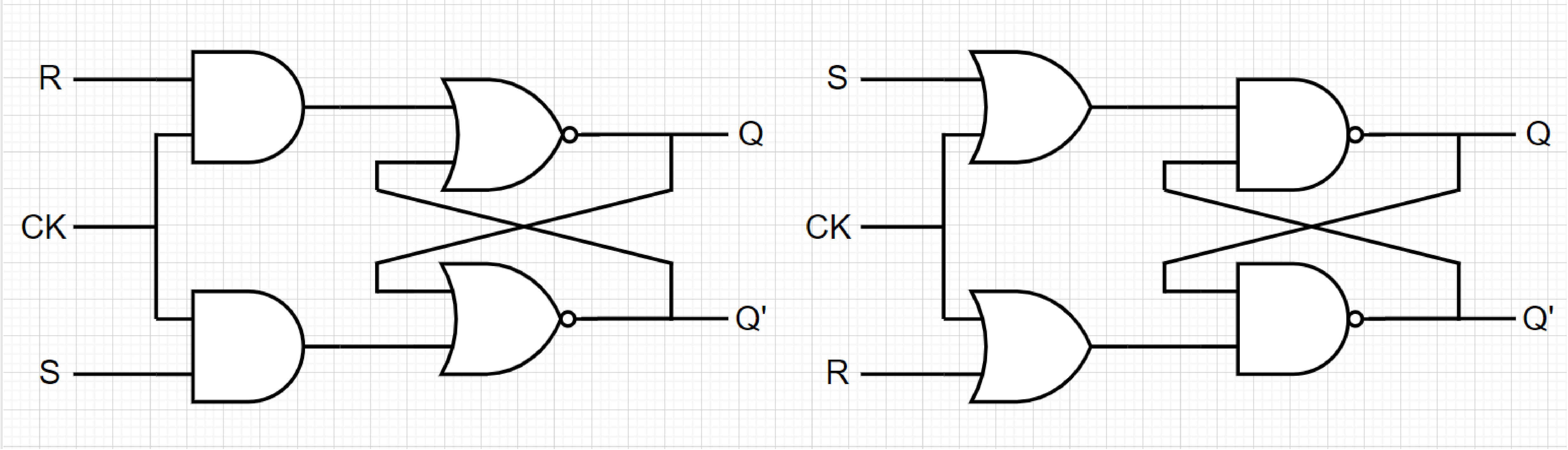
S	R	Q_{n+1}	Q'_{n+1}	$Operation$
0	0	Q_n	Q'_n	Hold
0	1	0	1	Reset
1	0	1	0	Set
1	**1**	**0**	**0**	**Invalid**

S	R	Q_{n+1}	Q'_{n+1}	$Operation$
0	**0**	**1**	**1**	**Invalid**
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q_n	Q'_n	Hold

No clock or Enable input; Asynchronous

When S=R=0, output invalid

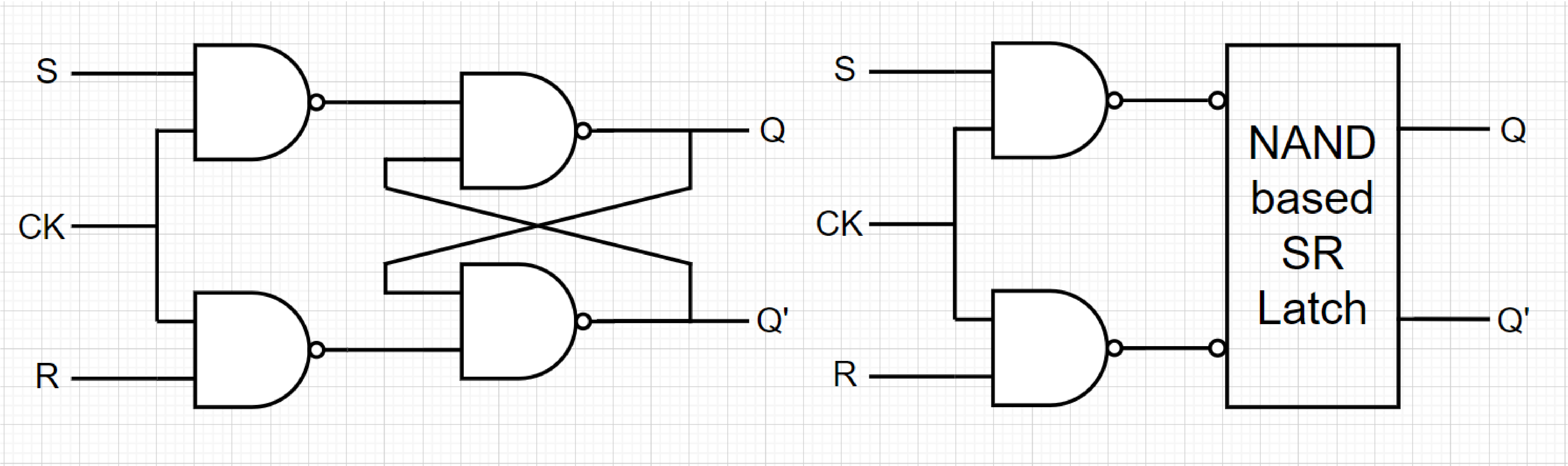
Clocked SR Latch



- NOR-based SR Latch circuit with active HIGH inputs.
- CLK=0, the input signal has no influence on the circuit.
- CLK=1, logic levels applied to S and R inputs are permitted to reach the SR logic.

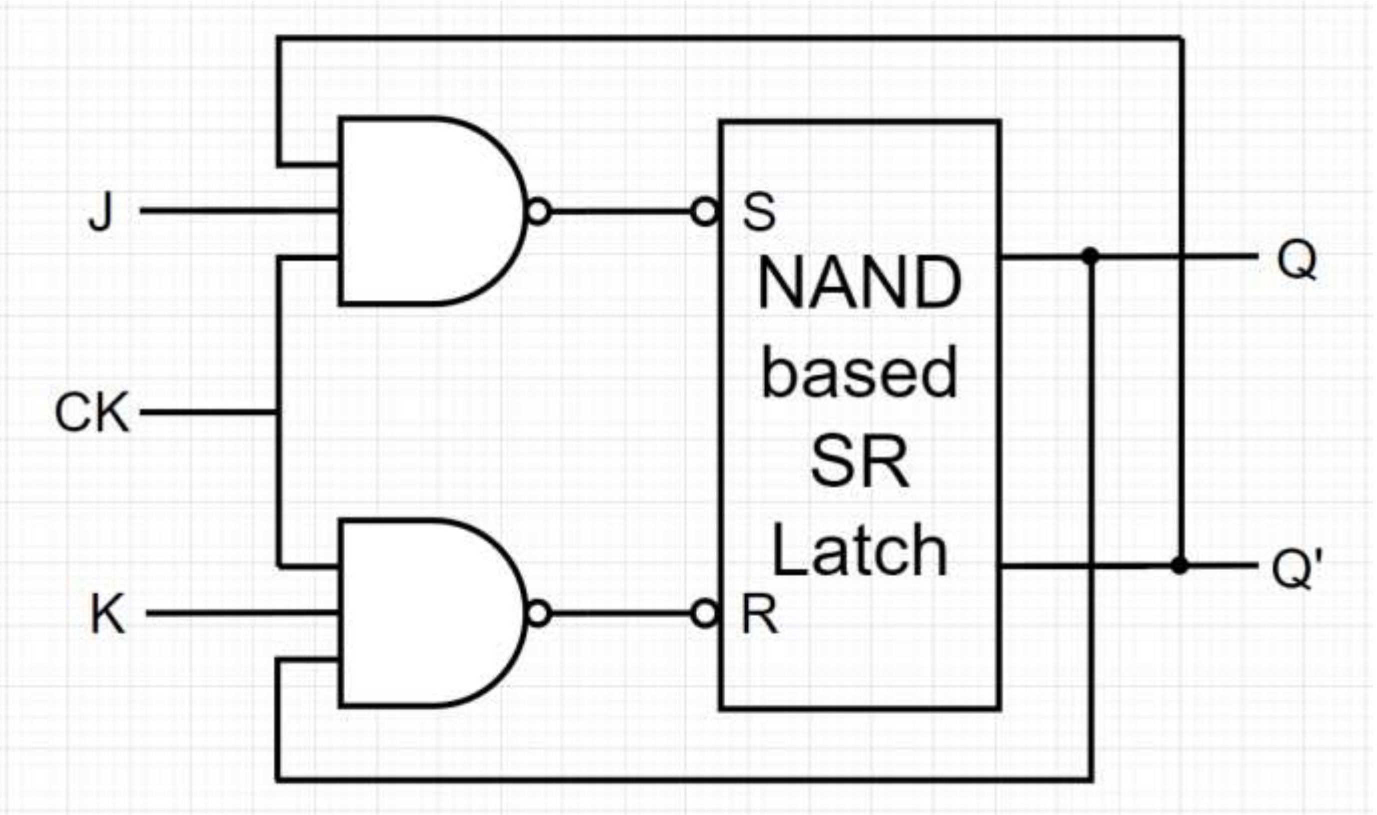
- NAND-based SR Latch circuit with active LOW inputs.
- CLK=0, the input signal has no influence on the circuit.
- CLK=1, logic levels applied to S and R inputs are permitted to reach the SR logic.

NAND Based Clocked SR Latch with Active HIGH Inputs



- Transistor count is high

JK Latch

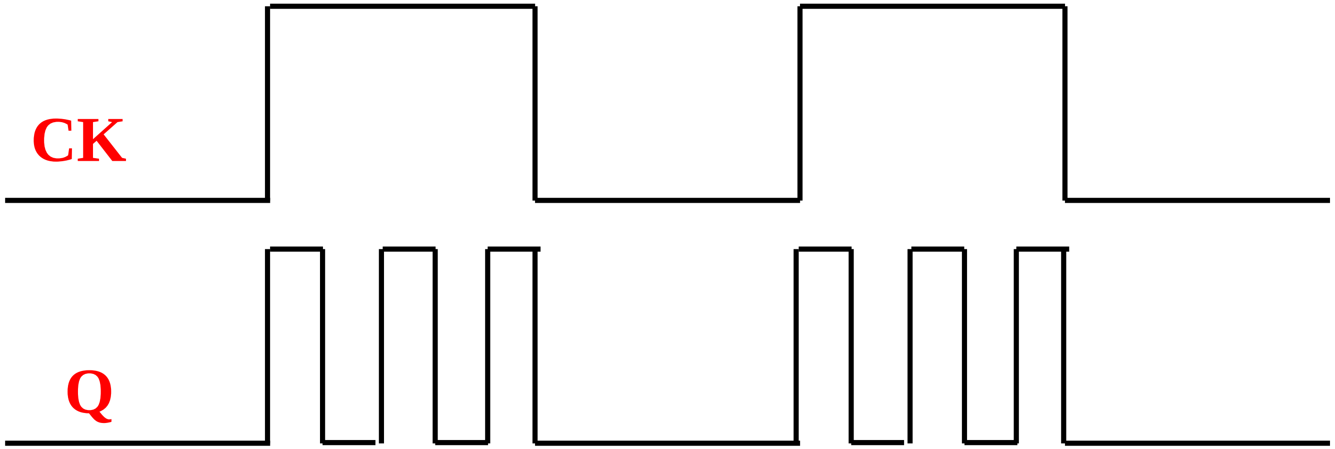


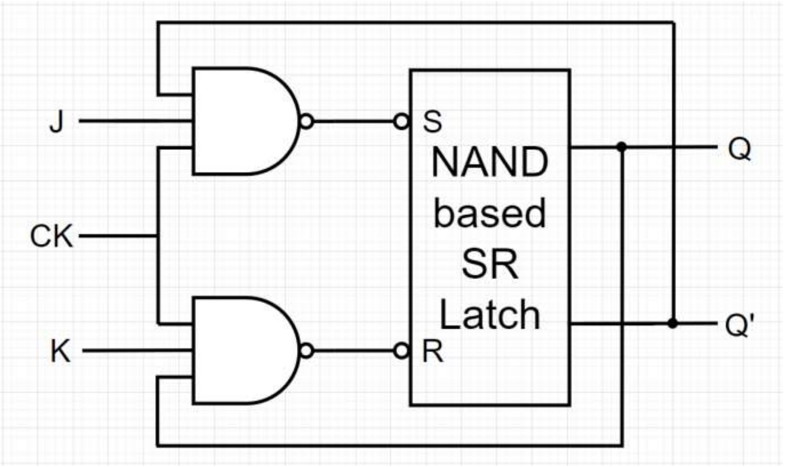
J	K	Q_n	Q'_n	S	R	Q_{n+1}	Q'_{n+1}	$operation$
0	0	0	1	1	1	0	1	Hold
		1	0	1	1	1	0	Hold
0	1	0	1	1	1	0	1	Reset
		1	0	1	0	0	1	Reset
1	0	0	1	0	1	1	0	Set
		1	0	1	1	1	0	Set
1	1	0	1	0	1	1	0	Toggle
		1	0	1	0	0	1	Toggle

- If both inputs are equal to logic 1 during the active phase of clock pulse, the output of the circuit will oscillate (toggle) continuously until either the clock becomes inactive (goes to zero), or one of the input signals goes to zero
- To prevent this undesirable timing problem, the clock pulse width must be made smaller than the input-to-output propagation delay of JK Latch circuit.

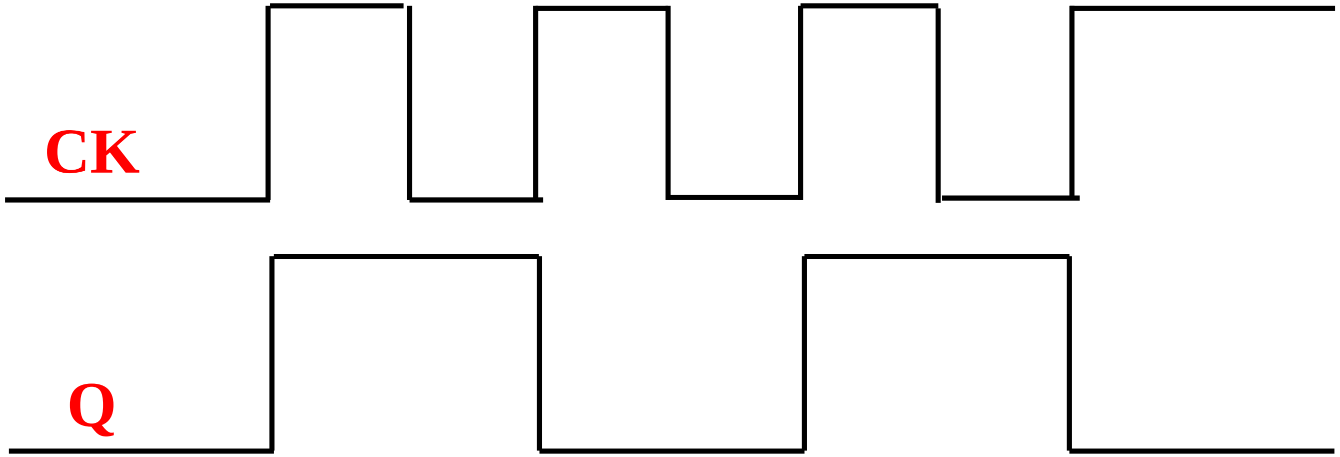
JK Latch

Case1: Clock period is much higher than the propagation delay of JK Latch

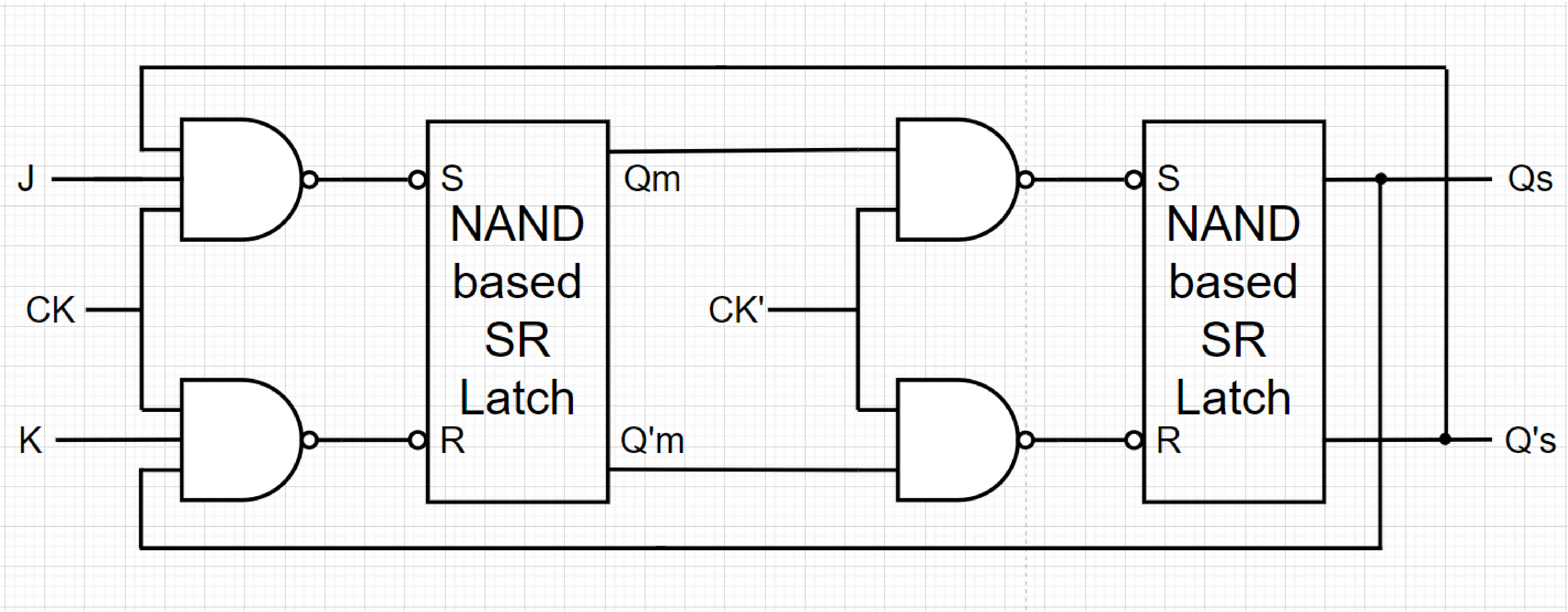




Case2: Clock period is same as the propagation delay of JK Latch

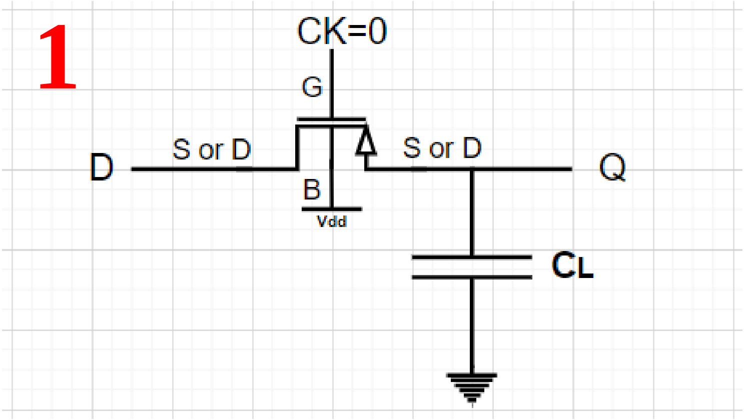


Master-Slave JK Flip-Flop

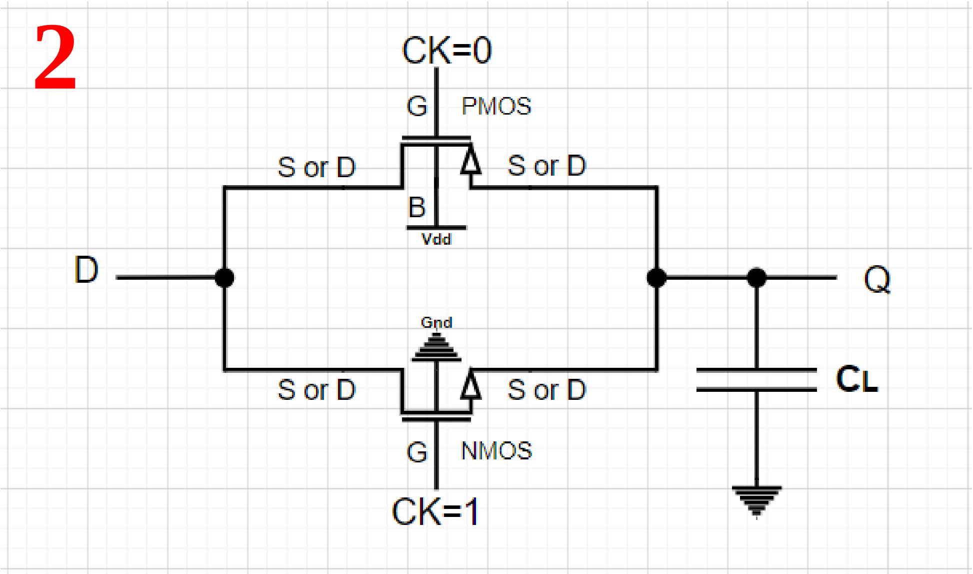


- Most of the timing limitations encountered in JK Latch can be prevented by using two latch stages in cascaded configuration.
- The input latch, called Master is activated when the clock pulse is high
- The output latch is called slave is activated when the clock pulse is low.

Conventional CMOS Latches

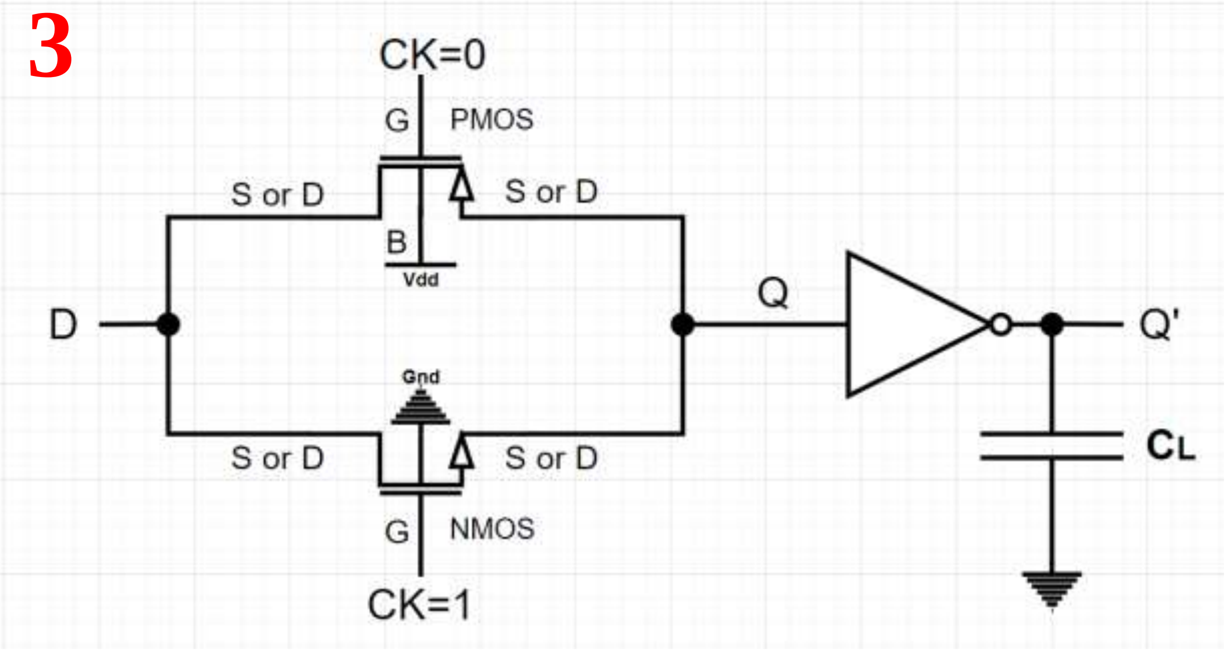


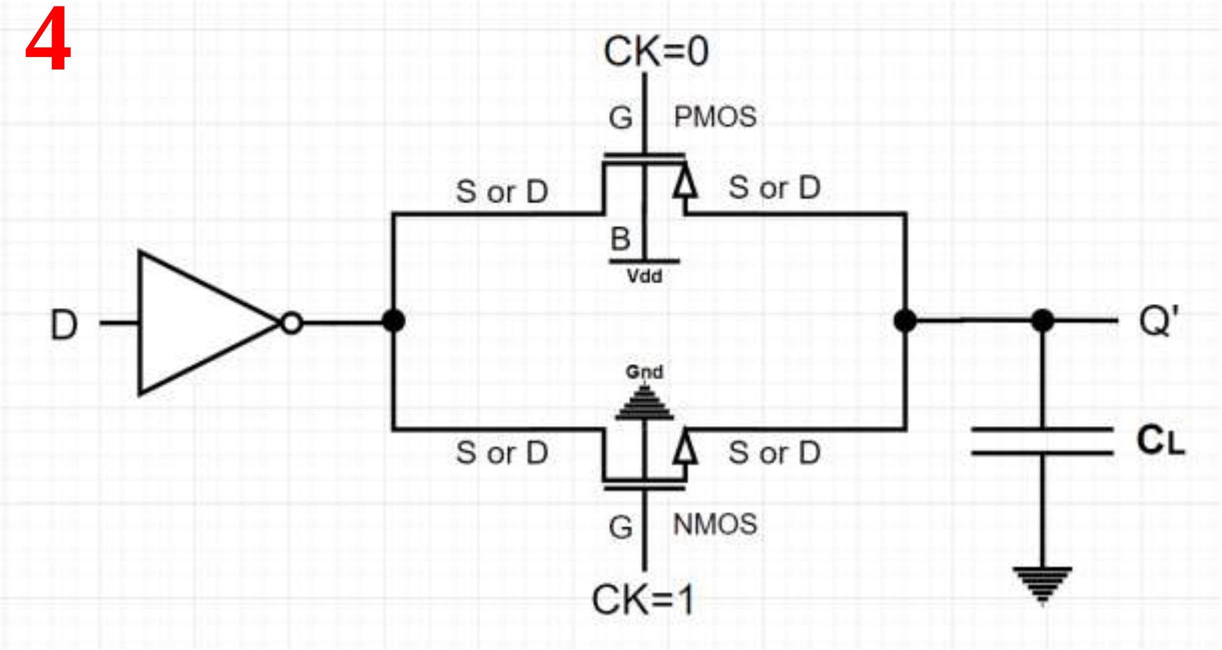
- Very simple transparent latch built from a single transistor
- Advantages:
  - Compact and Fast
- Disadvantages:
  - Output swing is not rail-to-rail
  - The output is dynamic: floats when the latch is opaque
  - D drives the diffusion input
  - The state node is exposed, so noise on the output can corrupt the output.



- Very simple transparent latch built from a single transistor
- Advantages:
  - Rail-to-rail swing
  - Fast
- Disadvantages:
  - Two clock input required

Conventional CMOS Latches





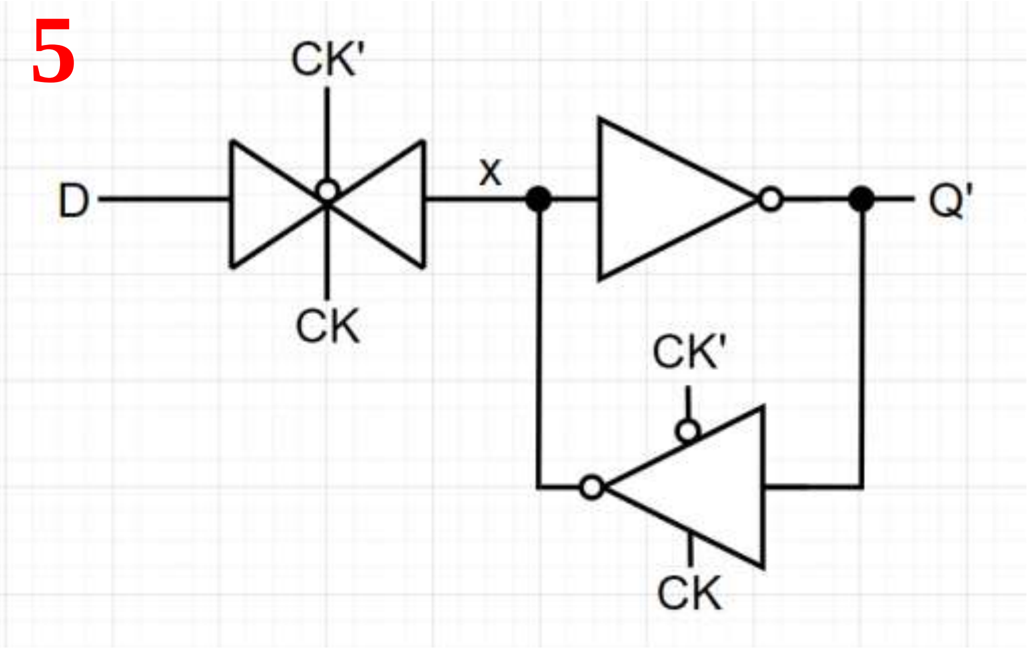
- Advantages:
  - State node Q isolates from output
  - It is also act as an inverting latch

- Advantages:
  - Buffered input but unbuffered output
  - It is also act as a tri-state buffer

- Bothe 3 and 4 are fast dynamic latches
- In modern processes, subthreshold leakages are large enough that dynamic nodes retain their values for only a short time, especially at the high temperature.
- Therefore practical latches need to be staticized adding feedback to prevent the output from floating.

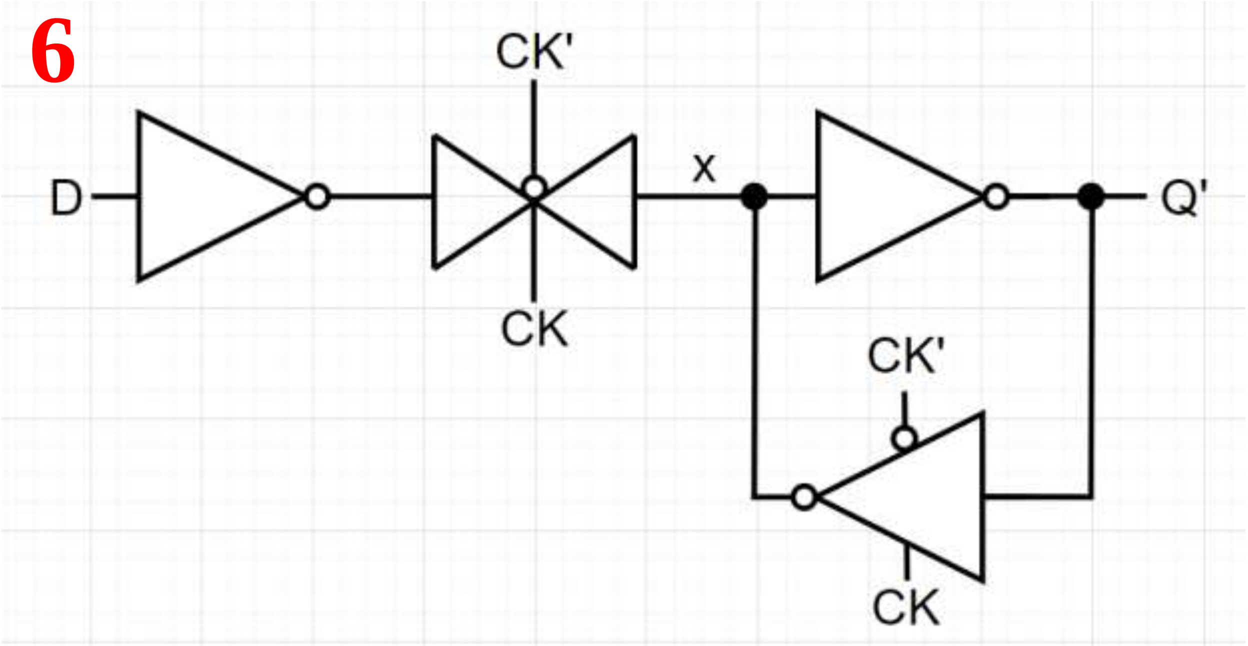
Conventional CMOS Latches

5



- CK=1, input TG is ON, and feedback tri-state is OFF, and latch is transparent.
- When CK=0, input TG is OFF, tri-state is ON, holding X at correct level.

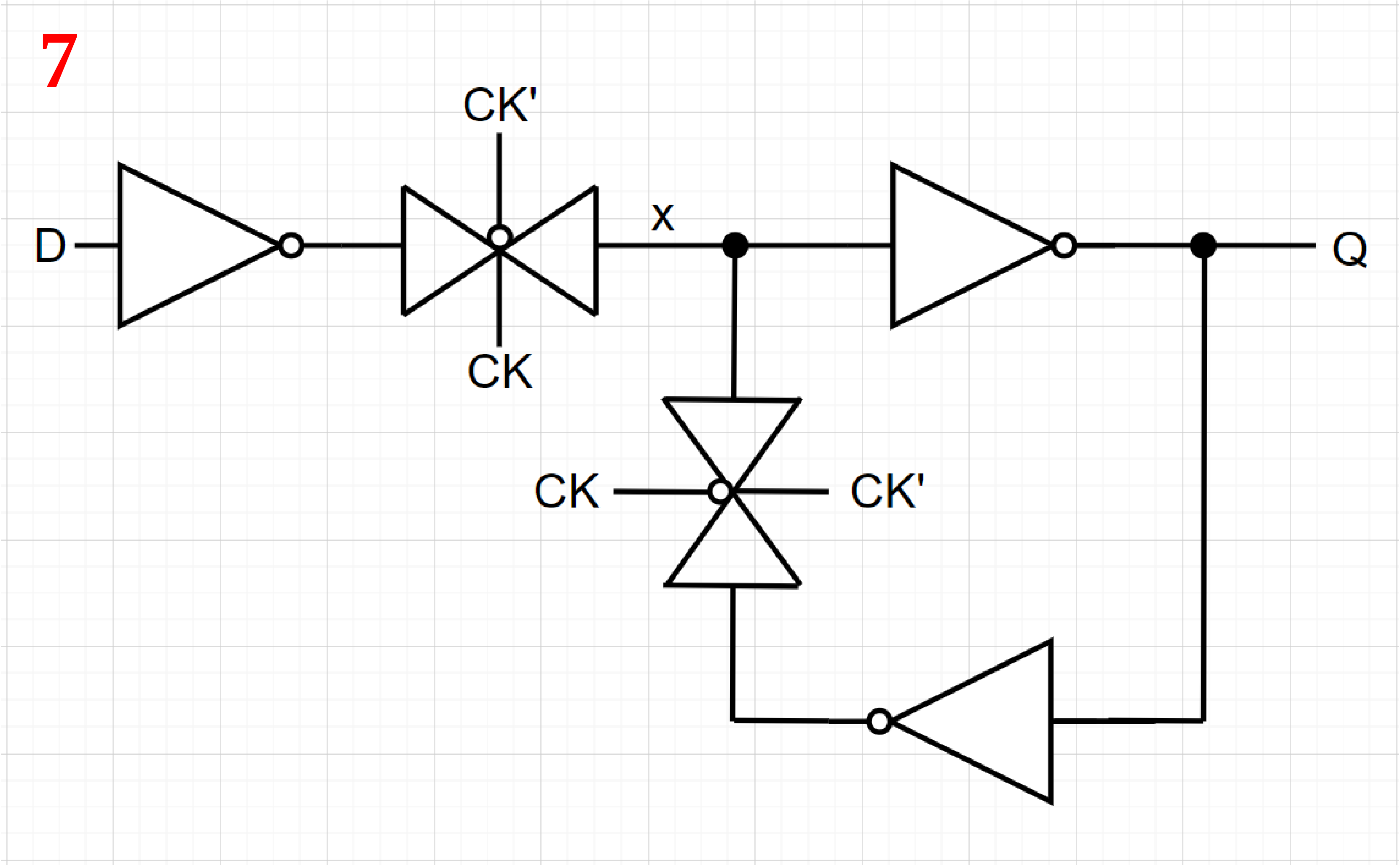
6



- Adds an inverter at the input, so the input is a transistor gate rather than unbuffered diffusion.
- CK=1, input TG is ON, and feedback tri-state is OFF, and latch is transparent.
- When CK=0, input TG is OFF, tri-state is ON, holding X at correct level.

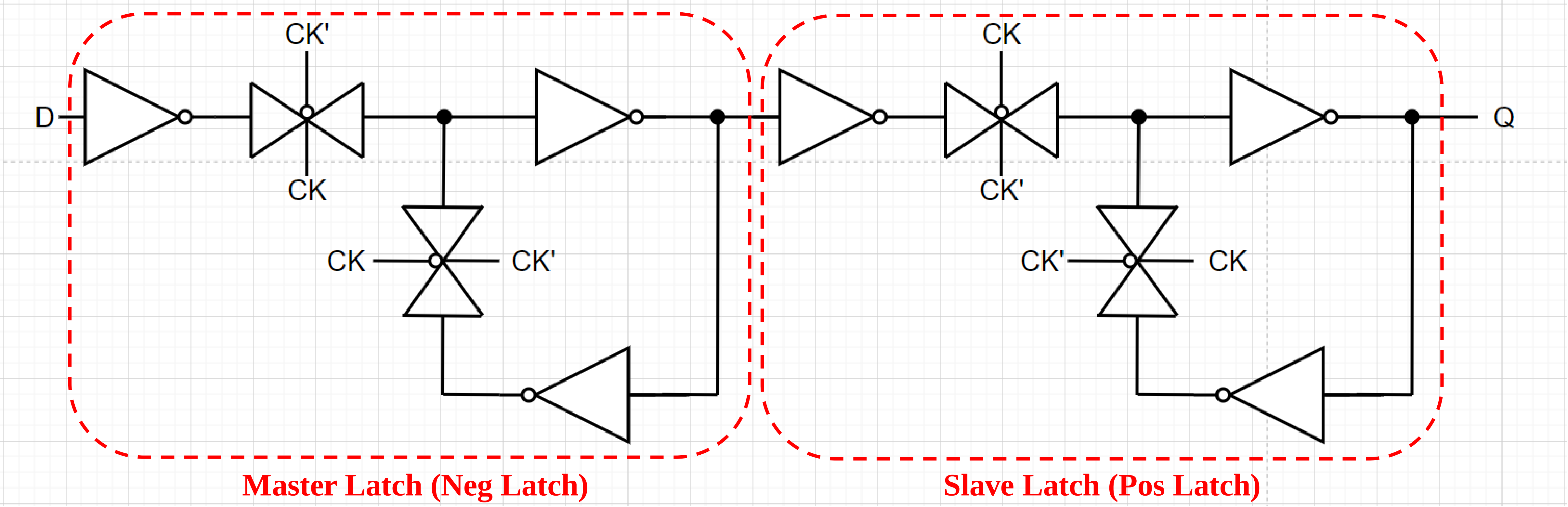
- Unfortunately, both 5 and 6 reintroduced output noise sensitivity; a large noise spike on the output can propagate backward through the feedback gate and corrupt the state node x.

Conventional CMOS Latches



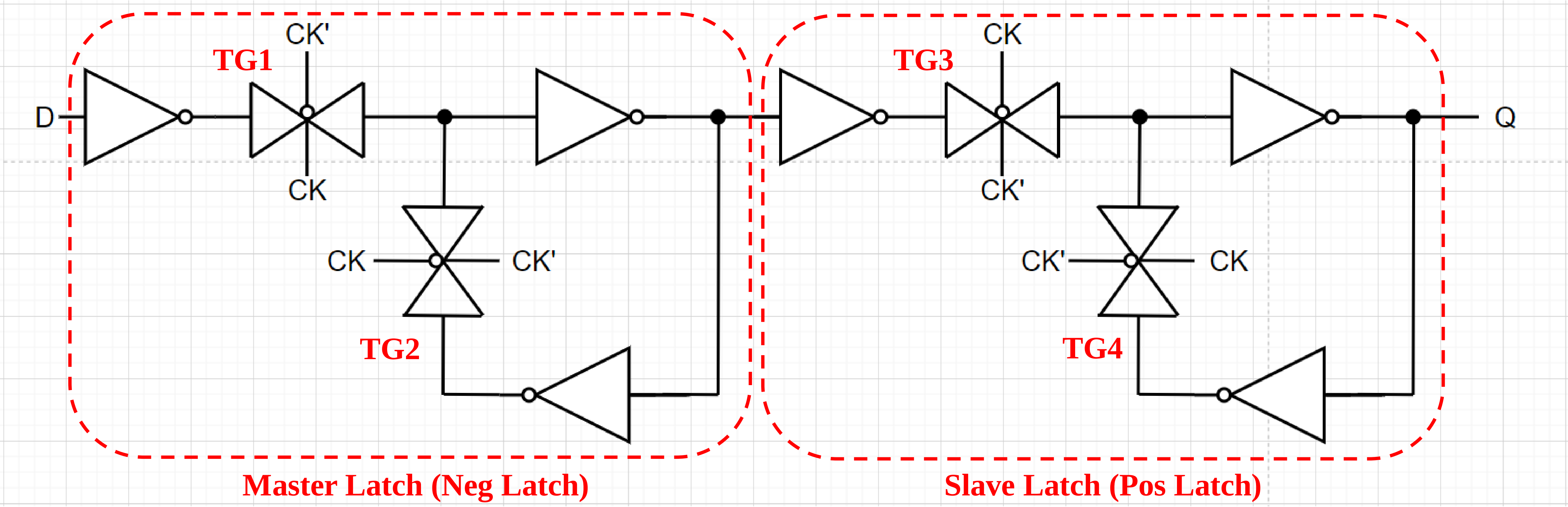
- This is the robust transparent latch that addresses all of the deficiencies mentioned so far.
  - The latch is static
  - All nodes swing rail-to-rail
  - Sate noise isolated from output noise
  - Input drives transistor gate rather than diffusion.

Structure of D-FF



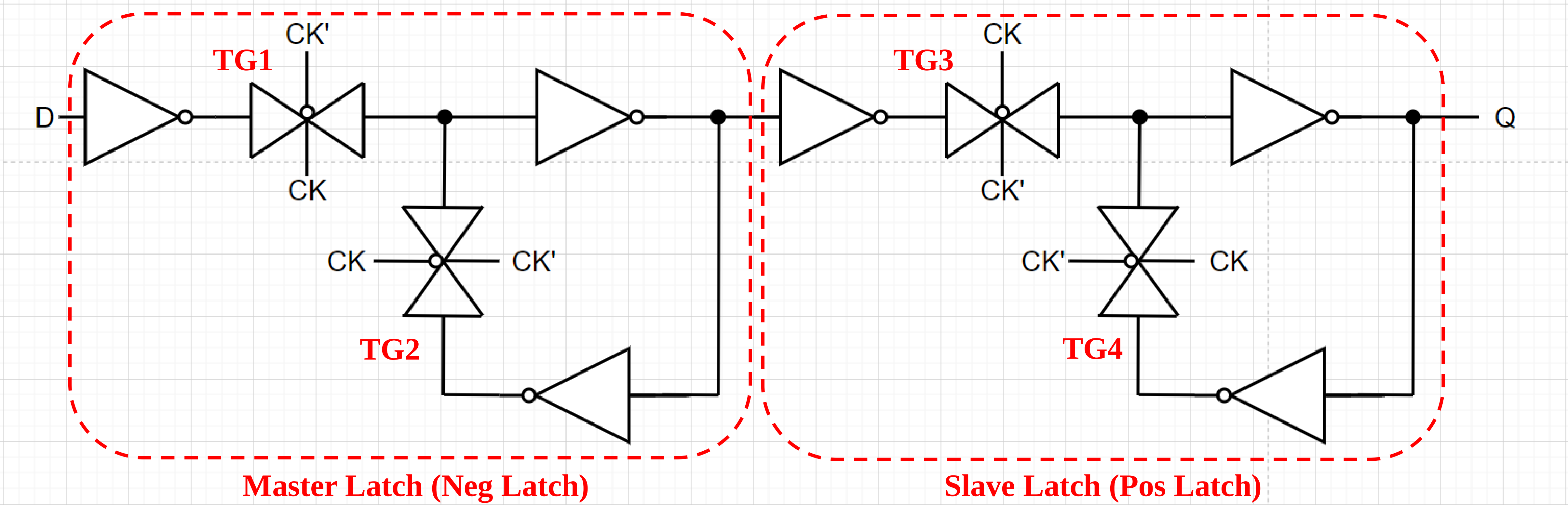
- Flip-flop building blocks include Inverters and Transmission gates.
  - Inverter inverts the signal
  - Transmission gate passes the signal
- This is a positive edge D-Flip-flop
- Here the Master Latch is a Negative Level Latch and the Slave Latch is a Poitive Level Latch.

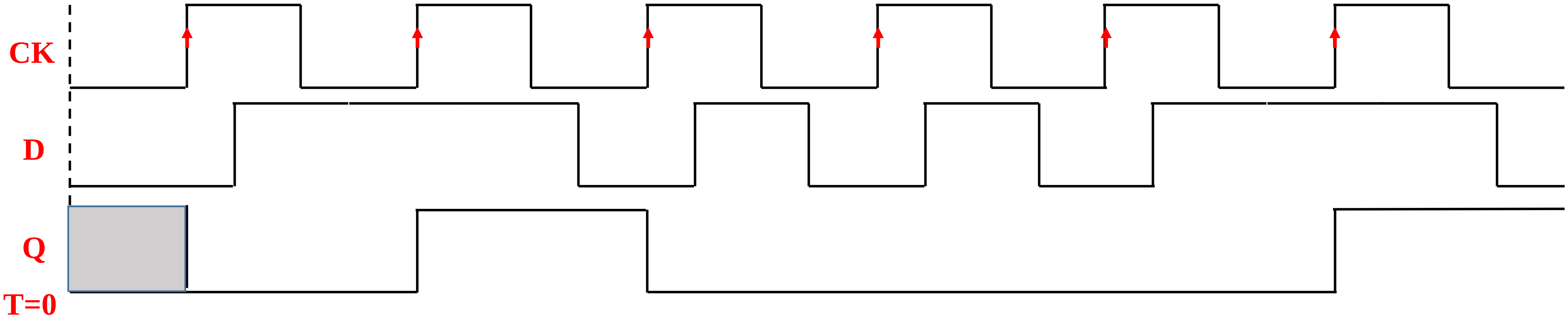
Basic Operation of D-FF



- Case1: CK=Low
  - TG1 is OFF and TG2 is ON, Master latch is latch mode.
  - TG3 is ON and TG4 is OFF, Slave latch in transparent mode. So Q=D
- Case2: CK=High
  - TG1 is ON and TG2 is OFF, Mater latch is transparent mode,
  - TG3 is OFF and TG4 is ON, Slave latch is in latch mode. So Q= Last data

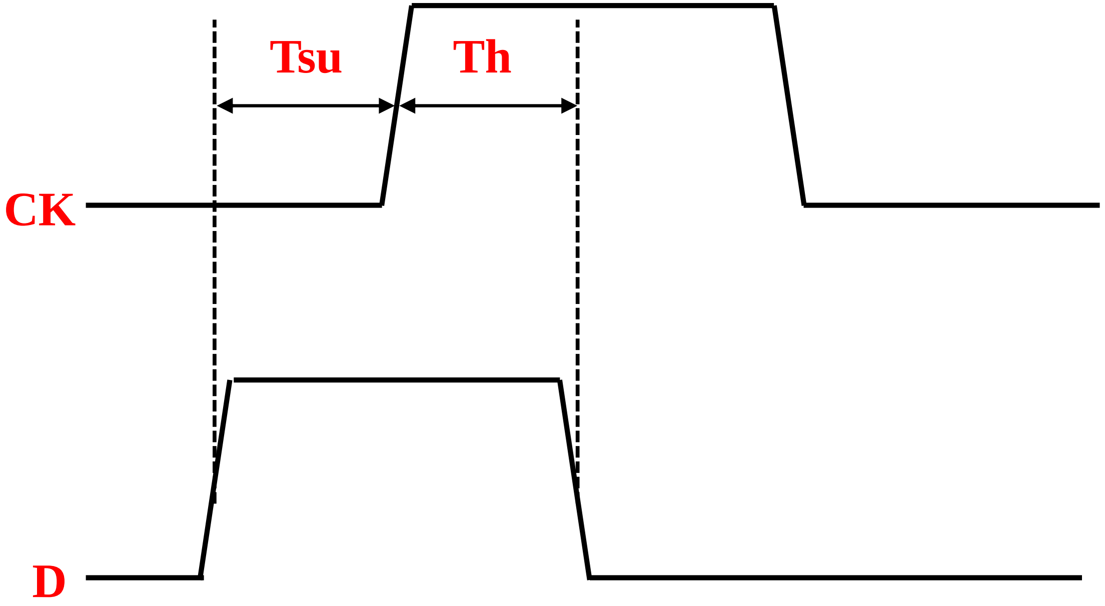
Basic Operation of D-FF





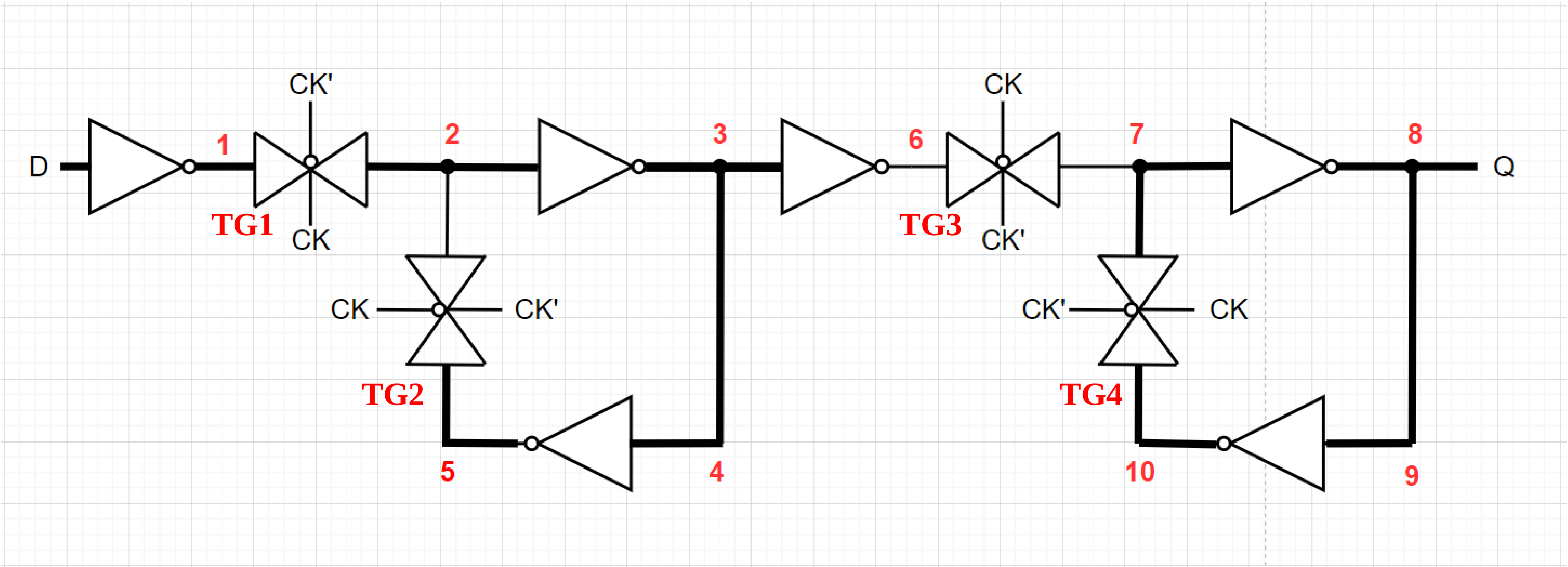
Setup and Hold Time

- **Setup Time:** It is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly.
- Any violation may cause incorrect data to be captured, which is known as setup violation.
- **Hold Time:** It is defined as the minimum amount of time after the clock's active edge during which data must be stable.
- Violation in this case may cause incorrect data to be latched, which is called as hold violation.



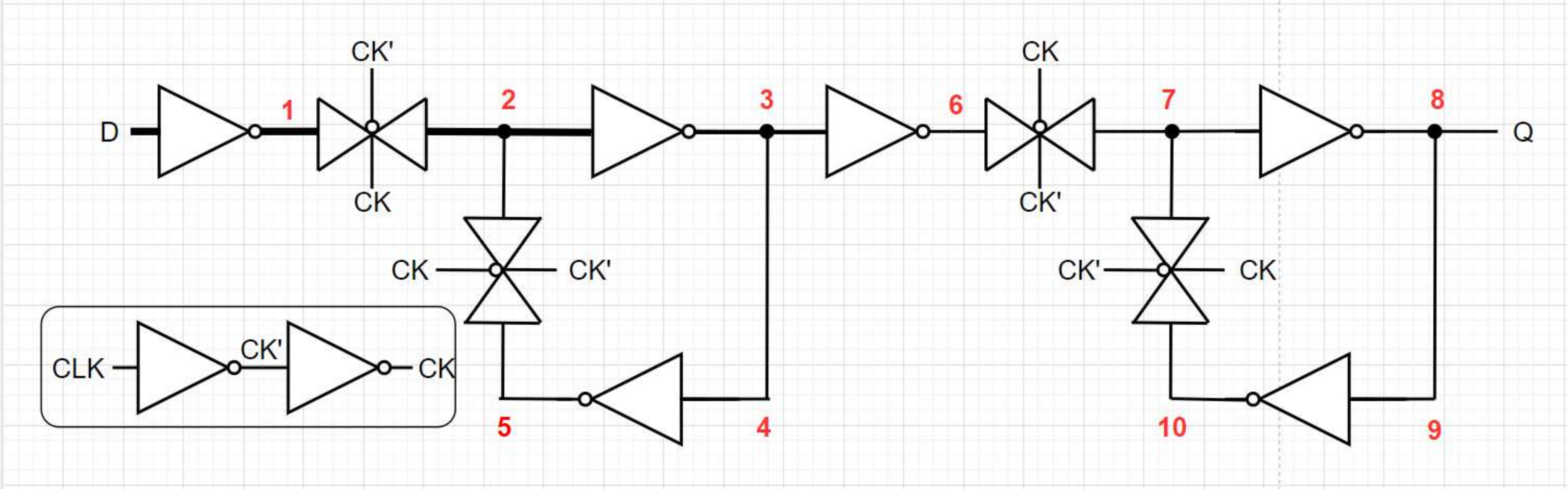
Tsu: Setup Time
Th: Hold Time

Reason for Setup Time



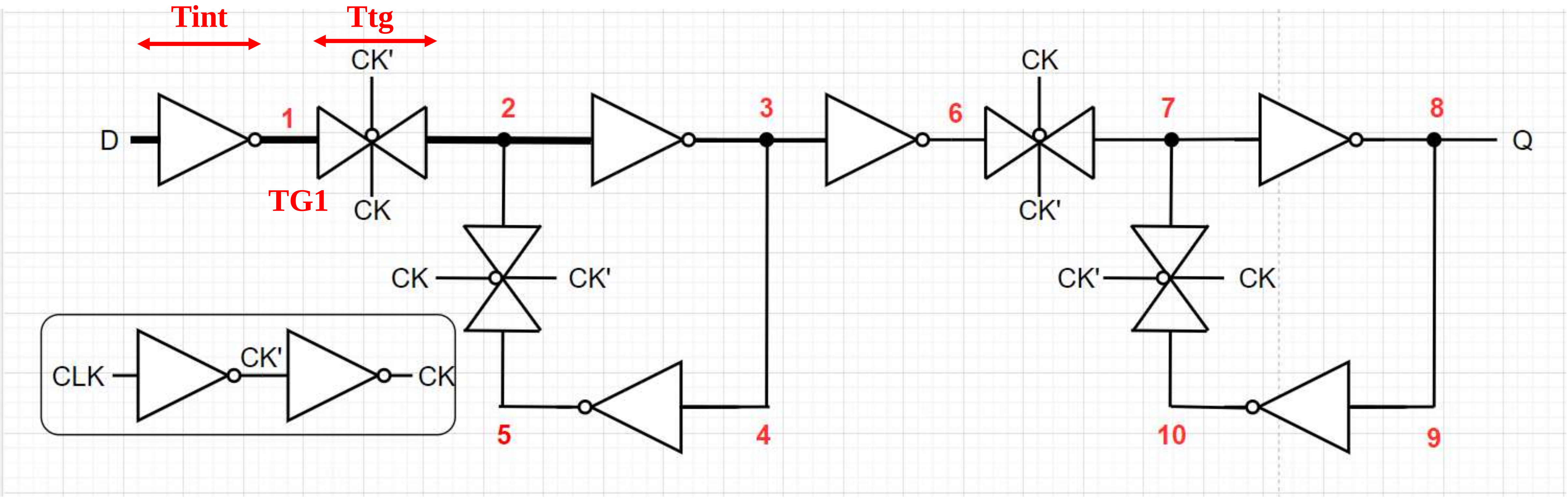
- When CK=High, input D is traverse through 1-2-3-4 and reflected at node 5 after some time.
- The time that it takes D to reach node 5 is called the setup time.
- When CK=Low, TG1 is switched OFF and TG2 is switched ON. Therefore, the LHS latching circuit kicks into action latching the value present at node D and producing it in the output (Q=D)
- Any data sent before the setup time, will produce a stable value at node 5. This defines the reason for the setup time within a flop.

Reason for Hold Time



- D given to the inverter or any other logic sitting before TG1, is a part of the flip-flop.
- The CK and CK’ control the TG, comes after buffers and inverters as shown in figure.
- There is a finite delay between the CK and CK’, so TG takes some time to ON or OFF.
- In the mean time it is necessary to maintain a stable value at the input to ensure a stable value at node-2, which in turn translates to the output defining the reason for hold time.

Hold Time Analysis



- **Tint:** Time delay introduced by combinational gates before TG1
- **Ttg:** Time taken for the transmission gate to switch ON or OFF.
- The relationship between Tint and Ttg gives rise to various types of hold time that exists;
  - Case1: Ttg > Tint → Positive hold time
  - Case2: Ttg = Tint → Zero hold time
  - Case3: Ttg < Tint → Negative hold time

Assignment

- Design SR latch, check the functionality and plot the timing diagram (CK, S, R and Q)
- Design JK Latch, check the functionality and plot the timing diagram.
- Design Master-Slave JK flip-flop and plot the timing diagram
- Design CMOS D-Latch, check the functionality and draw the timing diagram
- Design CMOS D-FF and plot the timing diagram
- Simulate D-FF and calculate the setup and hold time.

Thank You