MOSFET Parameter Extraction, Scaling, Short Channel Effects and PVT Variations

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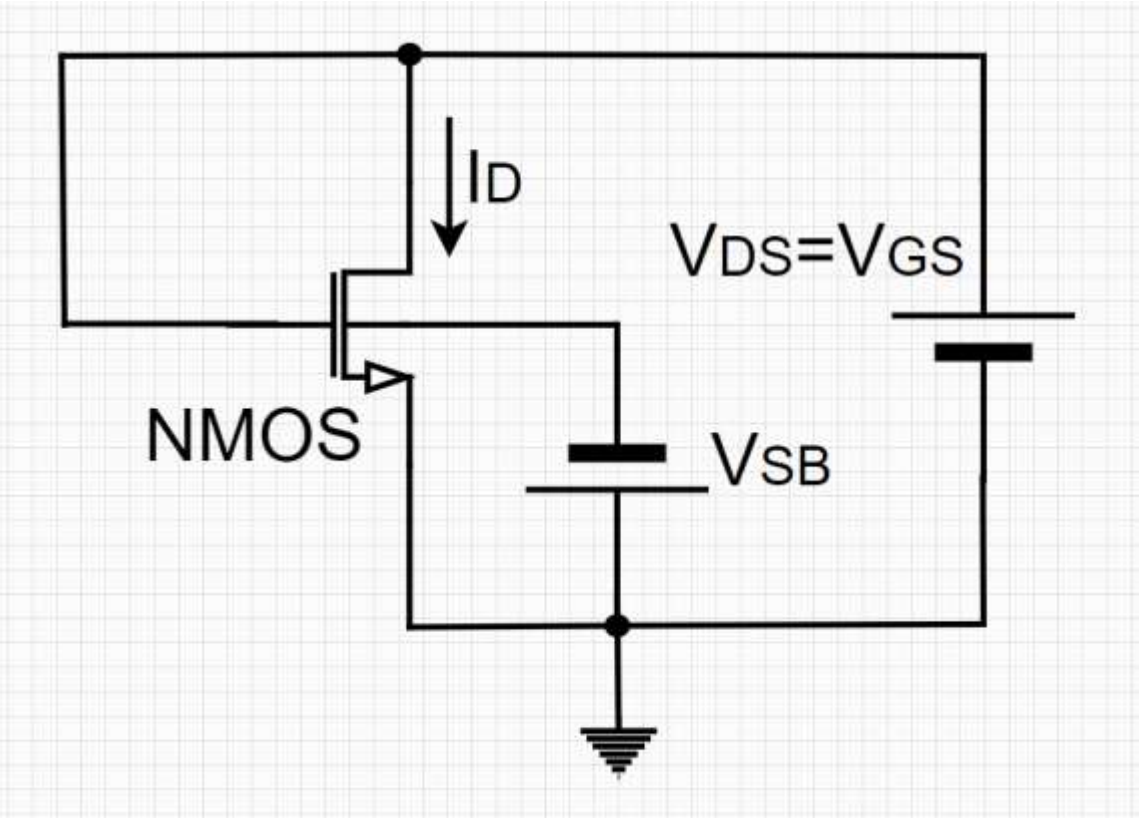
MOSFET Parameter Extraction

MOSFET Parameter Extraction: Large Signal Model Parameters

MOSFET Level1 Model Parameters:

1. V_{T0}: Zero body biased threshold voltage
2. γ (GAMMA): Body bias parameter
3. λ (LAMBDA): Channel length modulation parameter
4. k_n (KN): Transconductance parameter
5. ϕ_f (PHI): Surface Potential



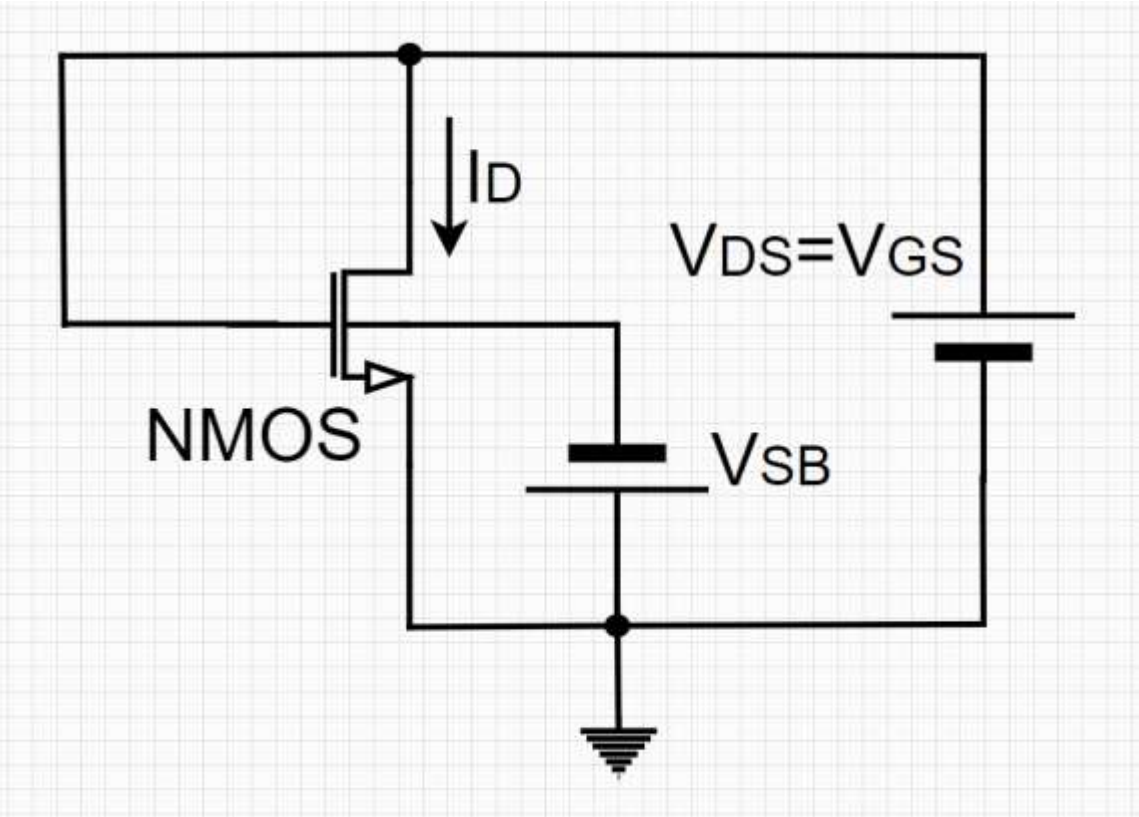
MOSFET Parameter Extraction

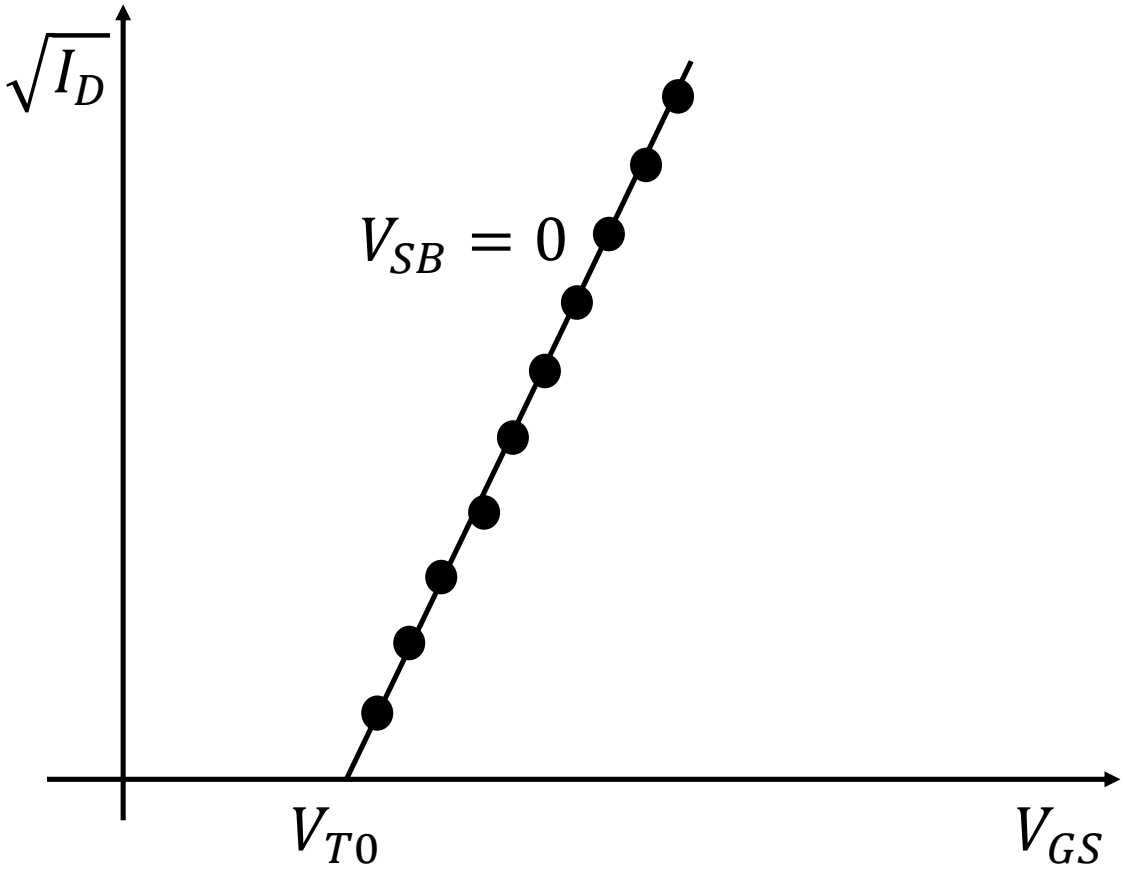
Calculation of V_{T0}:

$$I_D(Sat) = \frac{k_n}{2}.(V_{GS} - V_T)^2 .(1 + \lambda V_{DS})$$

$$\sqrt{I_D} = \sqrt{\frac{k_n}{2}}.(V_{GS} - V_T)$$

$$I_D(Sat) = \frac{k_n}{2}.(V_{GS} - V_T)^2$$





MOSFET Parameter Extraction

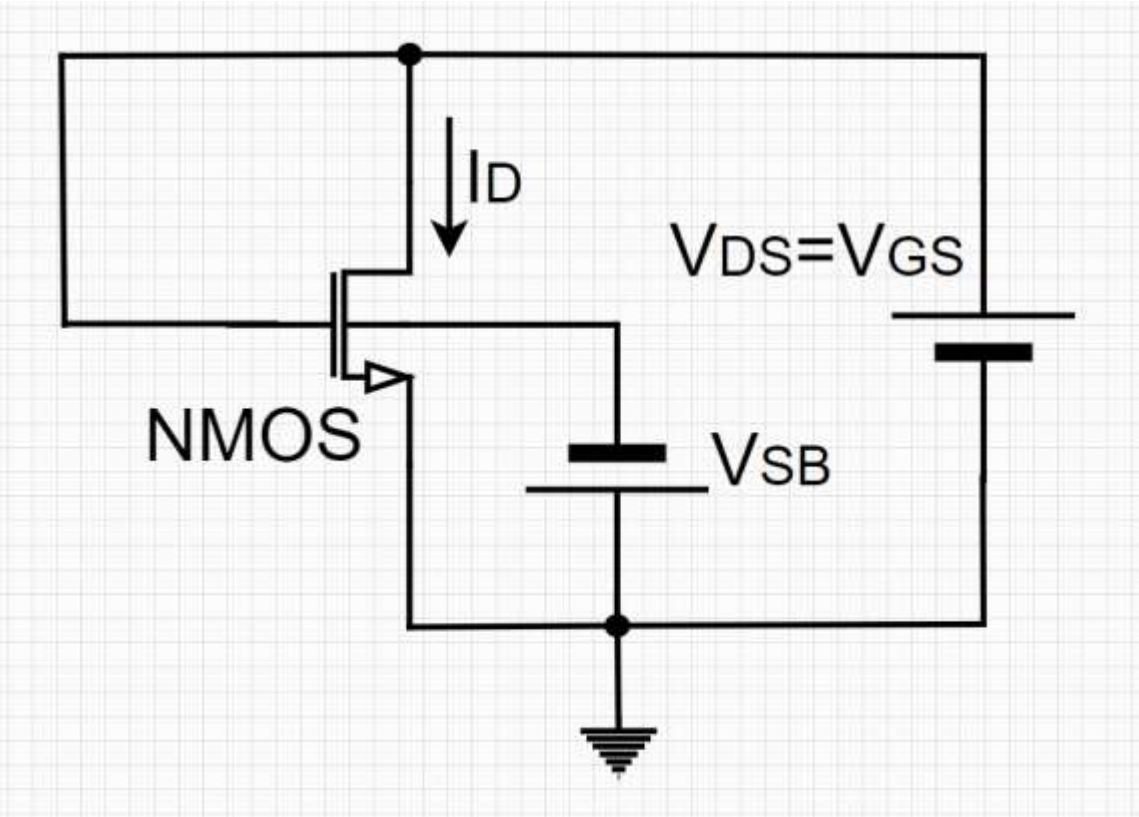
Calculations of Gamma:

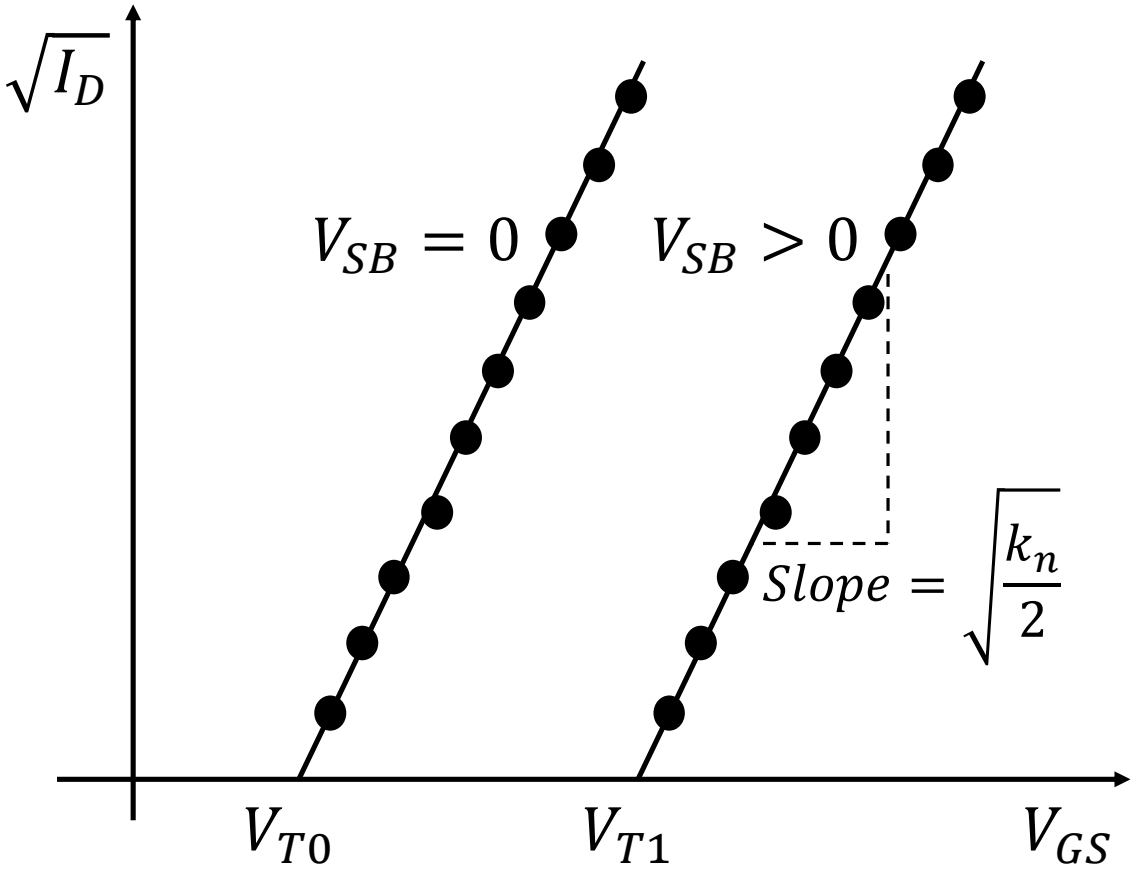
$$I_D(Sat) = \frac{k_n}{2}.(V_{GS} - V_T)^2 .(1 + \lambda V_{DS})$$

$$I_D(Sat) = \frac{k_n}{2}.(V_{GS} - V_T)^2$$

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}}$$

$$\sqrt{I_D} = \sqrt{\frac{k_n}{2}}.(V_{GS} - V_T)$$



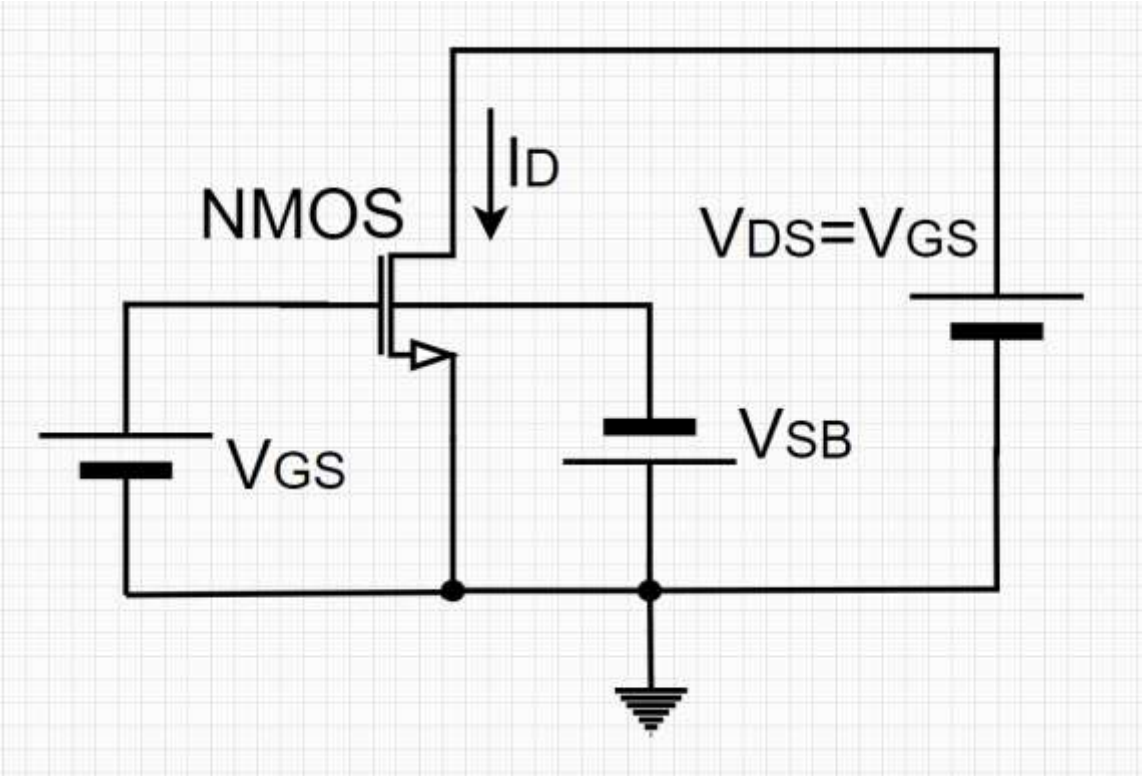


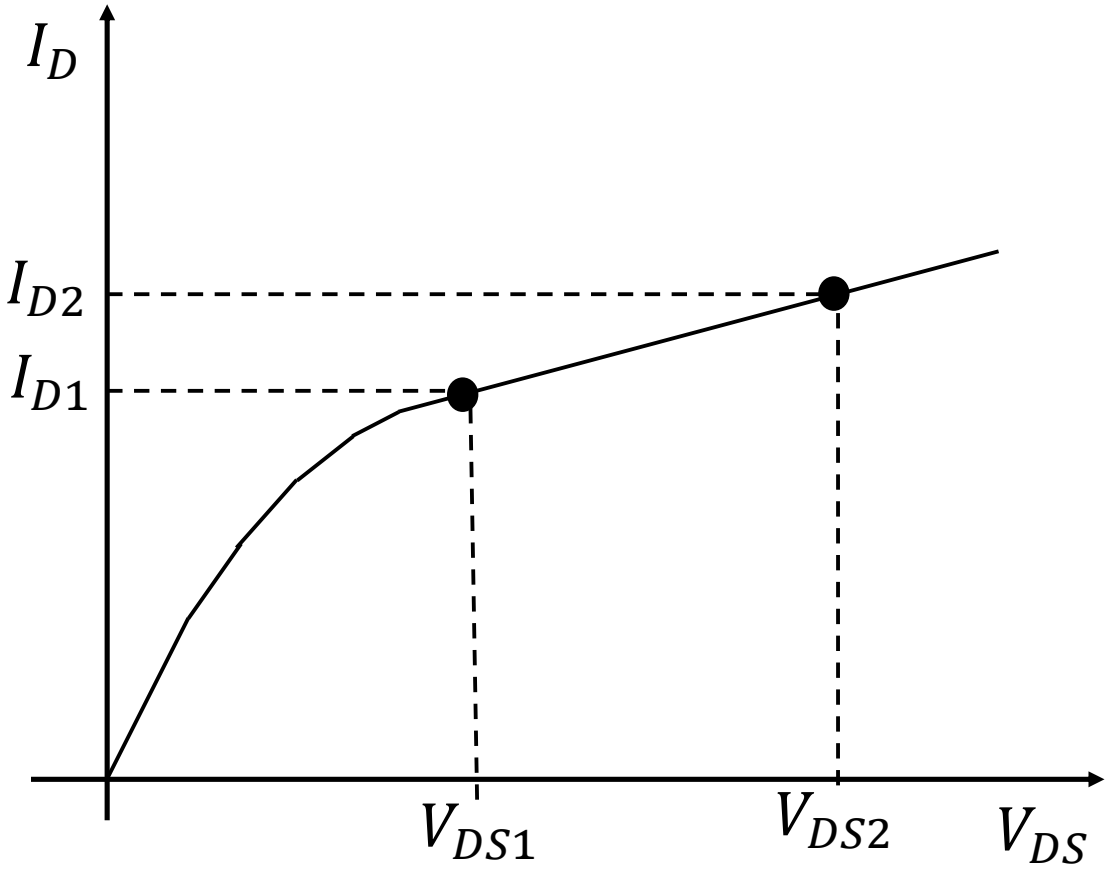
MOSFET Parameter Extraction

Lambda Calculation:

$$I_D(Sat) = \frac{k_n}{2} . (V_{GS} - V_T)^2 . (1 + \lambda V_{DS})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$





MOSFET Parameter Extraction: Assignment

Assignment:

1. Measured voltage and current data for MOSFET are given in the table. Determine the type of device, and calculate the parameters $k_n, V_{T0}, and\ \gamma$. Assume $\phi_F = -0.3\,V$. Neglect the channel length modulation effect.

$V_{GS}(V)$	$V_{DS}(V)$	$V_{SB}(V)$	$I_D(\mu A)$
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

$$I_D(Sat) = \frac{k_n}{2}.(V_{GS} - V_T)^2$$

$$\sqrt{I_D} = \sqrt{\frac{k_n}{2}}.(V_{GS} - V_T)$$

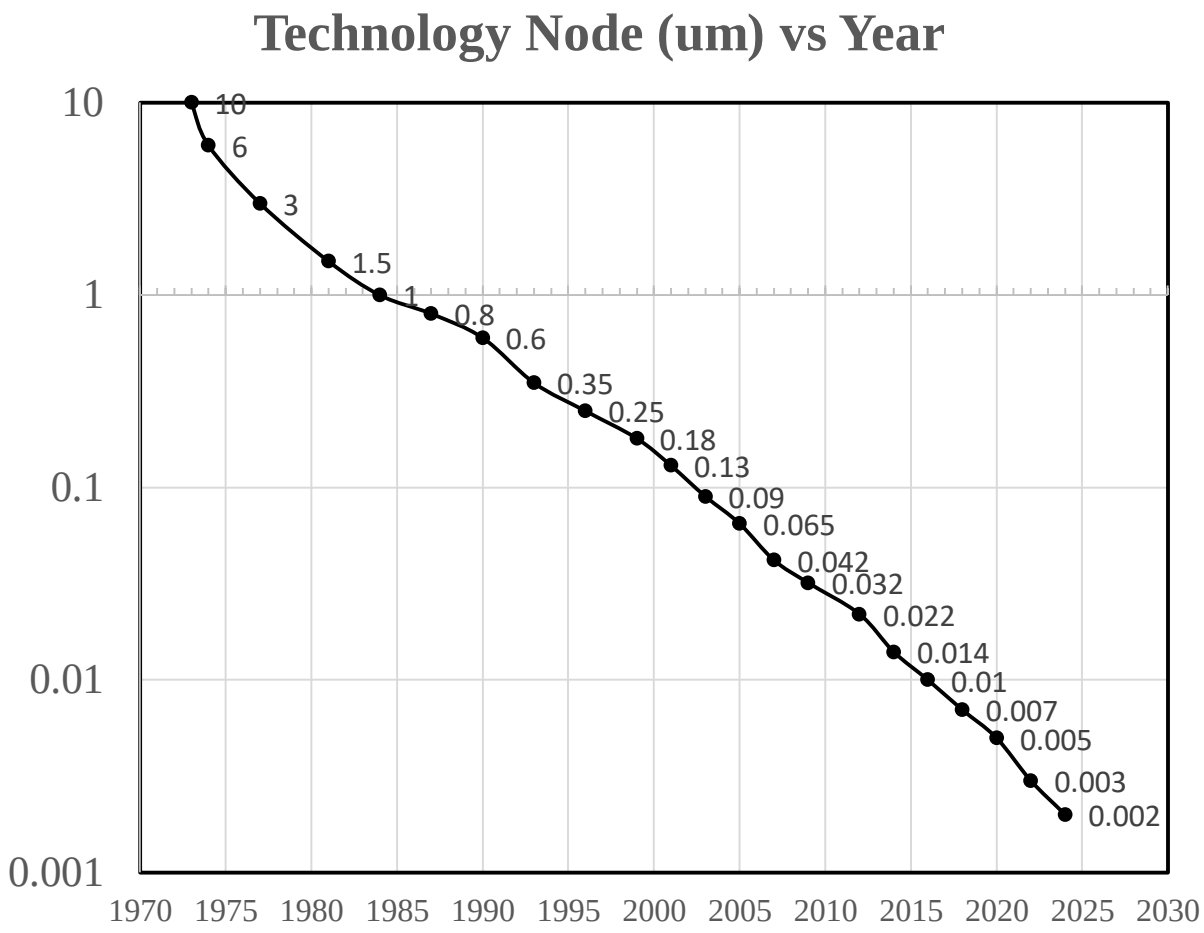
$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}}$$

$$V_T = V_{T0} + \gamma\left\{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right\}$$

MOSFET Scaling

MOSFET Scaling

- In semiconductor electronics, Dennard scaling, also known as MOSFET scaling, is a scaling law which states roughly that, as transistors get smaller, their power density stays constant, so that the power use stays in proportion with area; both voltage and current scale (downward) with length.
- The reduction of the size (dimensions of the MOSFET) commonly referred to as ***scaling***.
- Fig, shows the MOSFET gate length (technology node) versus year.
- There are two basic types of size-reduction strategies: ***full scaling*** (also called constant-field scaling) and ***constant voltage scaling***.



International Technology Roadmap for Semiconductors data (2022)

MOSFET Scaling: Constant Field Scaling

Constant Field Scaling:

- This scaling option attempts to preserve the magnitude of internal electric fields in the MOSFET, while the dimensions are scaled down by a factor of S.
- The charge densities must be increased by a factor of S in order to maintain the field conditions.

Quantity	Before Scaling	After Scaling
Oxide Capacitance	C_{ox}	$S.C_{ox}$
On Current	I_{on}	I_{on}/S
Power Dissipation	P_{diss}	P_{diss}/S^2
Time Delay	T_D	T_D/S
Power Density	P/A	P/A

Quantity	Before Scaling	After Scaling
Electric Field (E)	1	1
Channel Length (L)	L	L/S
Channel Width (W)	W	W/S
Gate Oxide Thickness (Tox)	t_{ox}	t_{ox}/S
Junction Depth (Xj)	x_j	x_j/s
Supply Voltage (V)	V_{DD}	V_{DD}/S
Threshold Voltage (VT)	V_{T0}	V_{T0}/S
Doping Densities	N_a, N_d	$N_a.S, N_d.S$

MOSFET Scaling: Constant Voltage Scaling

Constant Voltage Scaling:

- In constant-voltage scaling, all dimensions of the MOSFET are reduced by a factor of S, as in full scaling. The power supply voltage and the terminal voltages, on the other hand, remain unchanged.
- The doping densities must be increased by a factor of S^2in order to preserve the charge-field relations.

Quantity	Before Scaling	After Scaling
Oxide Capacitance	C_{ox}	$S.C_{ox}$
On Current	I_{on}	$S.I_{on}$
Power Dissipation	P_{diss}	$S.P_{diss}$
Time Delay	T_D	T_D/S
Power Density	$P/_A$	$S^3(P/_A)$

Quantity	Before Scaling	After Scaling
Electric Field (E)	E	$E.S$
Channel Length (L)	L	L/S
Channel Width (W)	W	W/S
Gate Oxide Thickness (Tox)	t_{ox}	t_{ox}/S
Junction Depth (Xj)	x_j	x_j/s
Supply Voltage (V)	V_{DD}	V_{DD}
Threshold Voltage (VT)	V_{T0}	V_{T0}
Doping Densities	N_a, N_d	$N_a.S^2, N_d.S^2$

MOSFET Scaling Summary

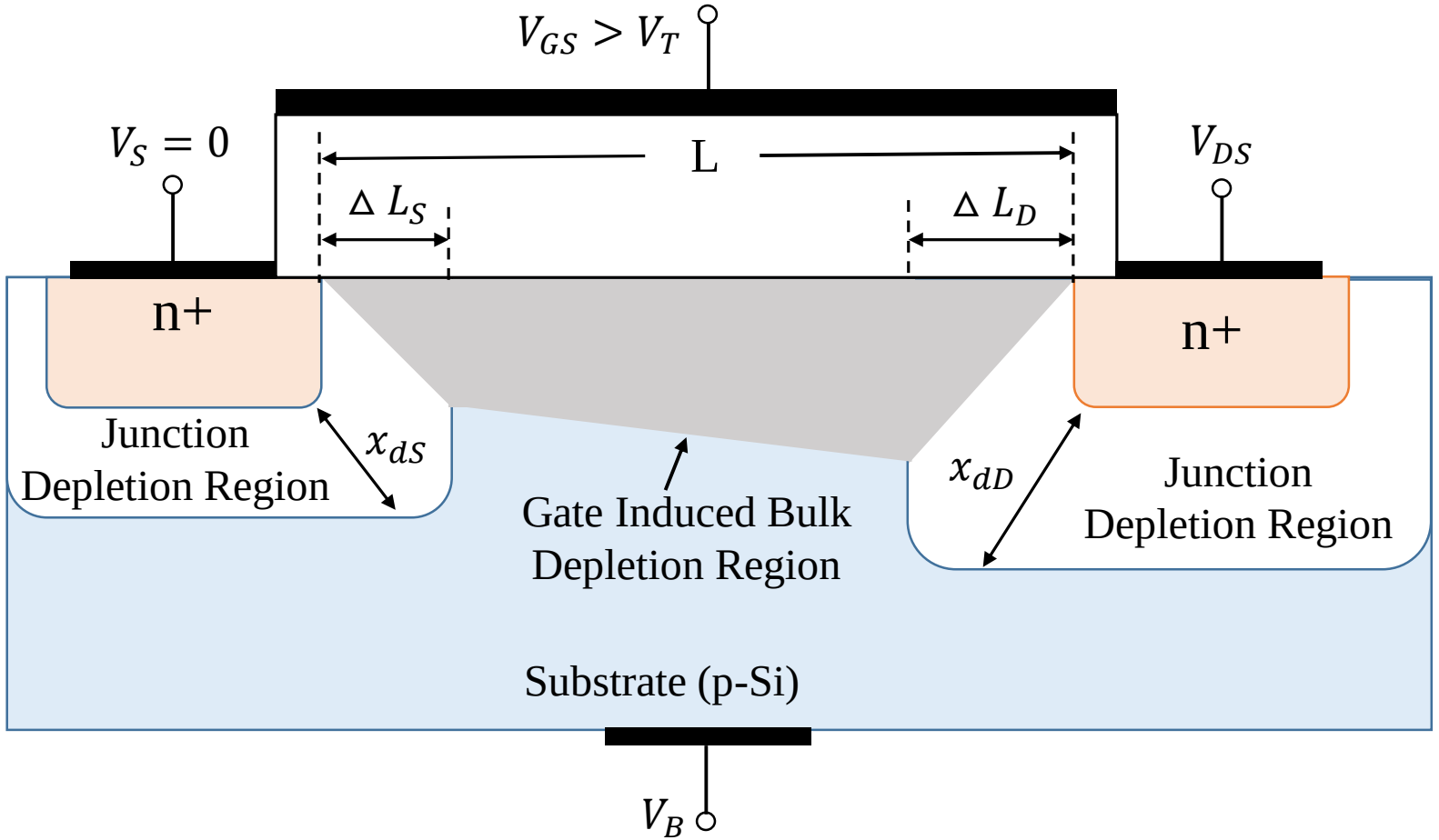
- constant-voltage scaling may be preferred over full (constant-field) scaling in many practical cases because of the external voltage-level constraints.
- It must be recognized, however, that constant-voltage scaling increases the drain current density and the power density by a factor of S^3.
- This large increase in current and power densities may eventually cause serious reliability problems for the scaled transistor, such as electromigration, hot-carrier degradation, oxide breakdown, and electrical over-stress.

Short Channel Effects

Short Channel Effects

Short Channel Devices:

- A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD} , x_{dS}) of the source and drain junction.
- Alternatively, a MOSFET can be defined as a short-channel device if the effective channel length L_{eff} is approximately equal to the source and drain junction depth x_j



- As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise.

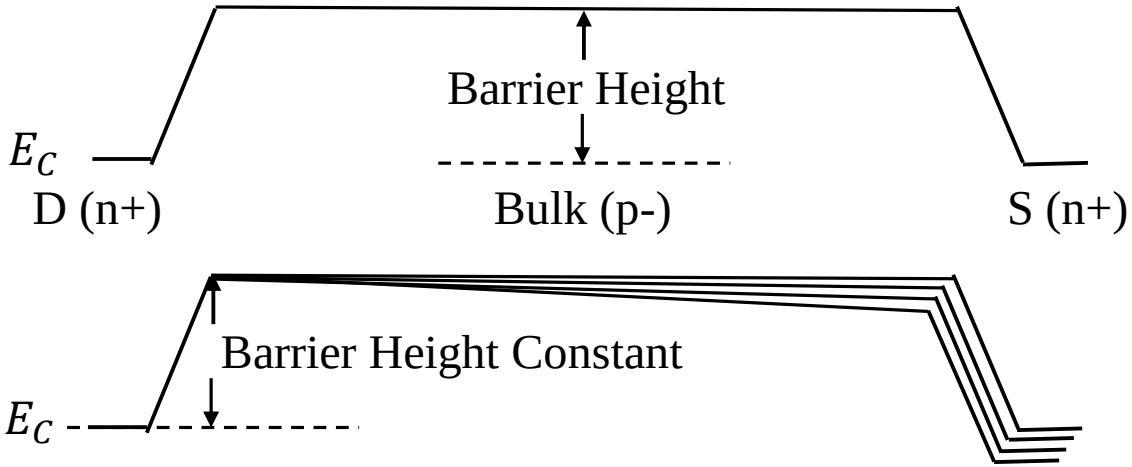
Short Channel Effects

Short Channel Effects:

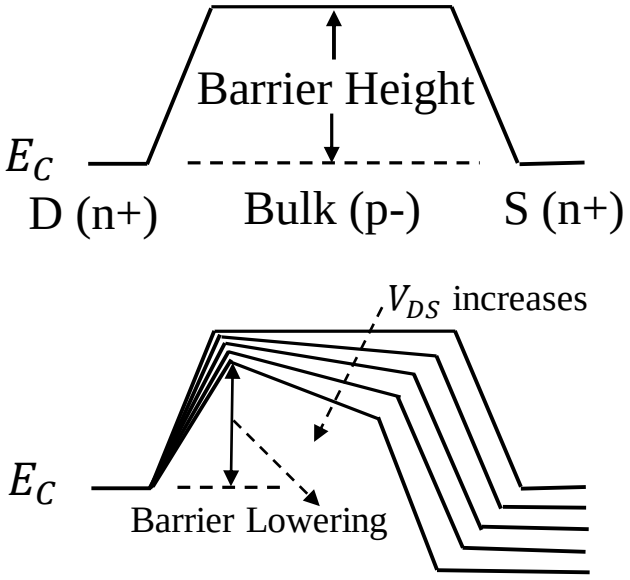
- The short channel effects are attributed to two physical phenomena:
    1. the limitation imposed on electron drift characteristics in the channel,
    2. the modification of the threshold voltage due to the shortening channel length.
- In particular seven different short channel effects can be distinguished
    1. drain-induced barrier lowering and punch through
    2. Mobility degradation or surface scattering
    3. velocity saturation
    4. impact ionization
    5. hot electrons
    6. Sub-threshold conduction
    7. Vt roll-off

Short Channel Effects: Drain Induced Barrier Lowering (DIBL)

- In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage VGS and the drain-to-source voltage VDS.
- If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL).
- The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage.
- The channel current that flows under this conditions (VGS<VT0) is called the sub-threshold current.



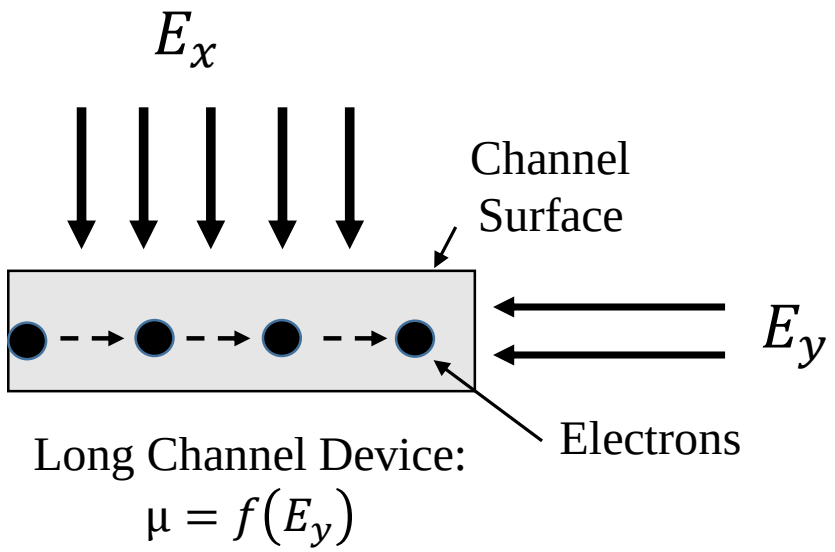
(A) Long Channel Device

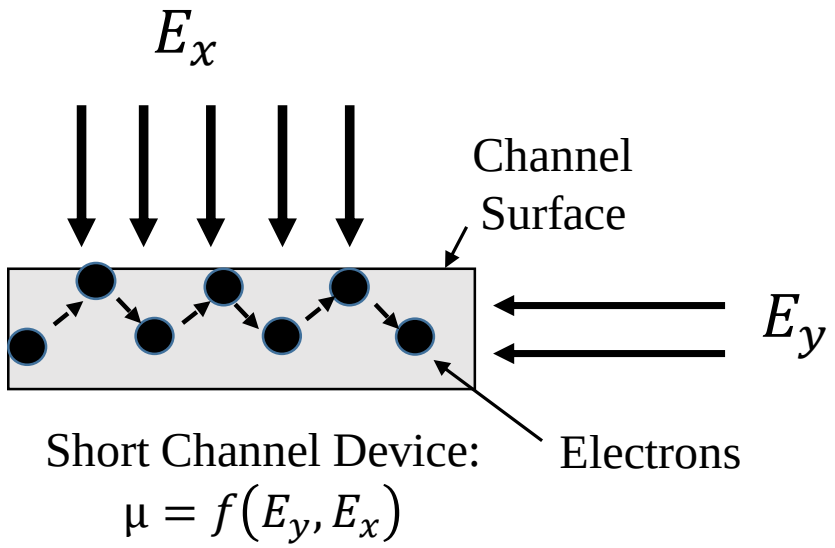


(B) Short Channel Device

Short Channel Effects: Mobility Degradation

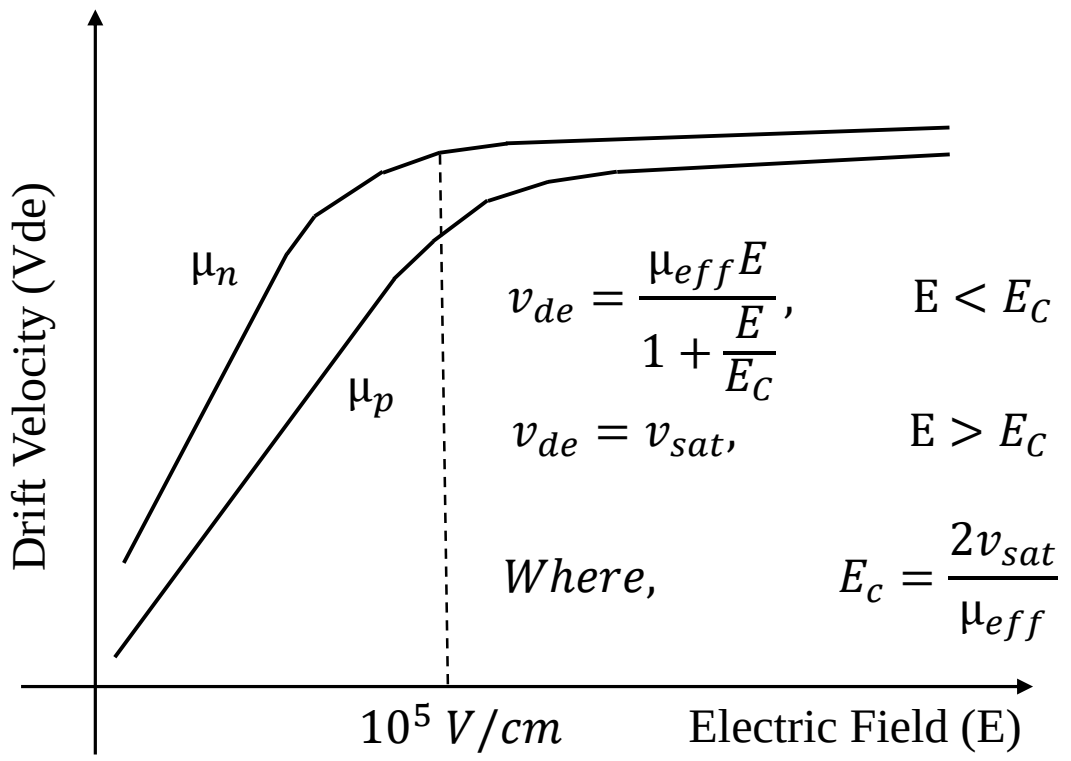
- As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component E_y increases, and the surface mobility μ becomes field-dependent.
- Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by E_x) causes reduction of the mobility.
- The electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y, is about half as much as that of the bulk mobility.





Short Channel Effects: Velocity Saturation

- At low E_y, the electron drift velocity v_{de} in the channel varies linearly with the electric field intensity. However, as E_y increases above 10^4 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of $v_{desat} = 10^7$ cm/s around $E_y = 10^5$ V/cm at 300 K.
- The performance of short-channel devices is also affected by velocity saturation, which reduces the transconductance in the saturation mode.
- Note that the drain current is limited by velocity saturation instead of pinch off. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages.

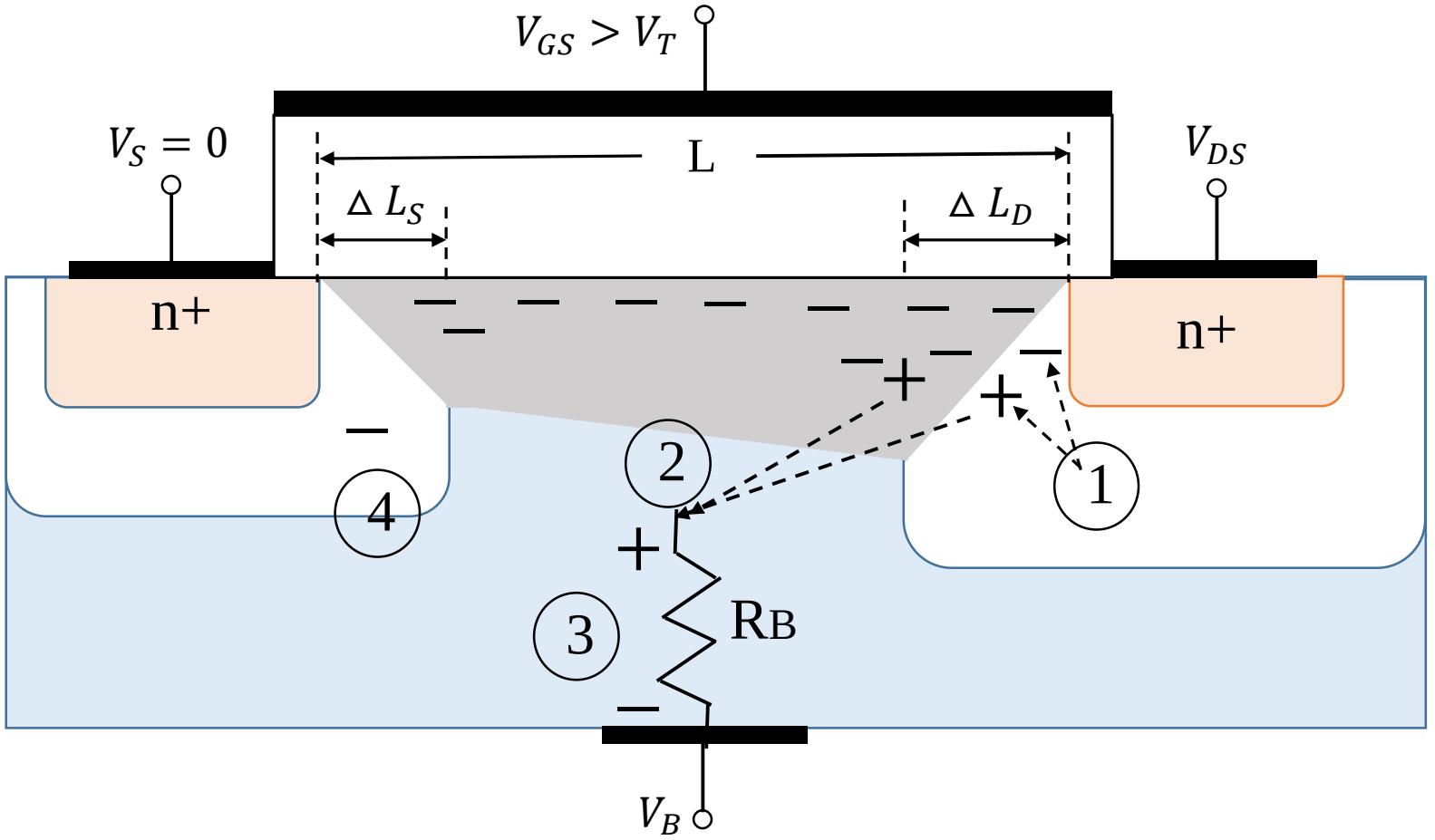


- The critical voltage V_c is the drain-to-source voltage at which the critical electric field is reached: $V_c = E_C . L$

Short Channel Effects: Impact Ionization

Impact Ionization:

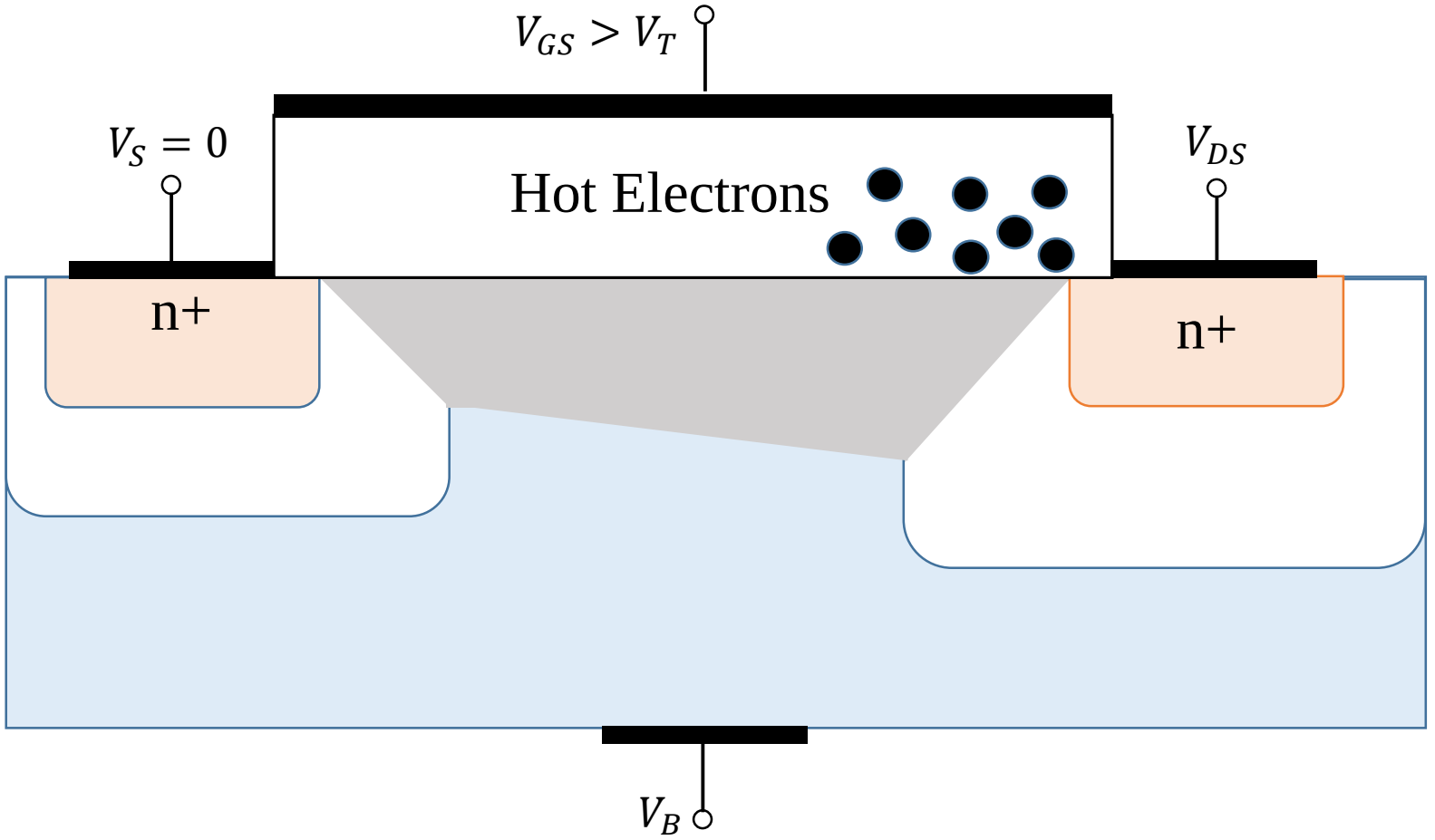
1. Electron-hole pair generated due to high longitudinal electric field by impact ionization
2. Holes swept into bulk
3. Potential drop by hole current create a bulk-to-source forward bias,
4. Additional electron injection and carrier flow into drain.



Short Channel Effects: Hot Carrier

Impact Ionization:

1. Another problem, related to high electric fields, is caused by so-called hot electrons.
2. This high energy can accumulate with time and degrade the device performance by increasing VT and affect adversely



Short Channel Effects: Sub-threshold Conduction

Sub-threshold Conduction:

1. When the gate voltage is high, the transistor is strongly ON. When the gate falls below Vt , the exponential decline in current appears as a straight line on the logarithmic scale.
2. This regime of Vgs < Vt is called weak inversion.
3. The subthreshold leakage current increases significantly with Vds because of drain-induced barrier lowering.
4. There is a lower limit on Ids set by drain junction leakage that is exacerbated by the negative gate voltage

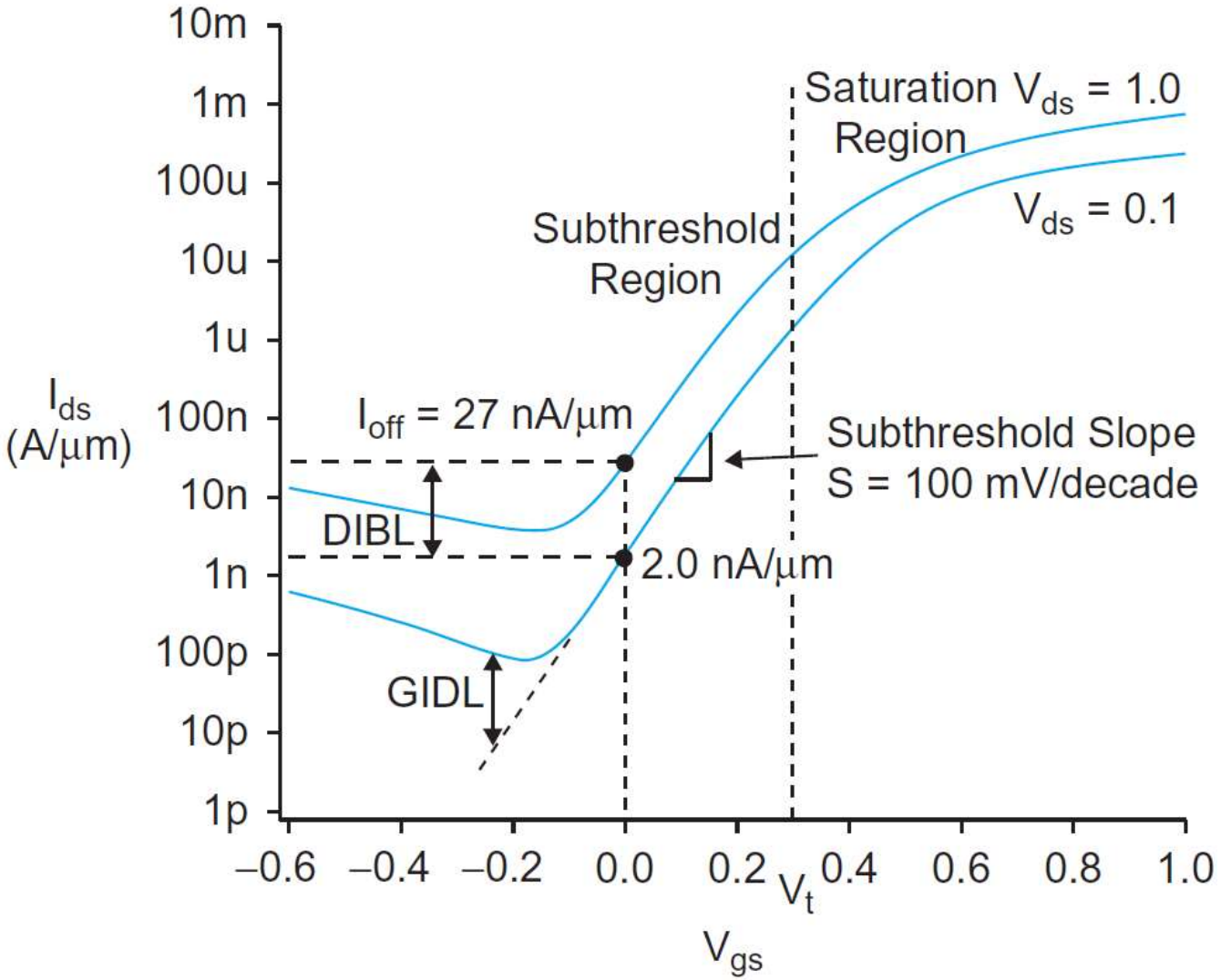


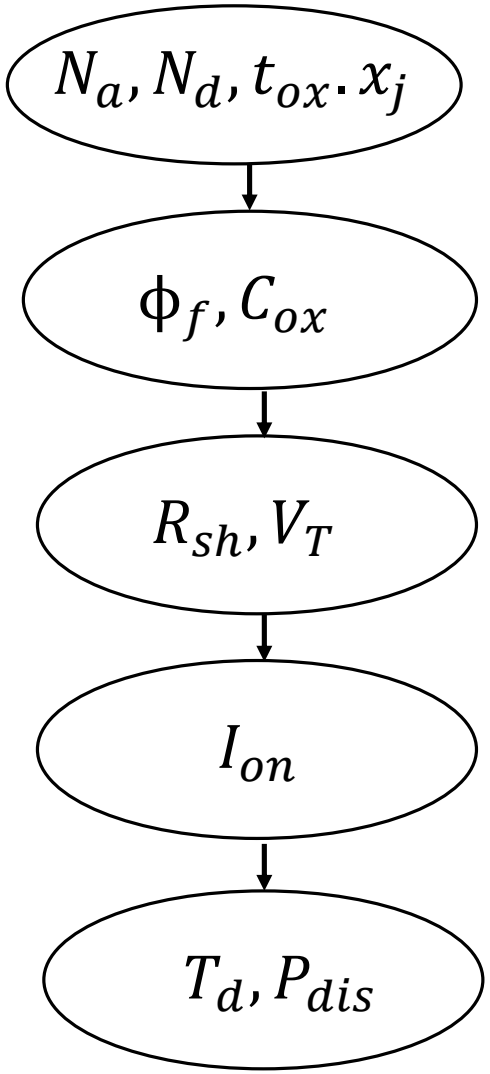
Fig.: Id-Vgs characteristics (Courtesy: Waste and Harris)

Process, Voltage and Temperature (PVT) Variations

PVT Variations: Processes Variation

Devices parameters vary between runs and even in on the same die.

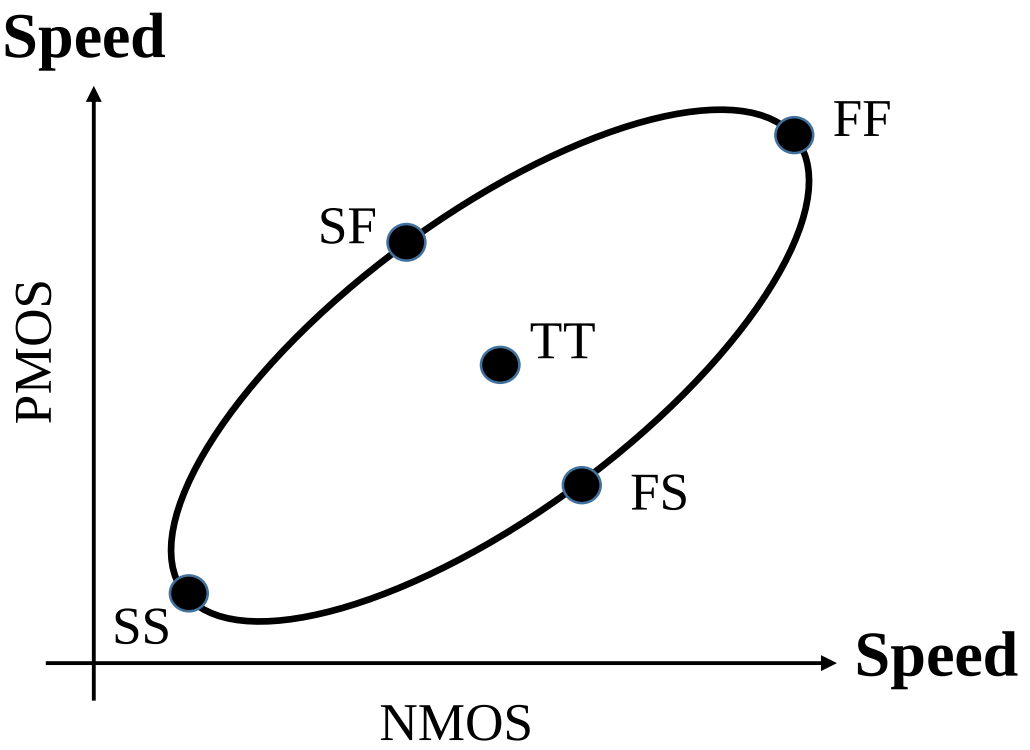
- **Variation in the process parameters:**
  - Impurity concentration densities
  - Oxide thicknesses
  - Diffusion depths
- These are caused by non-uniform conditions during the deposition and/or the diffusion of the impurities.
- This introduces the variation of the sheet resistances and threshold voltages of transistor.
- **Variation in the dimensions:**
  - Width and length variation of MOS Transistors, resistors and capacitors
  - Mismatches is emitter area in Bipolar devices
- These are caused by limited resolution of photolithographic process.
- This changes the device performance in the circuit.



Process Corners

There are 5 process corners

1. TT (Typical Typical): NMOS and PMOS Typical
2. SS (Slow Slow) : NMOS Slow and PMOS Slow
3. FF (Fast Fast) : NMOS Fast and PMOS Fast
4. SF (Slow Fast) : NMOS Slow and PMOS Fast
5. FS (Fast Slow) : NMOS Fast and PMOS Slow



VOLTAGE VARIATION

There are multiple reasons for voltage variation

- IR drop caused by the current flow over the power grid network
- Supply noise caused by parasitic inductance in combination with resistance and capacitance. When the current is flowing through parasitic inductance (L) it will cause the voltage bounce.

PVT Variations: Temperature Variation

- Two fundamental parameters, carrier mobility μ and threshold voltage V_T varies with temperature.
- Carrier mobility decrease with temperature

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu}$$

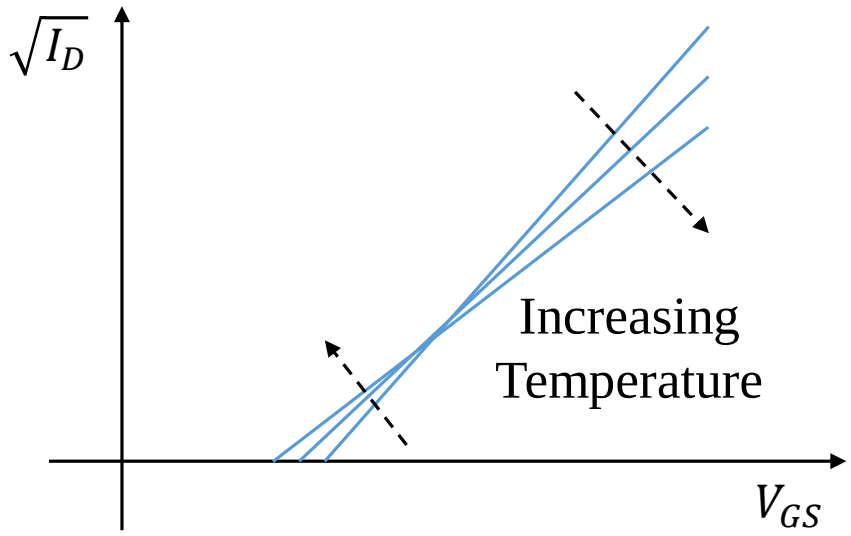
Where T is the absolute temperature, T_r is the room temperature and k_μ is the fitting parameter with a typical value of 1.5.

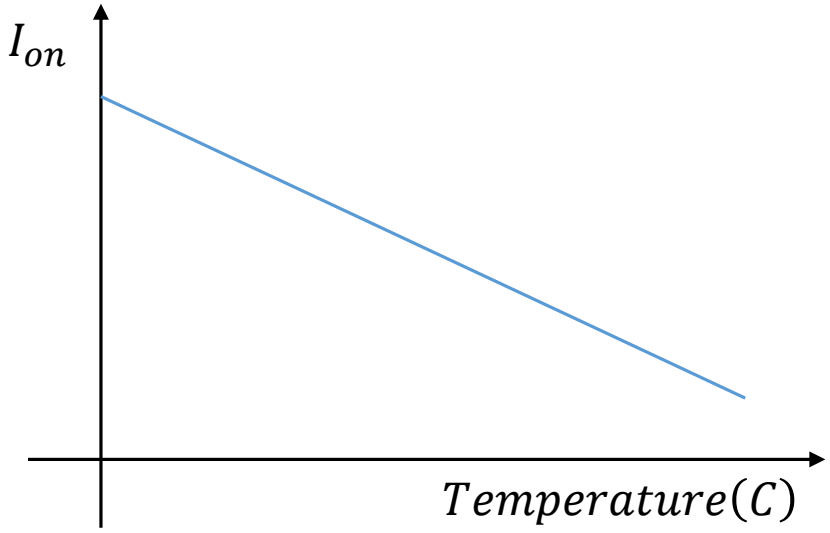
- The magnitude of threshold voltage decreases nearly with the temperature and may be approximated by,

$$V_T(T) = V_T(T_r) - k_{vt}(T - T_r)$$

Where, k_{vt} is typically about 1-2 mV/K

- I_{on} at high Vdd decreases with temperature, sub-threshold leakage increases exponentially with temperature, BTBT increases slowly with temperature and gate leakage is almost independent with temperature.





Thank You