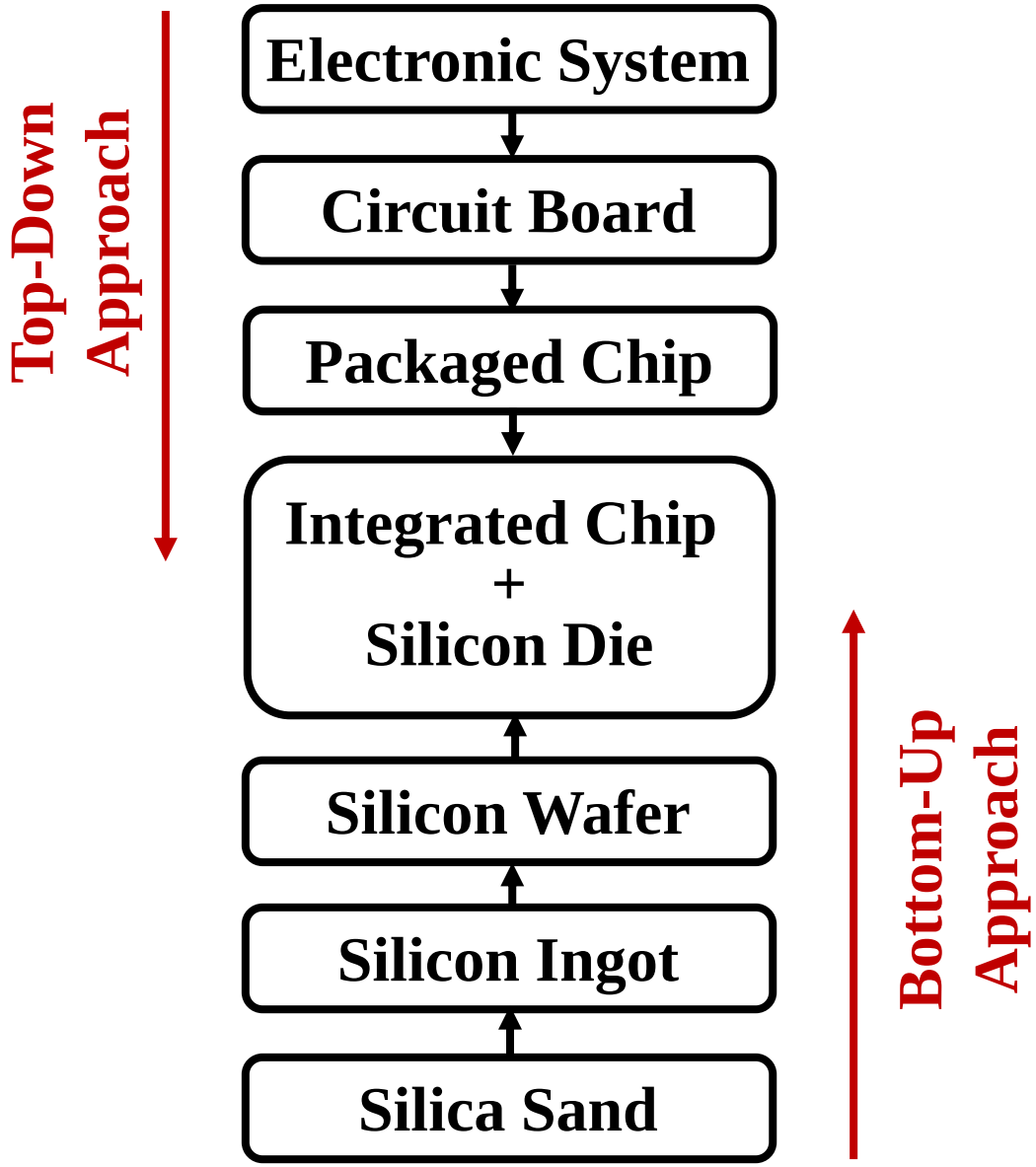
Broad View of VLSI Design
and
CMOS Manufacturing Process

Santunu Sarangi

Broad View of VLSI Design



Electronic System

Top-Down Approach

Bottom-Up Approach

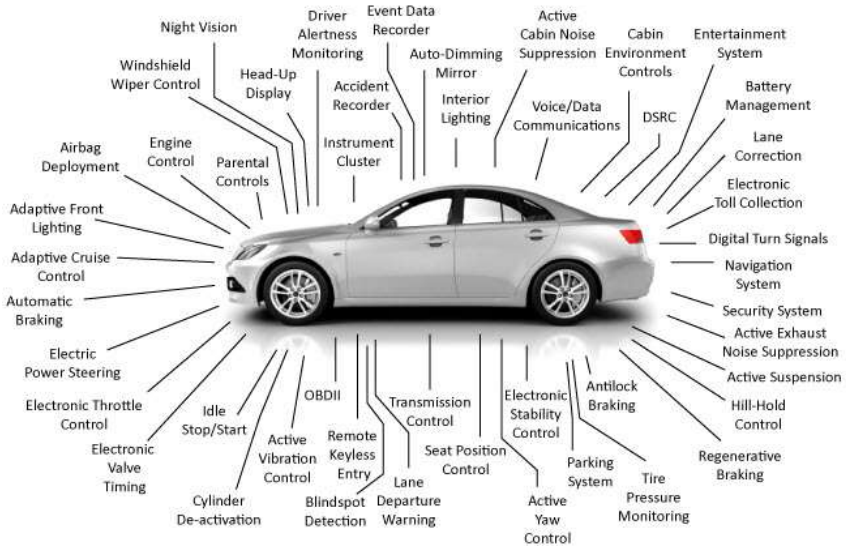
- **Electronic System**
- Circuit Board
- Packaged Chip
- Integrated Chip + Silicon Die
- Silicon Wafer
- Silicon Ingot
- Silica Sand

Computer

Smart phone

Smart Watch

Automotive Electronics



Circuit Board

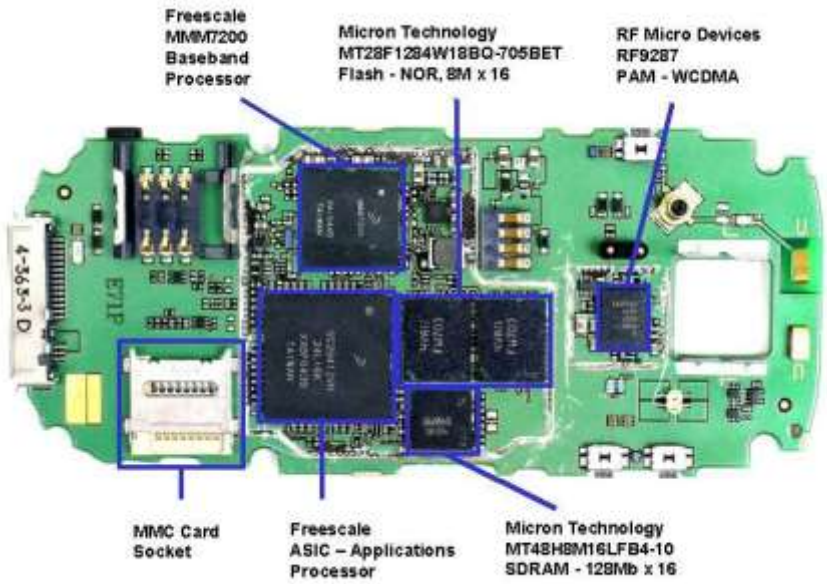
Top-Down Approach

Bottom-Up Approach

- Electronic System
- **Circuit Board**
- Packaged Chip
- Integrated Chip + Silicon Die
- Silicon Wafer
- Silicon Ingot
- Silica Sand

Mother board

Mobile board



Automotive Car PCB

Packaged Chip

Top-Down Approach

Bottom-Up Approach

- Electronic System
- Circuit Board
- **Packaged Chip**
- Integrated Chip + Silicon Die
- Silicon Wafer
- Silicon Ingot
- Silica Sand

Packaged Chip

Micro Processor

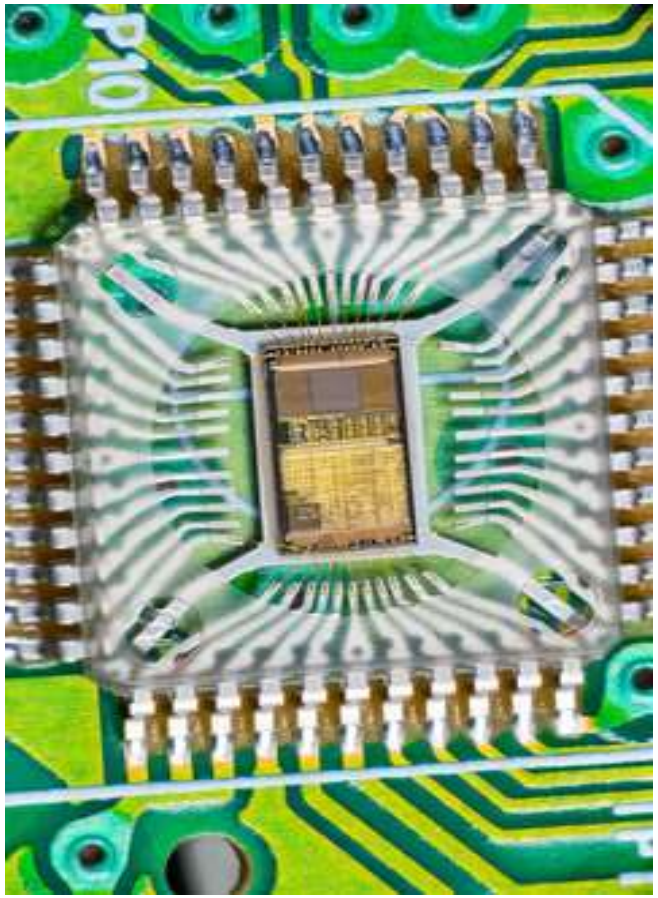
Integrated Chip and Silicon Die

Top-Down Approach

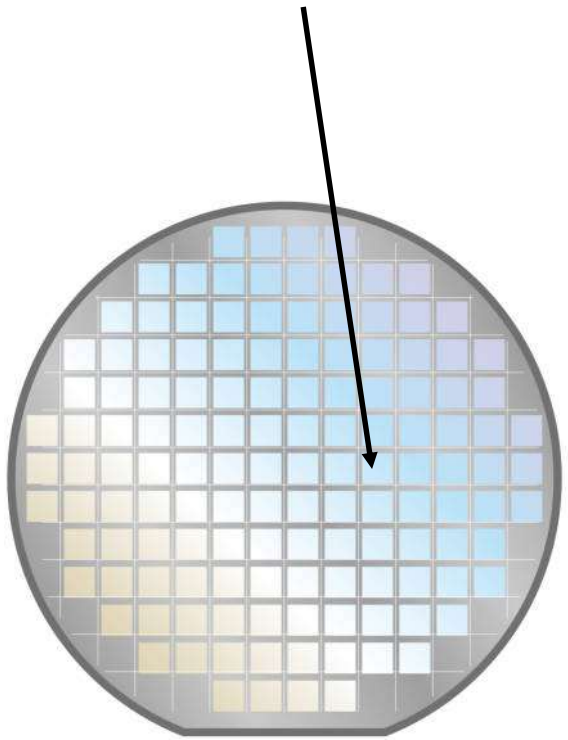
Bottom-Up Approach

- Electronic System
- Circuit Board
- Packaged Chip
- **Integrated Chip + Silicon Die**
- Silicon Wafer
- Silicon Ingot
- Silica Sand

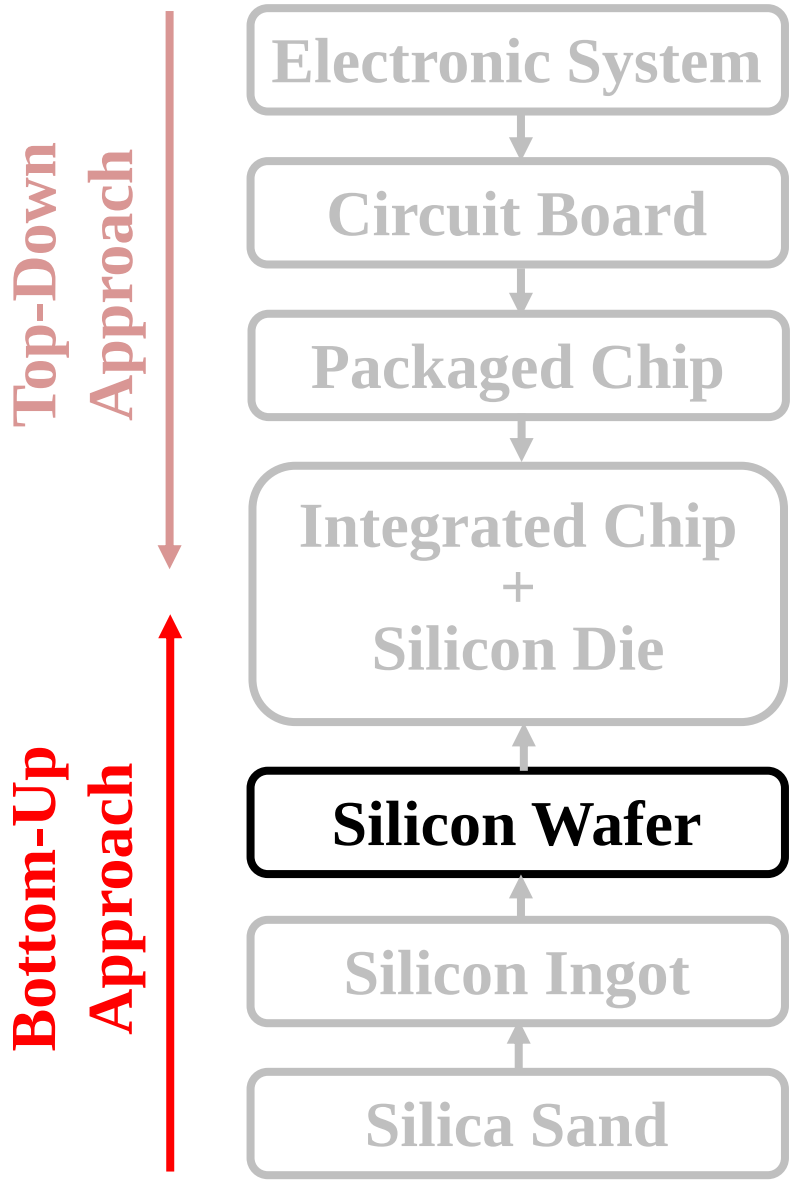
Integrated Chip



Silicon Die

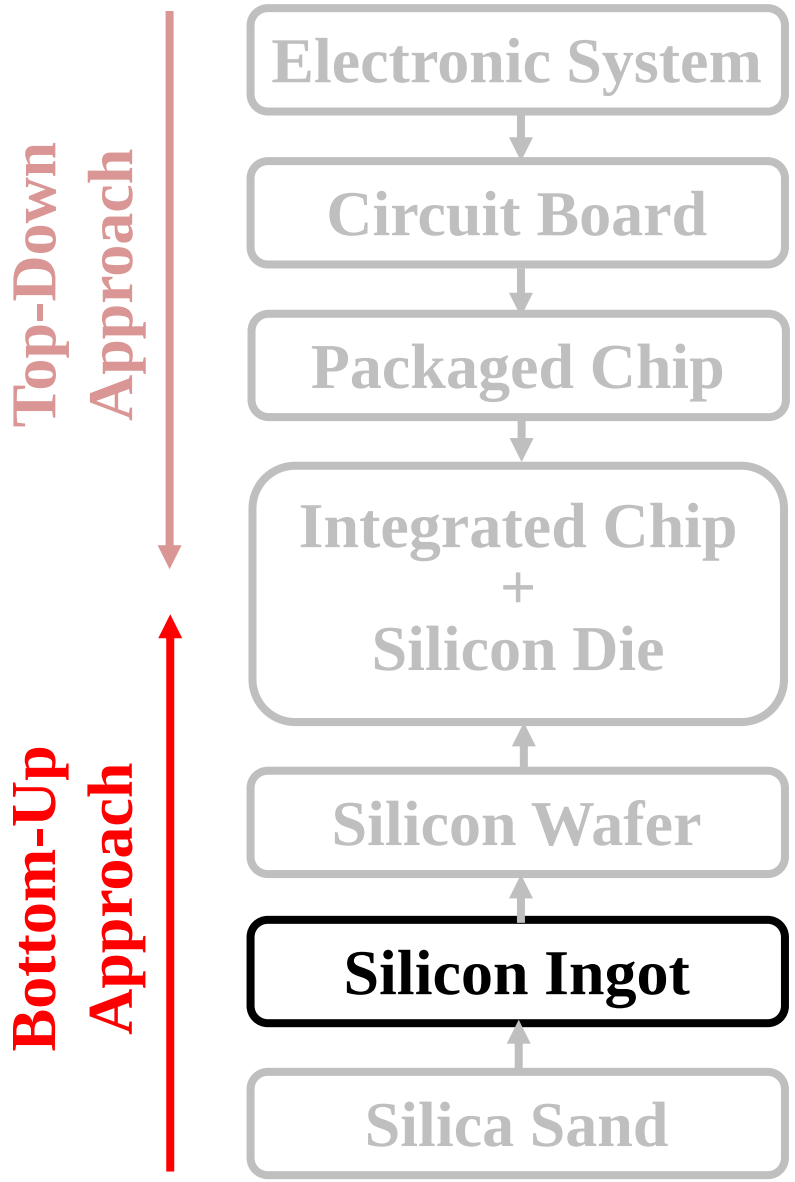


Silicon Wafer



Silicon Wafer

Silicon Ingot



Silicon ingot

Silica Sand

Top-Down Approach

Bottom-Up Approach

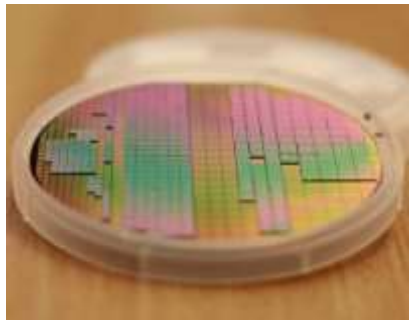
- Electronic System
- Circuit Board
- Packaged Chip
- Integrated Chip + Silicon Die
- Silicon Wafer
- Silicon Ingot
- **Silica Sand**

Silica Sand

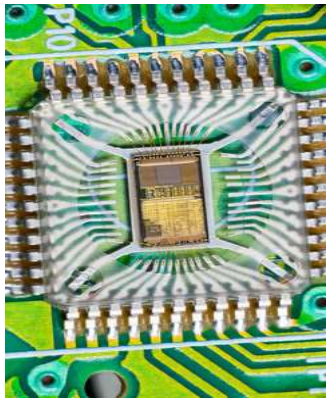
VLSI Design Summary

Silica Sand

Silicon Ingot



Silicon Wafer



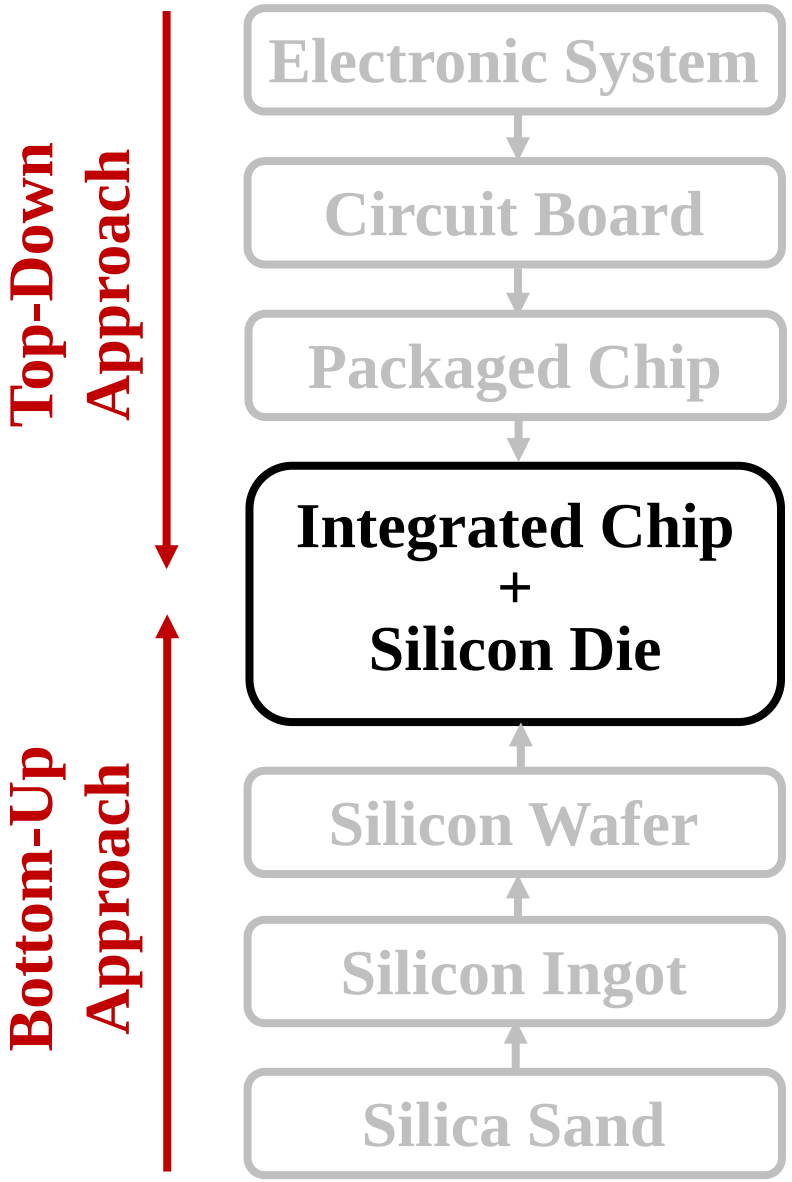
Integrated Chip

Packaged Chip

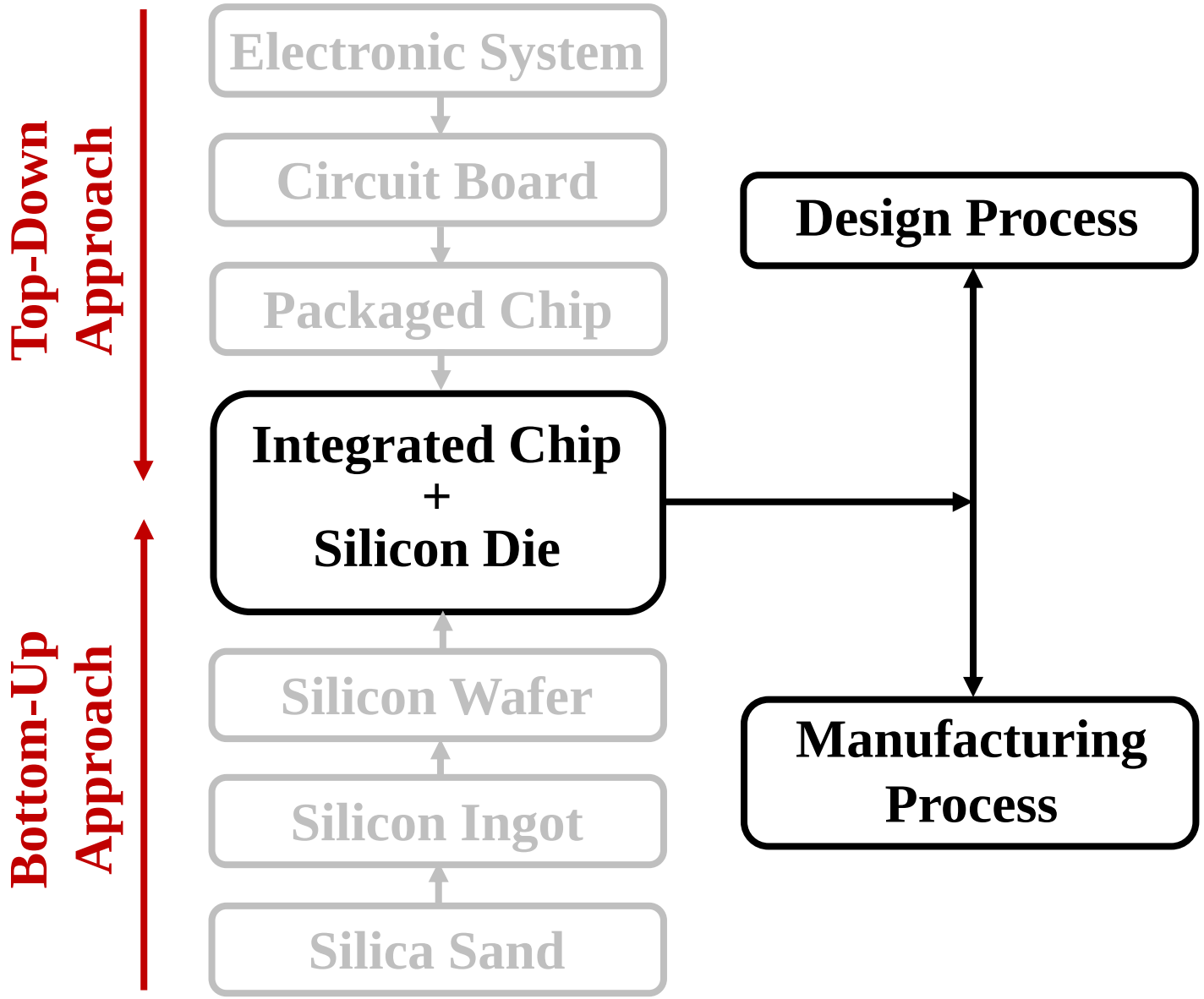
Circuit Board

Electronics System

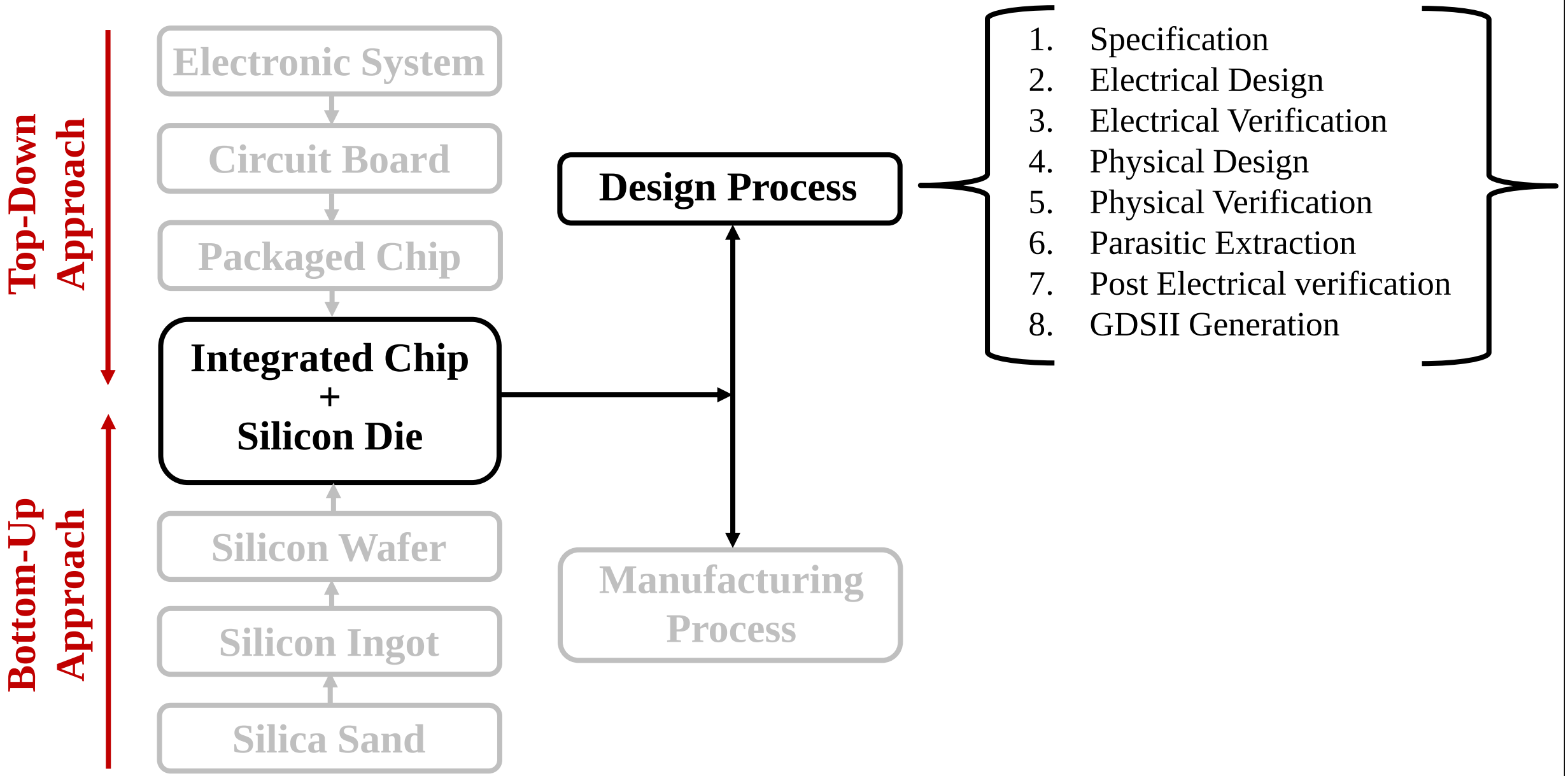
Outline


Top-Down Approach
Electronic System
Circuit Board
Packaged Chip
Integrated Chip
+
Silicon Die
Bottom-Up Approach
Silicon Wafer
Silicon Ingot
Silica Sand

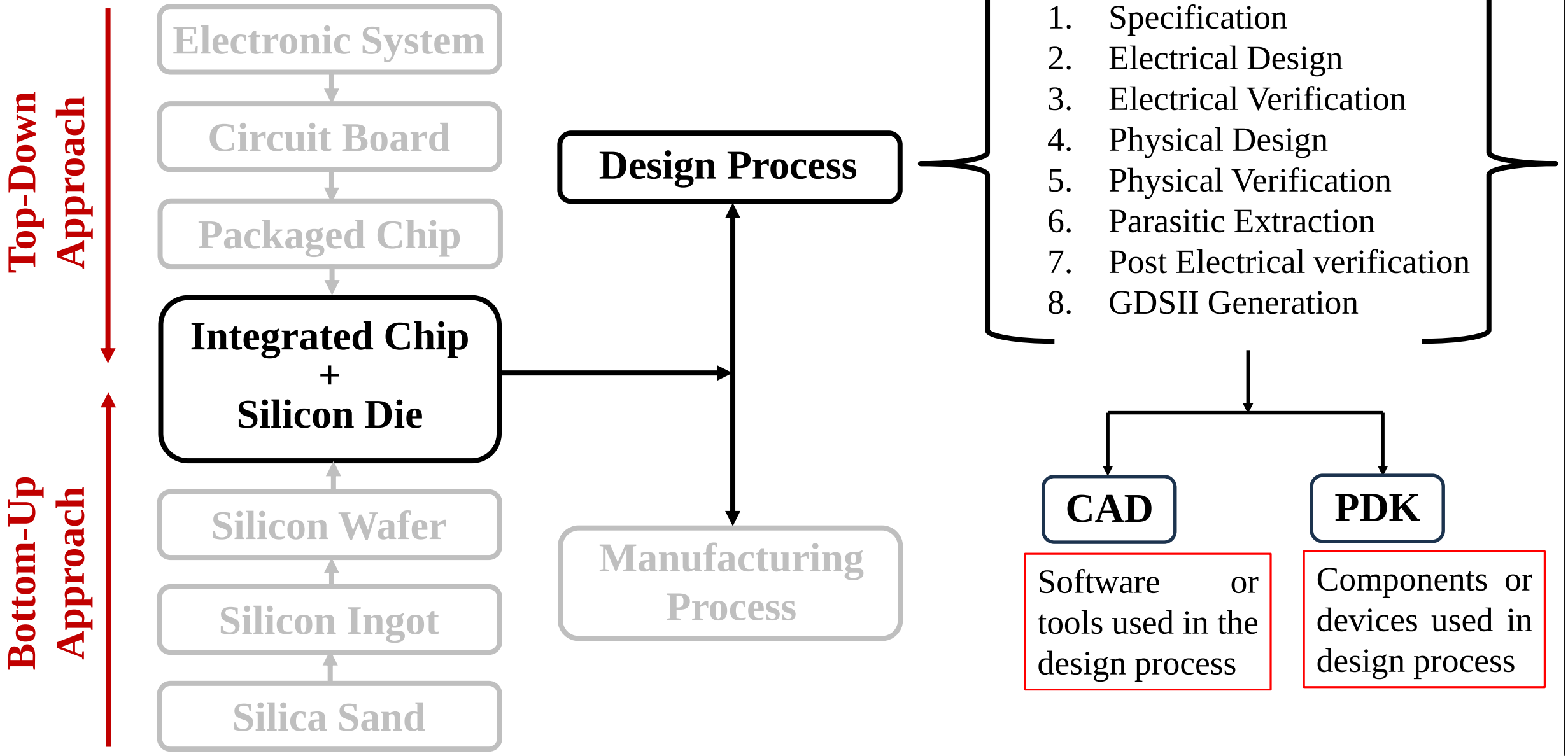
VLSI Design and Manufacturing Process



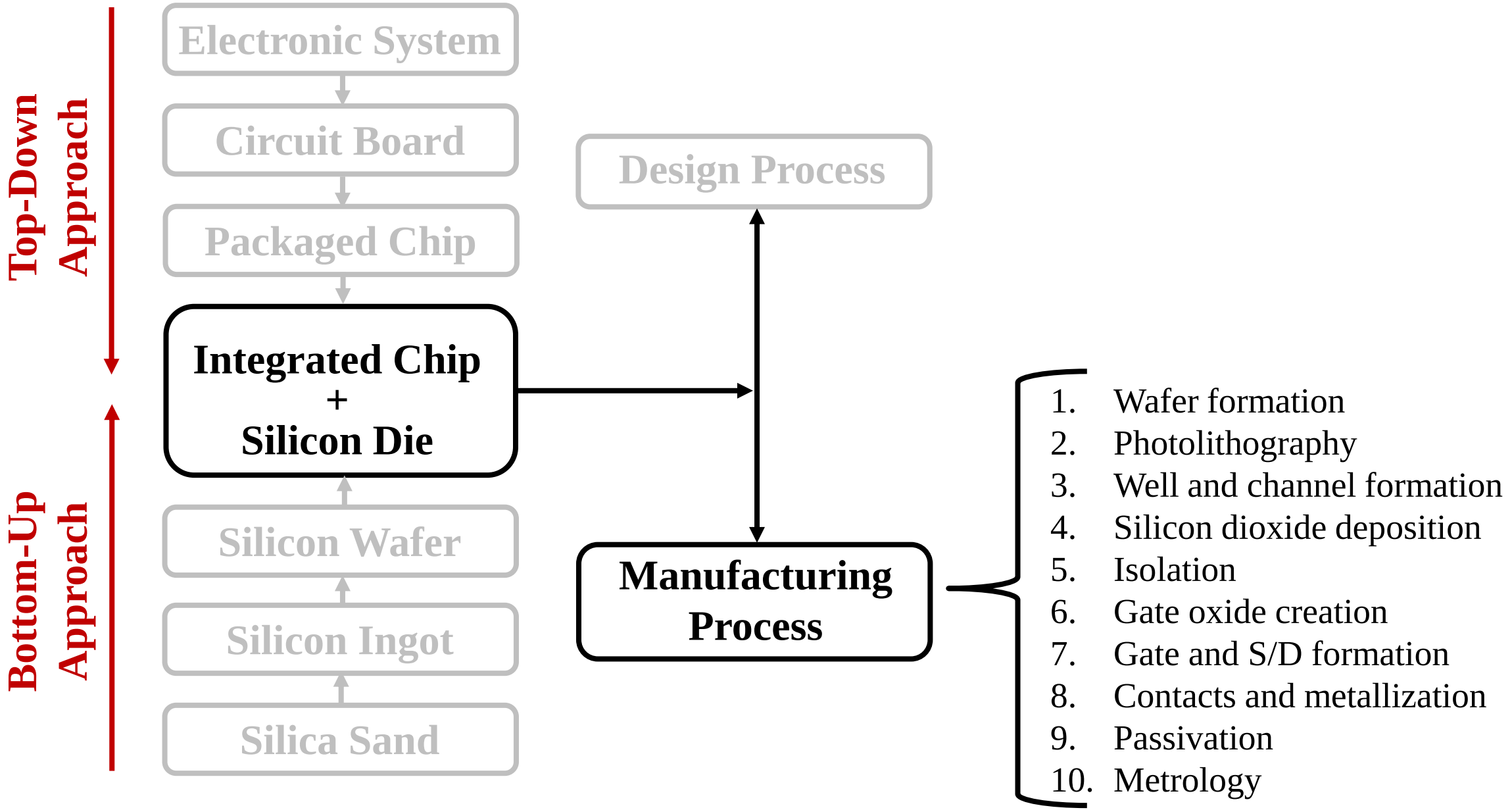
VLSI Design Process



VLSI Design Process



VLSI Manufacturing Process

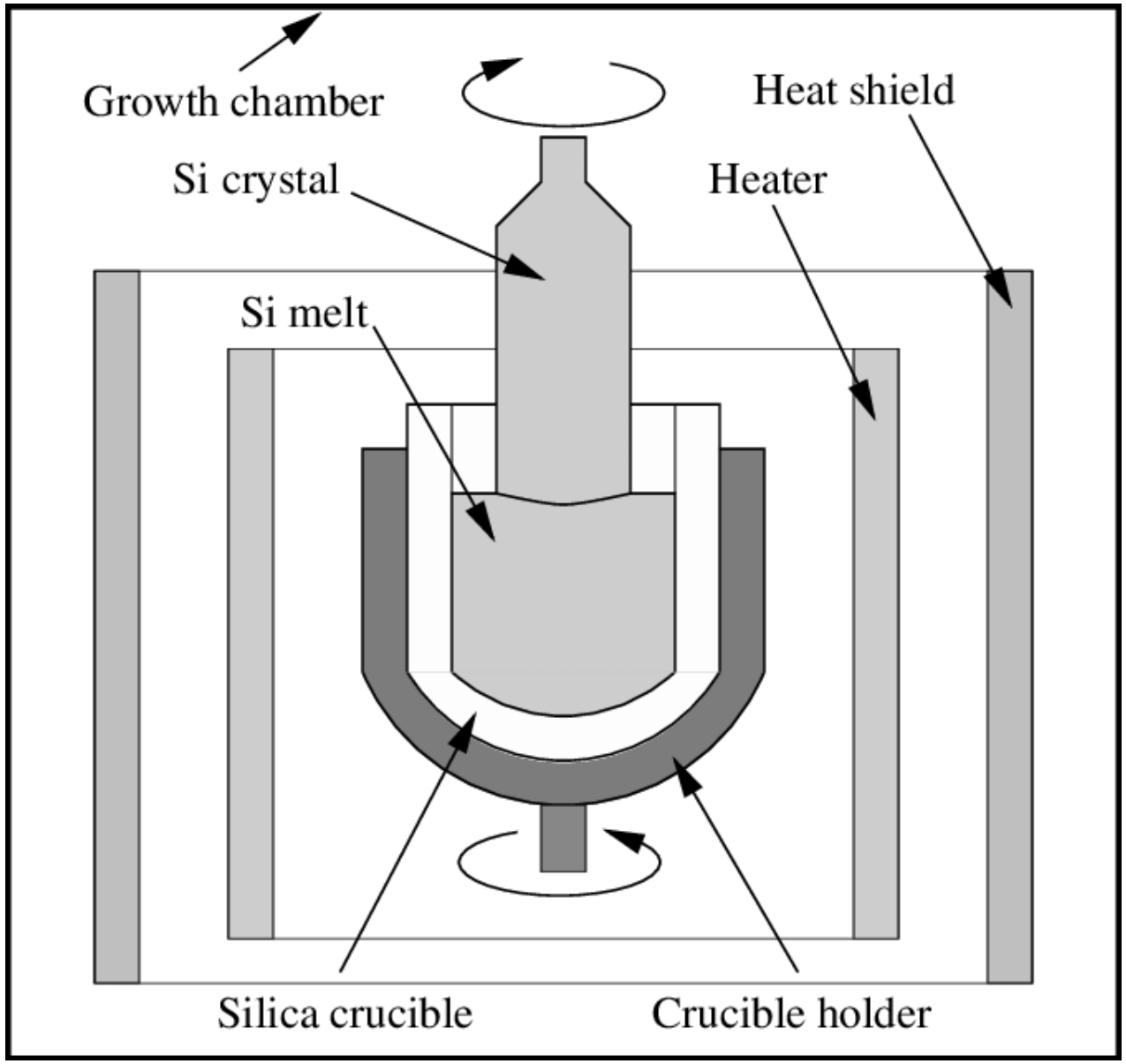


CMOS Fabrication Process

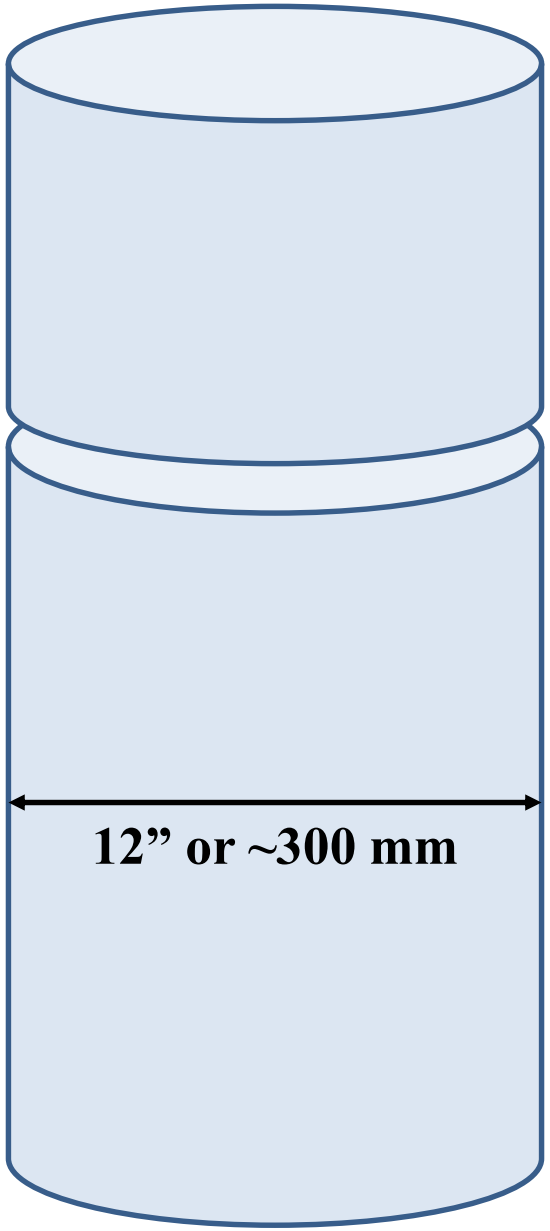
Process Steps:

1. Wafer formation (sand-to-silicon)
2. Photolithography
3. Well and Channel Formation
4. Silicon Dioxide (Sio2) Deposition
5. Isolation
6. Gate Oxide Creation
7. Gate and Source/Drain Formations
8. Contacts and Metallization
9. Passivation
10. Metrology

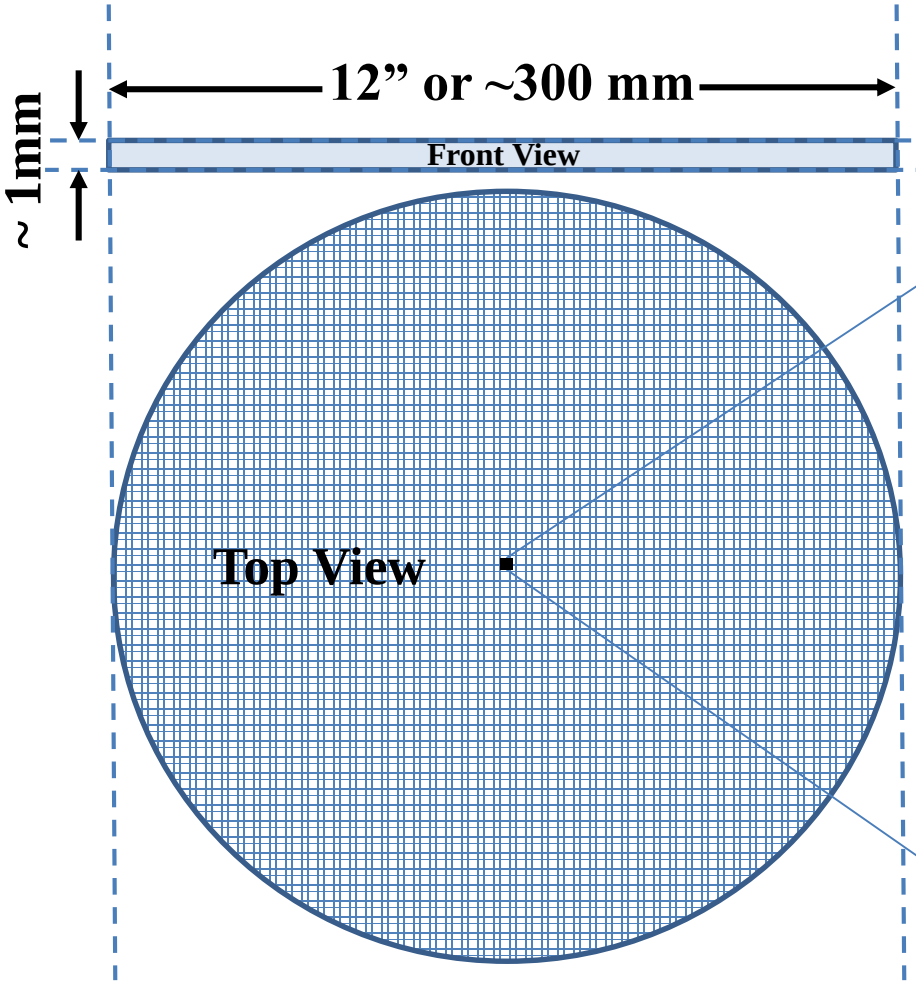
1. Wafer Formation (sand-to-silicon)



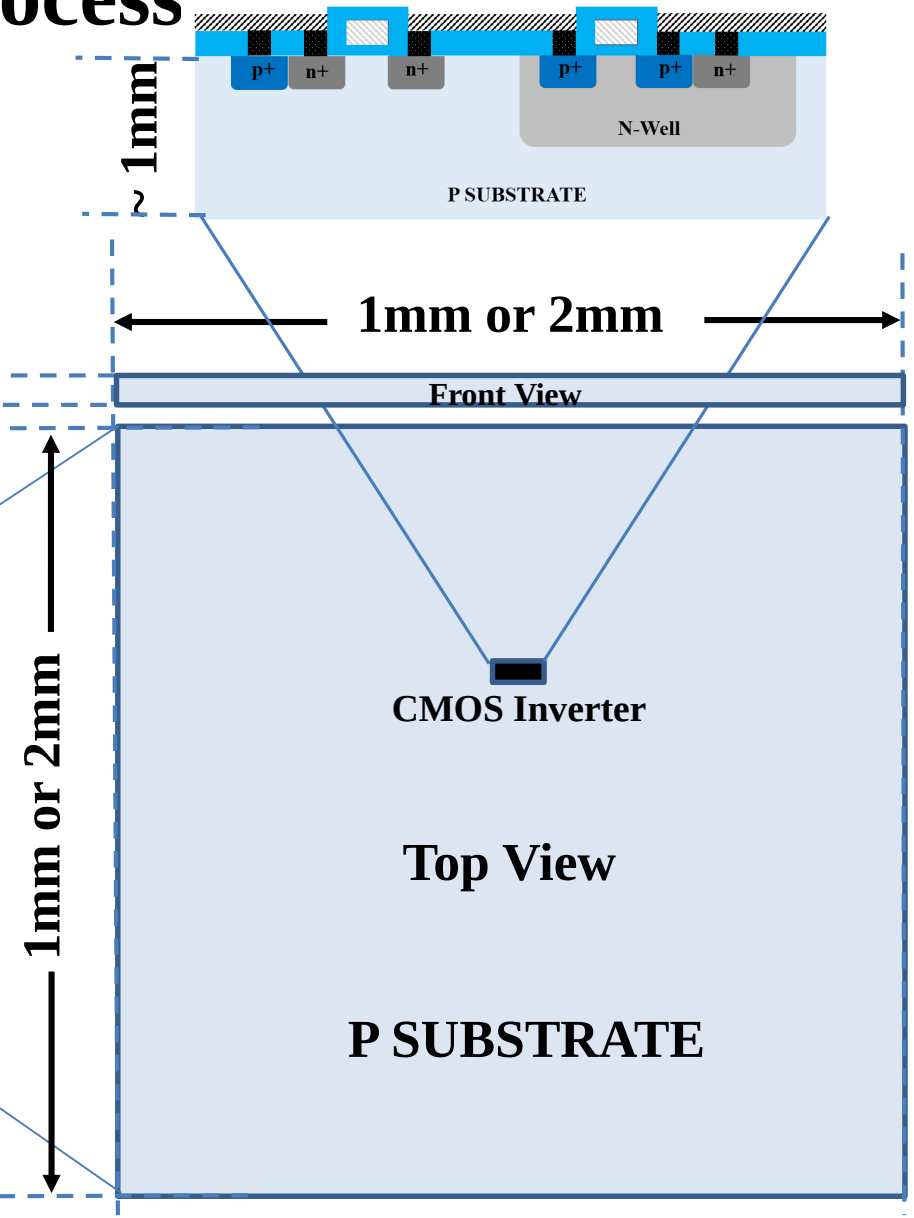
CMOS Fabrication Process



SILICON INGOT

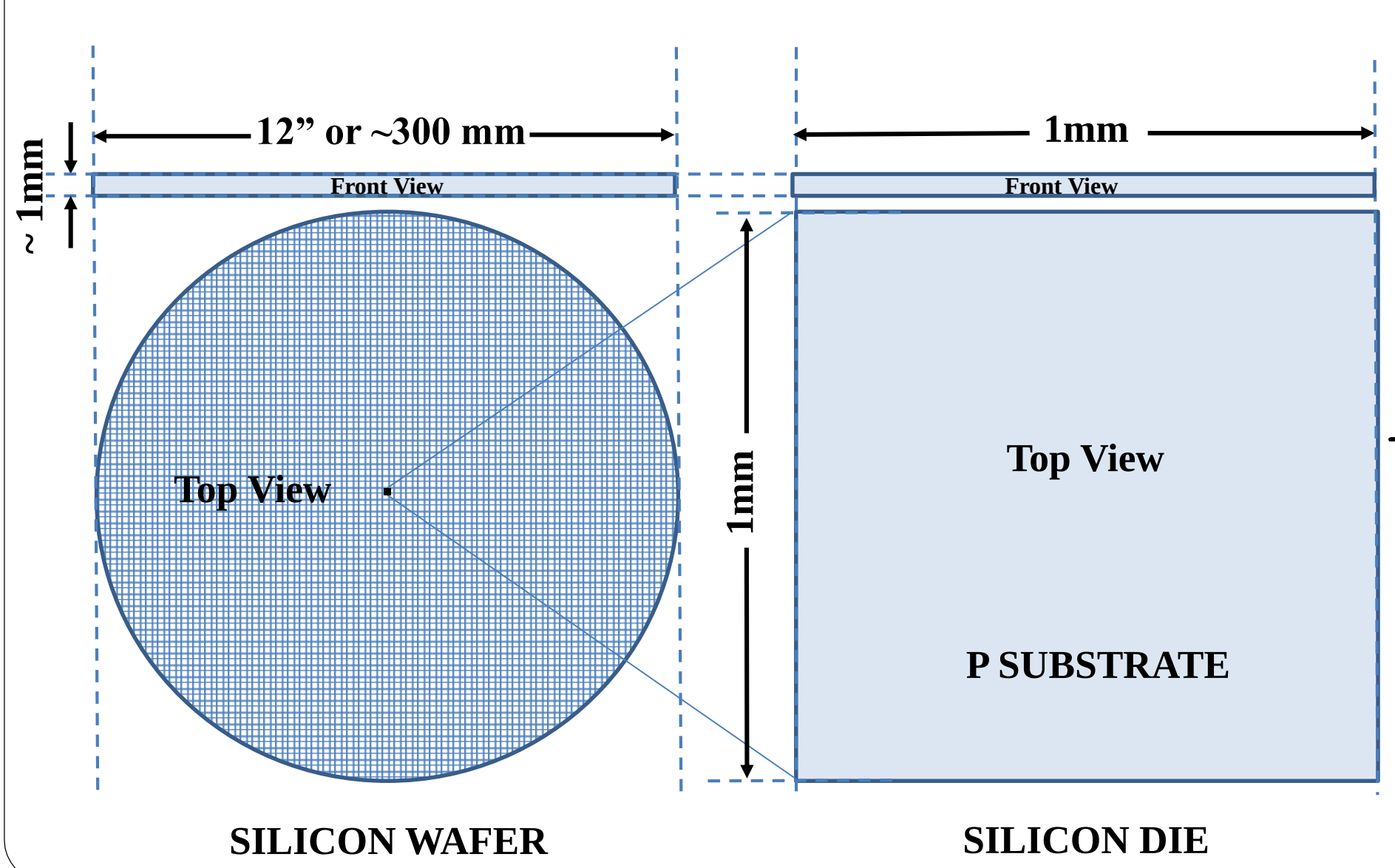


SILICON WAFER



SILICON DIE

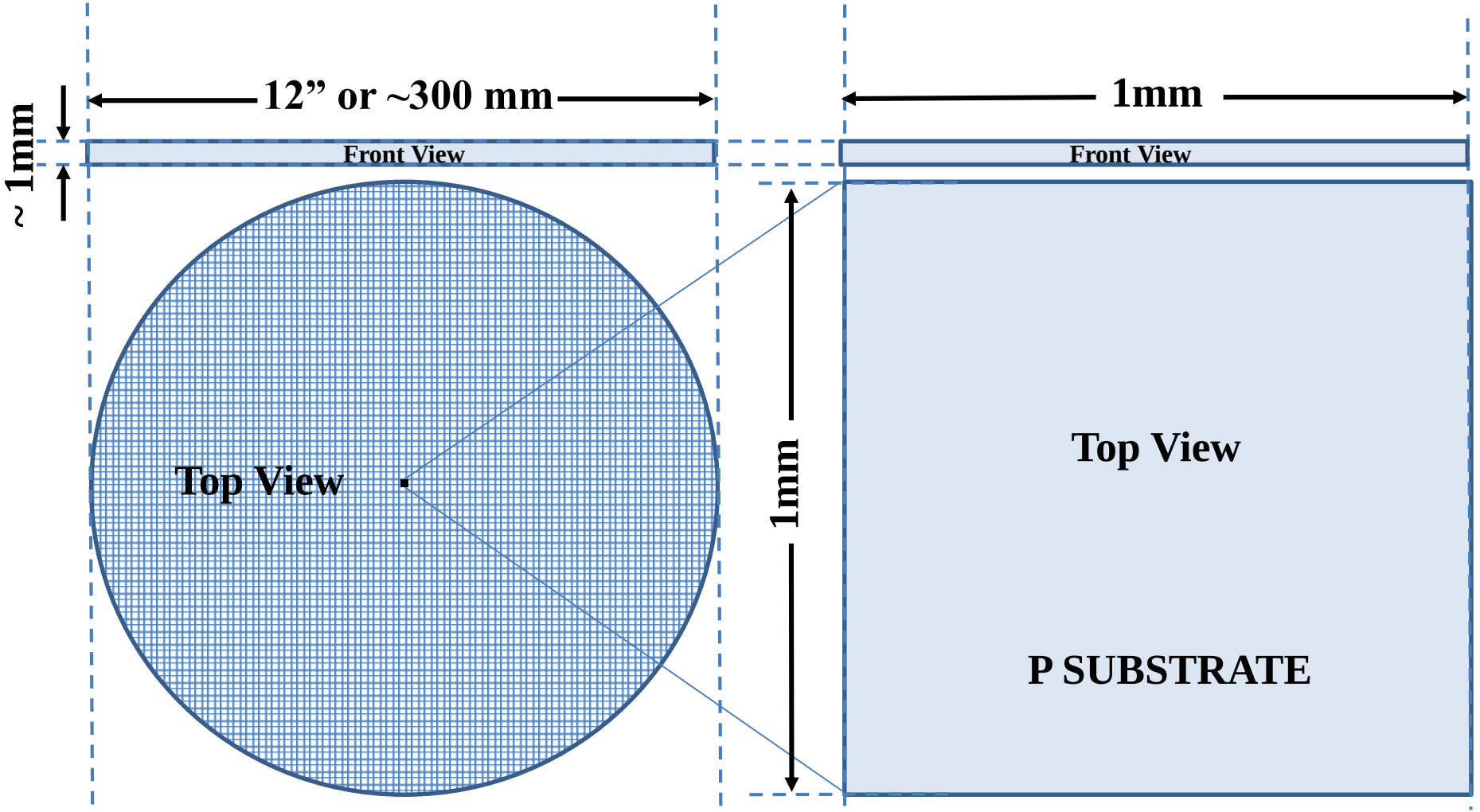
CMOS Fabrication Process



QUIZ: Refer the left side figure and calculate the number of silicon die can be formed from a single silicon wafer.

(a) ~300
(b) ~9,000
(c) ~70,000
(d) ~90,000

CMOS Fabrication Process



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(a) ~300
(b) ~9,000
(c) ~70,000
(d) ~90,000

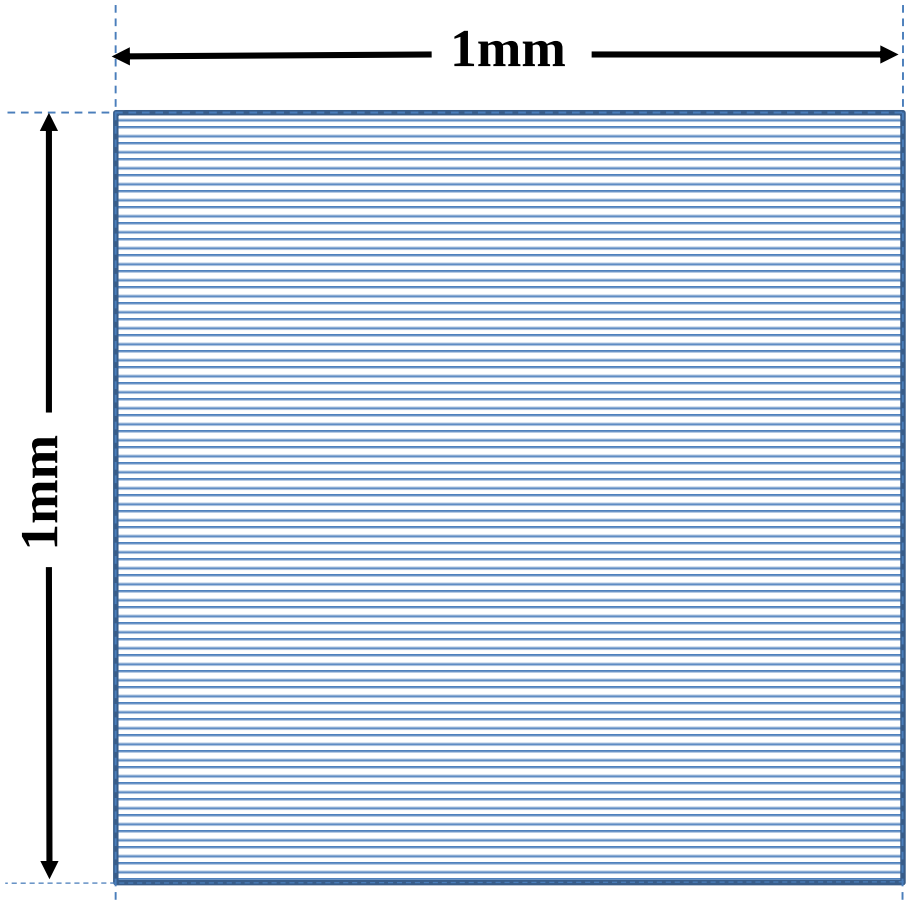
Answer:
Number of die = Area of wafer / Area of die

Area of wafer = PI*150*150 = 70,715 mm2

Area of die = 1 X 1 = 1 mm2

No, of die=70,715/1= 70,715

CMOS Fabrication Process



SILICON DIE

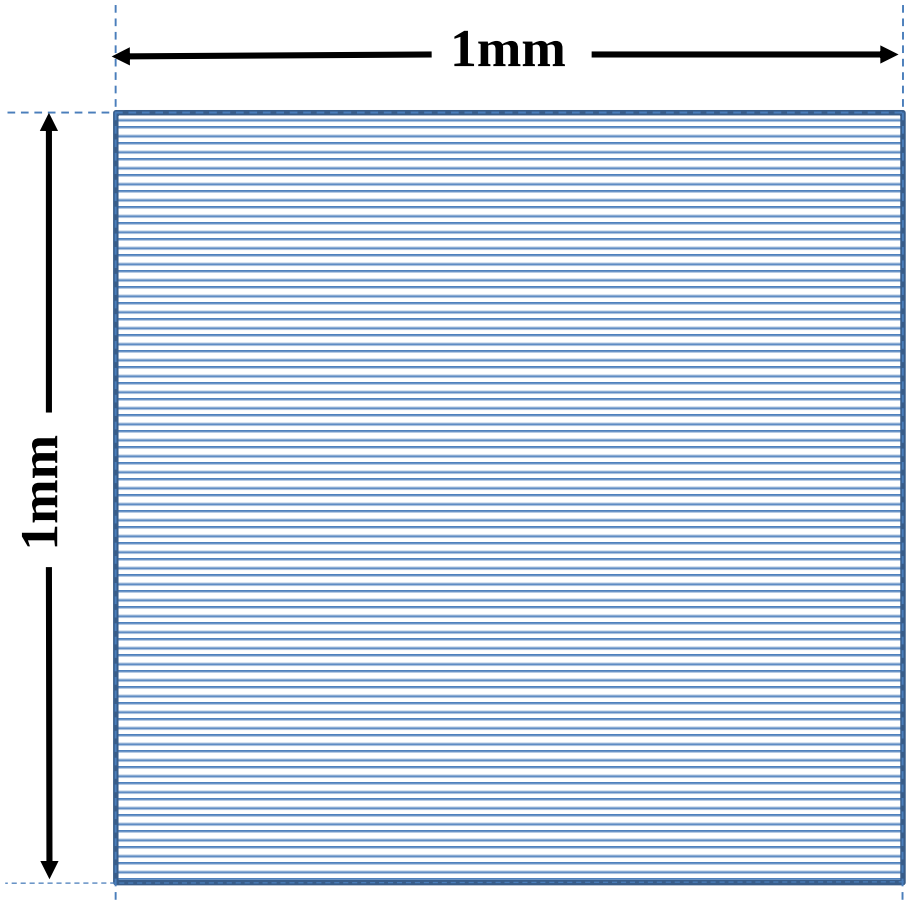
DATA

- Assume the entire silicon die is a digital chip have all the area filled by only standard cells.
- Assume that in one silicon die there are 1000 equal rows and each having 1µm hight.
- Assume that a standard cell having a height of 1µm and a width of 0.25µm.
- Assume standard cell has only one P-MOSFET and one N-MOSFET.
- Assume all the interconnection between all the standard cells are through top metals only.

QUIZ: Refer the left side figure and data given, calculate the number of MOS transistors can be put in a single 1mm X 1mm silicon die.

(a) 1 million
(b) 2 million
(c) 4 million
(d) 8 million

CMOS Fabrication Process



SILICON DIE

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(a) 1 million
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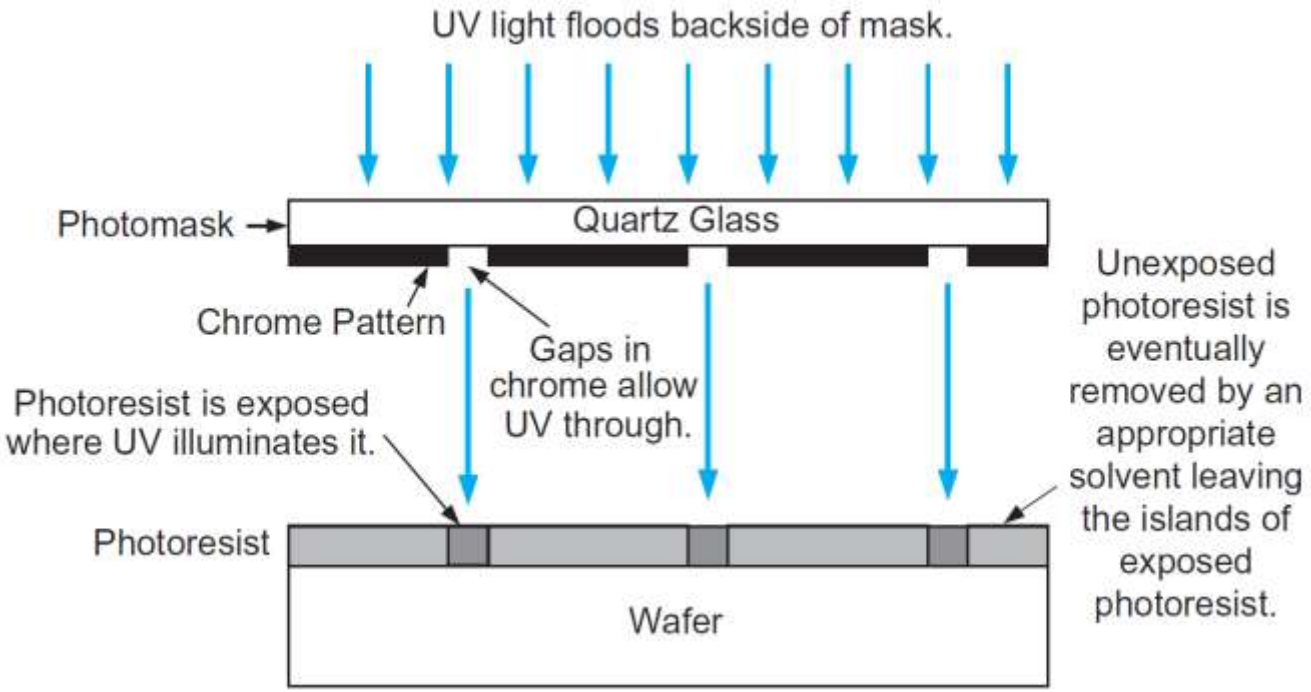
(c) 4 million
(d) 8 million

Answer:

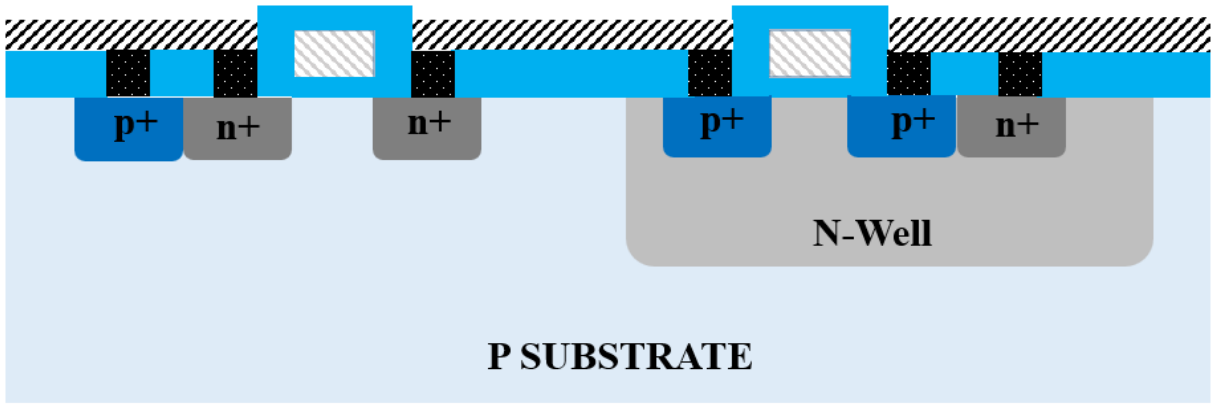
- There are 1000 rows and each having 1µm height.
- Per row 4000 standard cells
- Per row 8000 transistors
- In 1000 tows, 8000*1000=8000000
- Or 8 million transistors

2. Photolithography

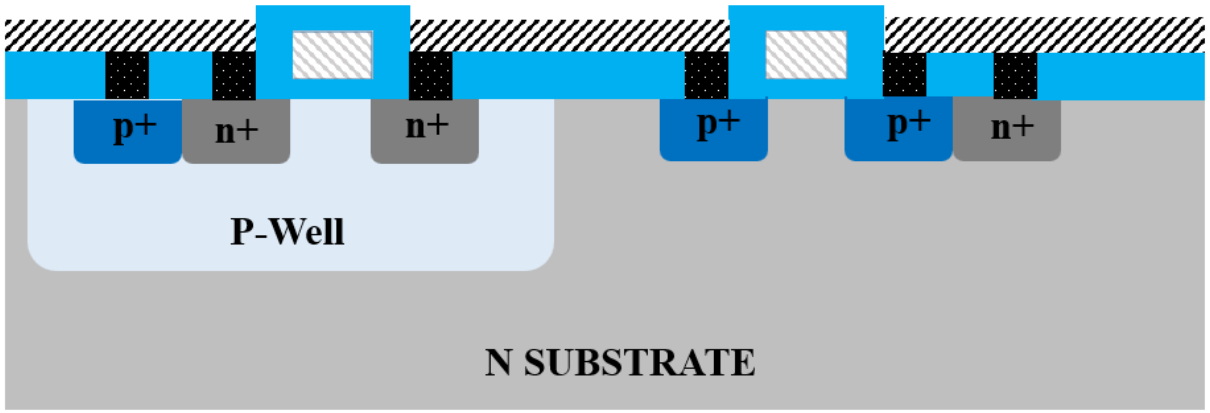


Photolithography process [Waste and Harris]

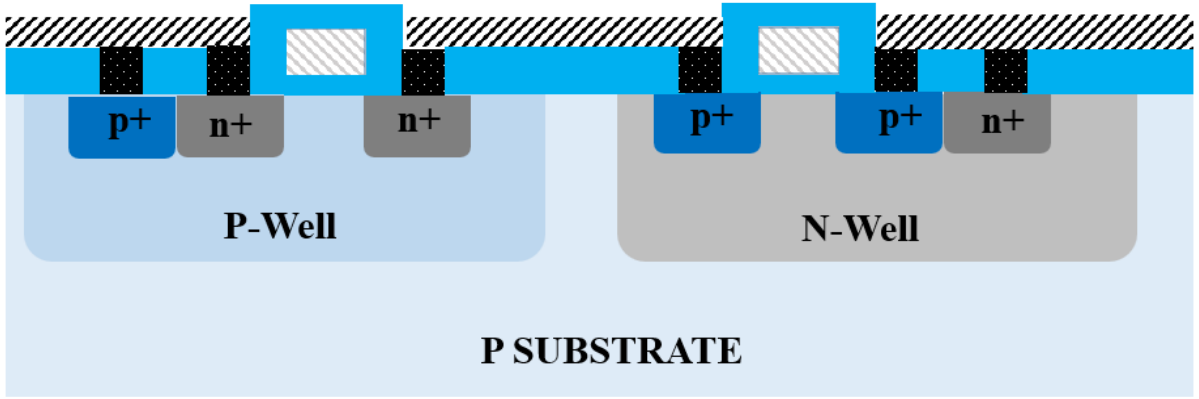
3. Well and Channel Formation



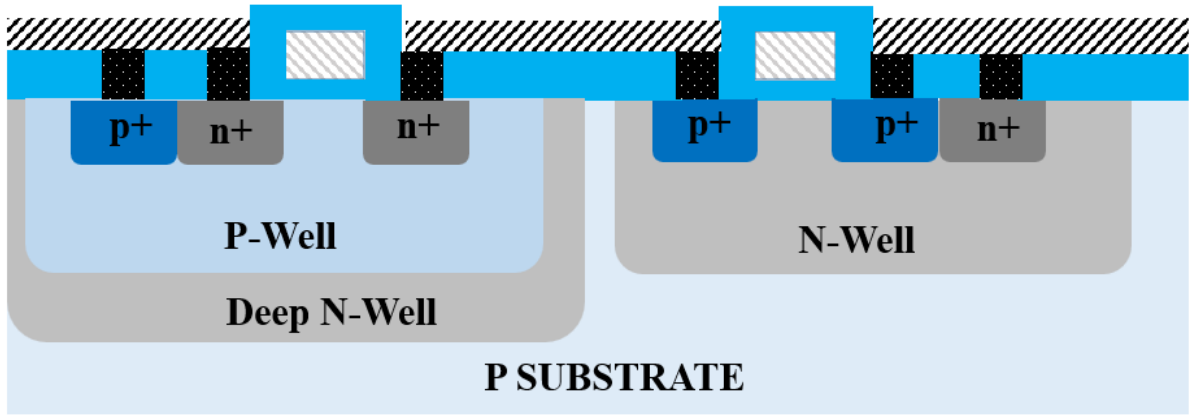
1. N-Well Process



2. P-Well Process



3. Twin-Well Process



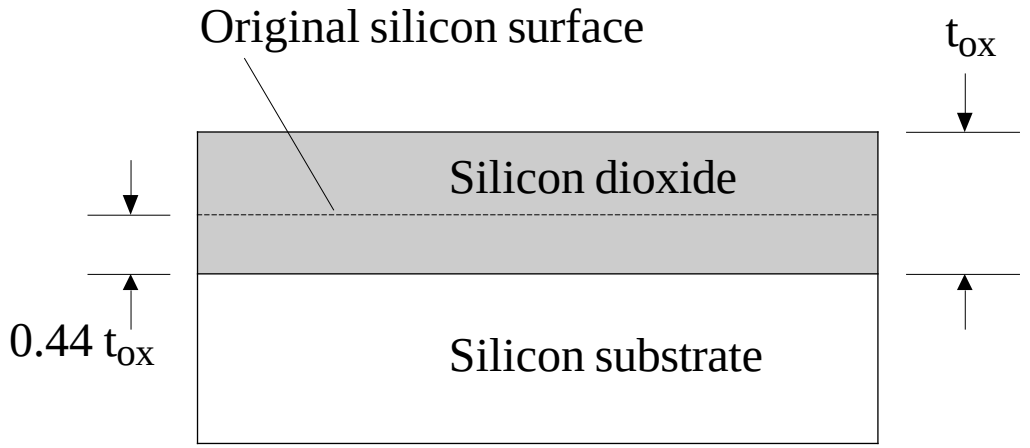
4. Tripple-Well Process

4. Silicon Dioxide (Sio2)

- Oxidation of silicon is achieved by heating silicon wafers in an oxidizing atmosphere. The following are some common approaches:

- **Wet Oxidation:** The oxidizing atmosphere contains water vapor.
  - The temperature is usually between 900 °C and 1000 °C.
  - Wet oxidation is a rapid process.
  - Used to form thick field oxides

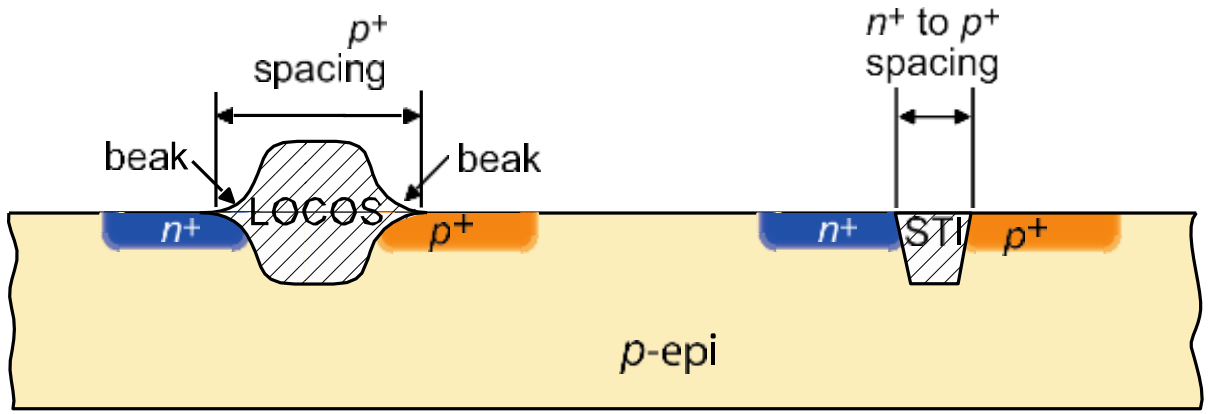
- **Dry Oxidation:** The oxidizing atmosphere is pure oxygen.
  - Temperatures are in the region of 1200 °C to achieve an acceptable growth rate.
  - Dry oxidation forms a better-quality oxide than wet oxidation.
  - Used to form thin, highly controlled gate oxides.



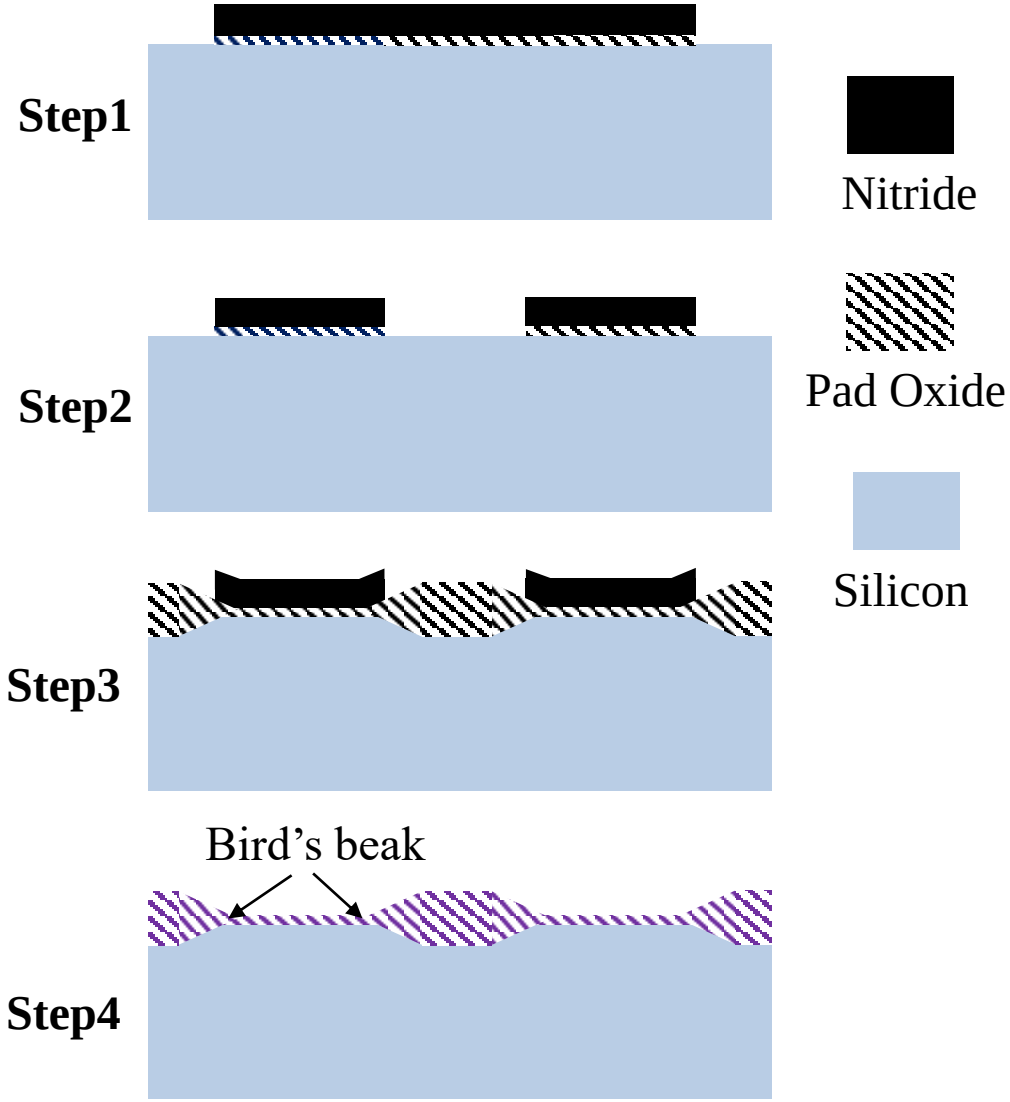
5. Isolation

5. Isolation

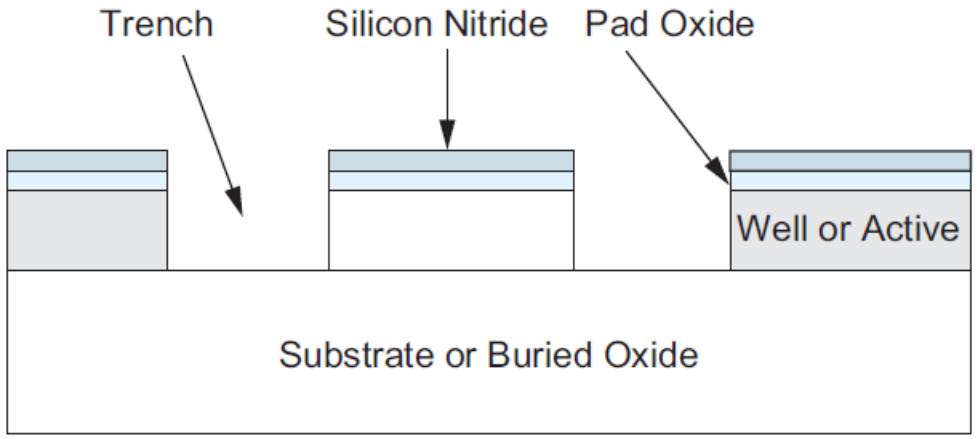
- Individual devices in a CMOS process need to be isolated from one another
- The transistor gate consists of a thin gate oxide layer.
- The thick oxide used to be formed by a process called Local Oxidation of Silicon (LOCOS).
- A problem with LOCOS-based processes is the transition between thick and thin oxide, which extends some distance laterally to form a so-called bird's beak.
- Starting around the 0.35 µm node, STI was introduced to avoid the problems with LOCOS.
- STI forms insulating trenches of SiO2 surrounding the transistors (everywhere except the active area).



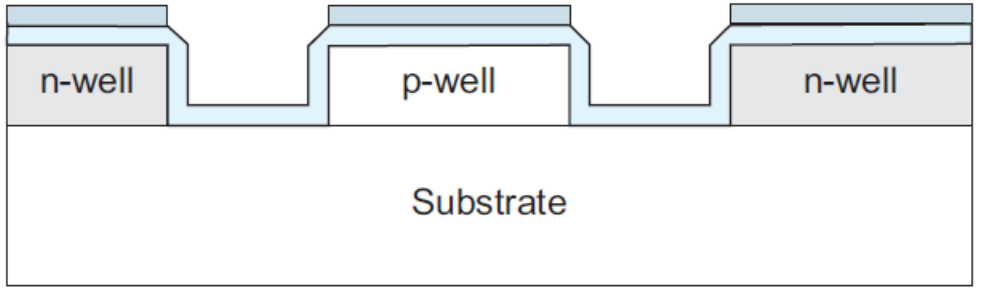
Local Oxidation of Silicon (LOCOS)



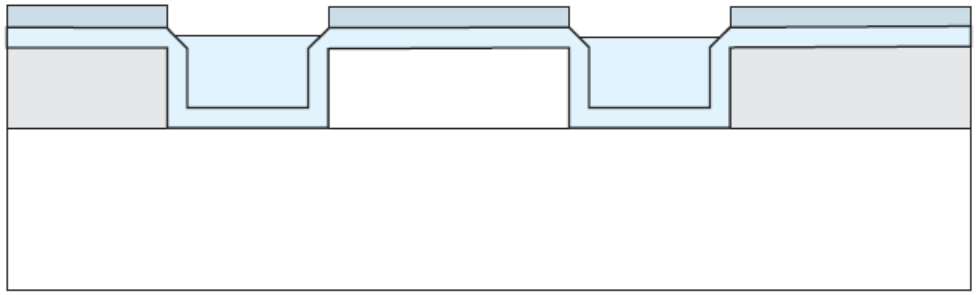
Sallow Trench Isolation



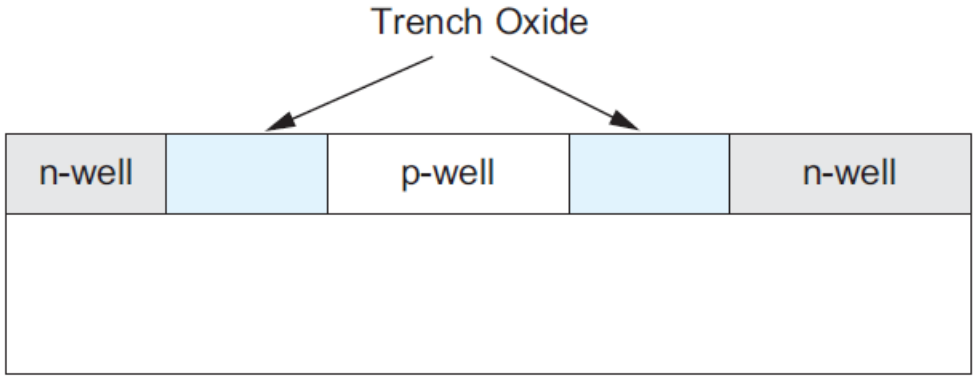
(a) Trench Etch



(b) Liner Oxidation



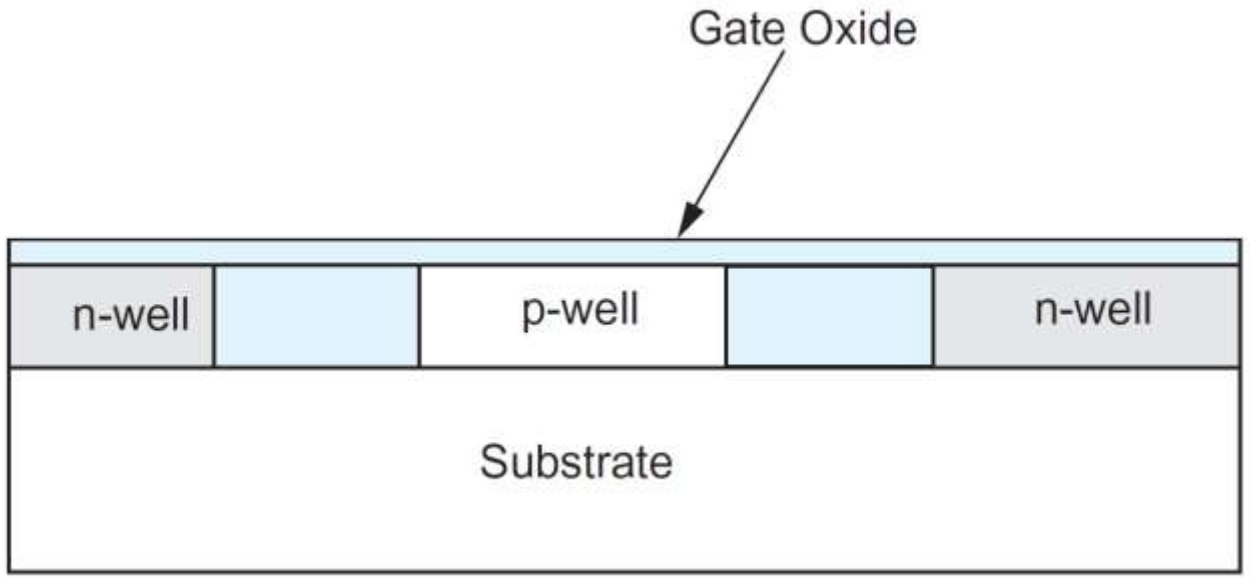
(c) Fill Trench with Dielectric



(d) CMP for Planarization

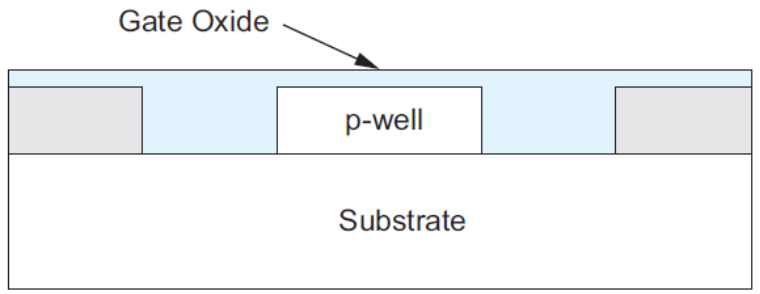
6. Gate Oxide

- The next step in the process is to form the gate oxide for the transistors. As mentioned, this is most commonly in the form of silicon dioxide (SiO2).The transistor gate consists of a thin gate oxide layer.

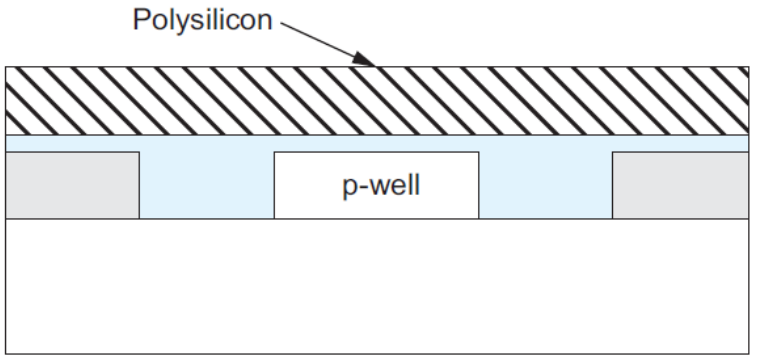


7. Gate and Source/Drain Formation

a) Grow gate oxide
b) Deposit polysilicon
c) Pattern polysilicon
d) Etch exposed gate oxide
e) Implant PMOS and NMOS

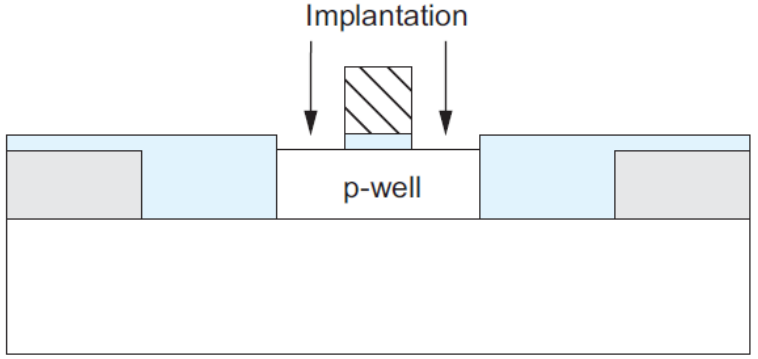


(a)

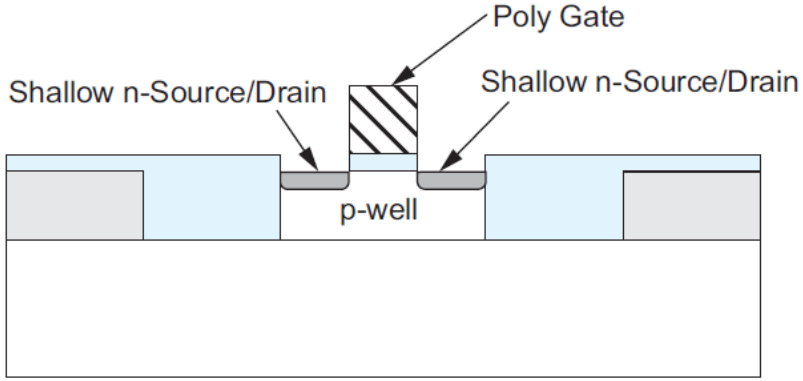


(b)

(c)



(d)



(e)

7. Gate and Source/Drain Formation

a) Grow gate oxide
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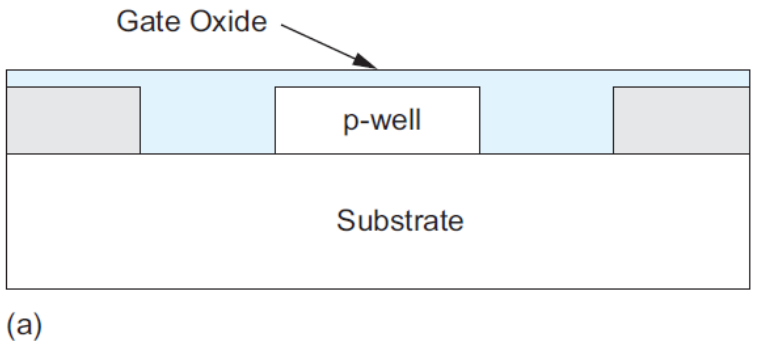
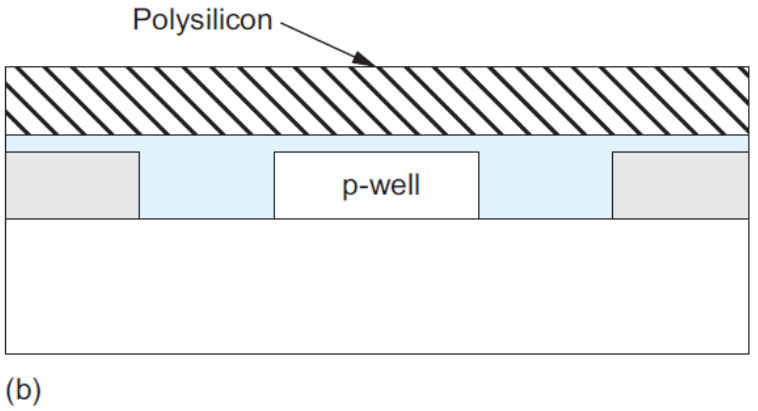
d) Etch exposed gate oxide
e) Implant PMOS and NMOS

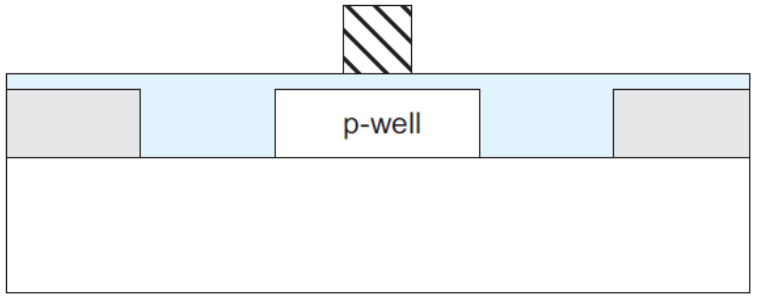
Why not Metal gate?



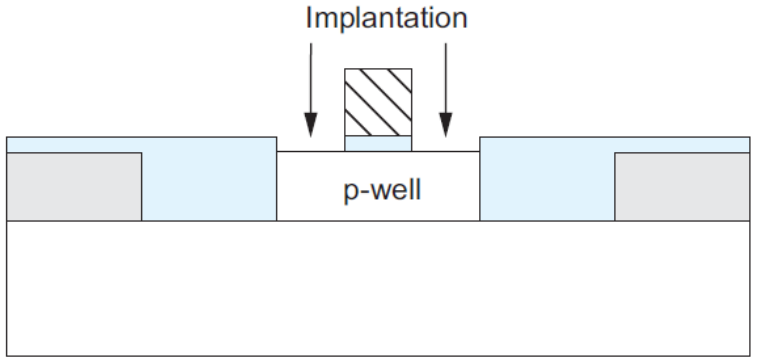
(a)



(b)



(c)



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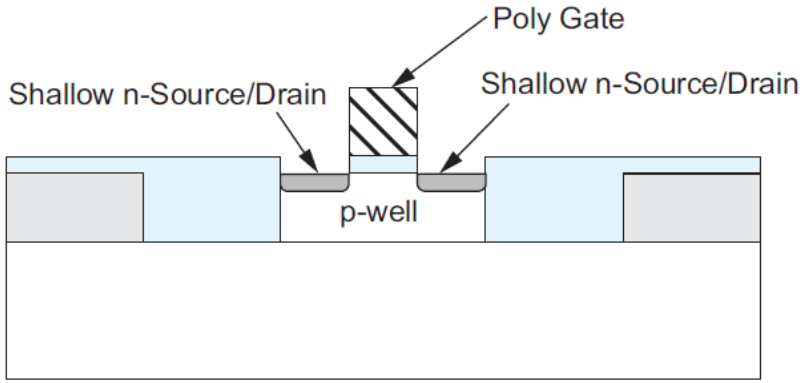


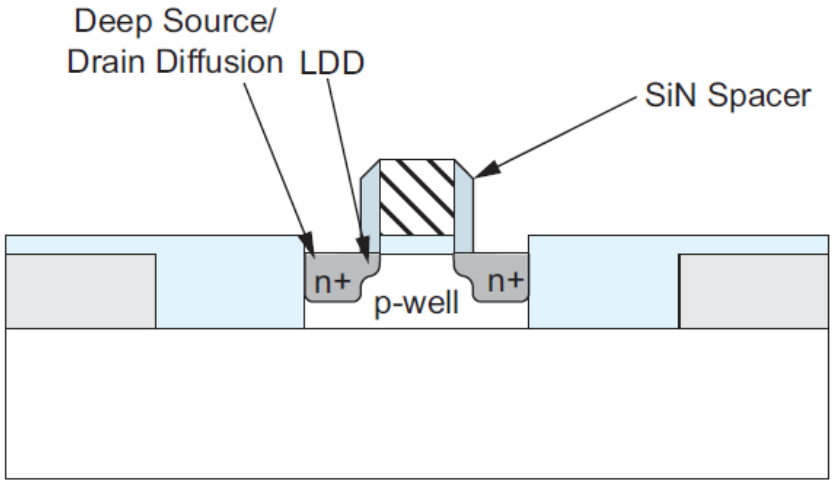
(e)

7. Gate and Source/Drain Formation

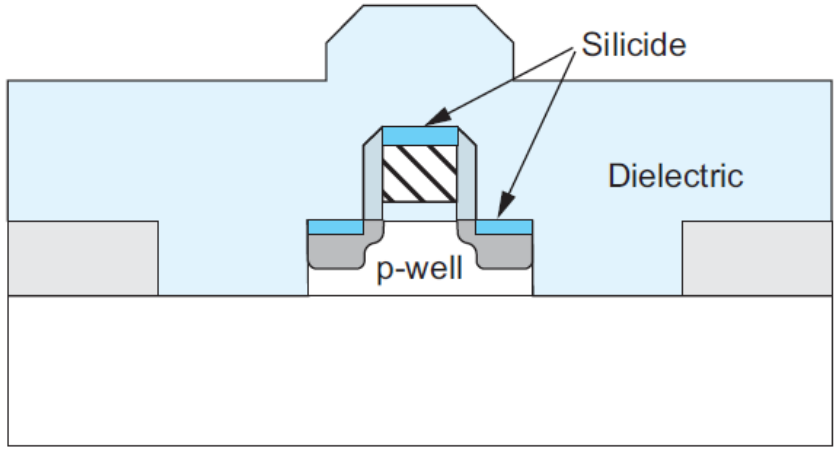
a) Short-channel engineering

b) Silicide Gate and Source/Drain

c) Chemical and Mechanical Polishing



(a)



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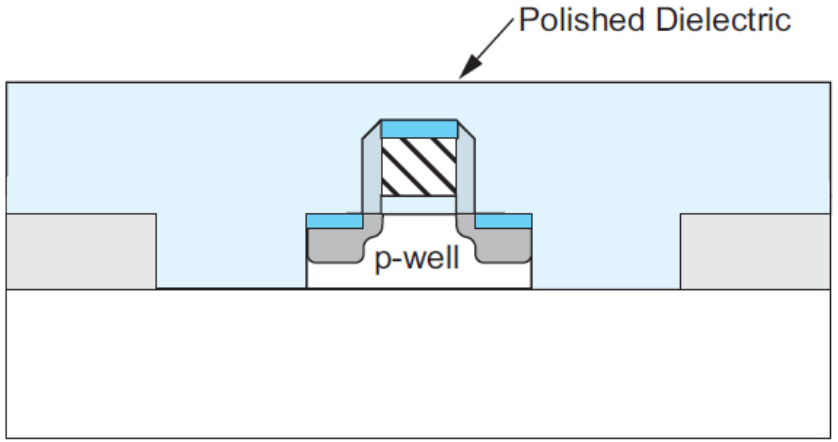
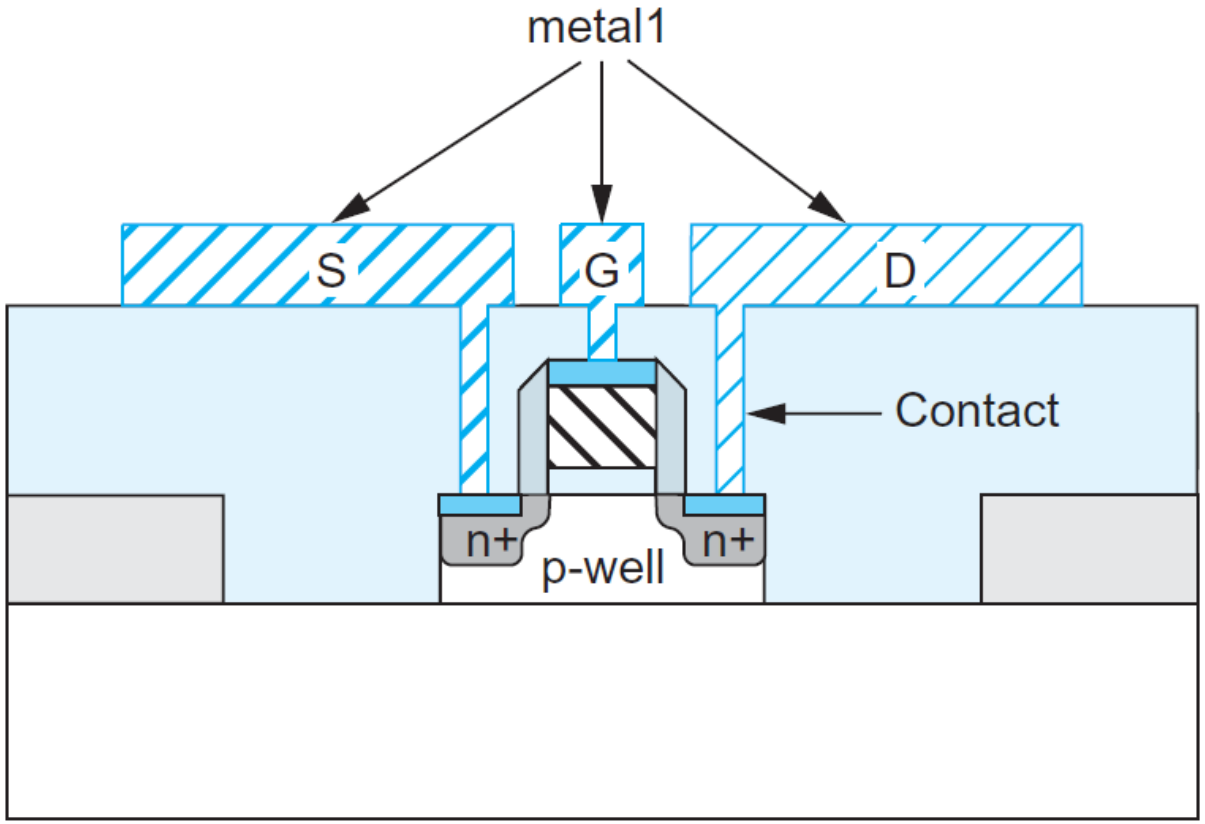
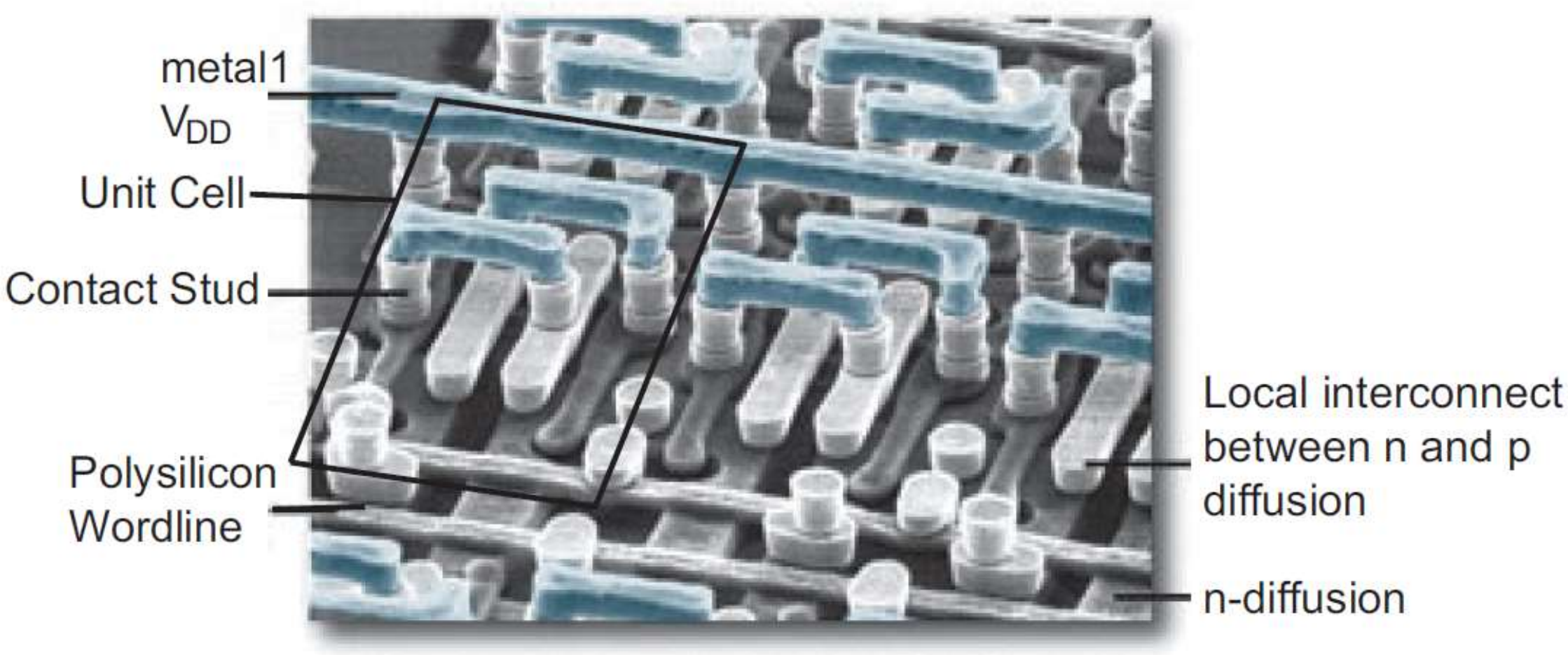


(c)

8. Contacts and Metalization



8. Contacts and Metallization



Partially completed 6-transistor SRAM array using local interconnect (Courtesy: Waste and Harris)

9. Passivation

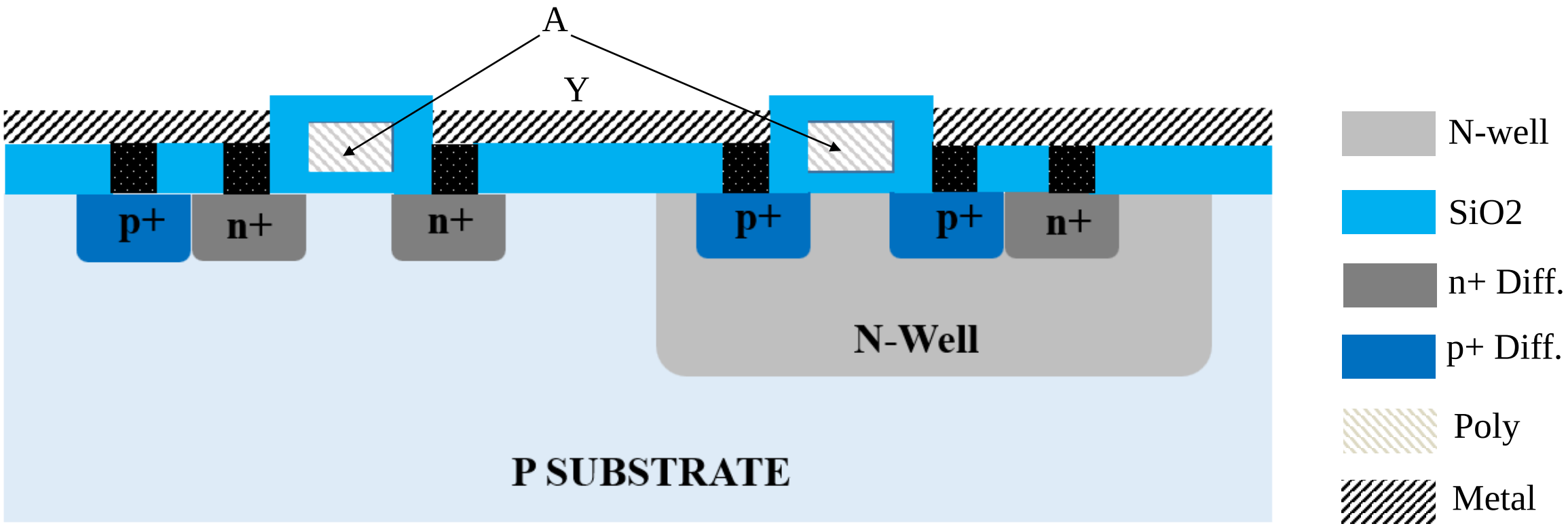
- The final processing step is to add a protective glass layer called passivation or over glass that prevents the ingress of contaminants.
- Openings in the passivation layer, called overglass cuts, allow connection to I/O pads and test probe points if needed.

10. Metrology

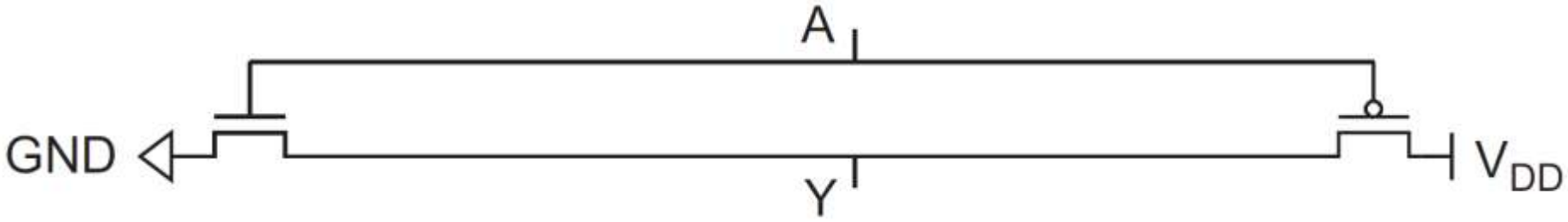
- Metrology is the science of measuring. Everything that is built in a semiconductor process has to be measured to give feedback to the manufacturing process**.**
- This ranges from simple optical measurements of line widths to advanced techniques to measure thin films and defects such as voids in copper interconnects.

CMOS Fabrication Process

CMOS Fabrication Process



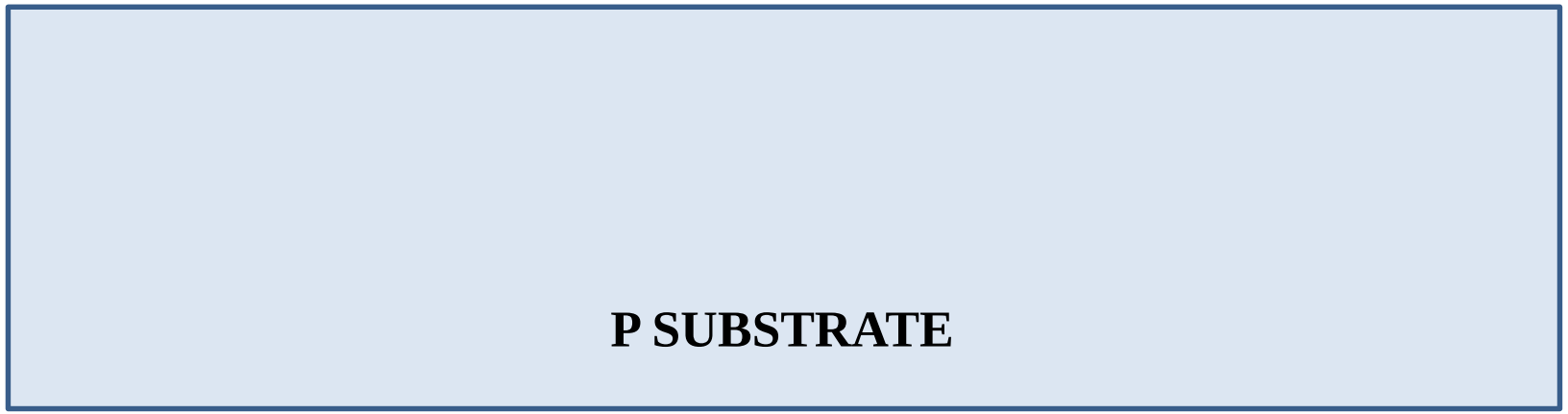
Inverter cross section with well and substrate contact



Inverter Schematic

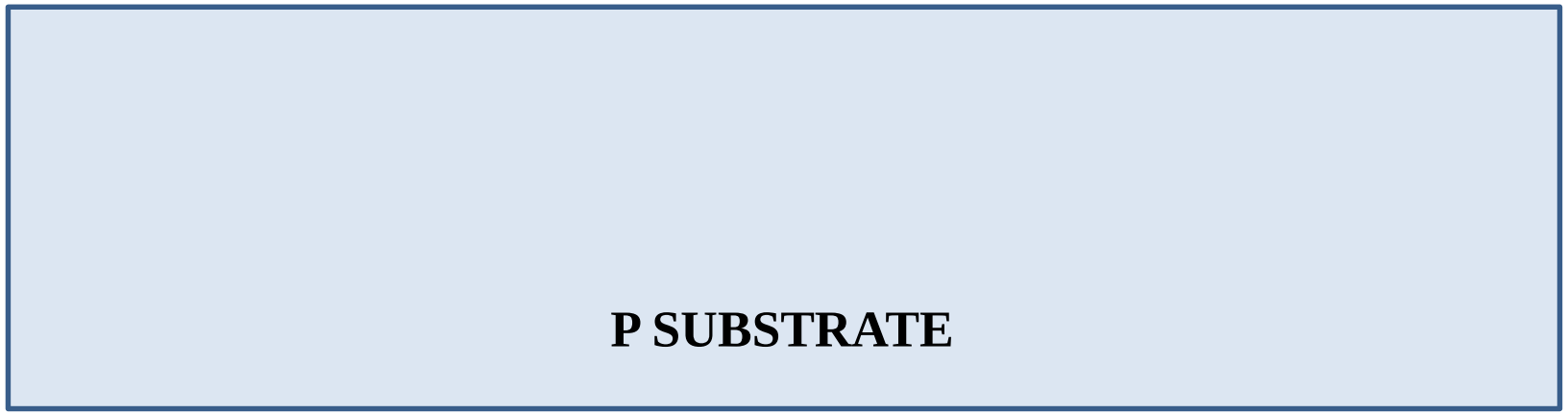
CMOS Fabrication Process

Substrate Creation

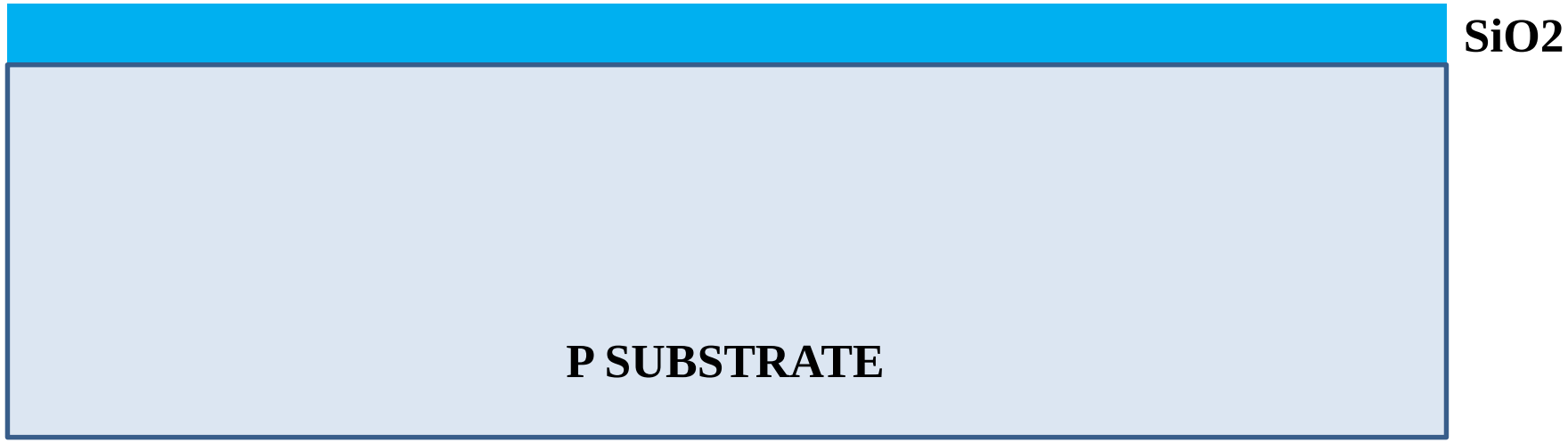


CMOS Fabrication Process

Substrate Creation

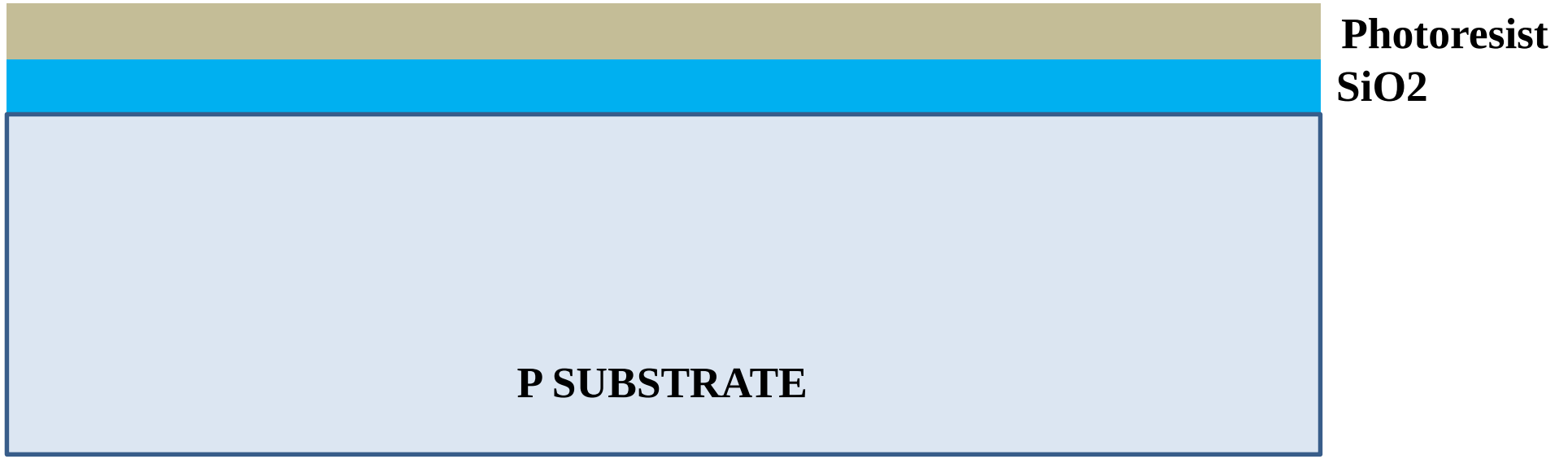


Deposition of protective SiO2



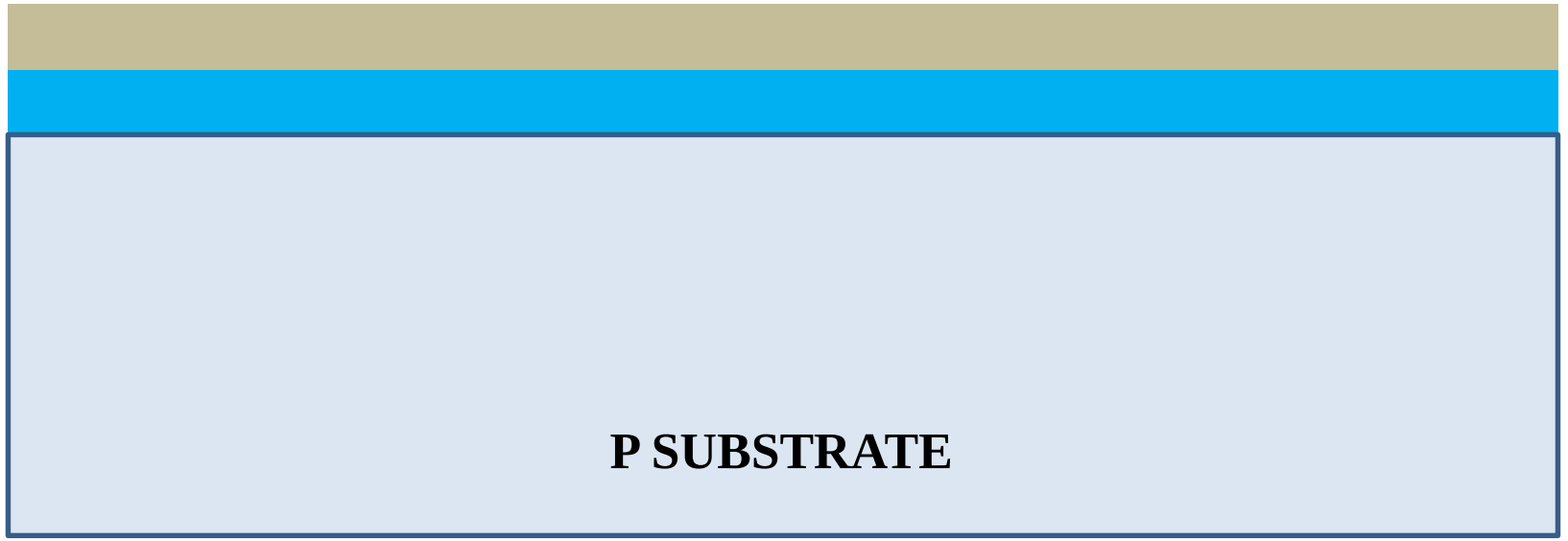
CMOS Fabrication Process

Deposition of photoresist material

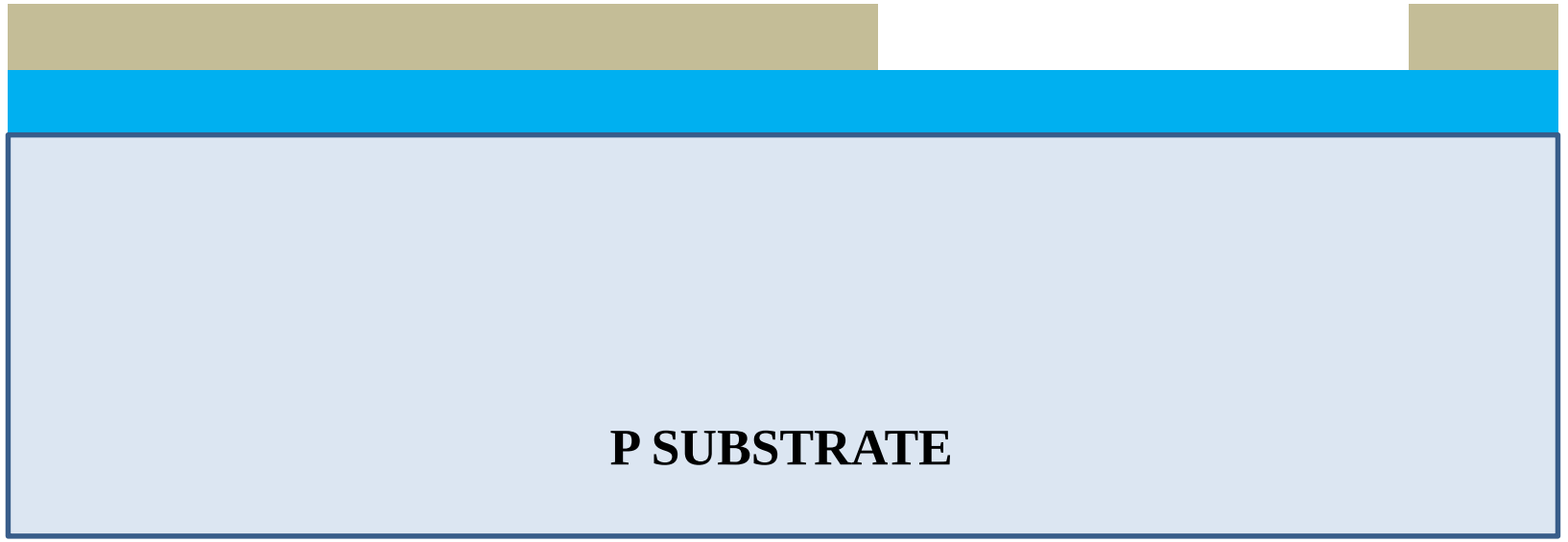


CMOS Fabrication Process

Deposition of photoresist material

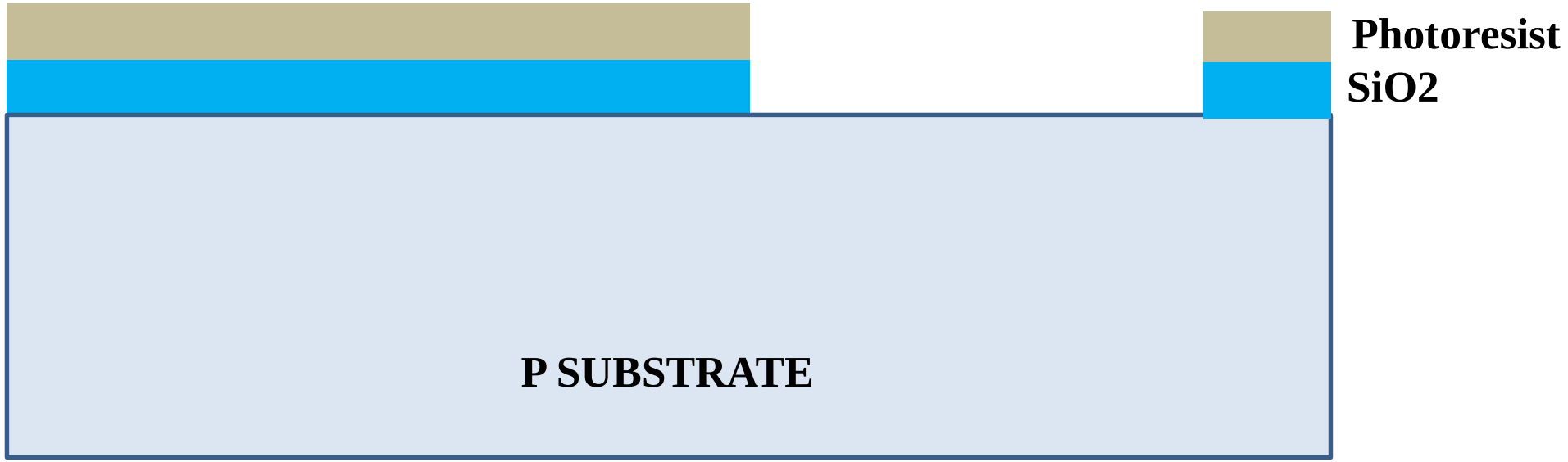


Etching of photoresist material



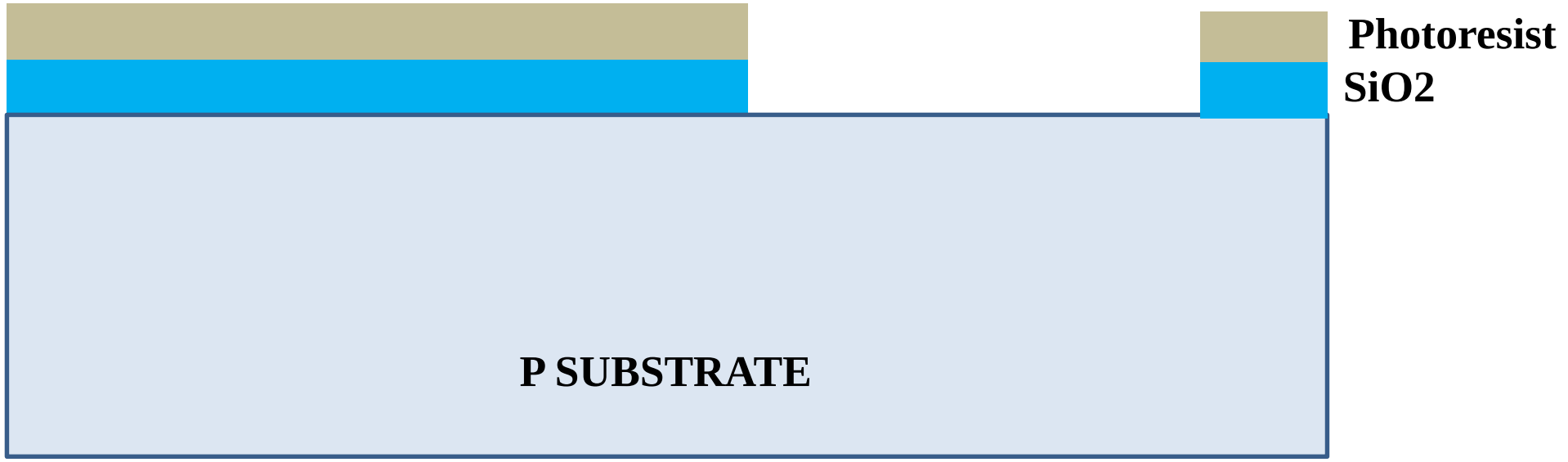
CMOS Fabrication Process

Etching of SiO2

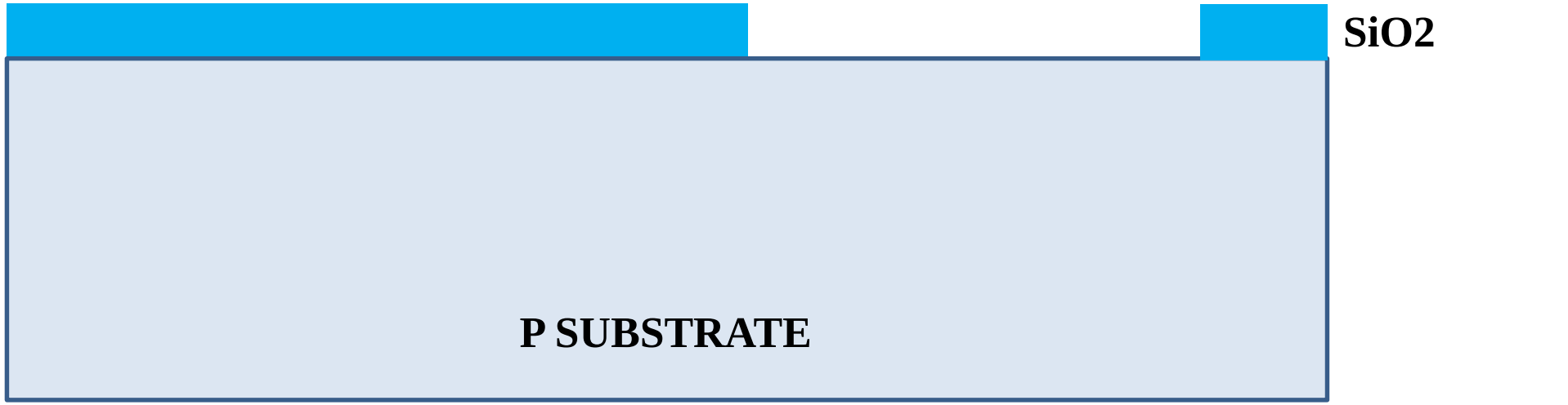


CMOS Fabrication Process

Etching of SiO2

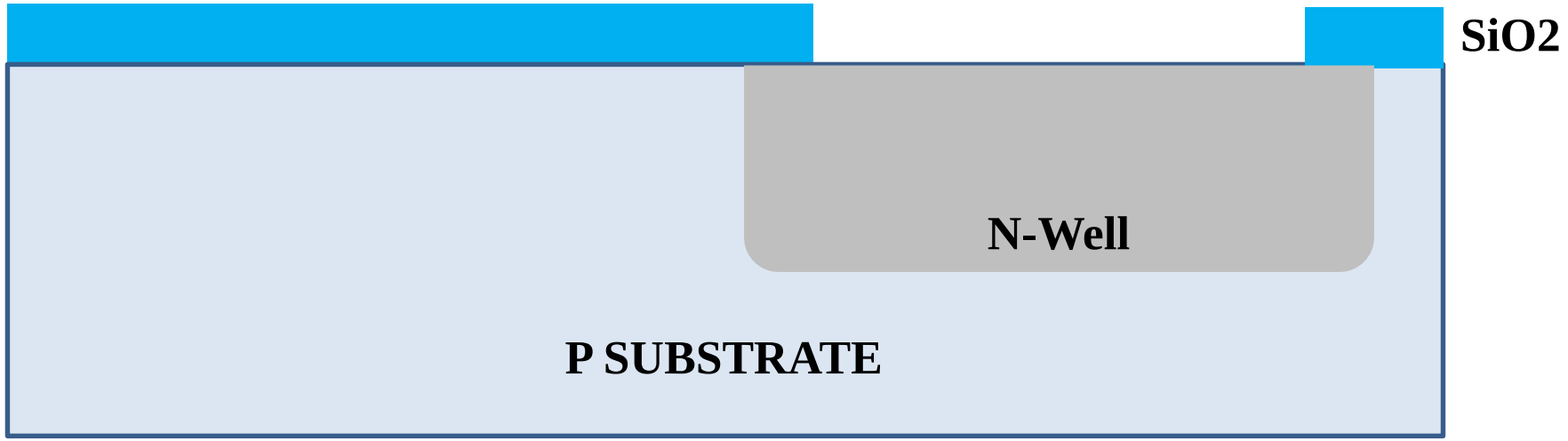


Complete Etching of photoresist material



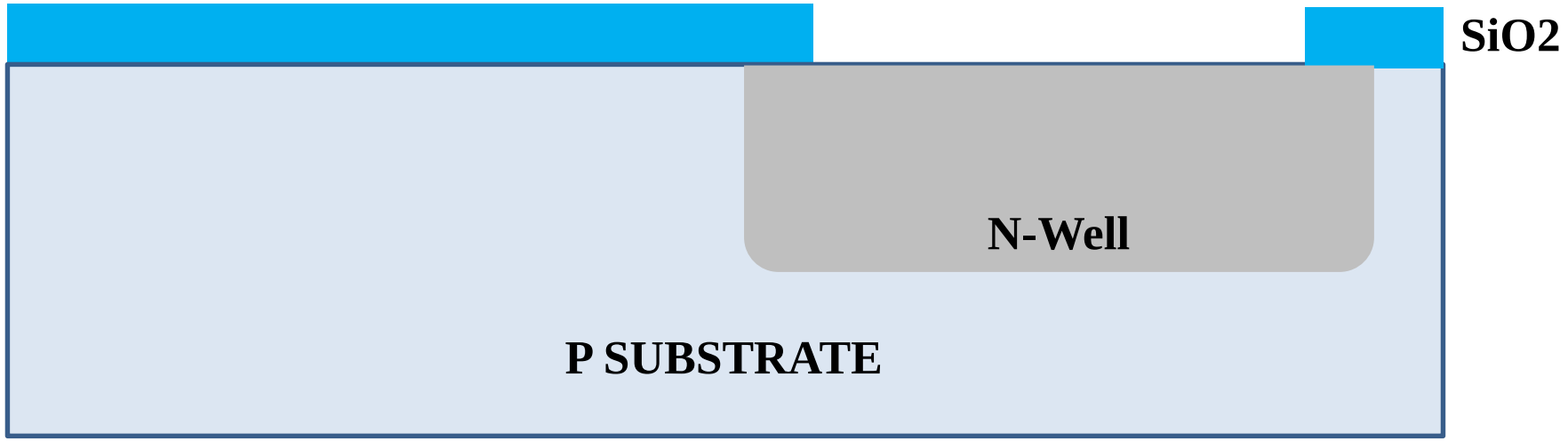
CMOS Fabrication Process

N-well Creation

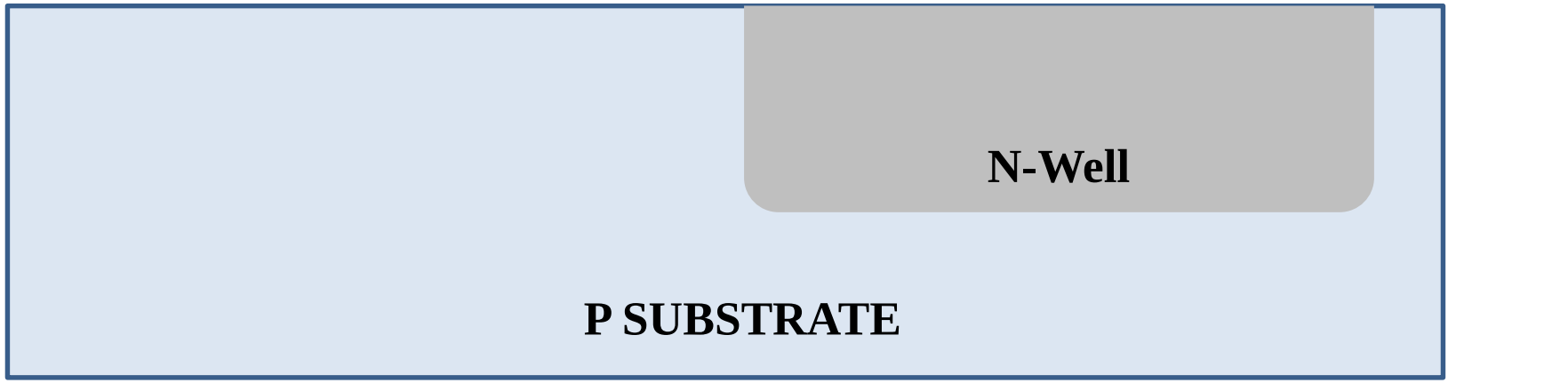


CMOS Fabrication Process

N-well Creation

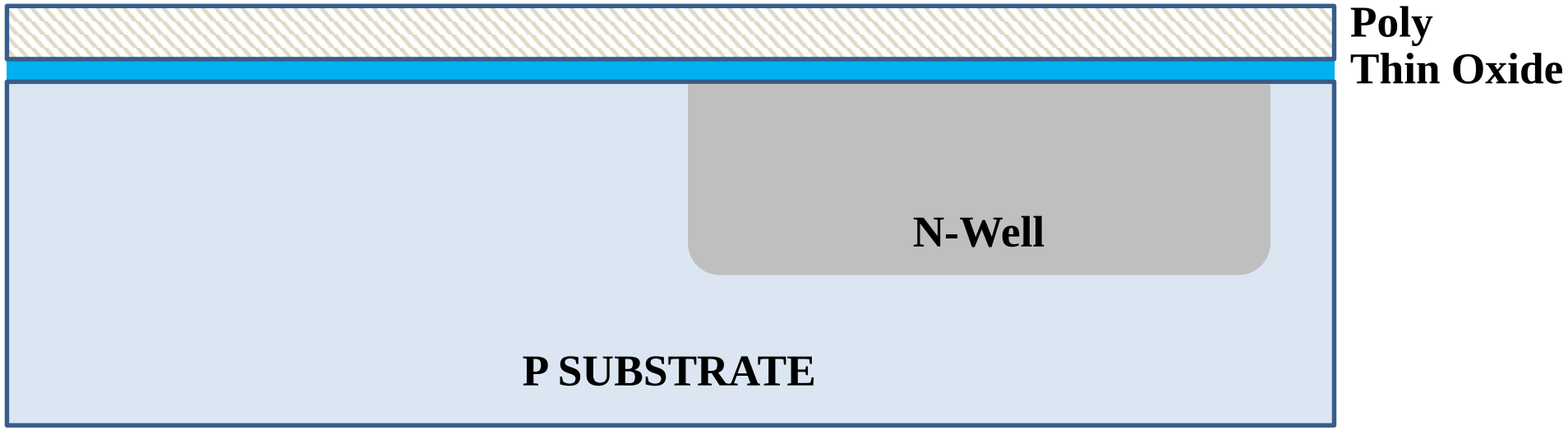


Etching of SiO2



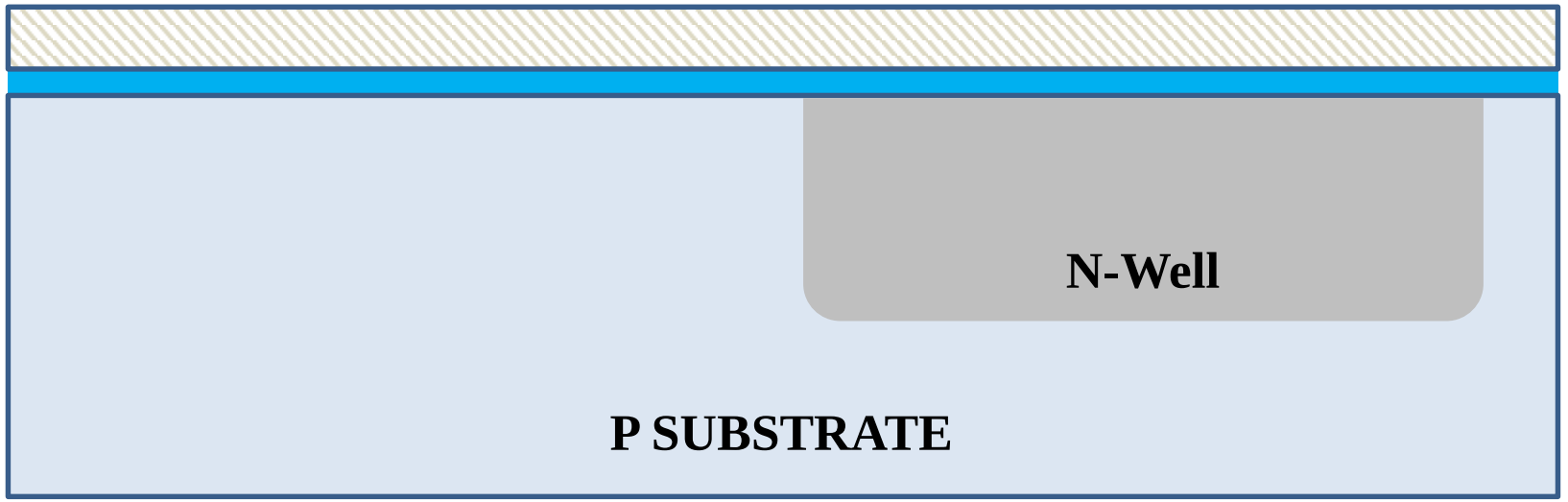
CMOS Fabrication Process

Thin Oxide and Poly Deposition

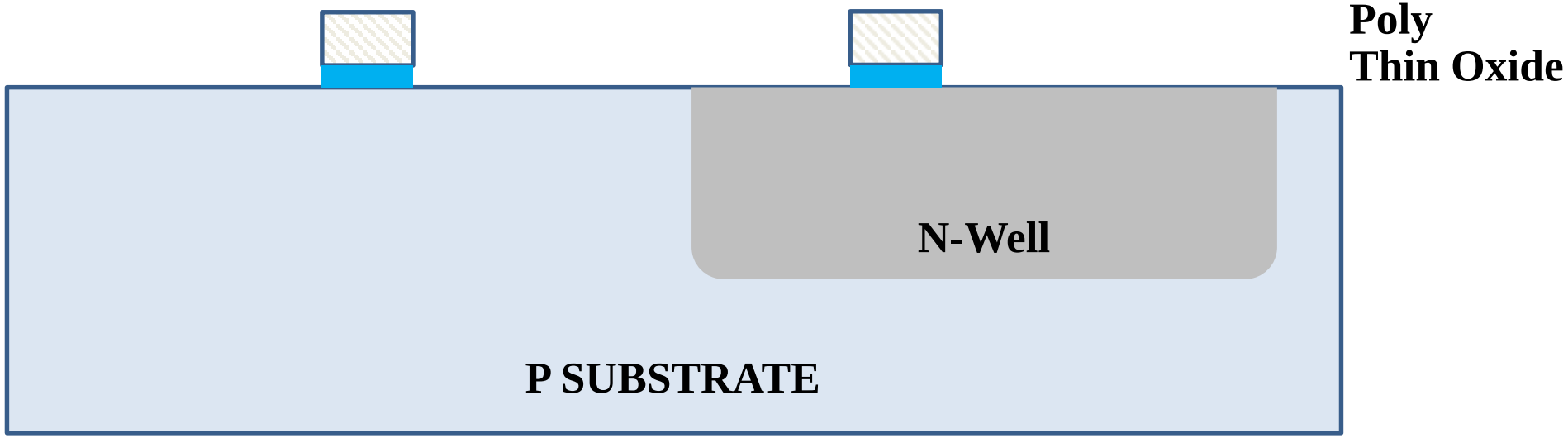


CMOS Fabrication Process

Thin Oxide and Poly Deposition

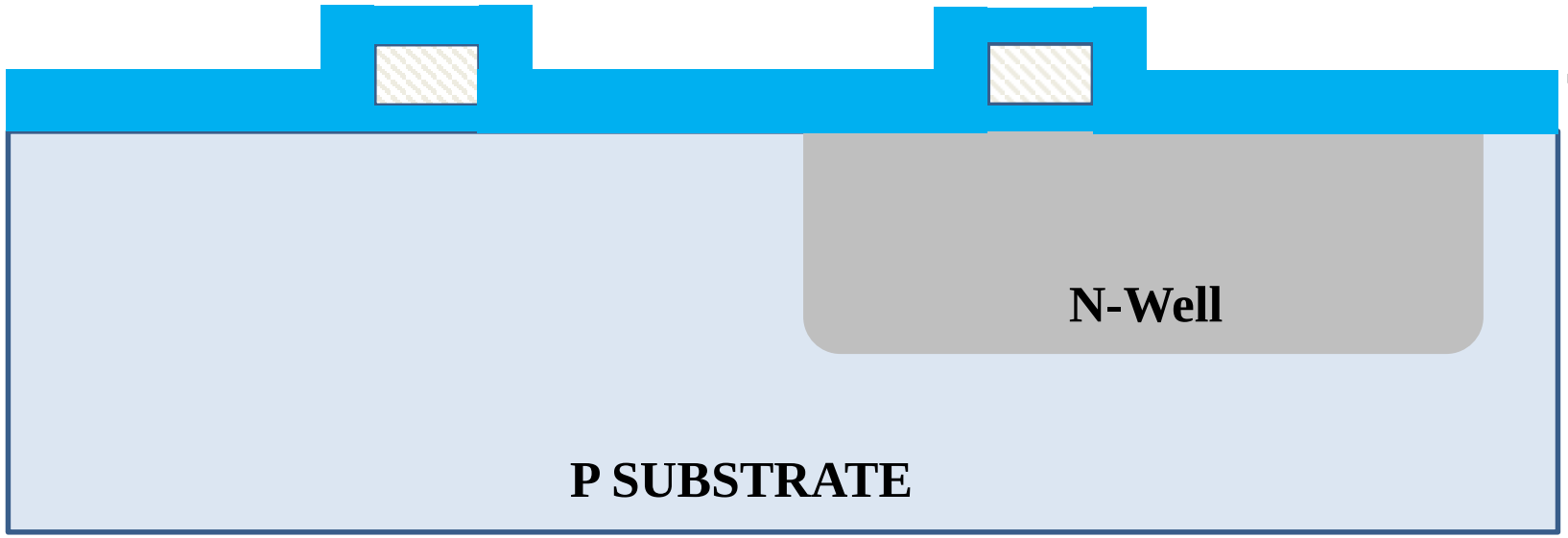


Etching of Thin Oxide and poly except the gate region



CMOS Fabrication Process

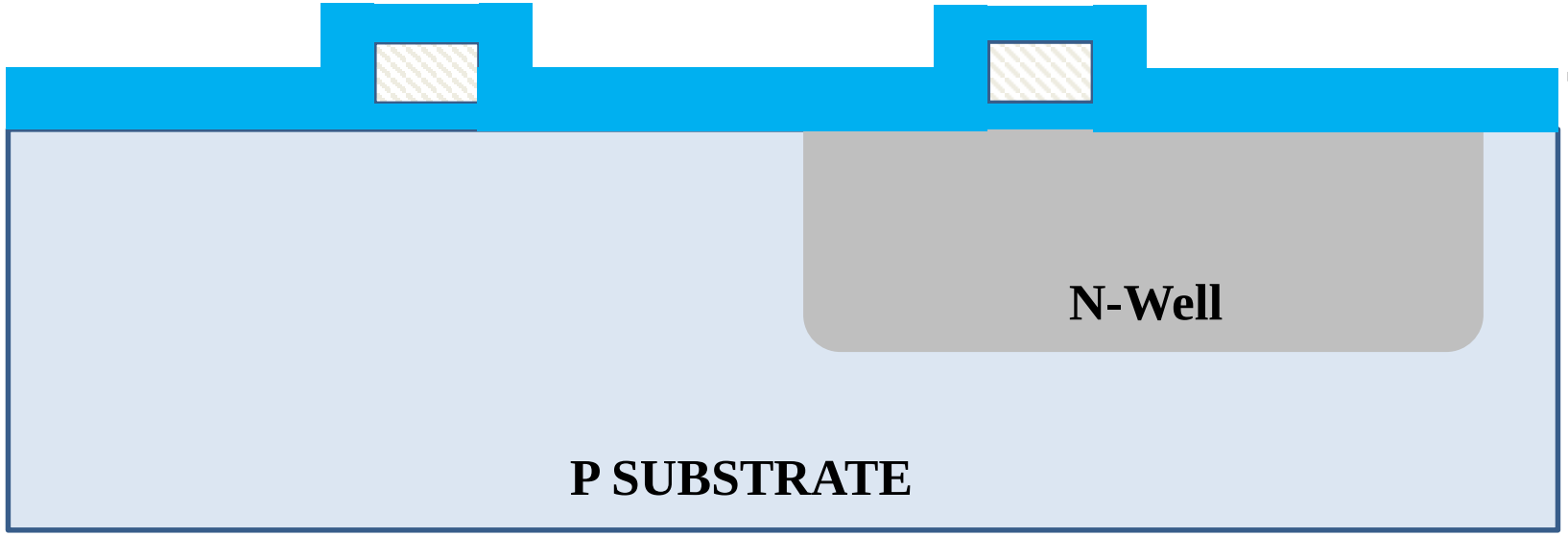
Thick Oxide Deposition



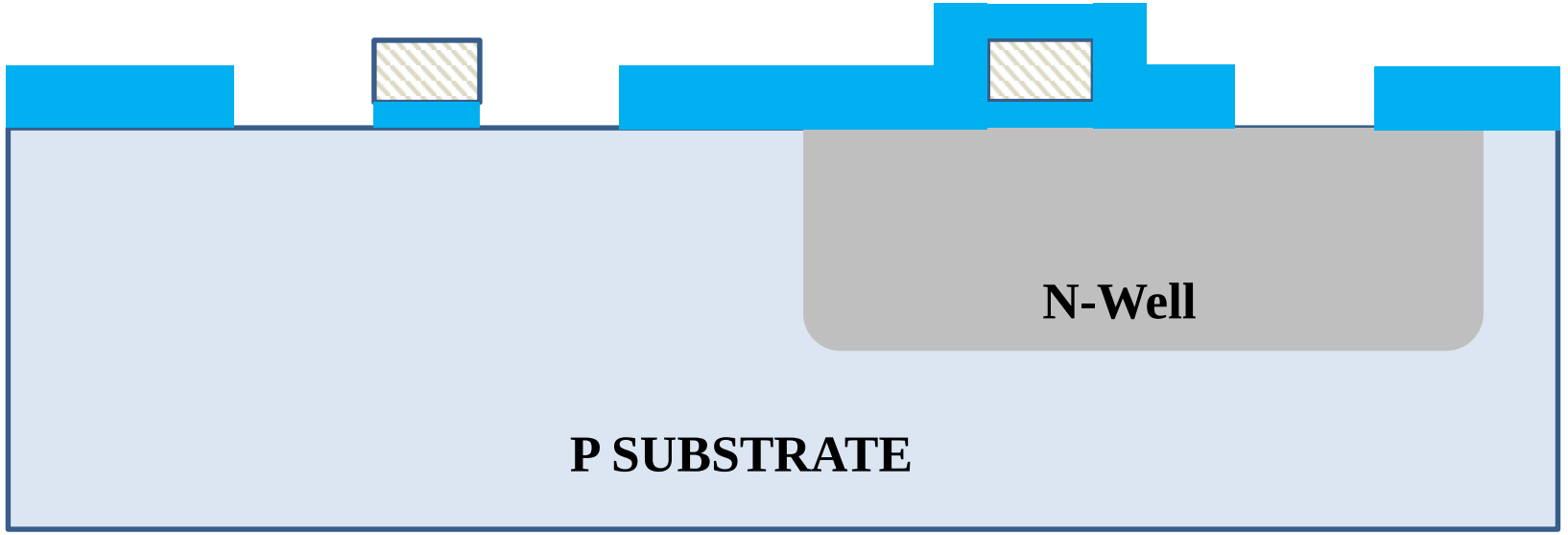
Thick Field Oxide

CMOS Fabrication Process

Thick Oxide Deposition

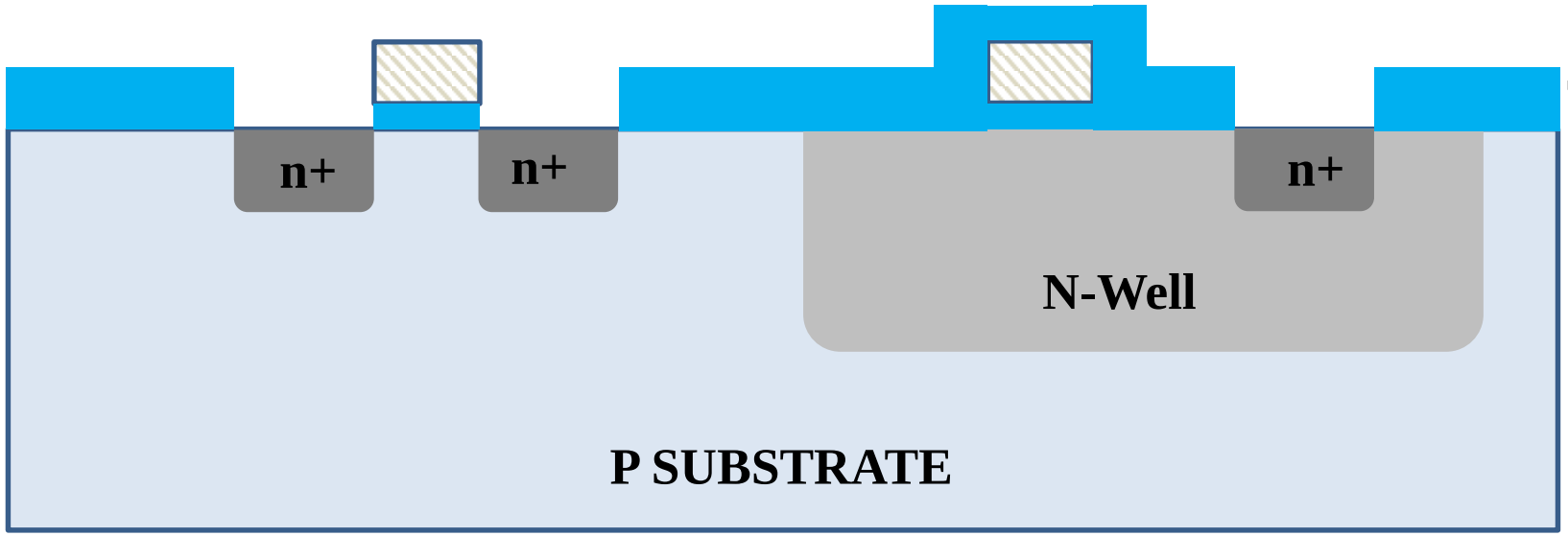


Etching of Thick Oxide



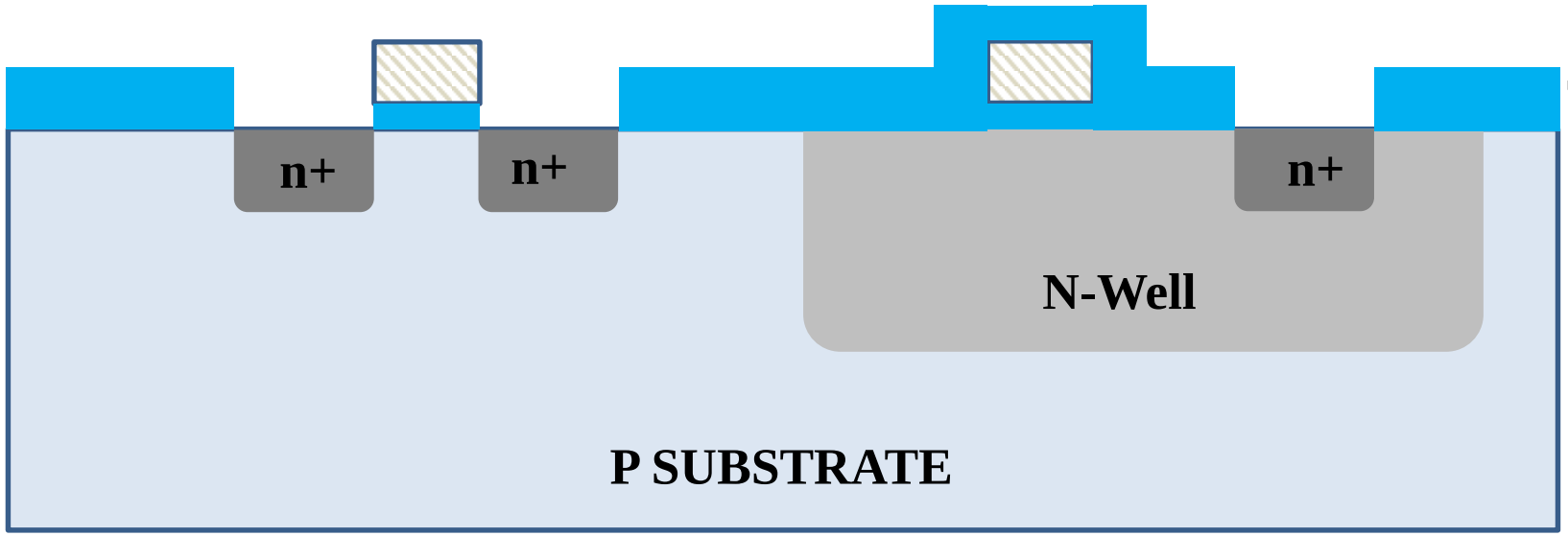
CMOS Fabrication Process

N+ diffusion region creation



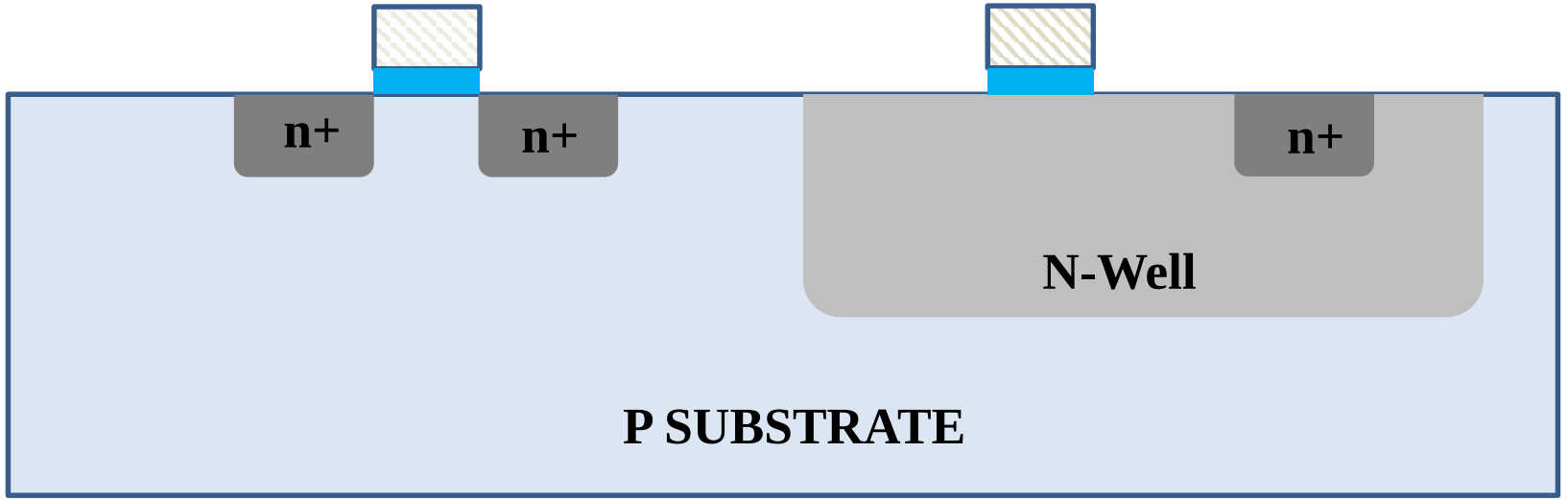
CMOS Fabrication Process

N+ diffusion region creation



Thick Field Oxide

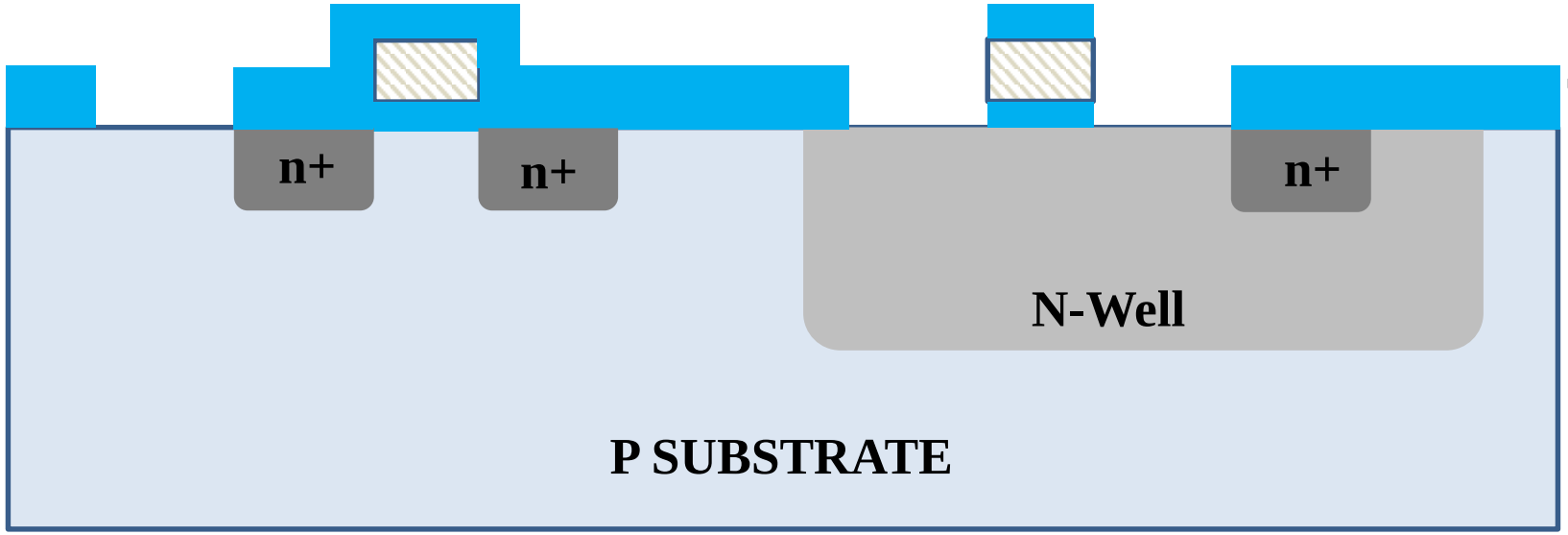
Etching of Thick Oxide



Poly Thin Oxide

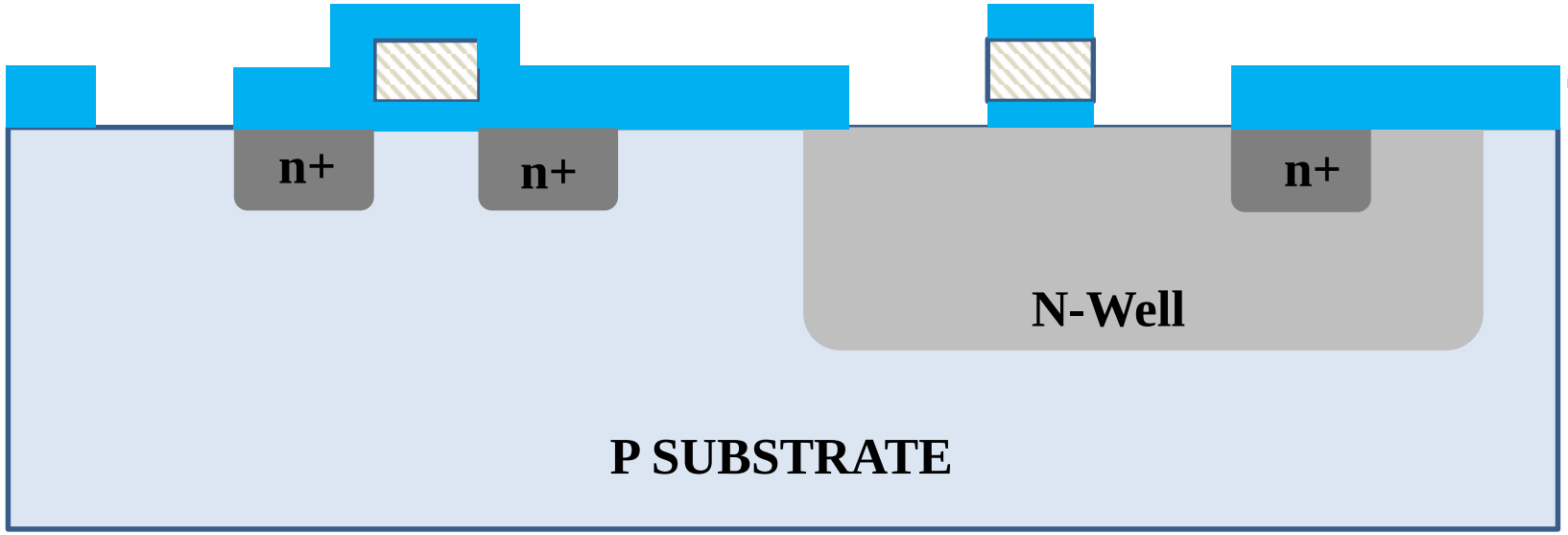
CMOS Fabrication Process

Deposition of Thick Oxide except the P+ region



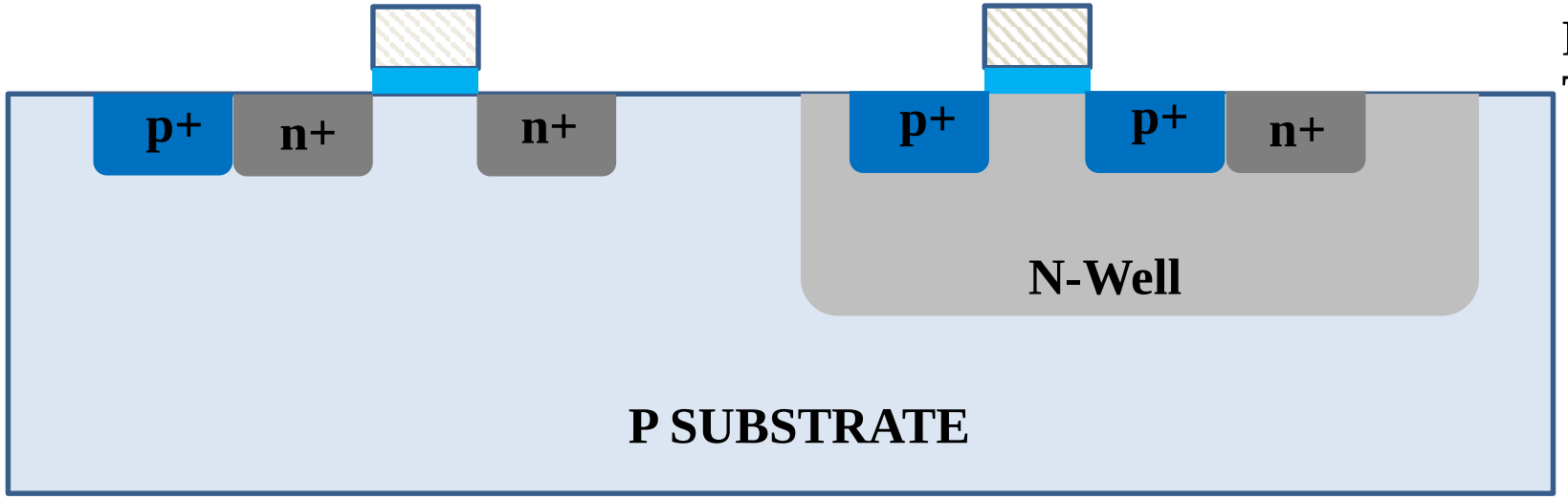
CMOS Fabrication Process

Deposition of Thick Oxide except the P+ region



Thick Field Oxide

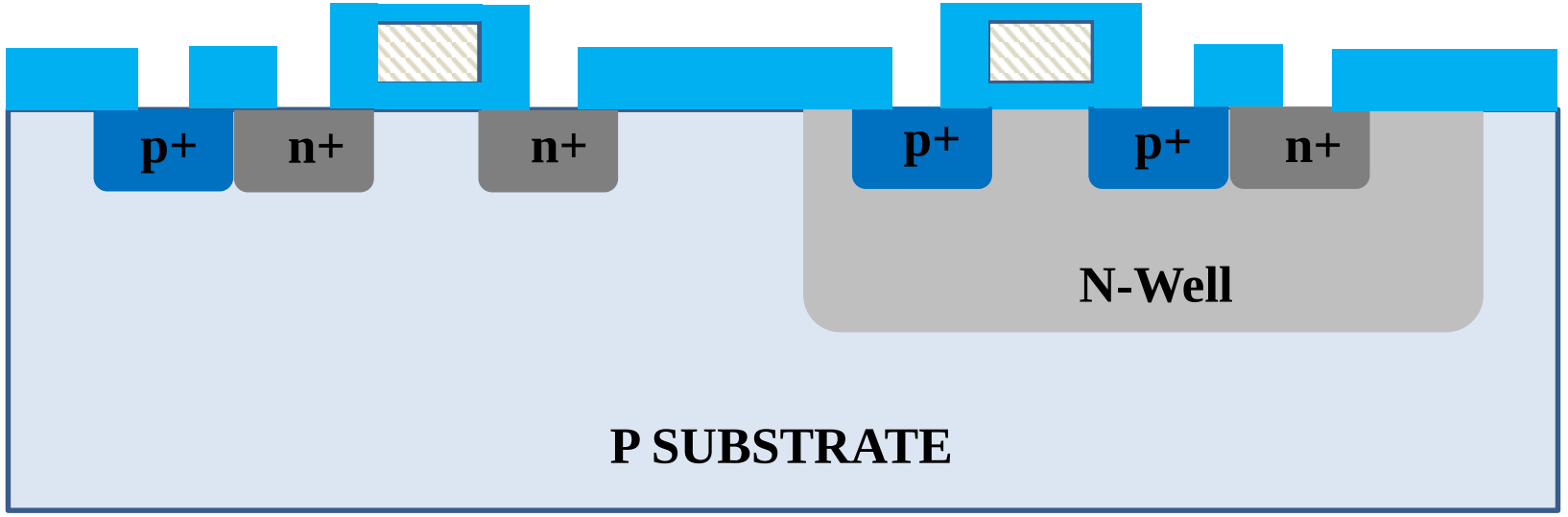
P+ region creation



Poly Thin Oxide

CMOS Fabrication Process

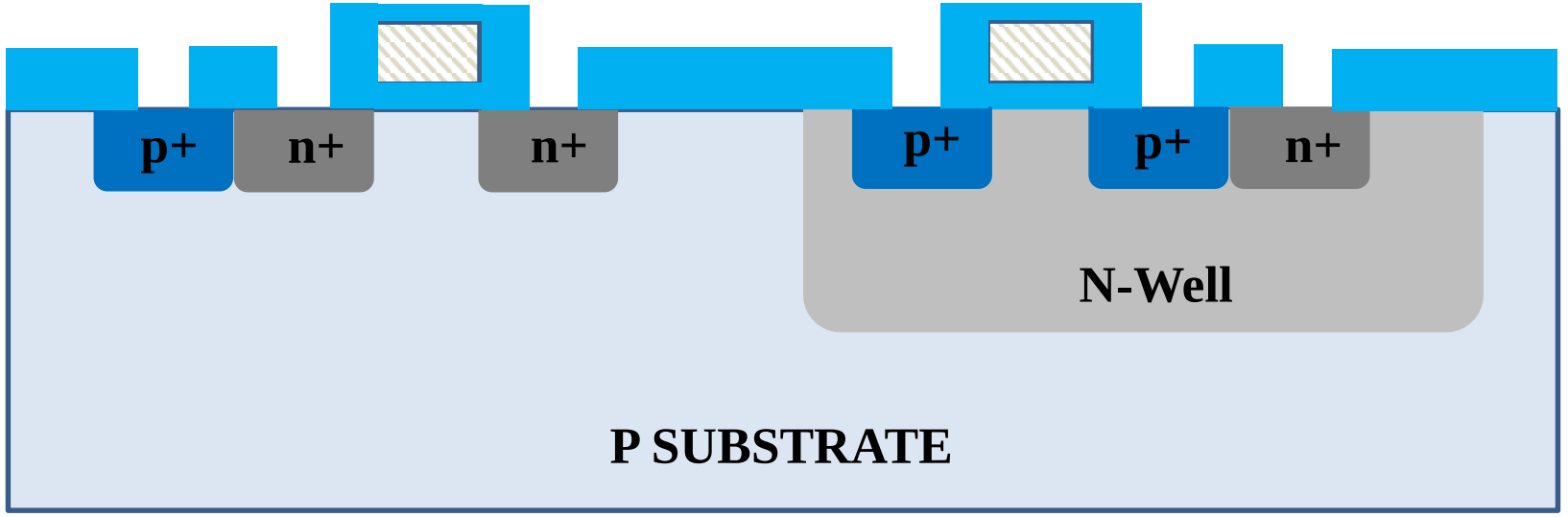
Thick Oxide deposition except the contact window



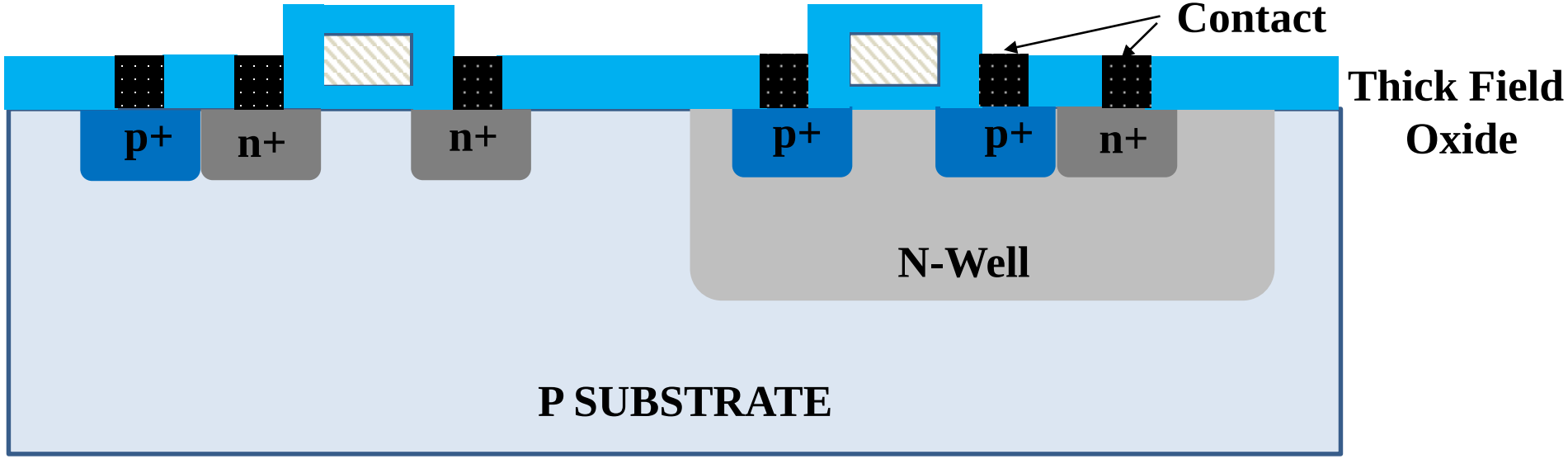
Thick Field Oxide

CMOS Fabrication Process

Thick Oxide deposition except the contact window

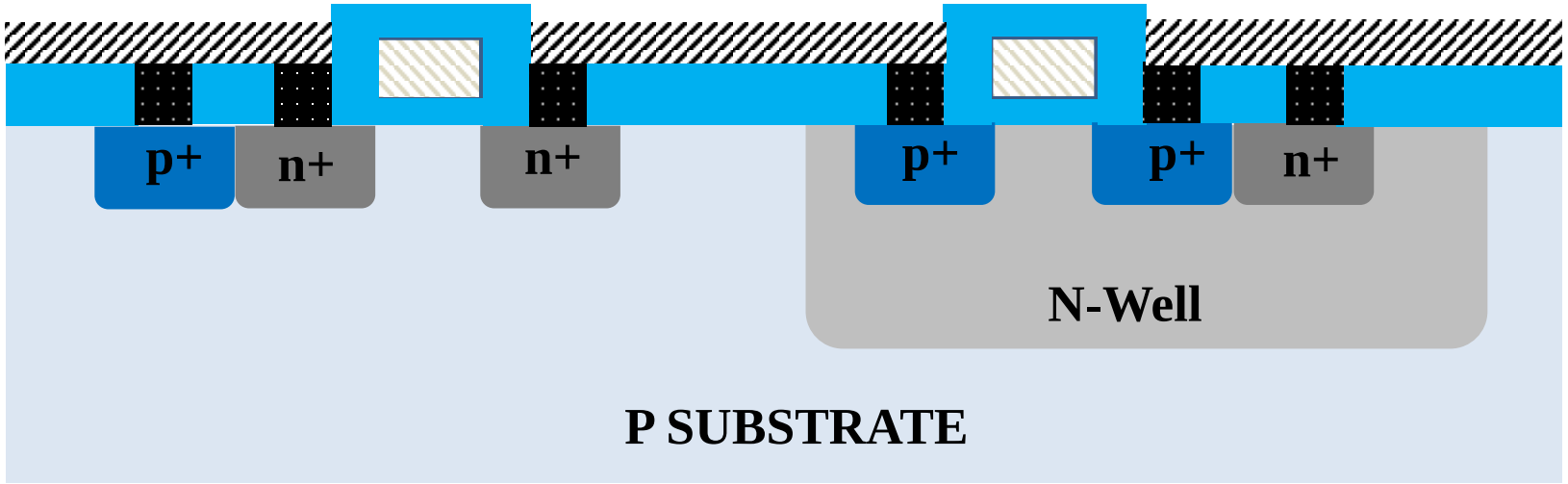


Contact Creation



CMOS Fabrication Process

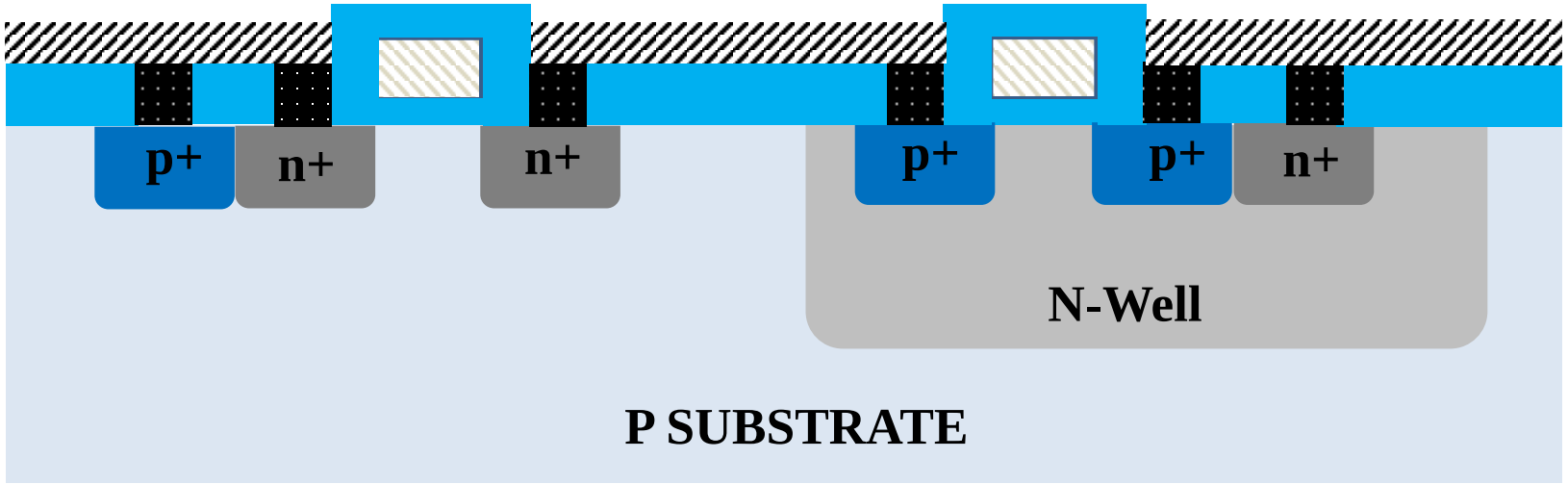
Metal Deposition



Metal
Thick Field
Oxide

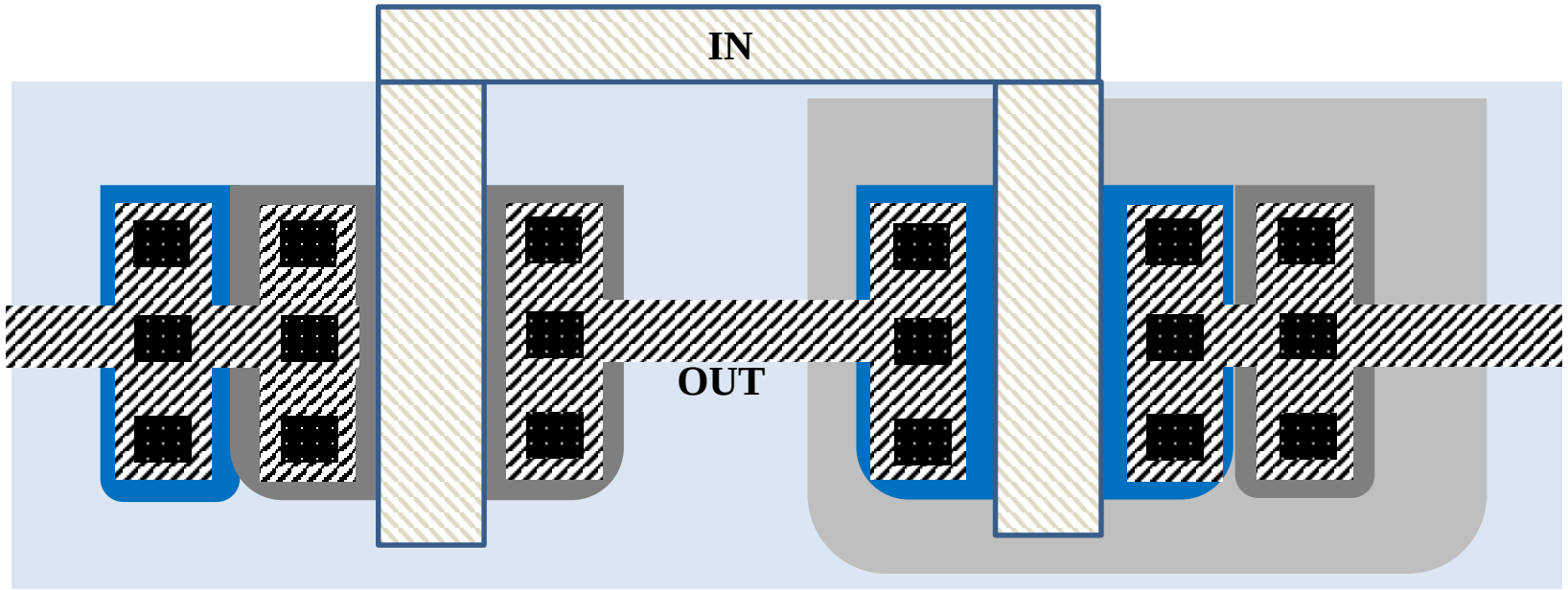
CMOS Fabrication Process

Metal Deposition

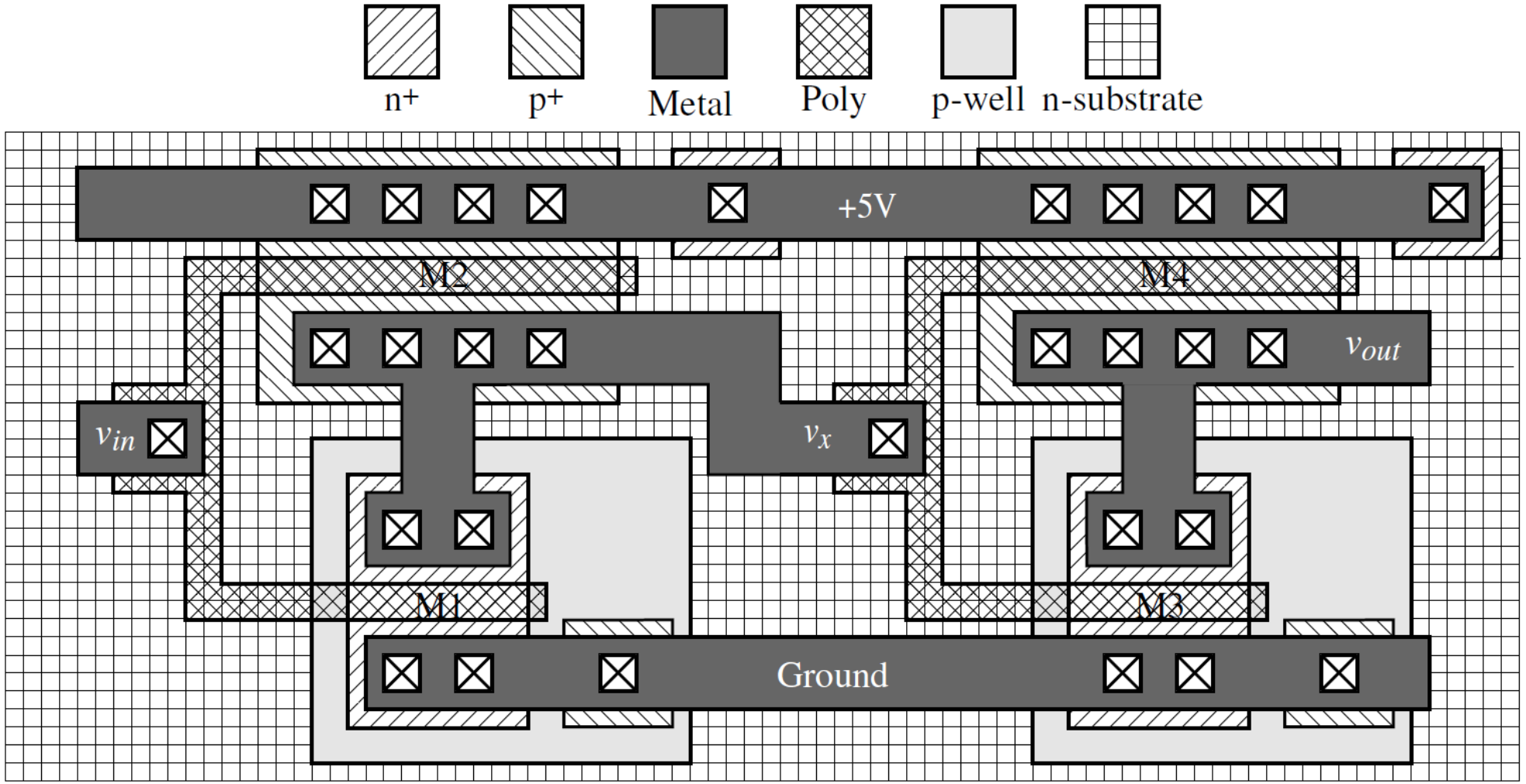


Metal
Thick Field
Oxide

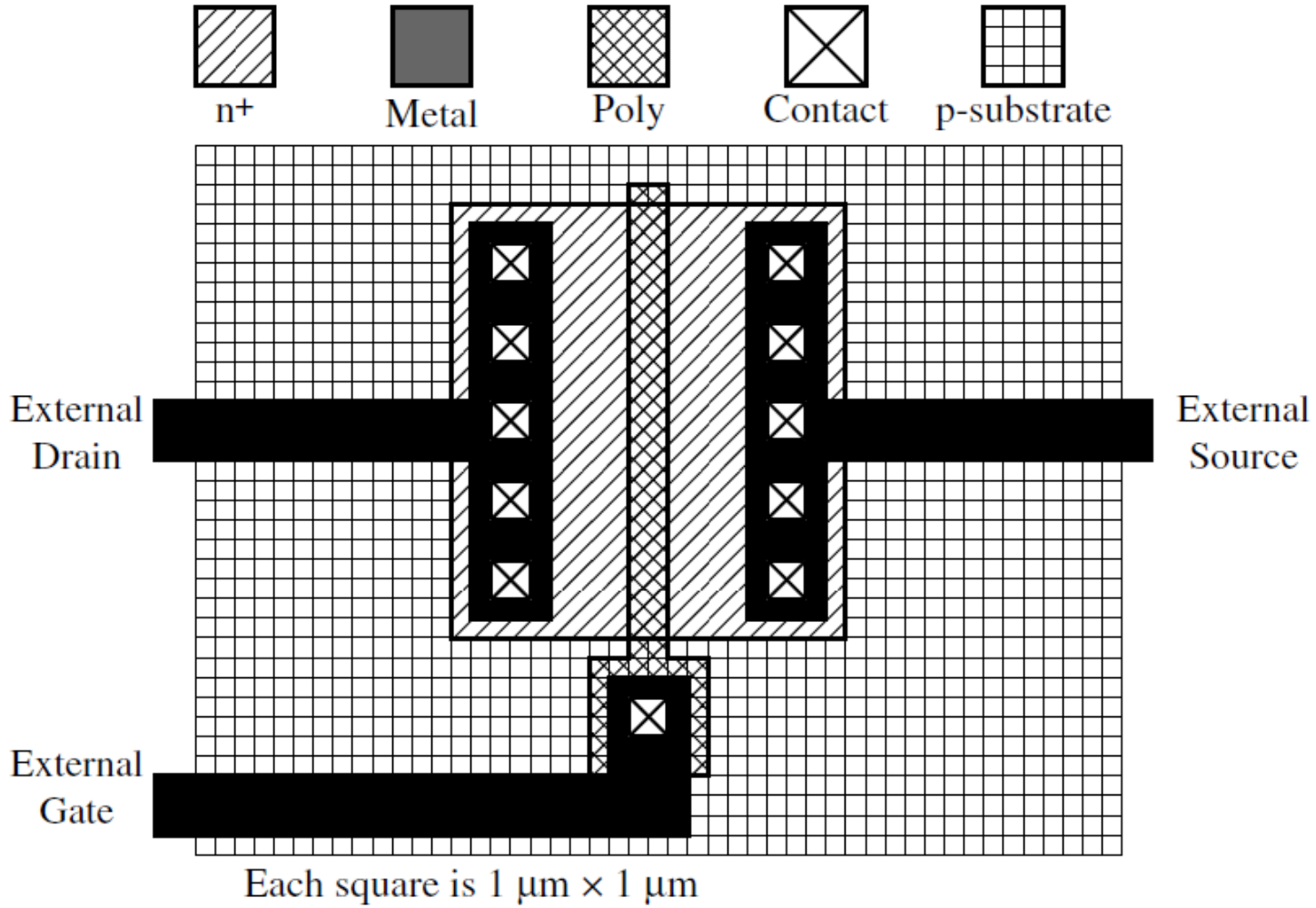
Layout

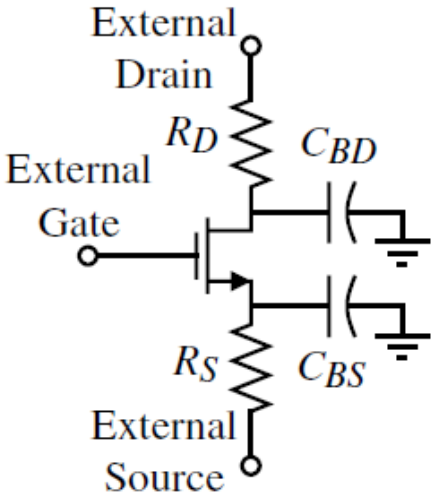


Layout Exercises

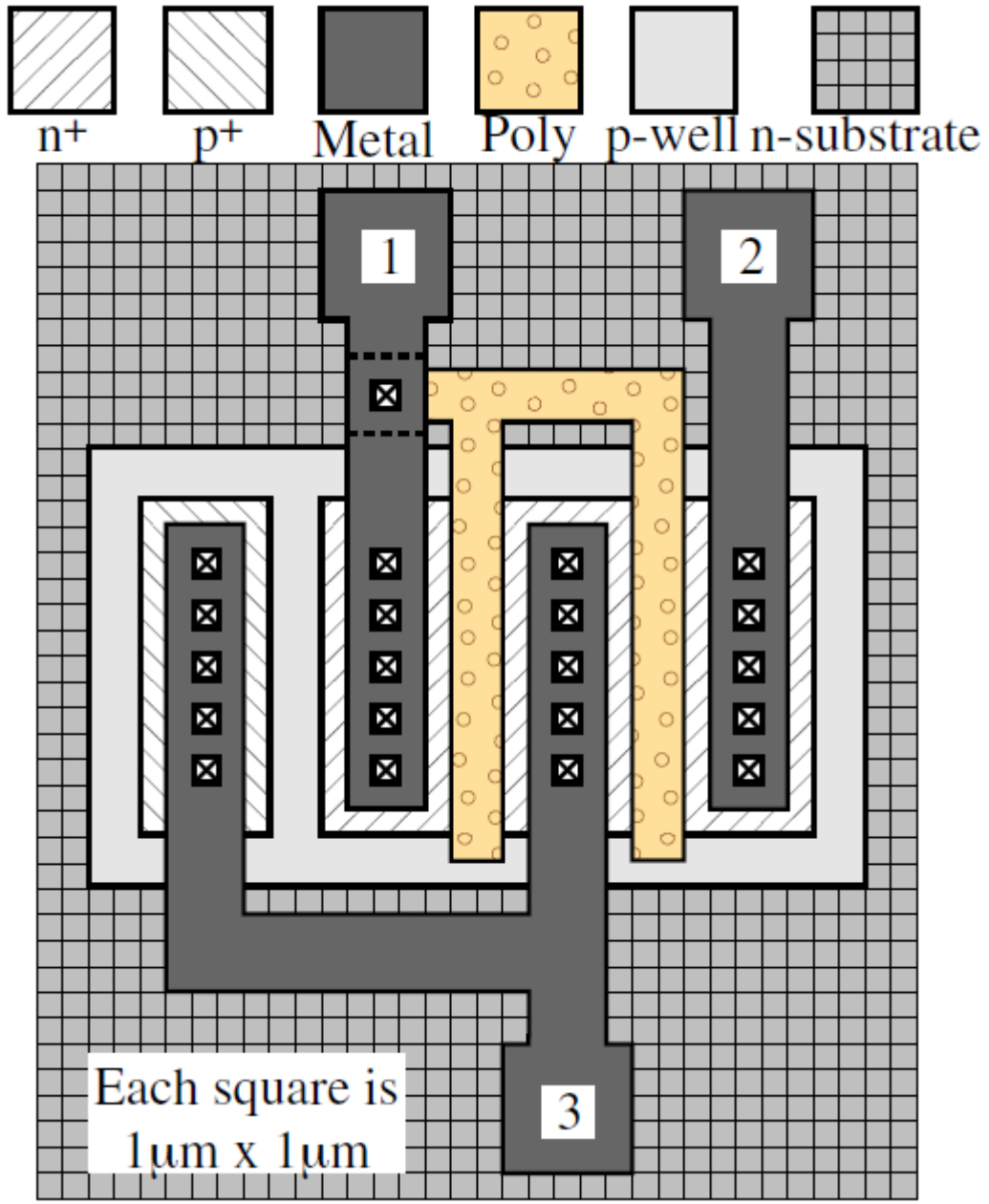


Layout Exercises

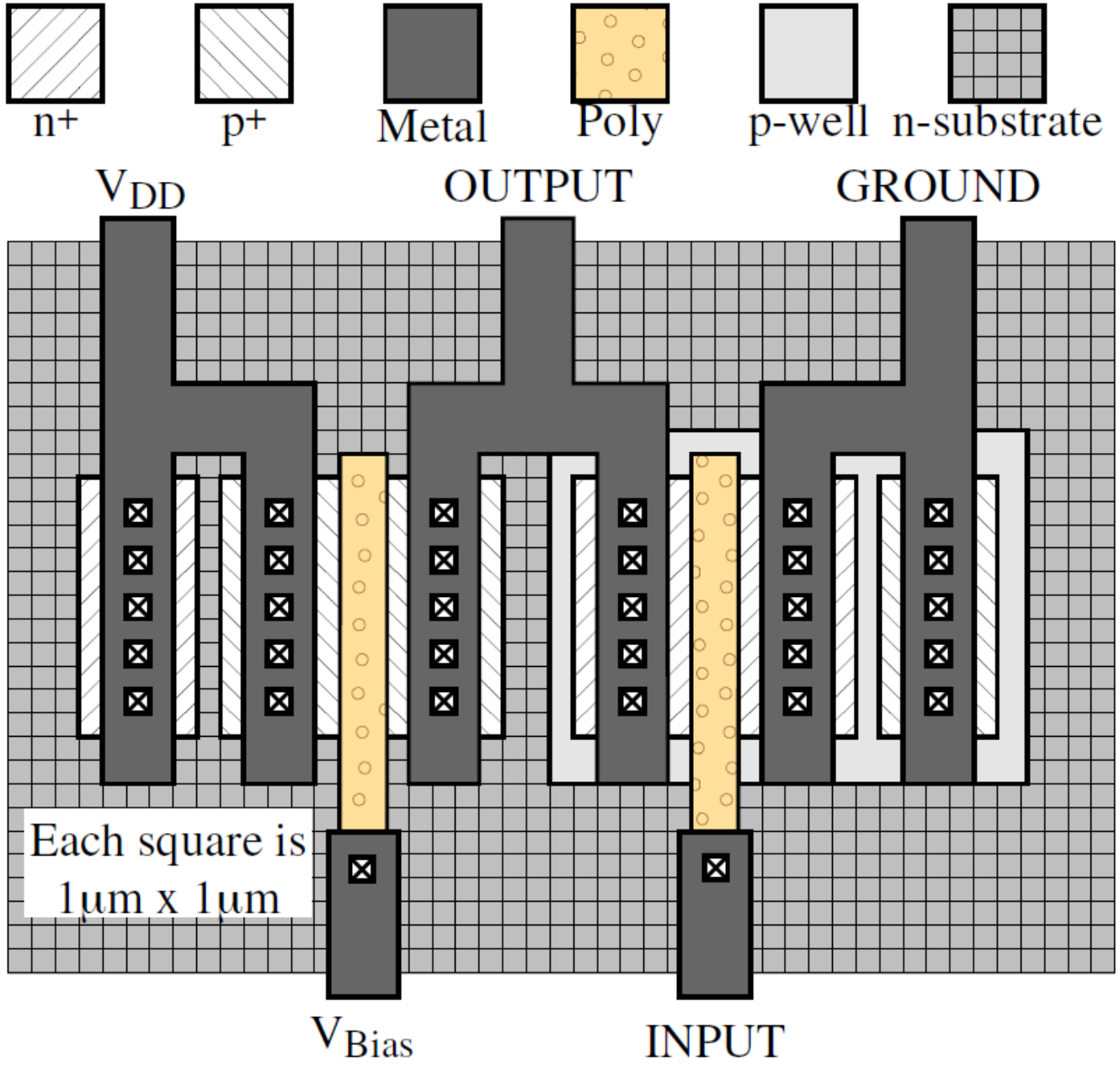




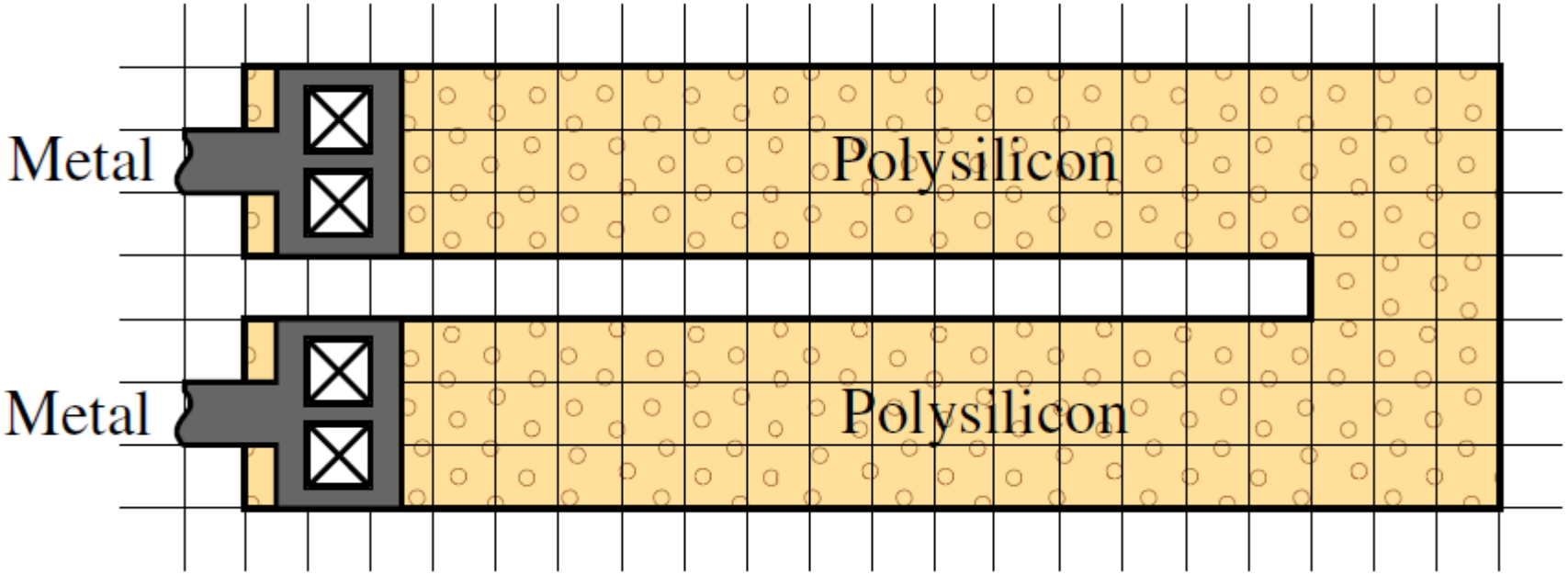
Layout Exercises



Layout Exercises



Layout Exercises



Thank You