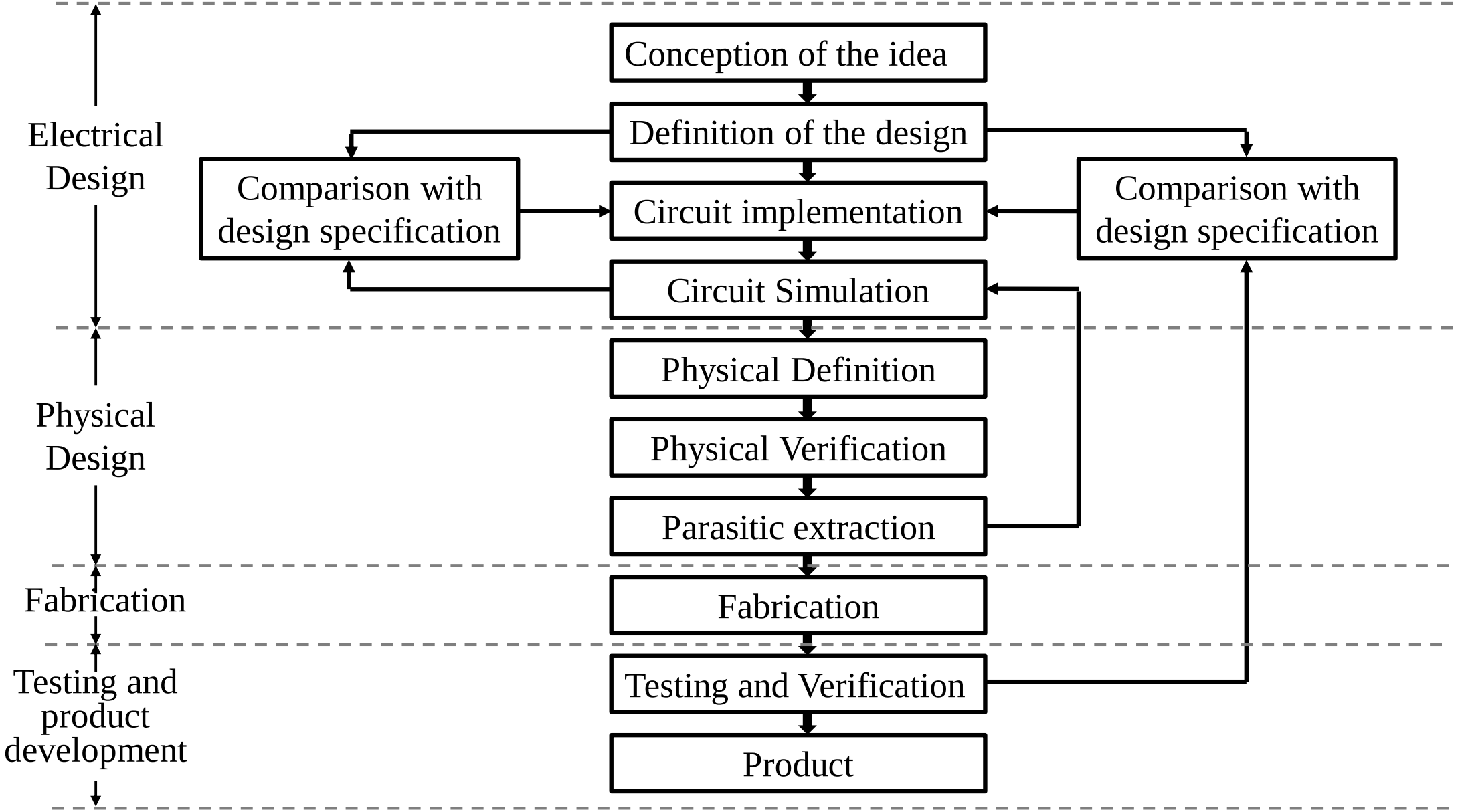
Analog VLSI Design Flow and CMOS Fabrication Process

Santunu Sarangi

Analog IC Design Process



Analog IC Design Process

Electrical Design:

- Electrical design is the process of going from the specification to a circuit solution
- The electrical design requires active and passive device electrical models for
  - Creating the design
  - Verifying the design
  - Determining the robustness of the design

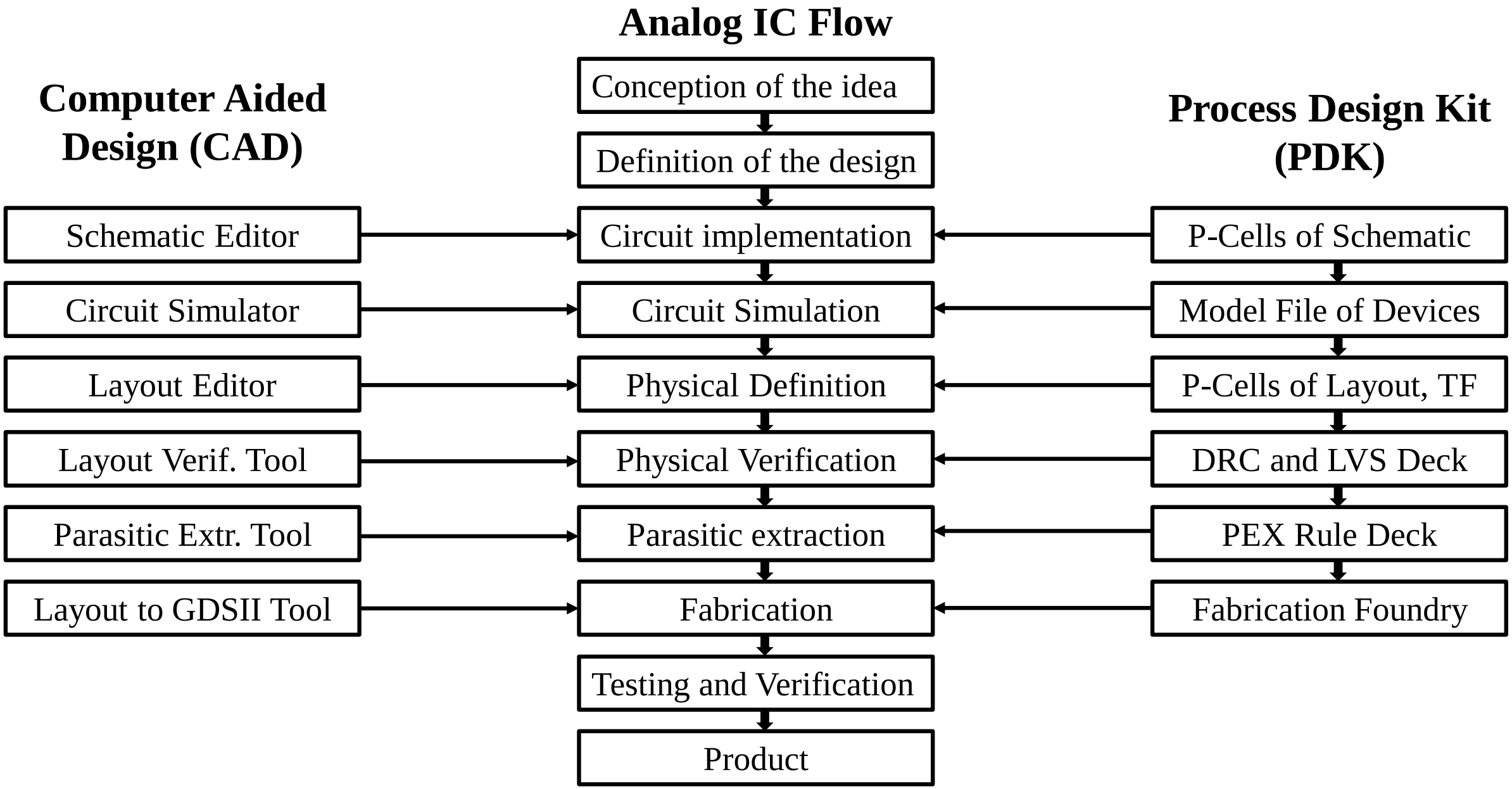
Physical Design:

- Physical design is the process of representing the electrical design in a layout consisting of many distinct geometrical rectangle at various levels.
- The physical design needs
  - Entering various geometries
  - Follow DRC
  - Check LVS
  - Extract Parasitic

Test Design:

- Test design is the process of coordinating, planning and implementing the measurement of the analog integrated circuit performance
- Types of test:
  - Functional
  - Parametric
  - Static
  - Dynamic

Analog IC Design Process and its Relation with CAD and PDK



Role of Circuit Designer

Why it is so important for a VLSI circuit designer to have a deeper understanding of CMOS manufacturing process?

- Physical implementation of the circuit has a major impact on performance, power and cost.
- A circuit designer should always design a practical circuit based on the device limits, technology constraints and physical implementations rather than a ideal circuit.
- A circuit designer should have very good understanding of layout design, so that in less iterations the design can be fridged.
- A good circuit designer should always discussed with the layout designer for better and efficient circuit design.

CMOS Technology

Why CMOS Technology?

Comparison of BJT and MOSFET Technology from an analog viewpoint [Allen-Holberg]

Comparison Feature	BJT	MOSFET
Cut-off Frequency (F_T)	High	Less
Noise (at same thermal noise)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus V_{BE}	2-3 decades of square law behaviour
Transconductance (Same Current)	Larger by 10X	Smaller by 10X
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor	Voltage dependent	More option
Performance/Power Ratio	High	Low
Technology Improvement	Slower	Faster

- Almost every comparison favours BJT, however a similar comparison made from digital viewpoint would come up on the side of CMOS. Since large volume mixed-mode technology will be driven by digital demands, CMOS is an obvious choice.

CMOS Technology

Categorization of the CMOS Technology:

1. Submicron Technology: Lmin ≥ 0.35 µm
2. Deep Submicron Technology (DSM): 0.1 µm ≤ Lmin ≤ 0.35 µm
3. Ultra-Deep Submicron Technology (UDSM): Lmin ≤ 0.1 µm
4. BiCMOS Technology: Lmin = 0.5 µm

In this lecture only the fabrication process of Submicron Technology will be discussed…

CMOS Fabrication Process

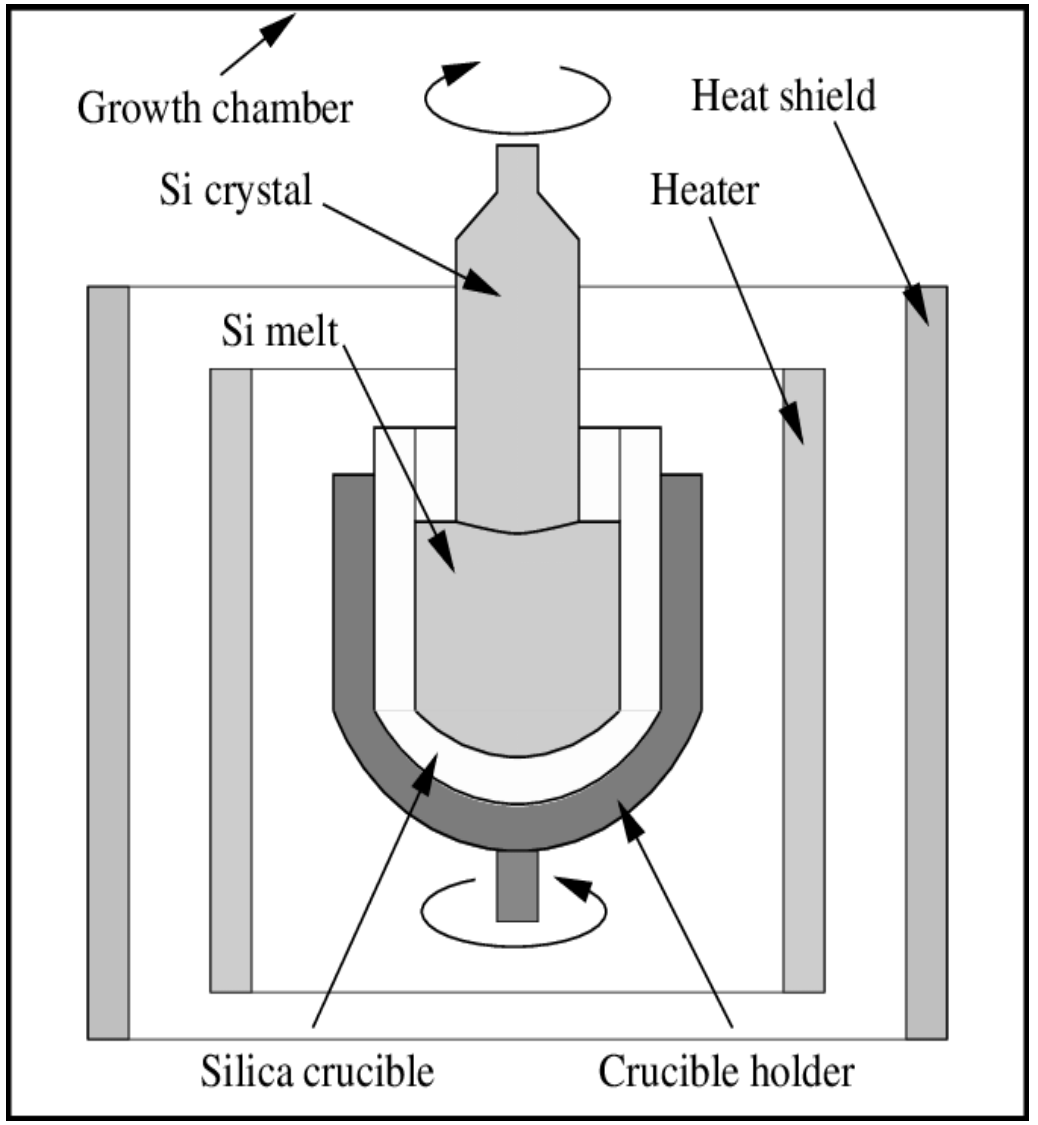
Process Steps:

1. Wafer formation (sand-to-silicon)
2. Photolithography
3. Well and Channel Formation
4. Silicon Dioxide (Sio2) Deposition
5. Isolation
6. Gate Oxide Creation
7. Gate and Source/Drain Formations
8. Contacts and Metallization
9. Passivation
10. Metrology

CMOS Fabrication Process

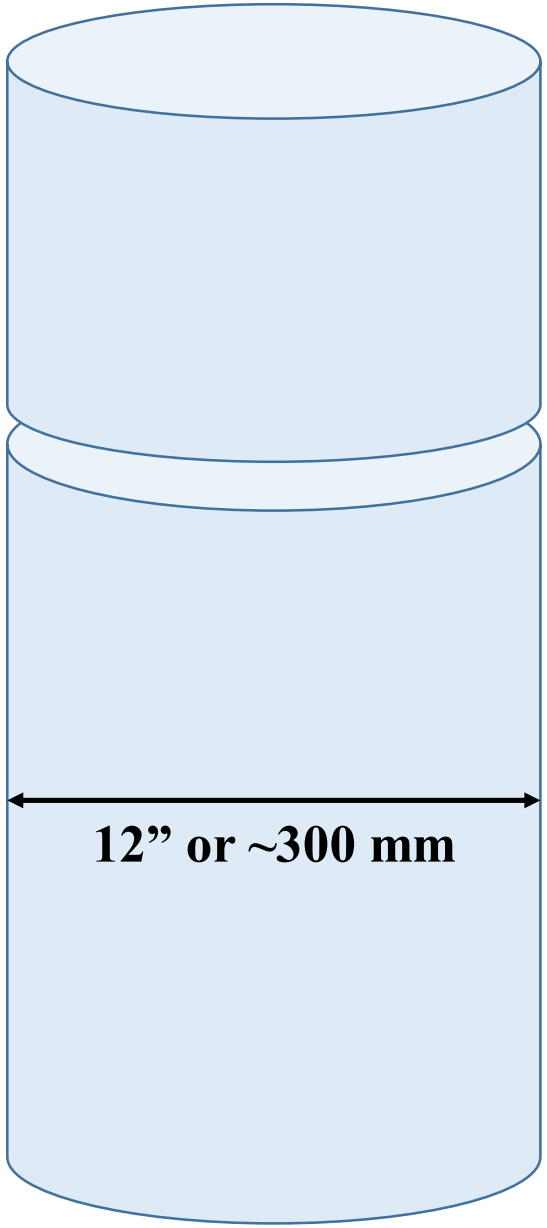
1. Wafer formation (sand-to-silicon)

- The basic raw material used in CMOS fabs is a wafer or disk of silicon, roughly 75 mm to 300 mm (12 inch) in diameter and less than 1 mm thick.
- Wafers are cut from boules, cylindrical ingots of single-crystal silicon, that have been pulled from a crucible of pure molten silicon.
- Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties.
- A seed crystal is dipped into the melt to initiate crystal growth.
- The seed is gradually withdrawn vertically from the melt while simultaneously being rotated, as shown in Figure.
- The molten silicon attaches itself to the seed and recrystallizes as it is withdrawn.
- The seed withdrawal and rotation rates determine the diameter of the ingot.
- Growth rates vary from 30 to 180 mm/hour.

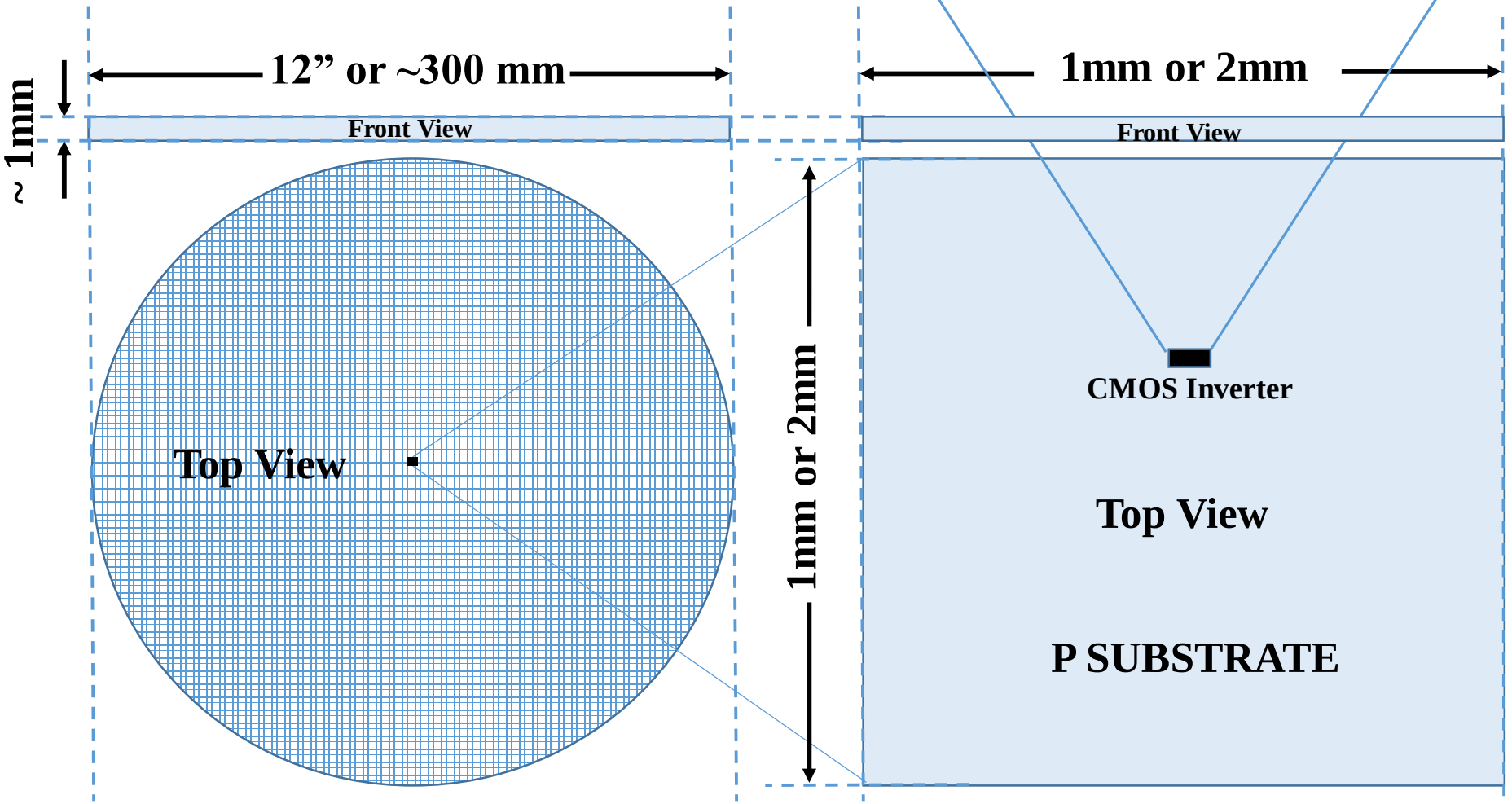


Czocralski silicon crystal growth system [Robert A. Brown]

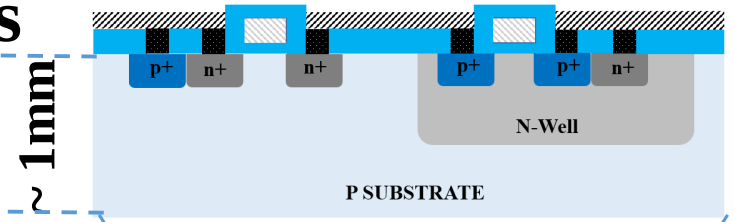
CMOS Fabrication Process



SILICON INGOT

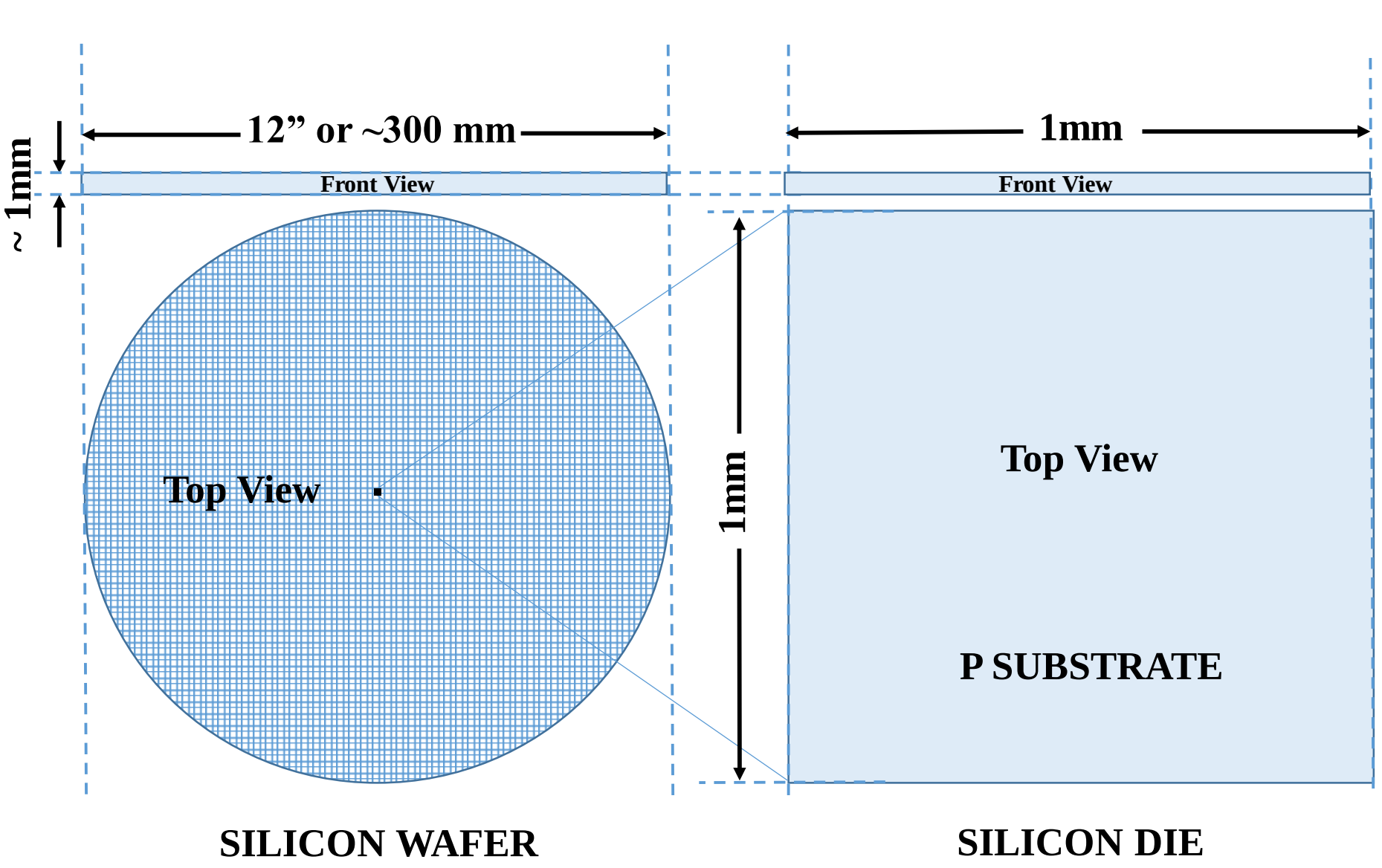


SILICON WAFER



SILICON DIE

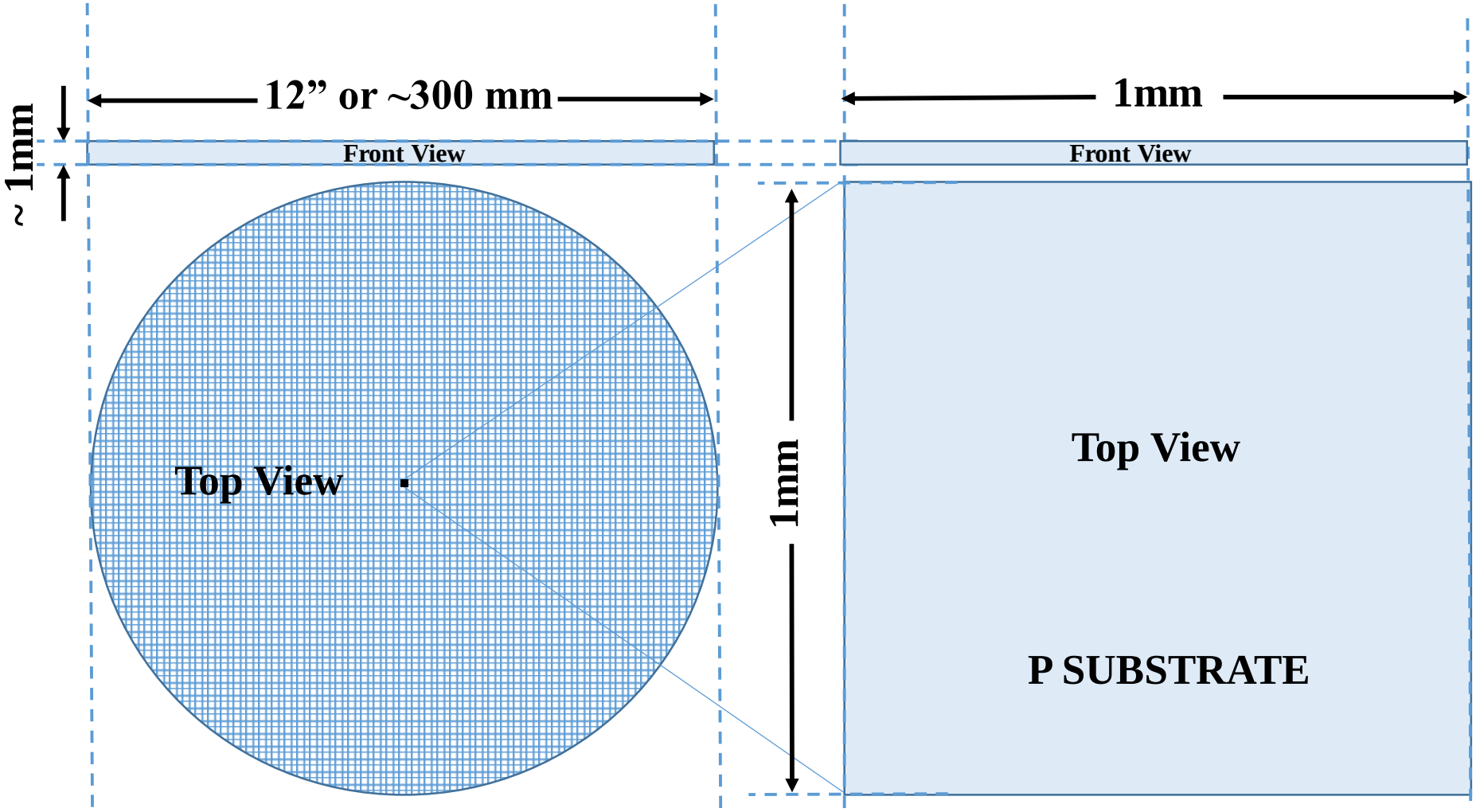
CMOS Fabrication Process



QUIZ: Refer the left side figure and calculate the number of silicon die can be formed from a single silicon wafer.

(a) ~300
(b) ~9,000
(c) ~70,000
(d) ~90,000

CMOS Fabrication Process



QUIZ: Refer the left side figure and calculate the number of silicon die can be formed from a single silicon wafer.

(a) ~300
(b) ~9,000
(c) ~70,000
(d) ~90,000

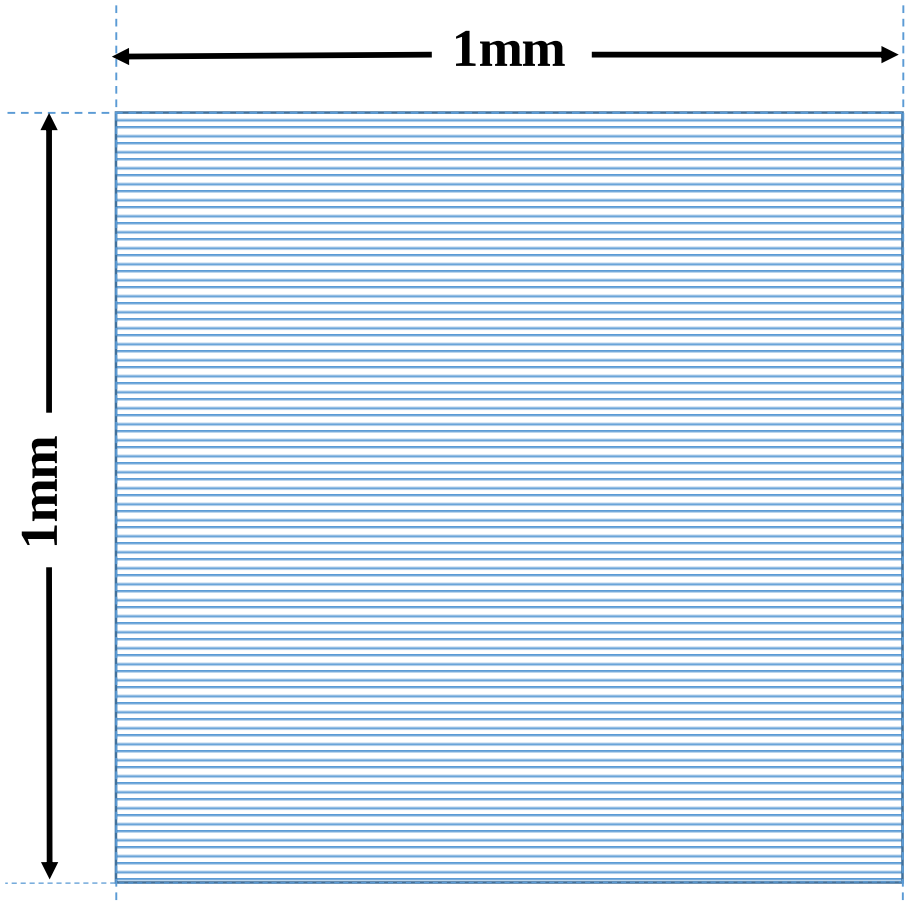
Answer:
Number of die = Area of wafer / Area of die

Area of wafer = PI*150*150 = 70,715 mm2

Area of die = 1 X 1 = 1 mm2

No, of die=70,715/1= 70,715

CMOS Fabrication Process



SILICON DIE

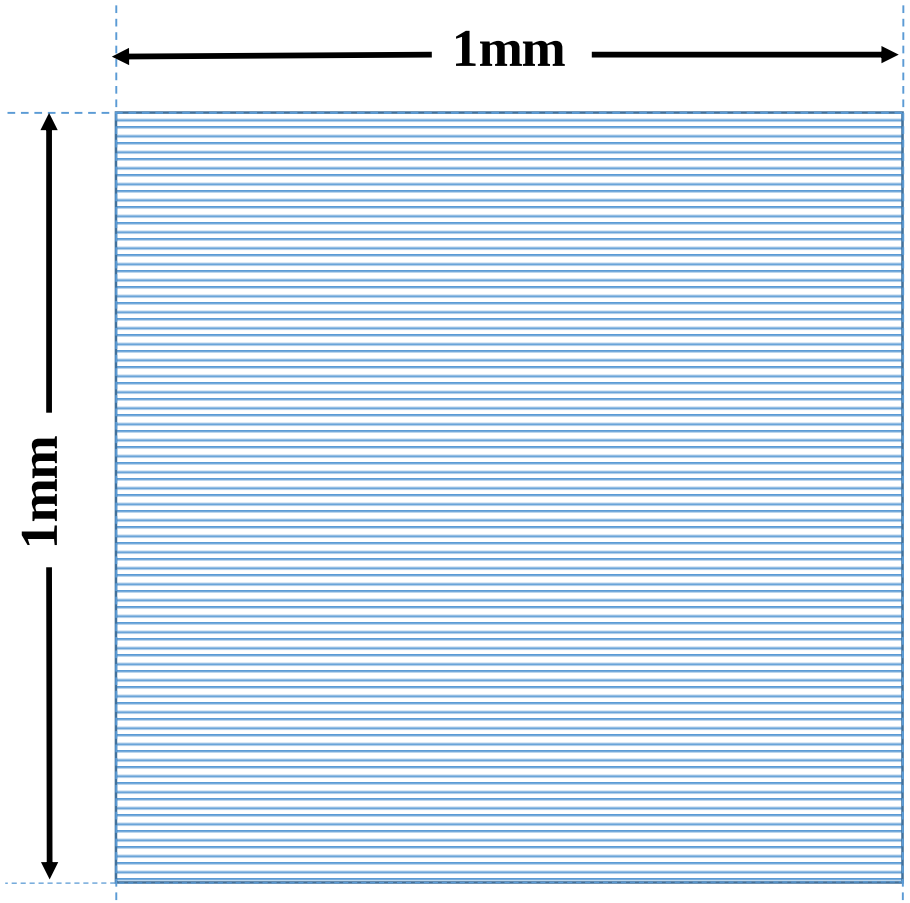
DATA

- Assume the entire silicon die is a digital chip have all the area filled by only standard cells.
- Assume that in one silicon die there are 1000 equal rows and each having 1µm hight.
- Assume that a standard cell having a height of 1µm and a width of 0.25µm.
- Assume standard cell has only one P-MOSFET and one N-MOSFET.
- Assume all the interconnection between all the standard cells are through top metals only.

QUIZ: Refer the left side figure and data given, calculate the number of MOS transistors can be put in a single 1mm X 1mm silicon die.

(a) 1 million
(b) 2 million
(c) 4 million
(d) 8 million

CMOS Fabrication Process



SILICON DIE

- Assume the entire silicon die is a digital chip have all the area filled by only standard cells.
- Assume that in one silicon die there are 1000 equal rows and each having 1µm hight.
- Assume that a standard cell having a height of 1µm and a width of 0.25µm.
- Assume standard cell has only one P-MOSFET and one N-MOSFET.
- Assume all the interconnection between all the standard cells are through top metals only.

QUIZ: Refer the left side figure and data given, calculate the number of MOS transistors can be put in a single 1mm X 1mm silicon die.

(a) 1 million
(b) 2 million
(c) 4 million
(d) 8 million

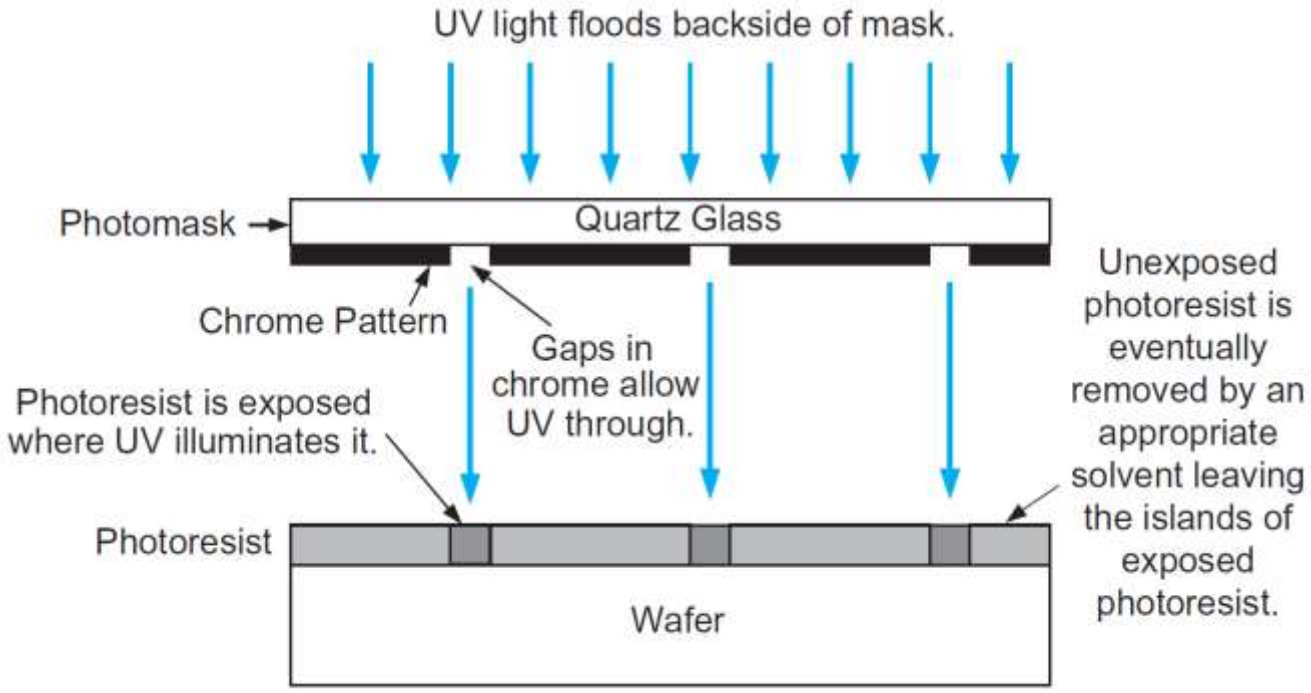
Answer:

- There are 1000 rows and each having 1µm height.
- Per row 4000 standard cells
- Per row 8000 transistors
- In 1000 tows, 8000*1000=8000000
- Or 8 million transistors

CMOS Fabrication Process

2. Photolithography

- The patterning is achieved by a process called photolithography.
- The primary method for defining areas of interest (i.e., where we want material to be present or absent) on a wafer is by the use of photoresists.
- The wafer is coated with the photoresist and subjected to selective illumination through the photomask.
- A photomask is constructed with chromium (chrome) covered quartz glass. A UV light source is used to expose the photoresist.
- A developer solvent is then used to dissolve the soluble unexposed photoresist, leaving islands of insoluble exposed photoresist.



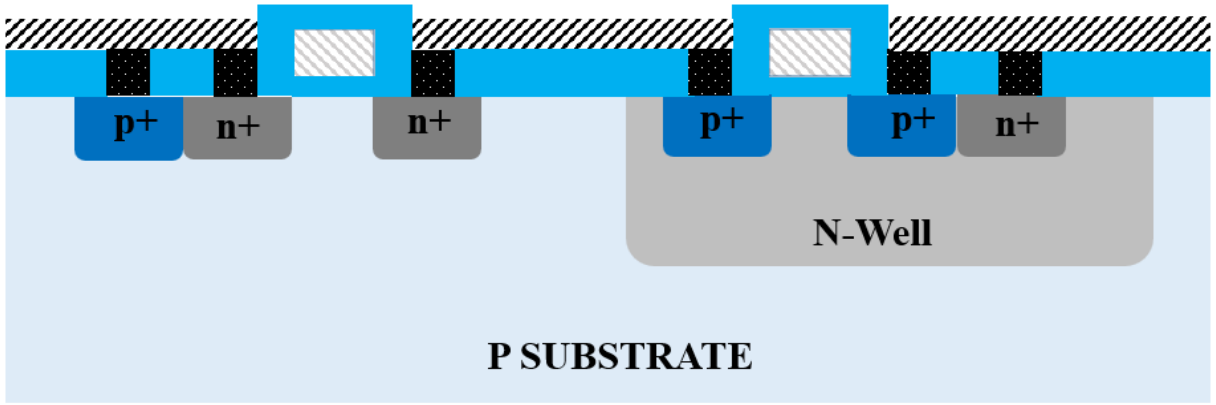
Photolithography process [Waste and Harris]

CMOS Fabrication Process

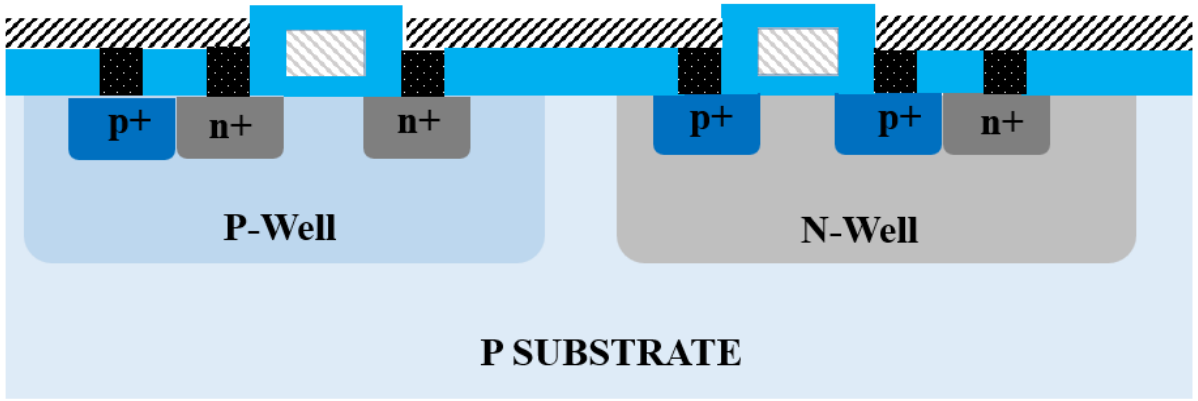
3. Well and Channel Formation

- There are 4 CMOS technology processes;
  - **N-well process: In a n-well process, the pMOS transistors are built in a n-well and the nMOS transistor is placed in the p-type substrate.**
  - **P-well process:** In a p-well process, the nMOS transistors are built in a p-well and the pMOS transistor is placed in the n-type substrate. p-well processes were used to optimize the pMOS transistor performance.
  - **Twin-well process:** Twin-well processes accompanied the emergence of n-well processes. A twin-well process allows the optimization of each transistor type.
  - **Triple-well process:** The triple-well process has emerged to provide good isolation between analog and digital blocks in mixed-signal chips; it is also used to isolate high-density dynamic memory from logic.

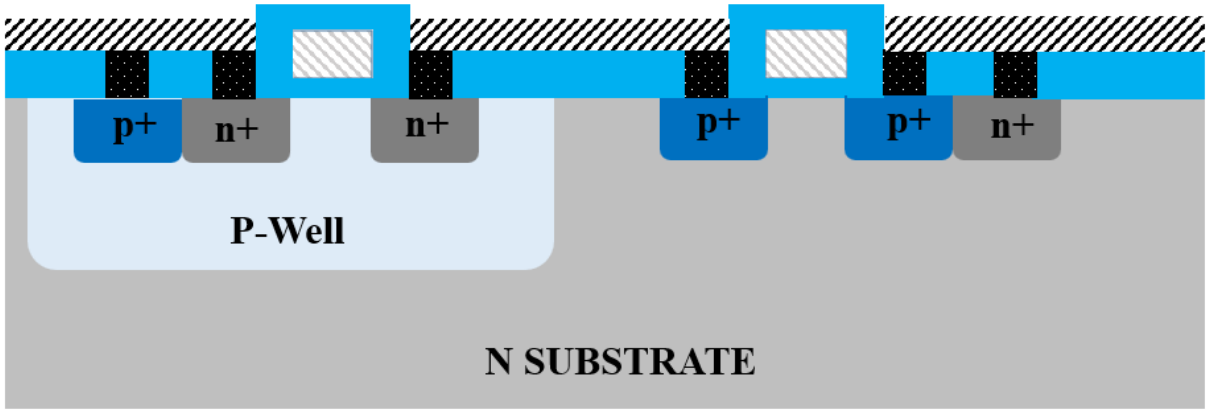
CMOS Fabrication Process



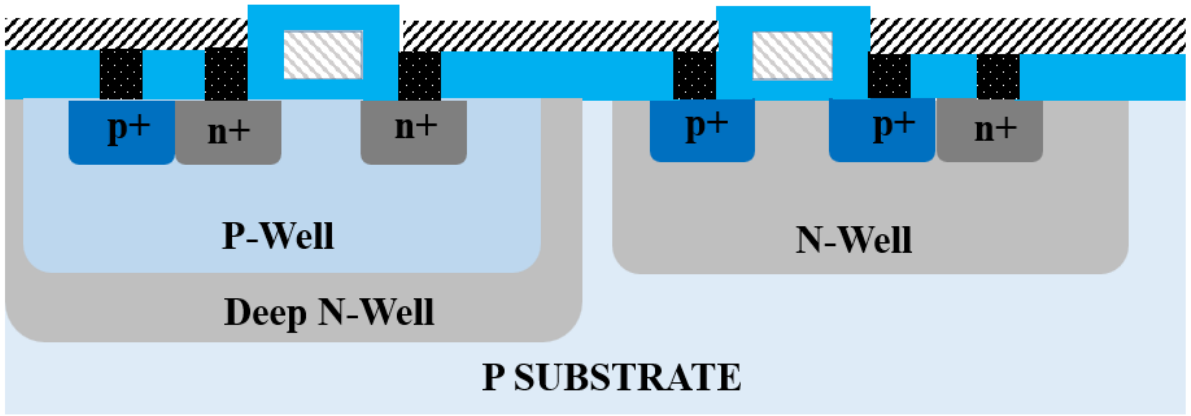
N-Well Process



Twin-Well Process



P-Well Process



Tripple-Well Process

CMOS Fabrication Process

4. Silicon Dioxide (Sio2)

- Oxidation of silicon is achieved by heating silicon wafers in an oxidizing atmosphere. The following are some common approaches:
- Wet Oxidation: when the oxidizing atmosphere contains water vapor.
  - The temperature is usually between 900 °C and 1000 °C.
  - Wet oxidation is a rapid process.
- Dry Oxidation: when the oxidizing atmosphere is pure oxygen.
  - Temperatures are in the region of 1200 °C to achieve an acceptable growth rate.
  - Dry oxidation forms a better quality oxide than wet oxidation.
  - It is used to form thin, highly controlled gate oxides, while wet oxidation may be used to form thick field oxides.
- Atomic Layer Deposition (ALD): when a thin chemical layer (material A) is attached to a surface and then a chemical (material B) is introduced to produce a thin layer of the required layer (i.e., SiO2—this can also be used for other various dielectrics and metals).

CMOS Fabrication Process

5. Isolation

- Individual devices in a CMOS process need to be isolated from one another so that they do not have unexpected interactions.
- The transistor gate consists of a thin gate oxide layer.
- The thick oxide used to be formed by a process called Local Oxidation of Silicon (LOCOS).
- A problem with LOCOS-based processes is the transition between thick andthin oxide, which extended some distance laterally to form a so-called bird’s beak.
- Starting around the 0.35 μm node, shallow trench isolation (STI) was introduced to avoid the problems with LOCOS.
- STI forms insulating trenches of SiO2 surrounding the transistors (everywhere except the active area).

CMOS Fabrication Process

6. Gate Oxide

- The next step in the process is to form the gate oxide for the transistors. As mentioned, this is most commonly in the form of silicon dioxide (SiO2).The transistor gate consists of a thin gate oxide layer.

7. Gate and Source/Drain Formations

- Grow gate oxide wherever transistors are required (area = source + drain + gate)—elsewhere there will be thick oxide or trench isolation.
- Deposit polysilicon on chip
- Pattern polysilicon (both gates and interconnect)
- Etch exposed gate oxide—i.e., the area of gate oxide where transistors are required that was not covered by polysilicon; at this stage, the chip has windows down to the well or substrate wherever a source/drain diffusion is required
- Implant pMOS and nMOS source/drain regions

CMOS Fabrication Process

8. Contacts and Metallization

- Contact cuts are made to source, drain, and gate according to the contact mask. These are holes etched in the dielectric after the source/drain formation.
- Older processes commonly use aluminum (Al) for wires, although newer ones offer copper (Cu) for lower resistance.
- Tungsten (W) can be used as a plug to fill the contact holes (to alleviate problems of aluminum not conforming to small contacts).

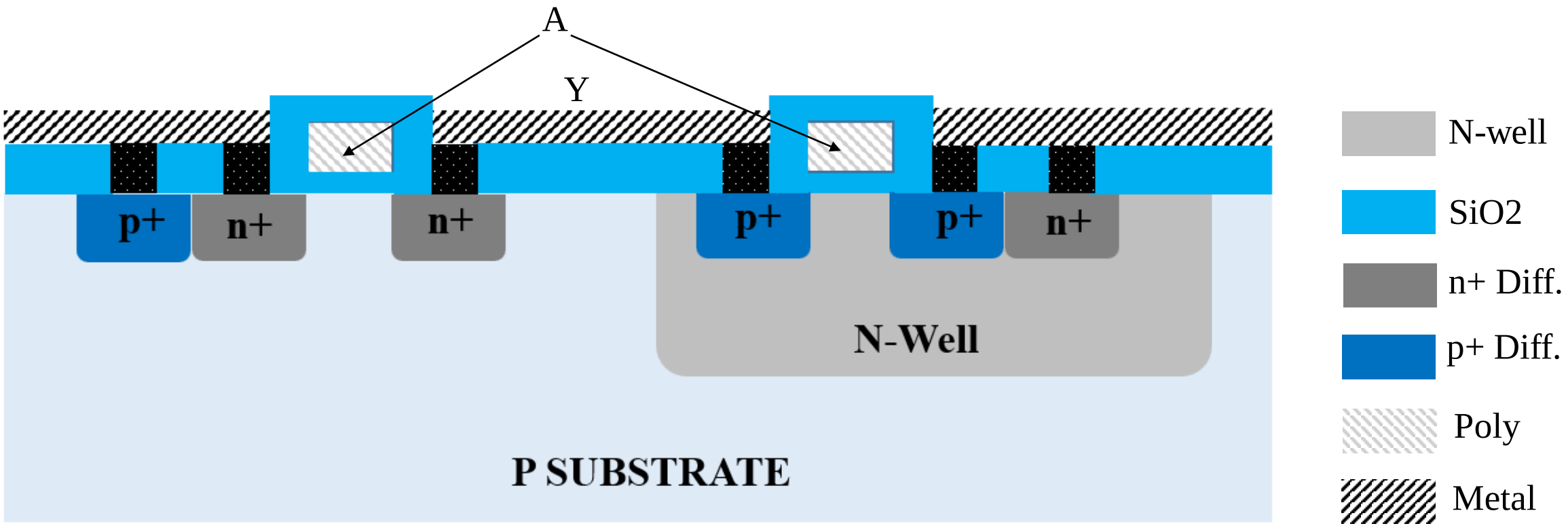
9. Passivation:

- The final processing step is to add a protective glass layer called passivation or over glass that prevents the ingress of contaminants.
- Openings in the passivation layer, called overglass cuts, allow connection to I/O pads and test probe points if needed.

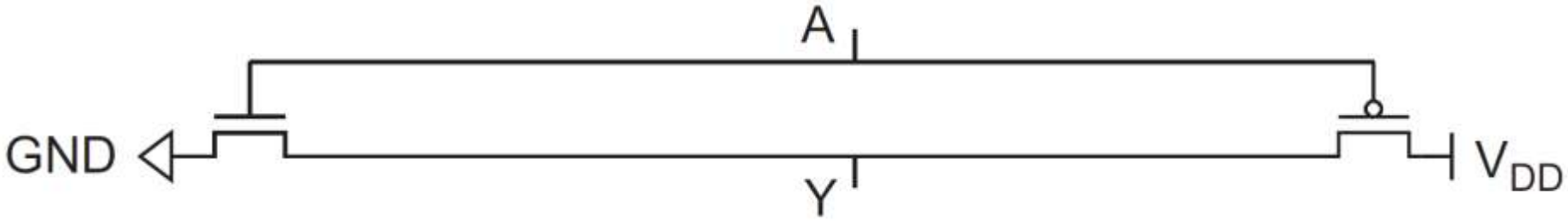
10. Metrology:

- Metrology is the science of measuring. Everything that is built in a semiconductor process has to be measured to give feedback to the manufacturing process**.**

CMOS Fabrication Process



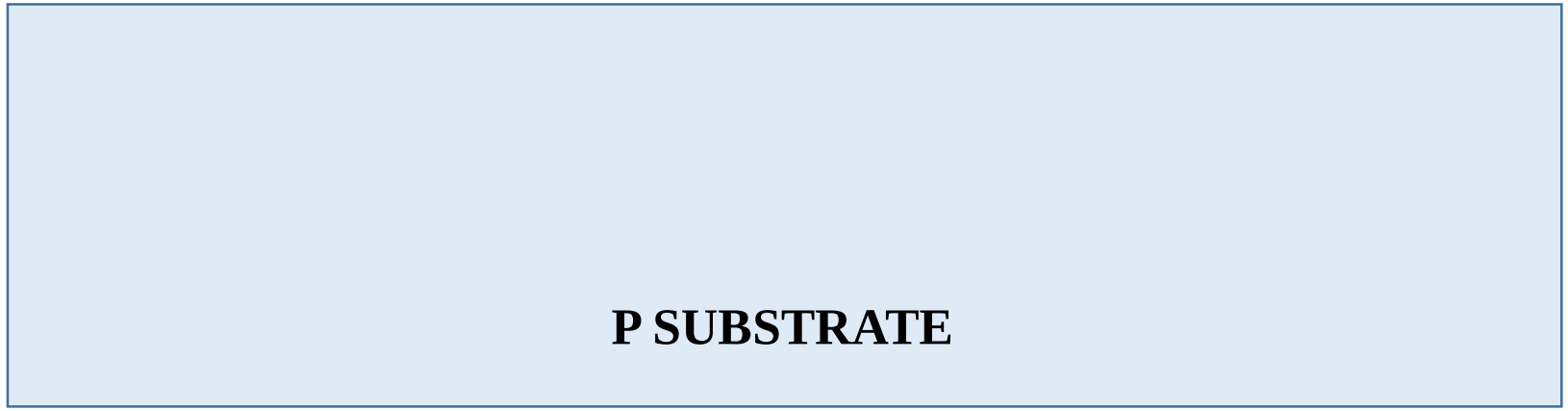
Inverter cross section with well and substrate contact



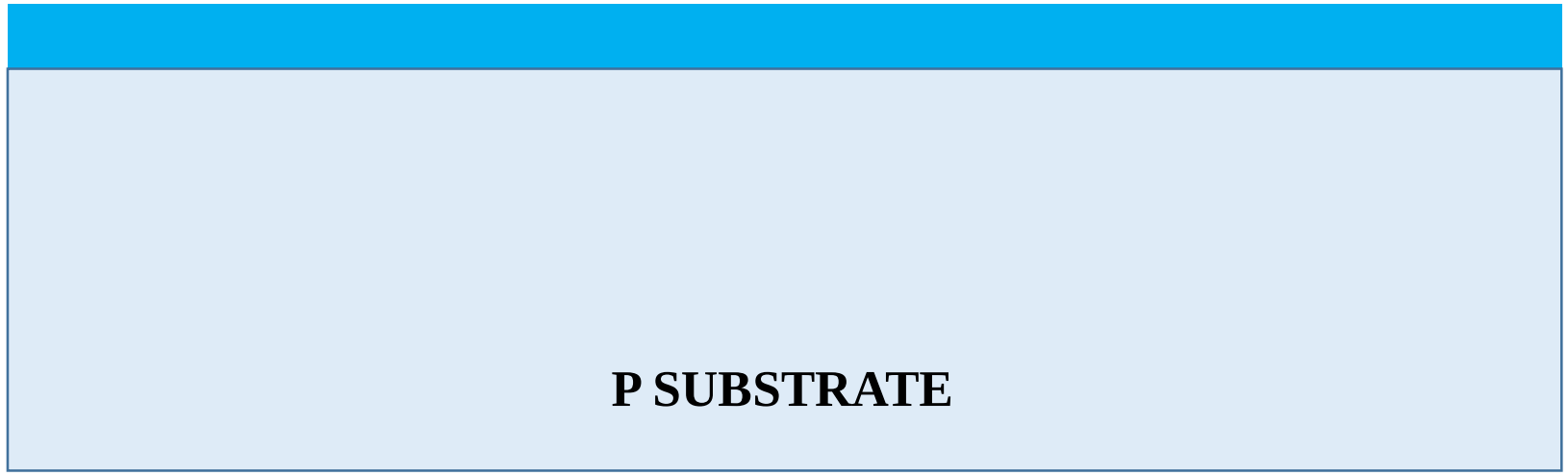
Inverter Schematic

CMOS Fabrication Process

Substrate Creation

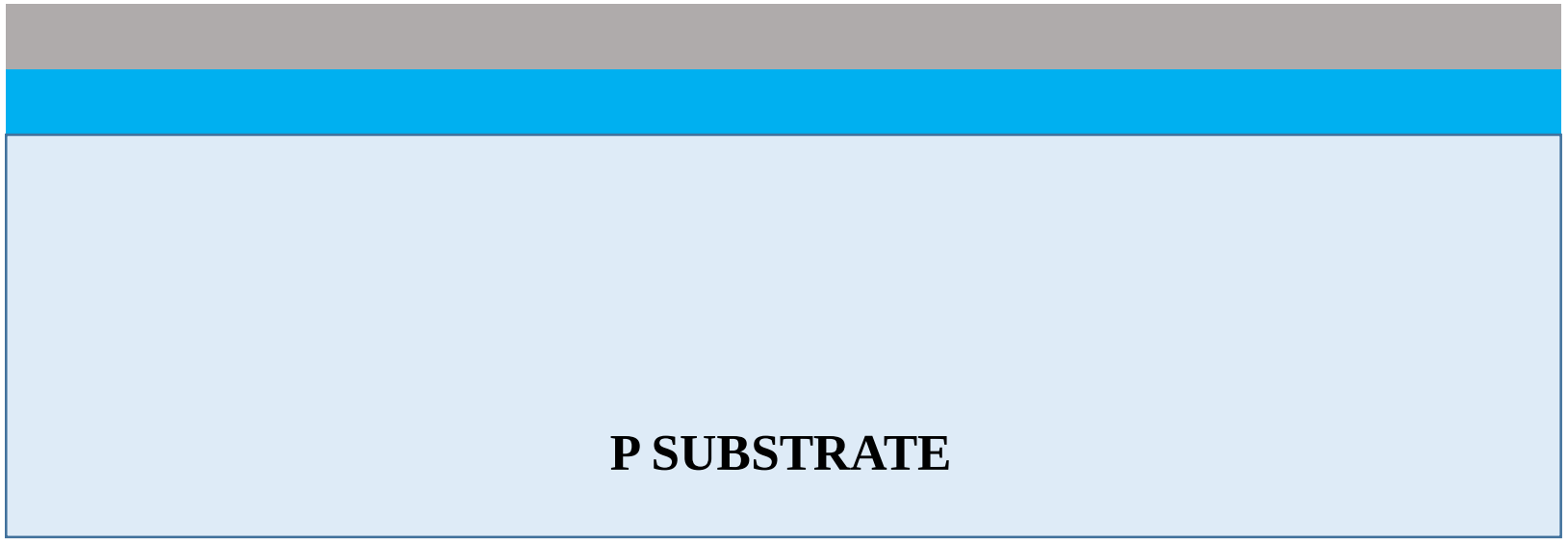


Deposition of protective SiO2

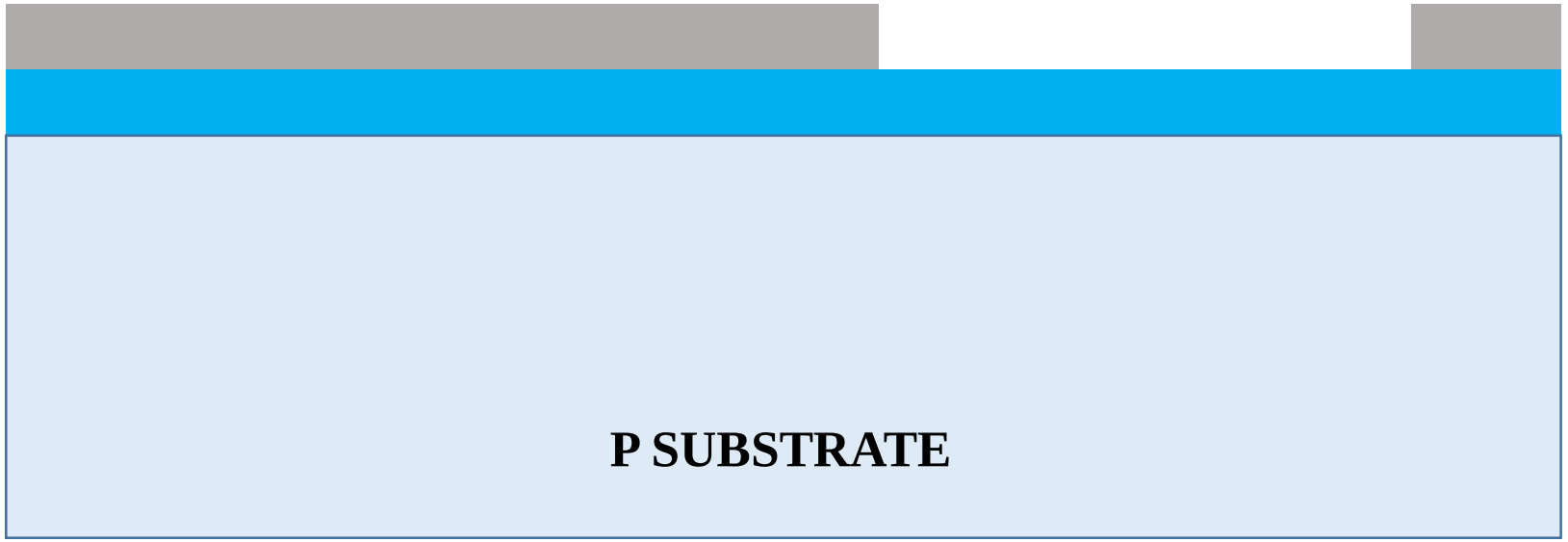


CMOS Fabrication Process

Deposition of photoresist material

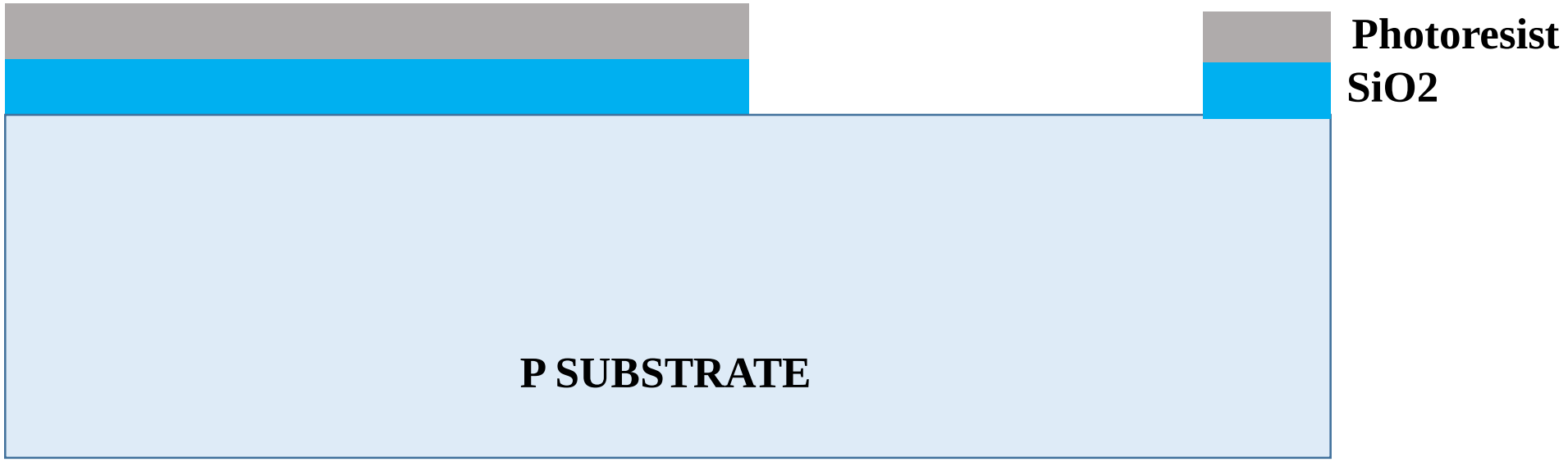


Etching of photoresist material

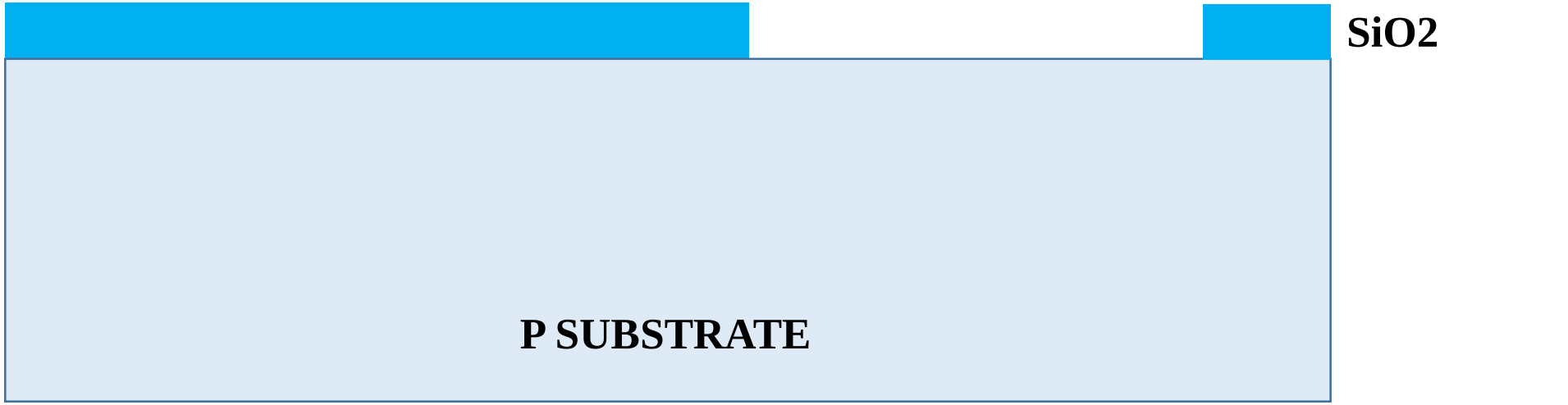


CMOS Fabrication Process

Etching of SiO2

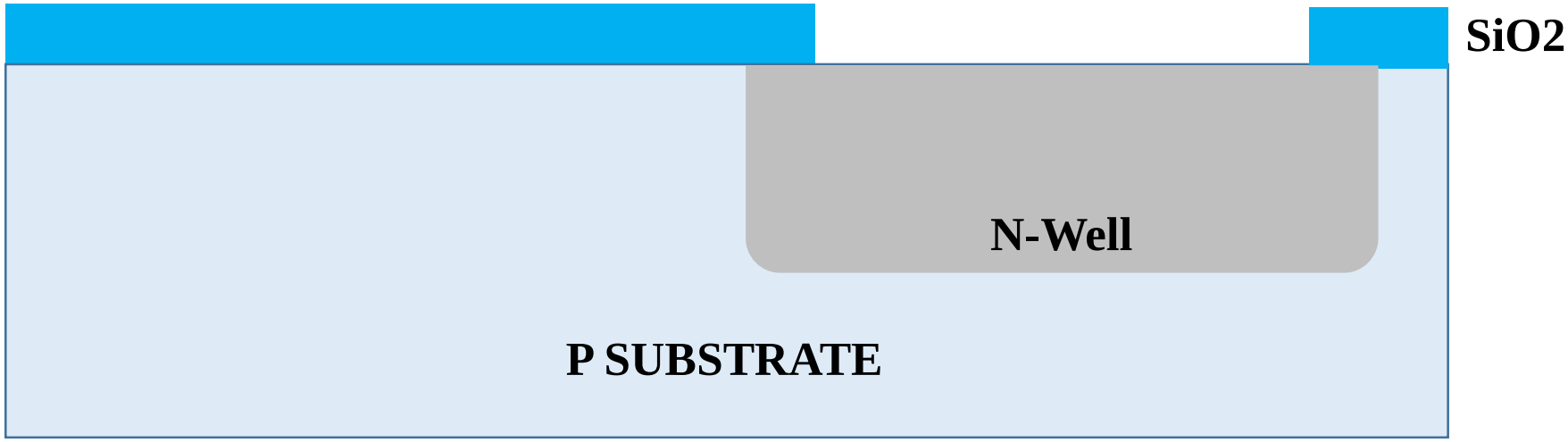


Complete Etching of photoresist material

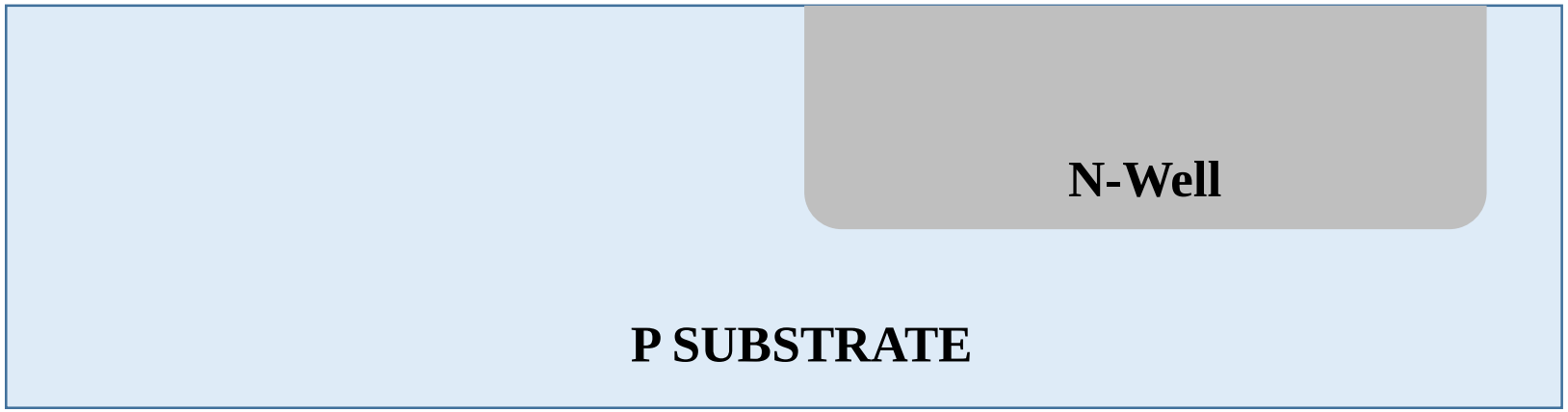


CMOS Fabrication Process

N-well Creation

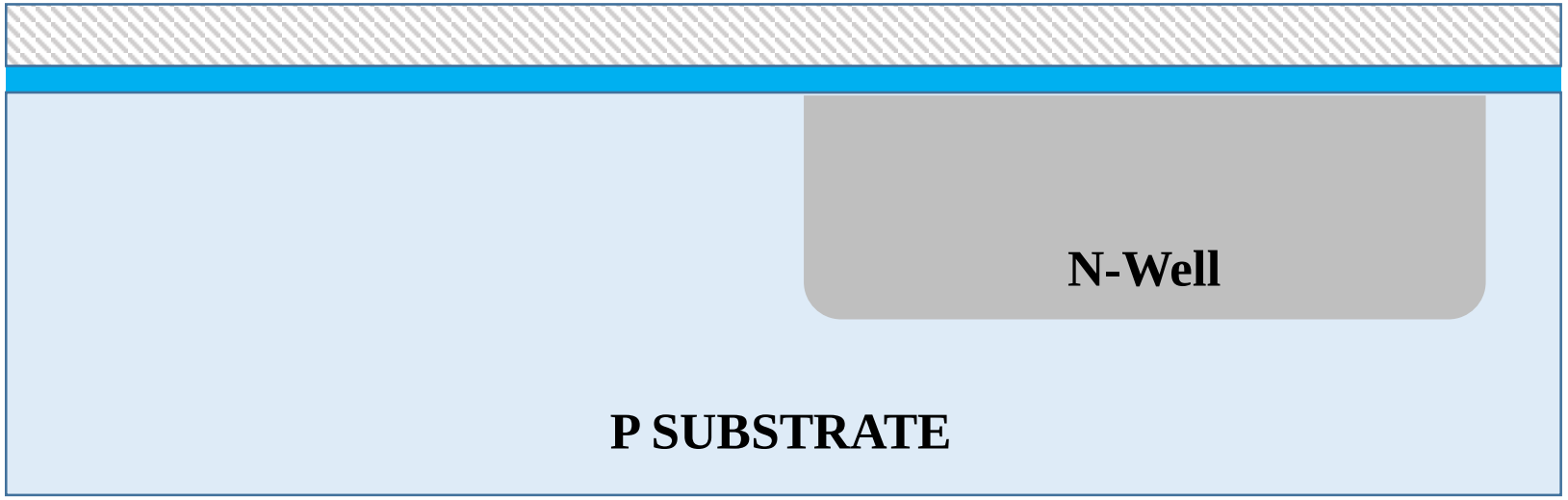


Etching of SiO2

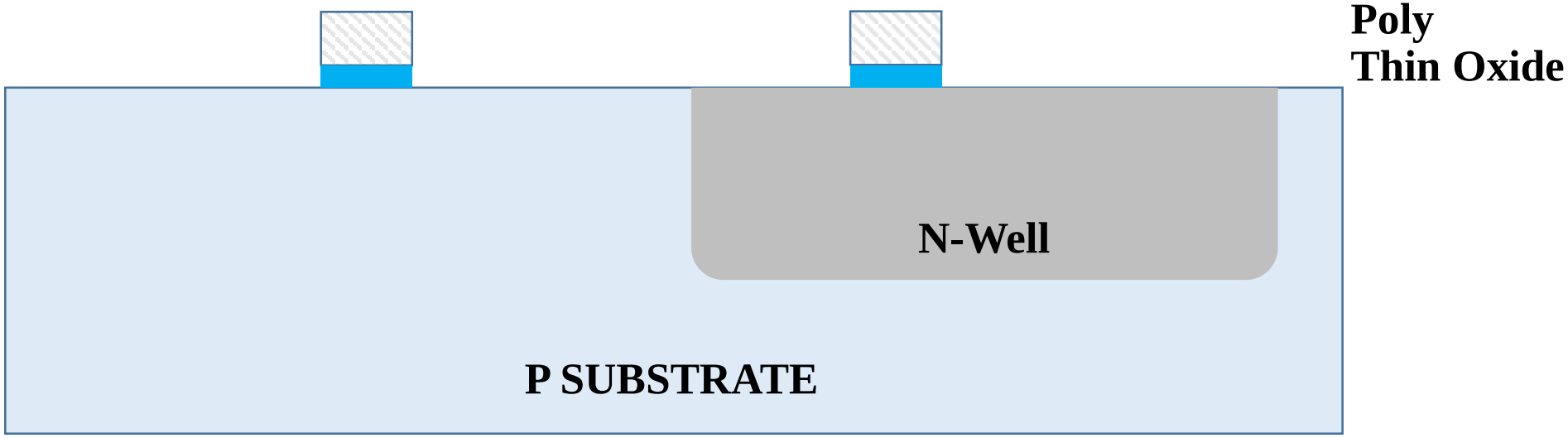


CMOS Fabrication Process

Thin Oxide and Poly Deposition

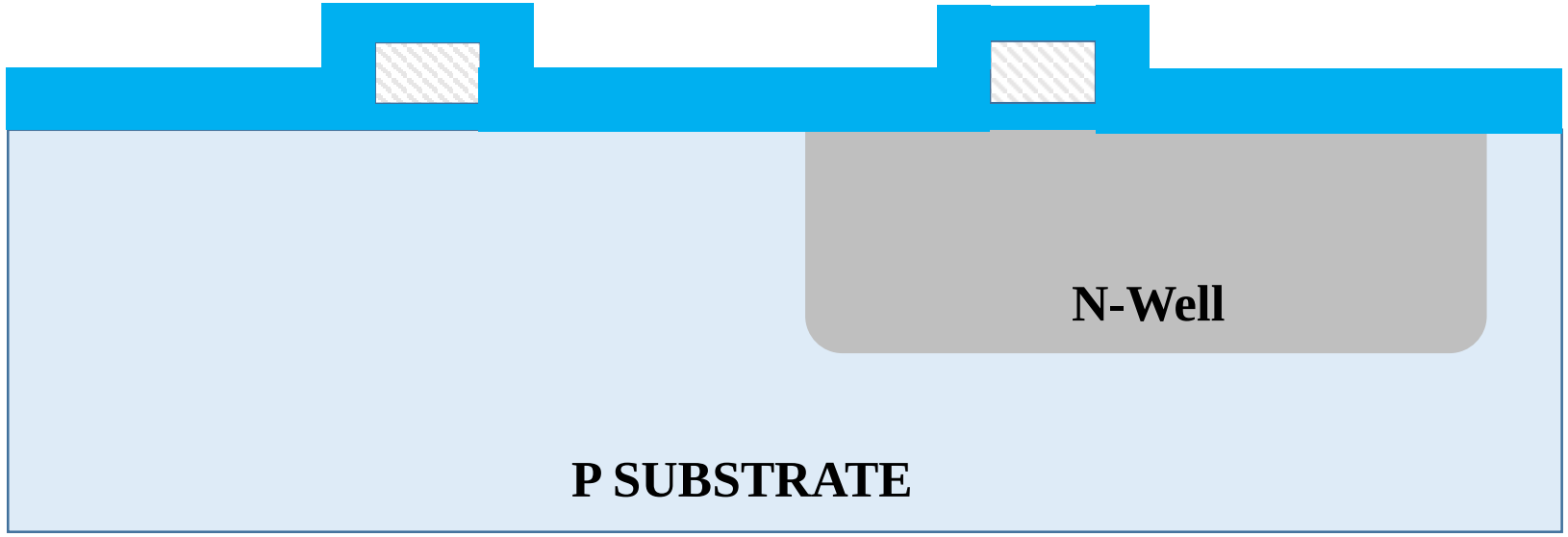


Etching of Thin Oxide and poly except the gate region

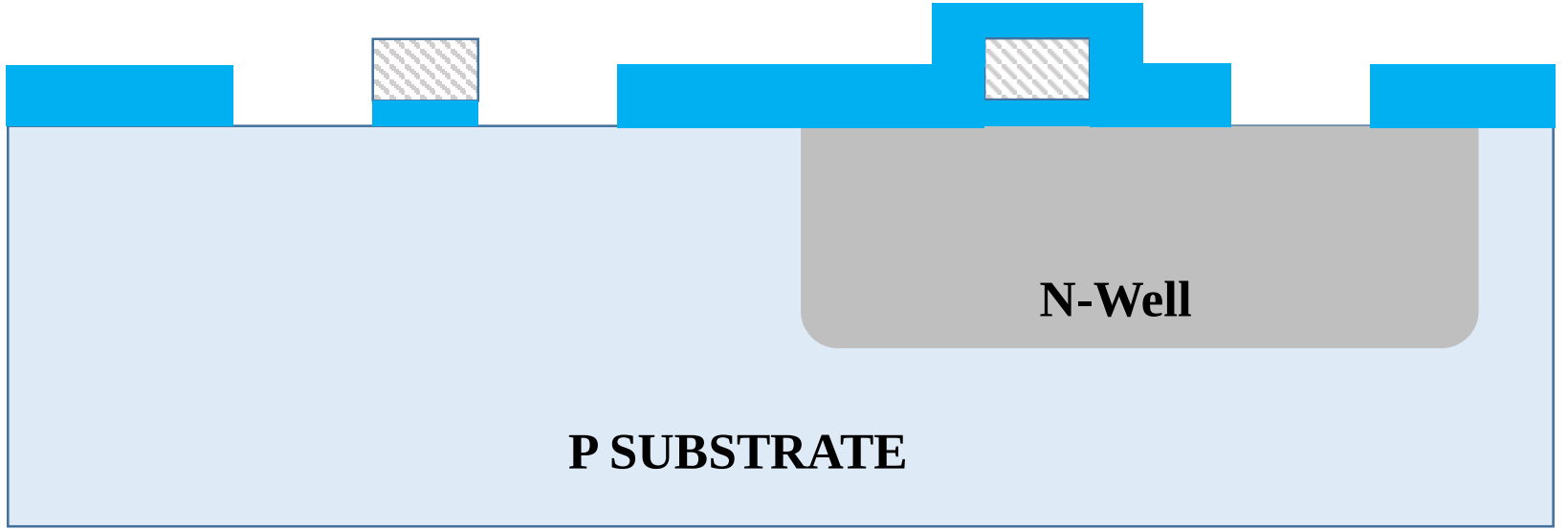


CMOS Fabrication Process

Thick Oxide Deposition

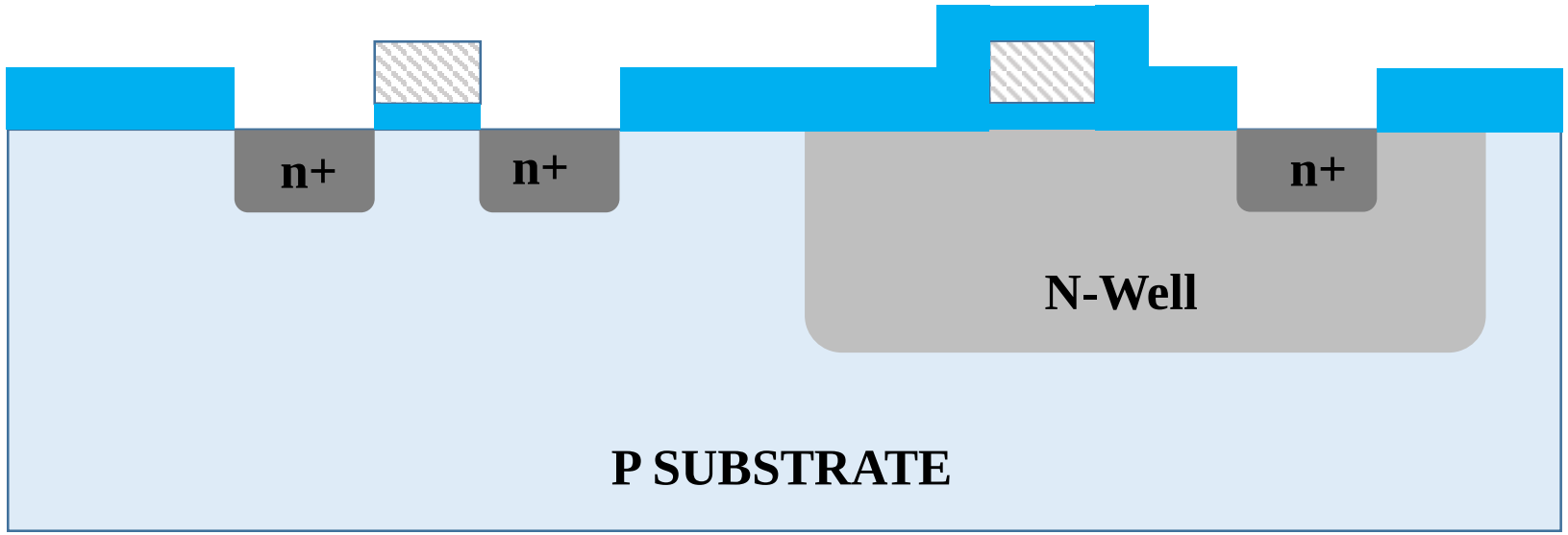


Etching of Thick Oxide



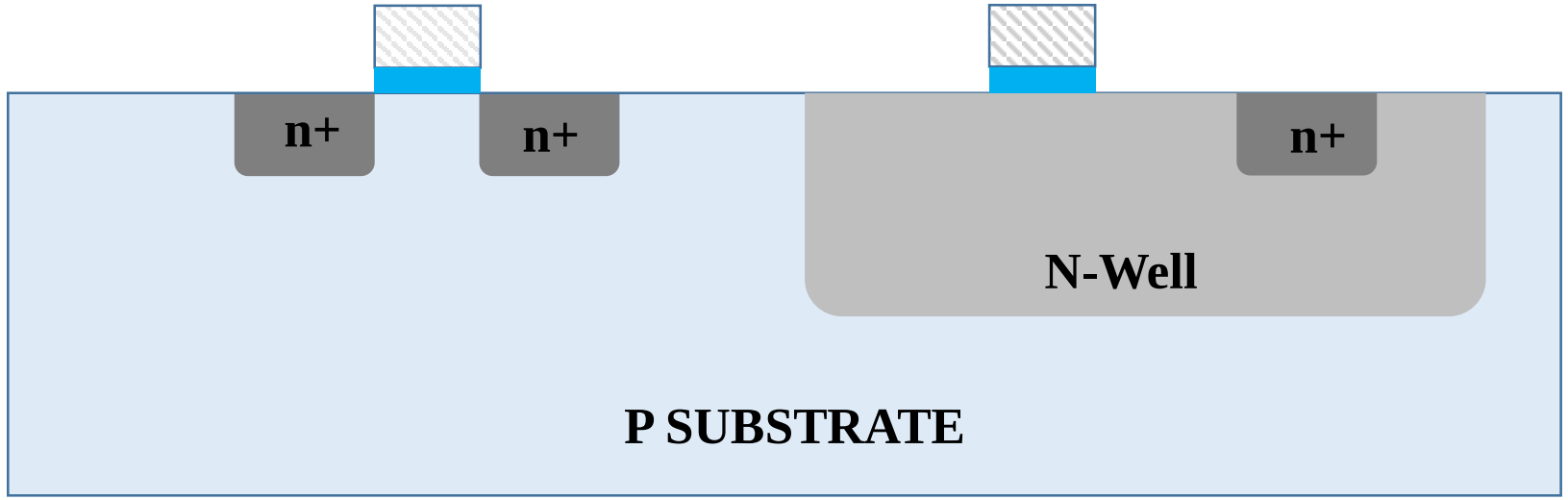
CMOS Fabrication Process

N+ diffusion region creation



Thick Field Oxide

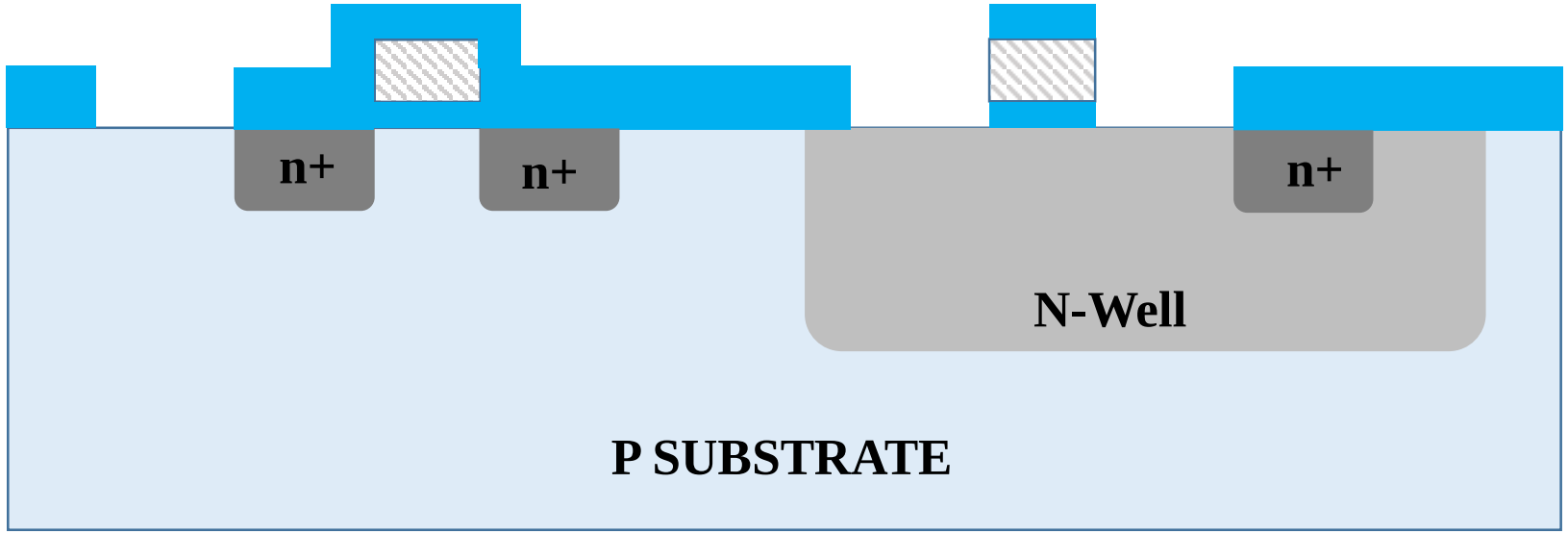
Etching of Thick Oxide



Poly Thin Oxide

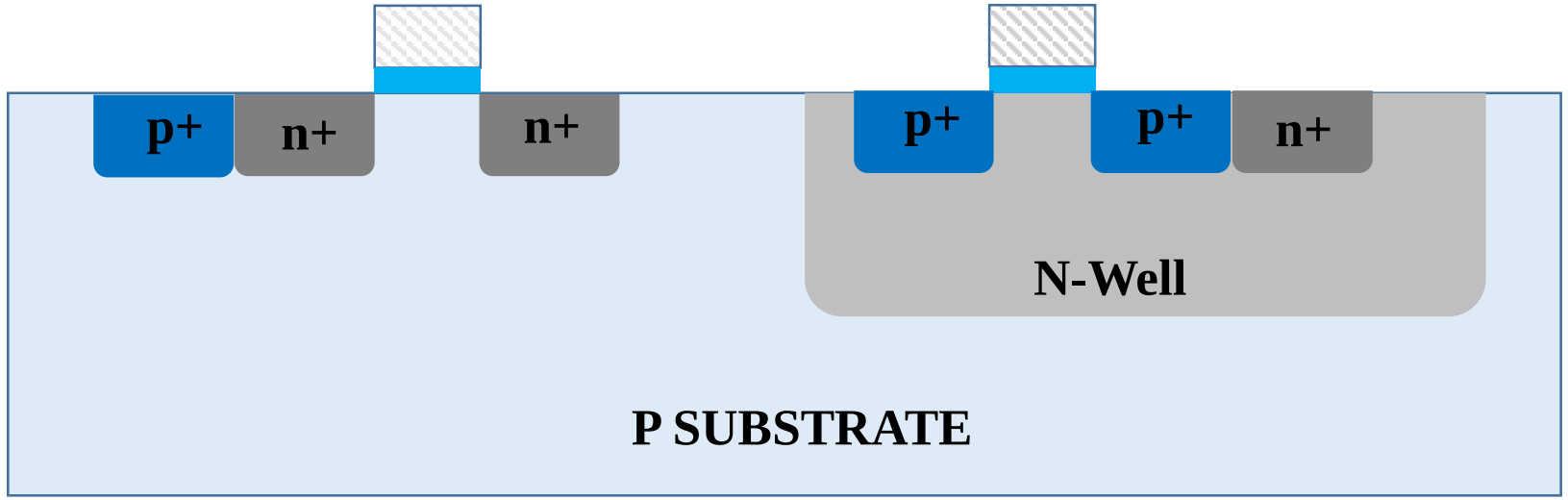
CMOS Fabrication Process

Deposition of Thick Oxide except the P+ region



Thick Field Oxide

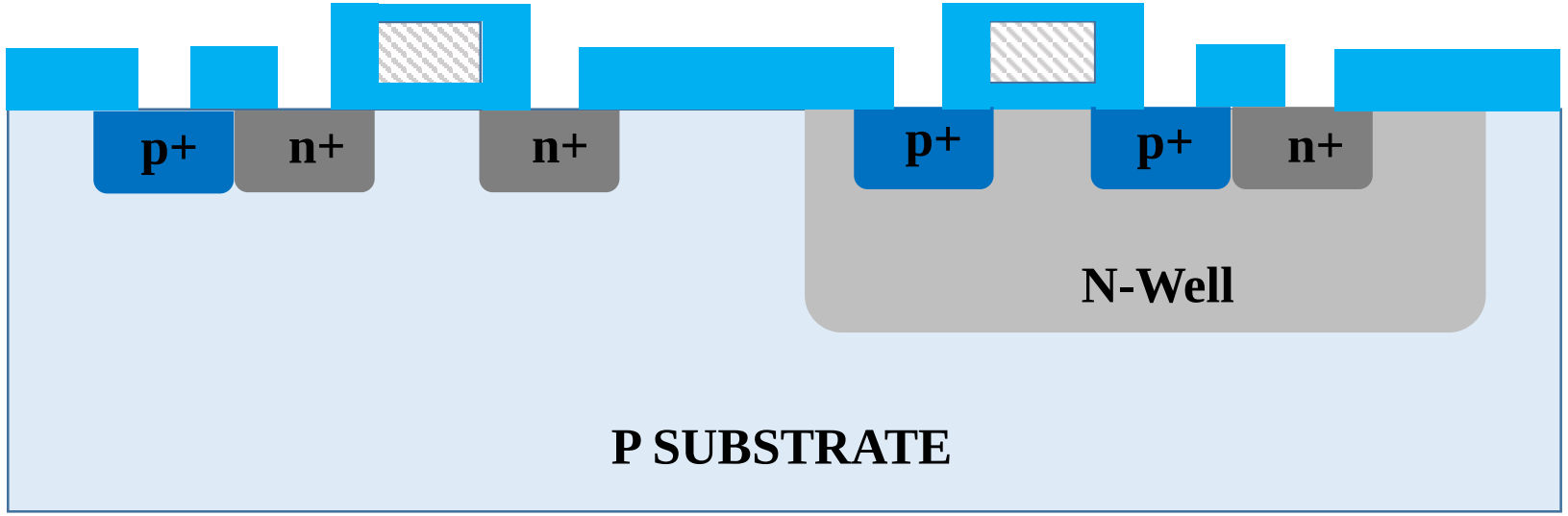
P+ region creation



Poly Thin Oxide

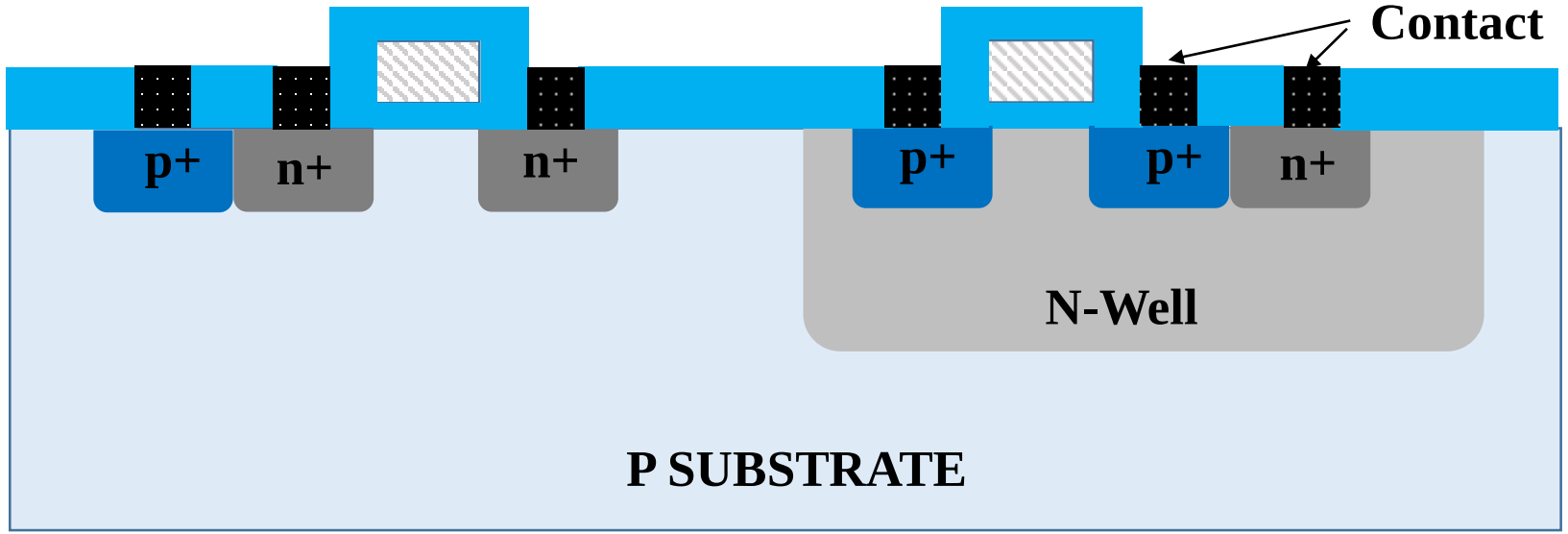
CMOS Fabrication Process

Thick Oxide deposition except the contact window



Thick Field Oxide

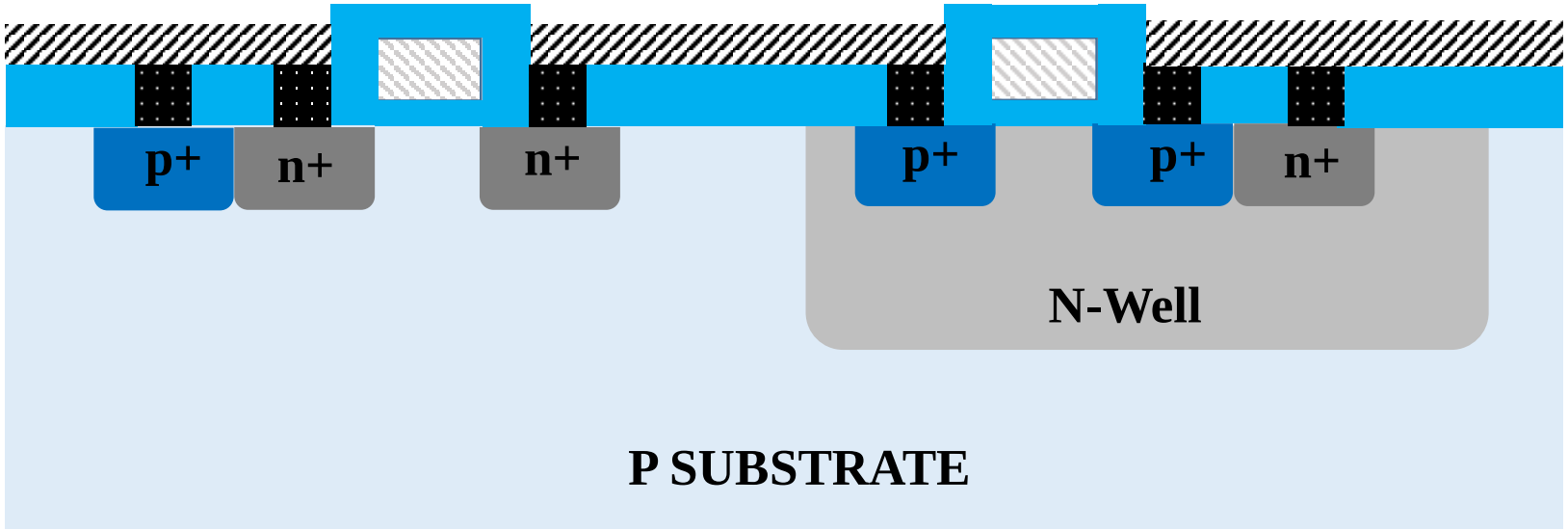
Contact Creation



Thick Field Oxide

CMOS Fabrication Process

Metal Deposition



Metal
Thick Field
Oxide

Thank You