# General Purpose Input and Output (GPIO) Design

**Santunu Sarangi**

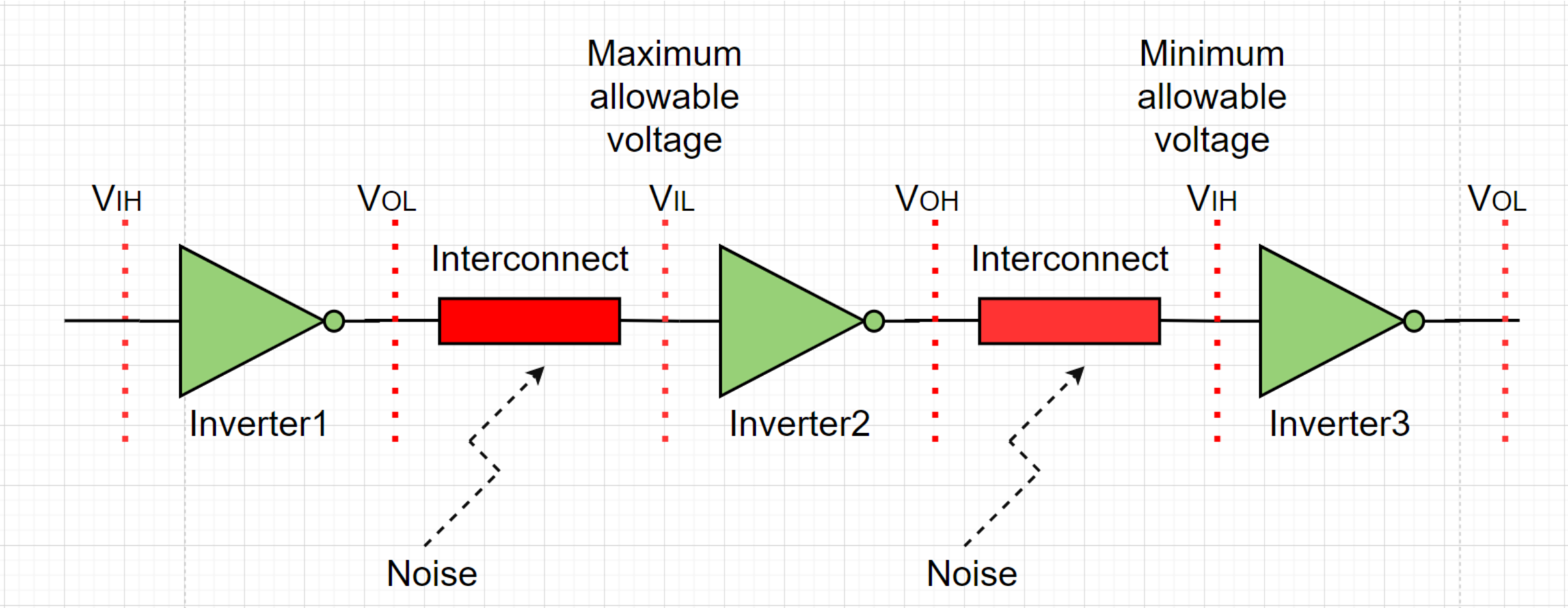
# Objectives

- Understanding of critical voltages VOH, VOL, VIH, VIL and VTH.

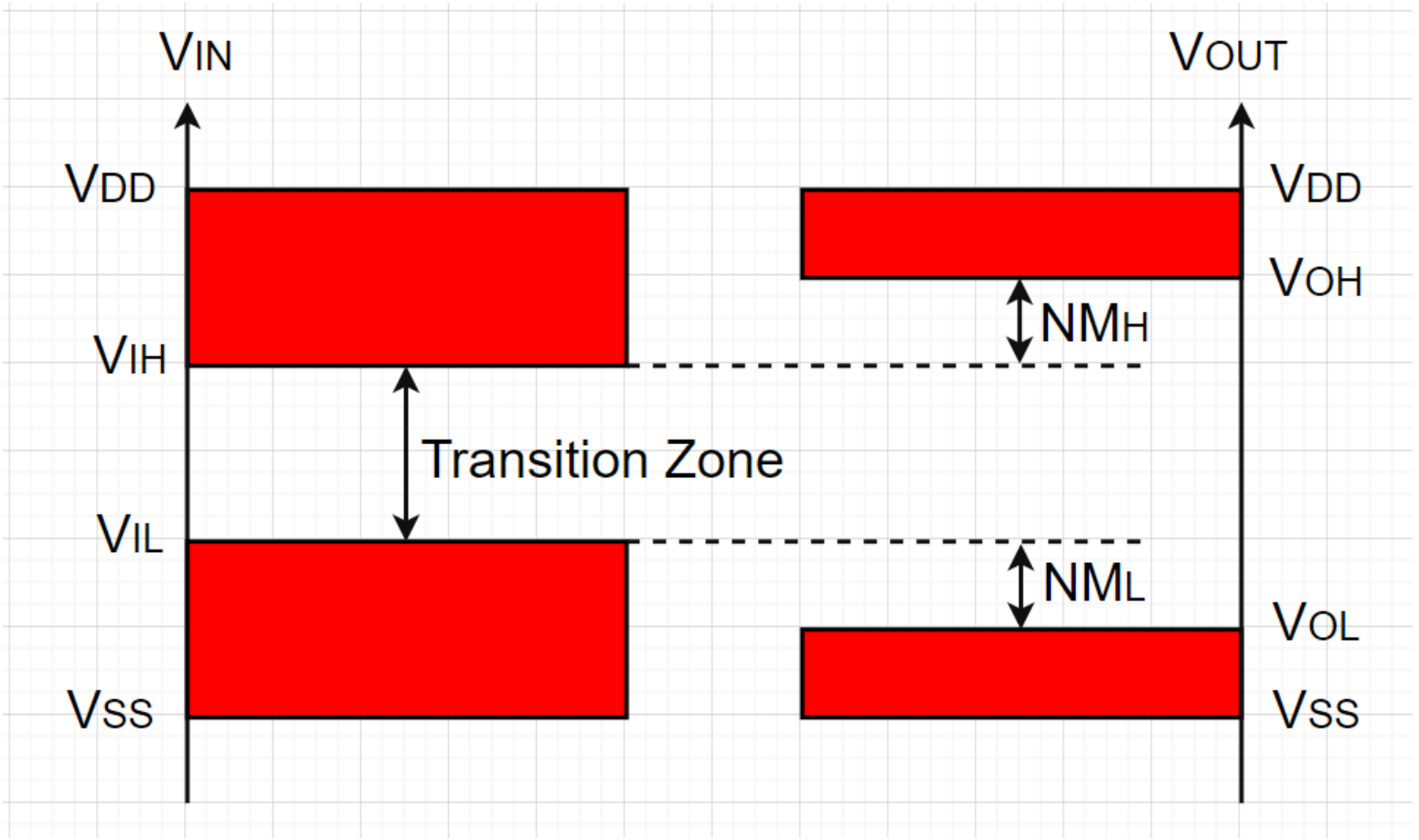
- Overall IO structure
  - Input Mode
  - Output mode

- TX Driver design (Buffer chain design)
  - Understanding Load Capacitance
  - Number of stages
  - Stage Ratio

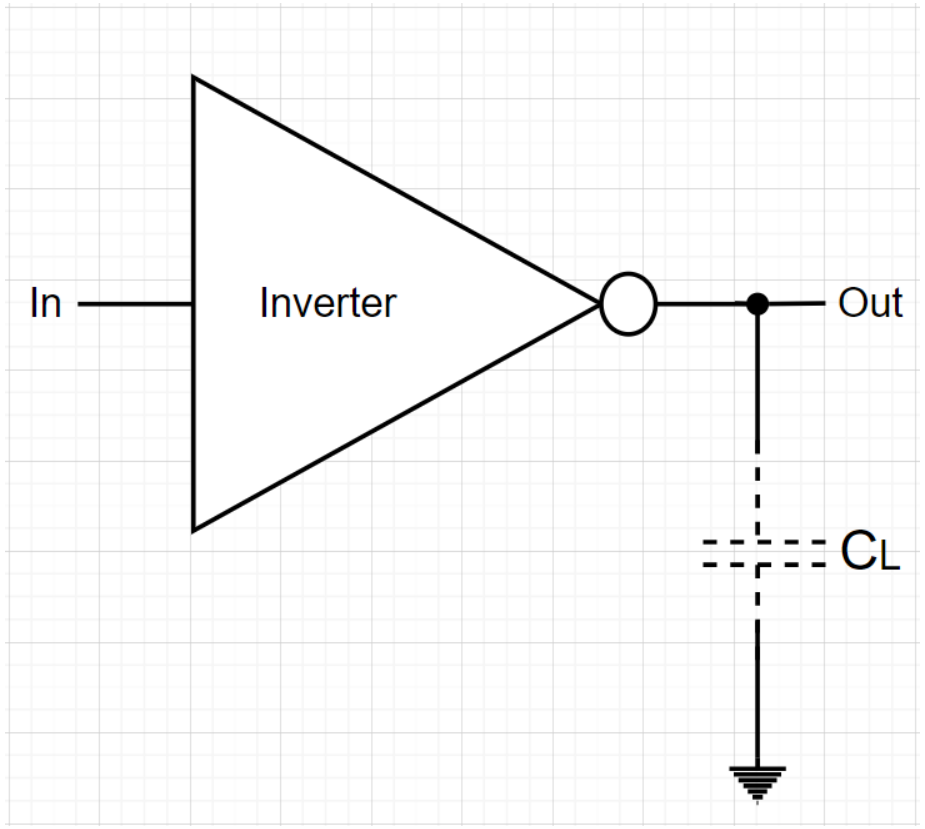
# Basics of Critical Voltage for Noise Margin

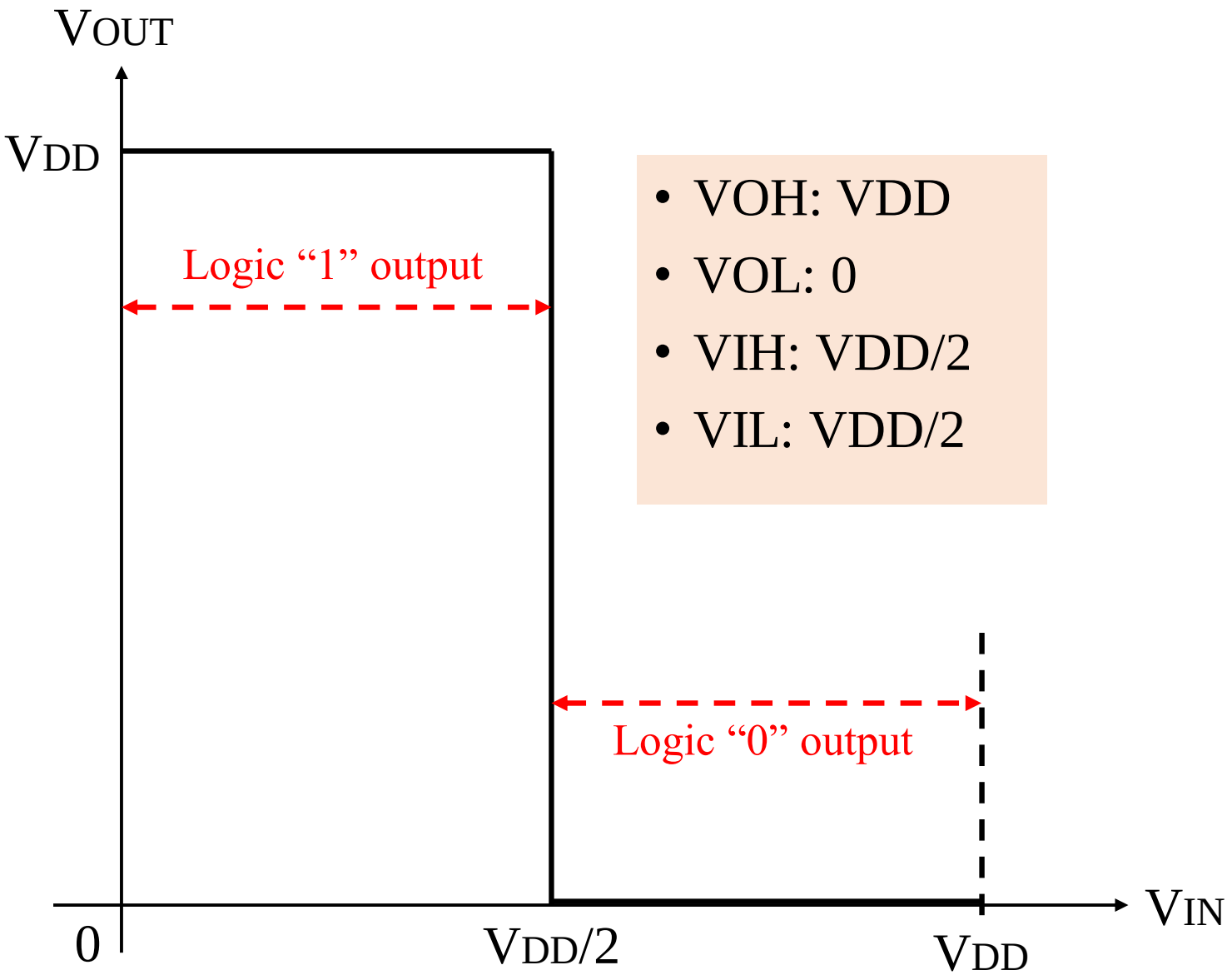


# Noise Margin



# Basics of Critical Voltage and Noise Margin: Ideal Inverter

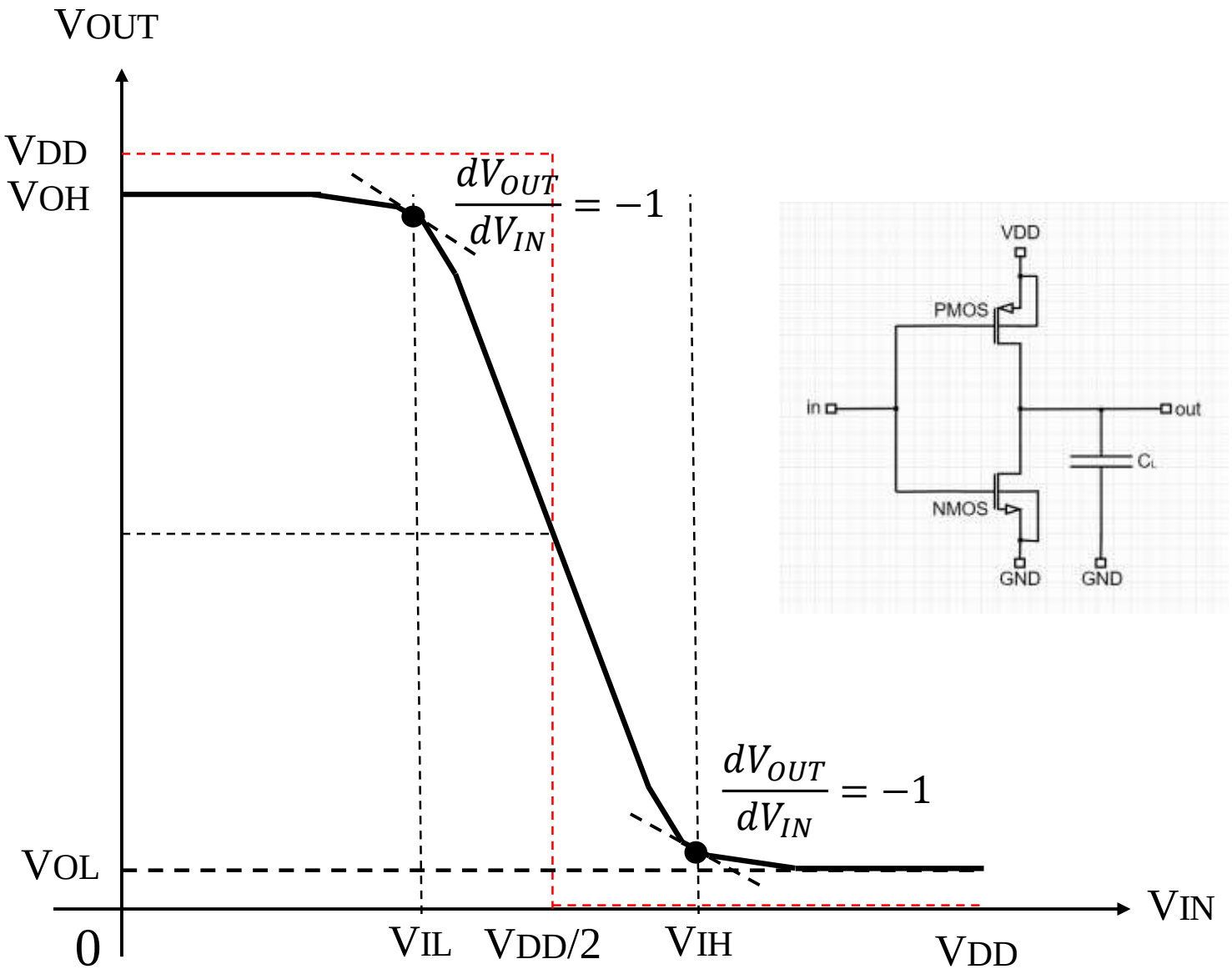



- VOH: VDD
- VOL: 0
- VIH: VDD/2
- VIL: VDD/2

# Basics of Critical Voltages: Practical Inverter

- VOH: Minimum output voltage considered as logic “HIGH”
- VOL: Maximum output voltage considered as logic “LOW”
- VIH: Minimum input voltage considered as logic “HIGH”
- VIL: Maximum input voltage considered as logic “LOW”



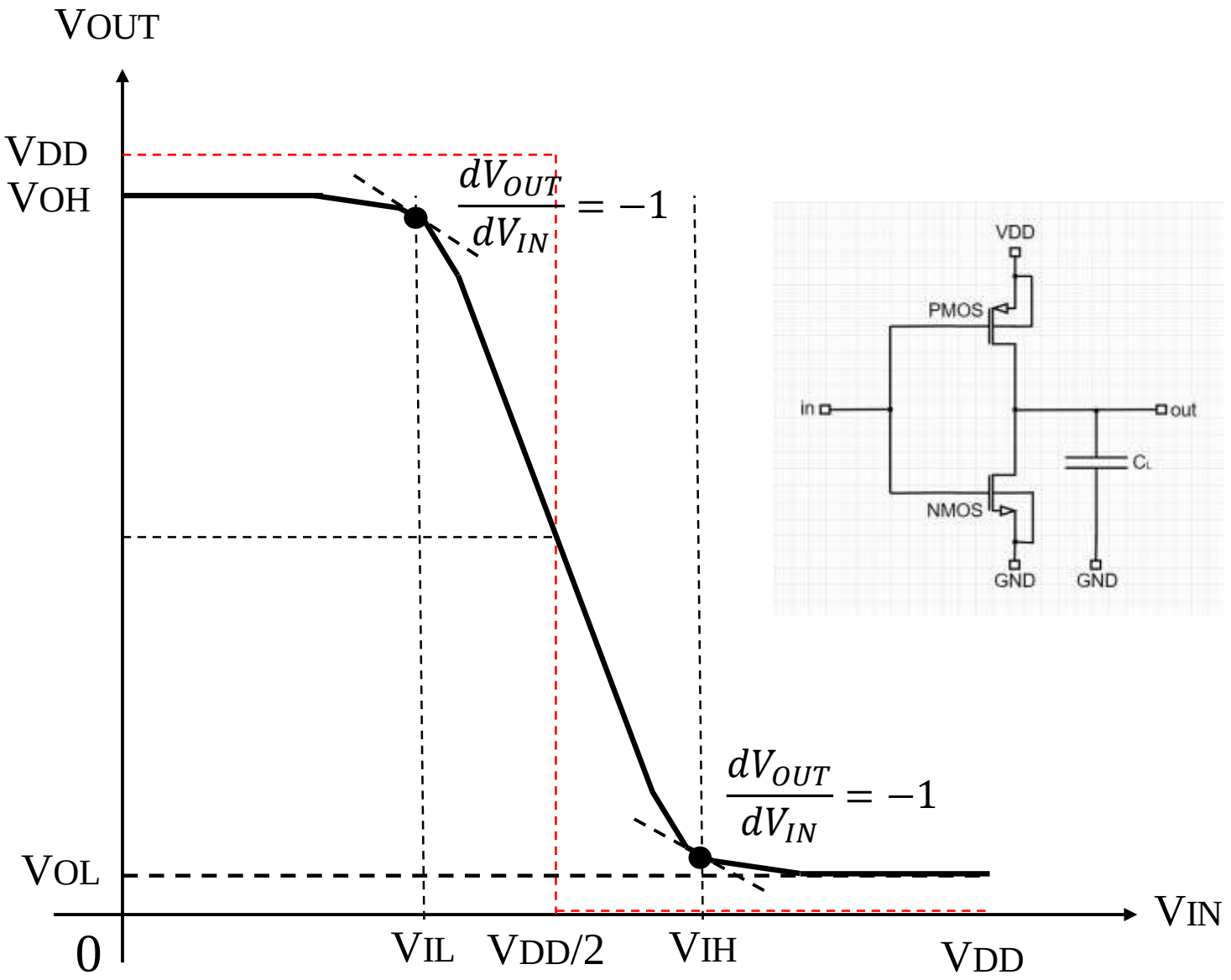
# Calculation of Critical Voltages

- $V_{OH} \approx V_{DD}$
- $V_{OL} \approx 0$
- $V_{IL} = \frac{2V_{OUT}+V_{T0,p}-V_{DD}+k_r V_{T0,n}}{1+k_r}$

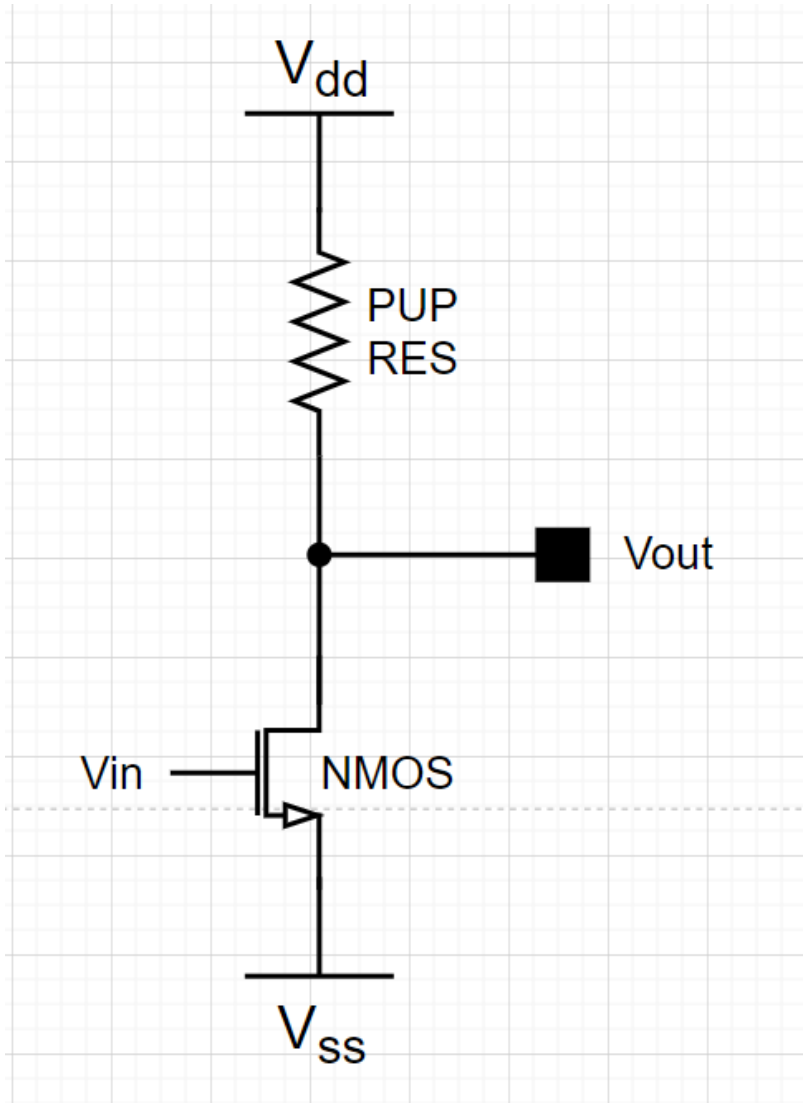
Where $k_r = \frac{k_n}{k_p}$

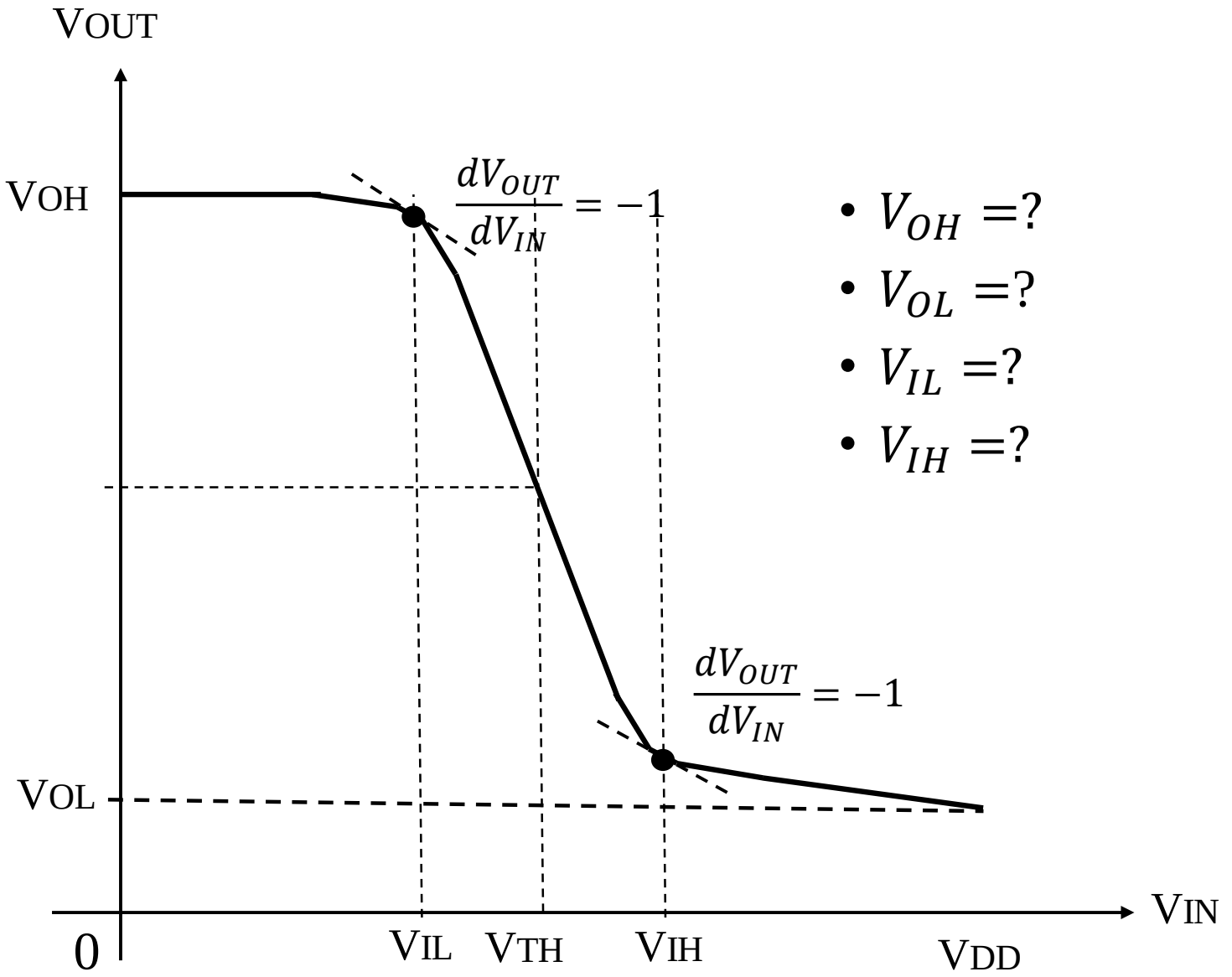
- $V_{IH} = \frac{V_{DD}+V_{T0,p}+k_r(2V_{OUT}+V_{T0,n})}{1+k_r}$

Where $k_r = \frac{k_n}{k_p}$



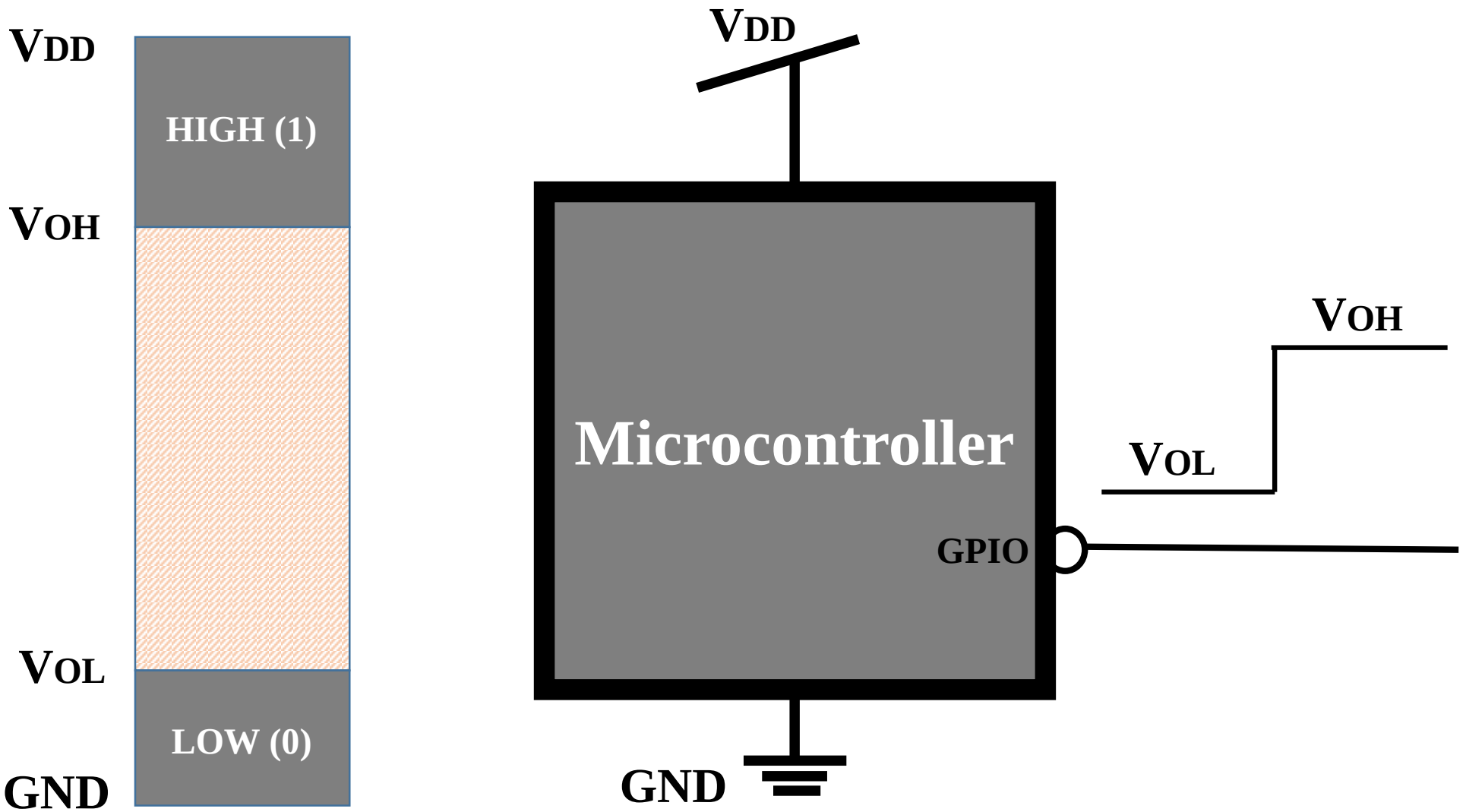
# Resistive Load Inverter



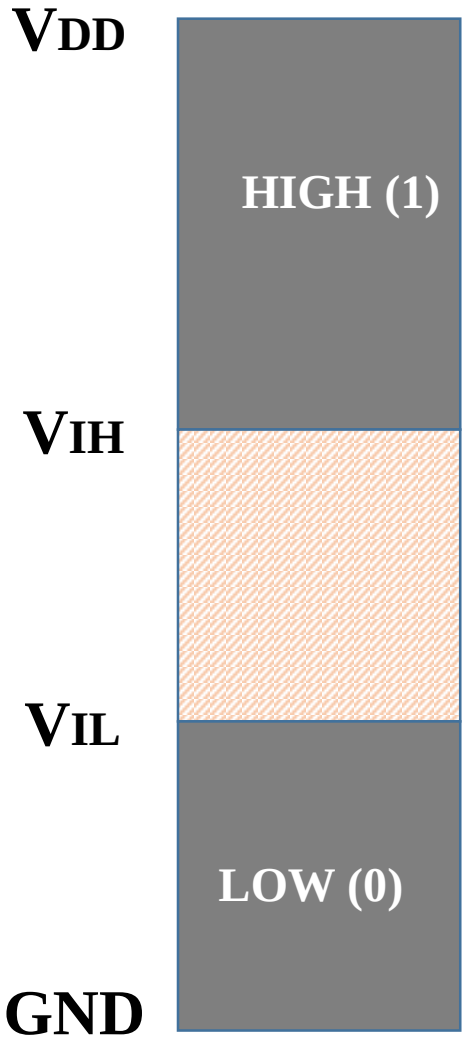



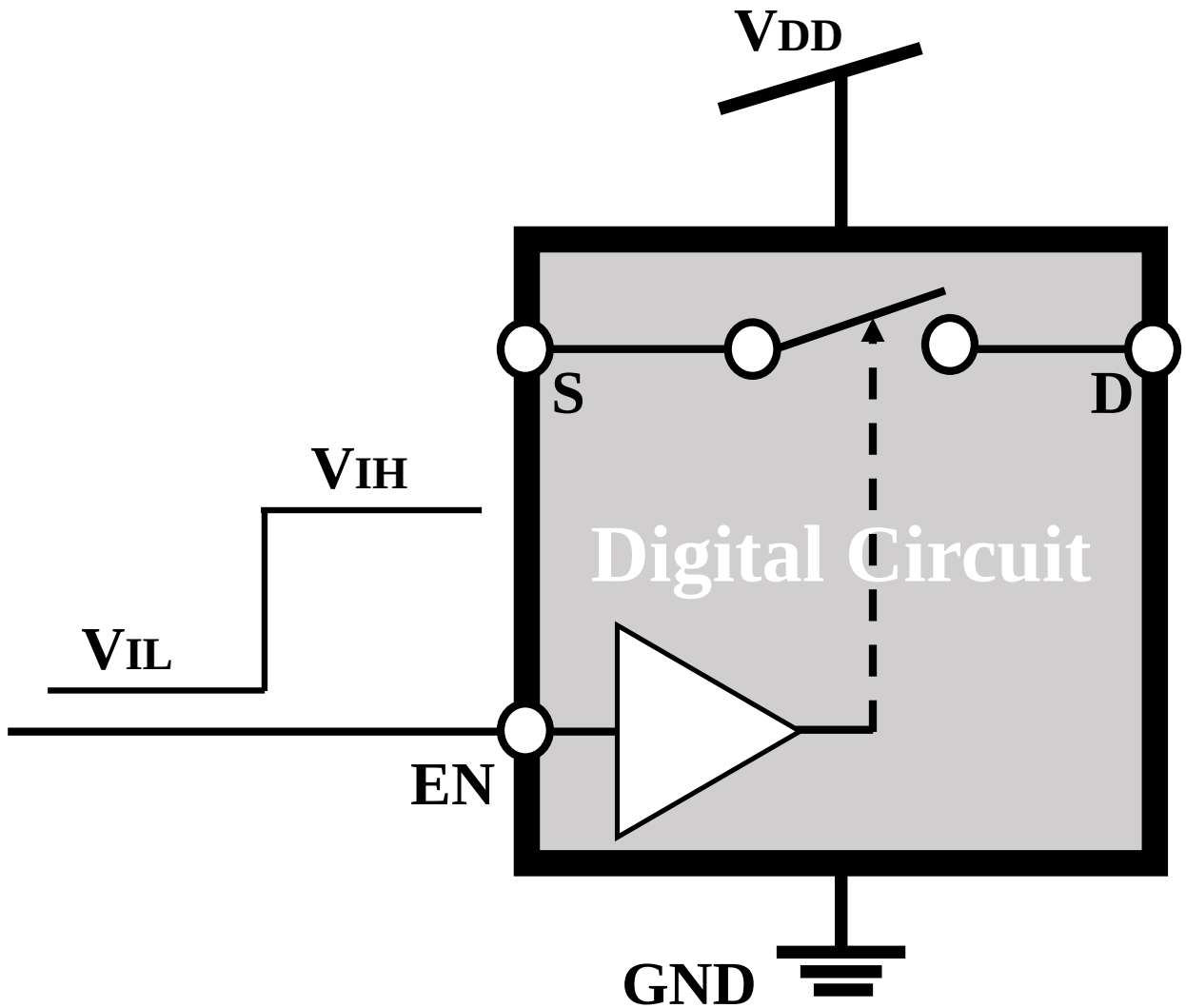

- $V_{OH} =?$
- $V_{OL} =?$
- $V_{IL} =?$
- $V_{IH} =?$

# Input and Output Logic Levels

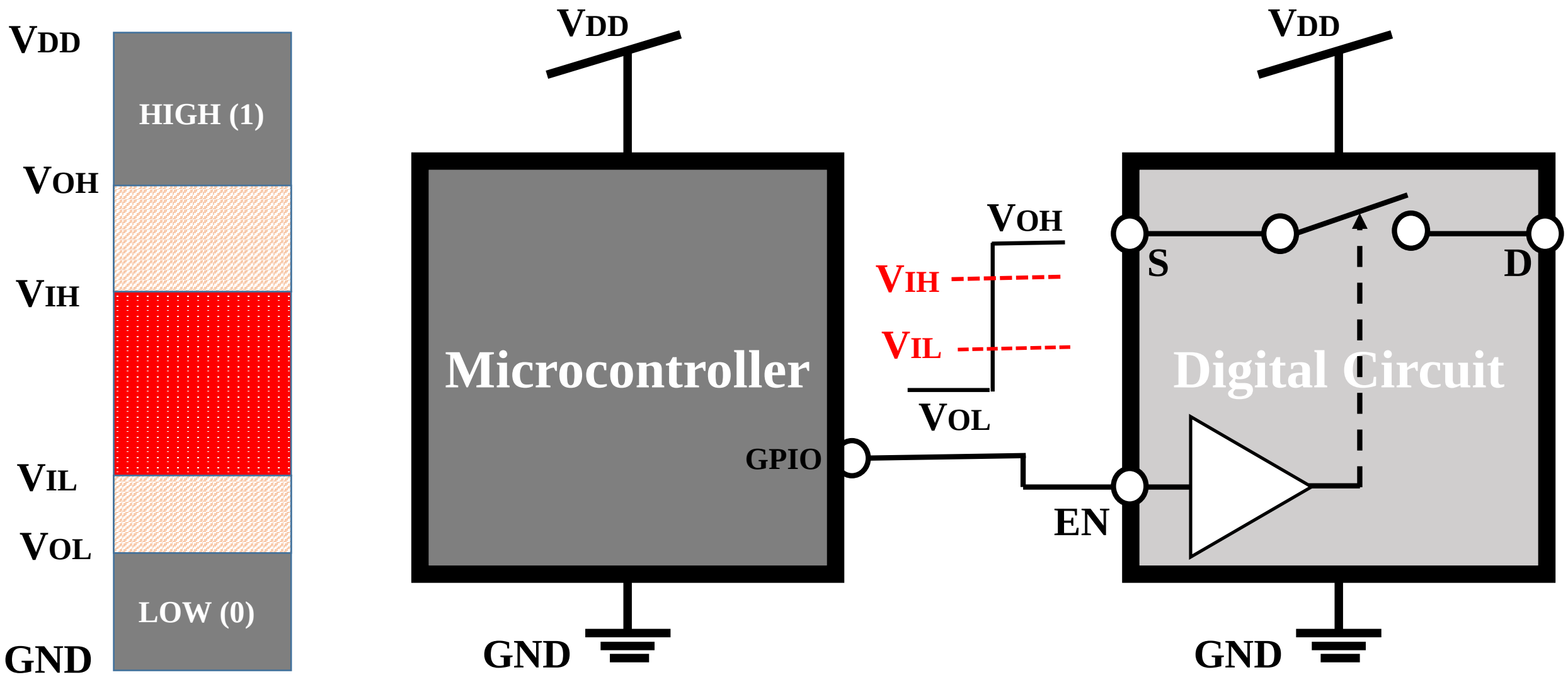


# Input Logic Levels: VIH and VIL

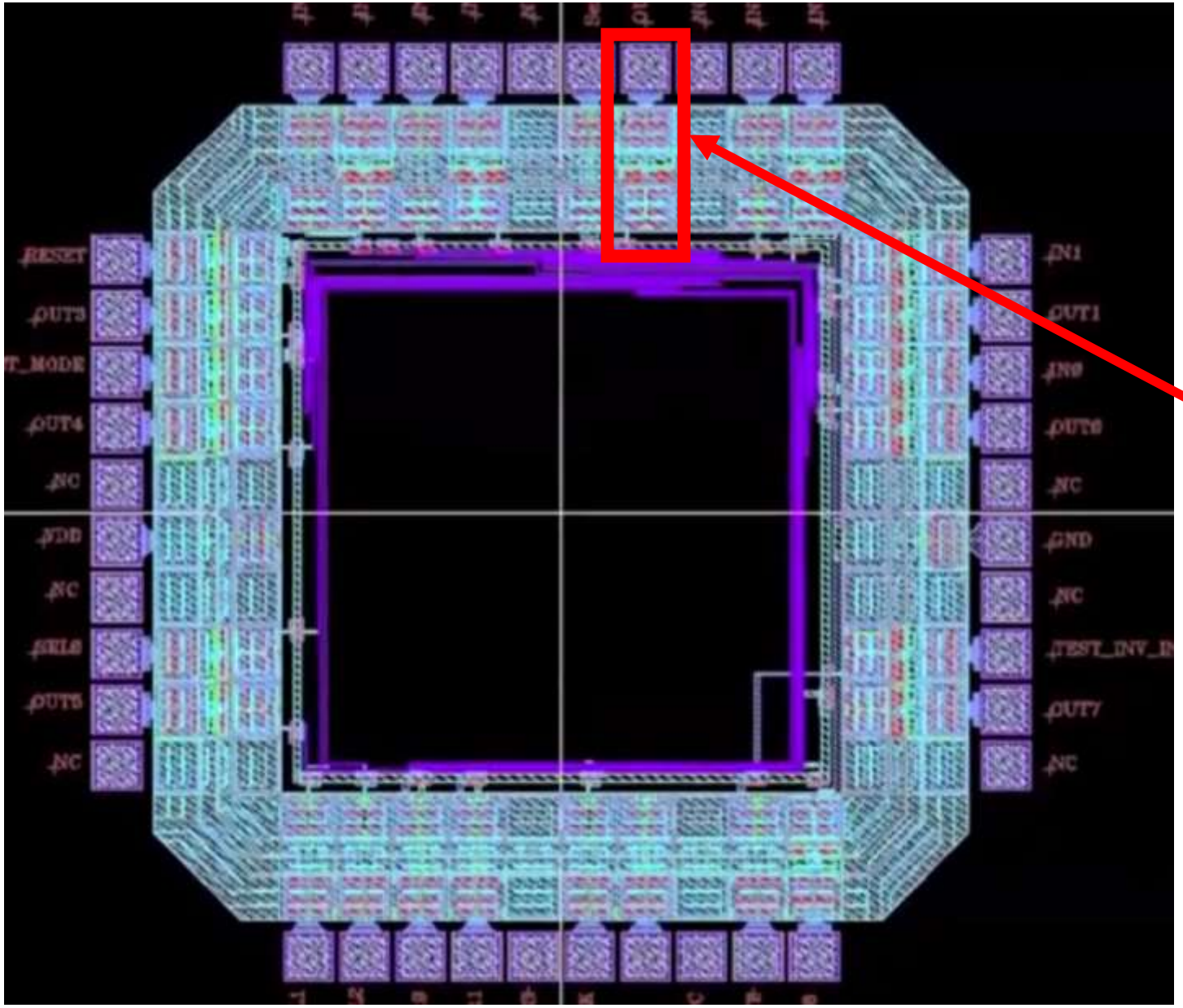


# Input Logic Levels: VIH and VIL



# GPIO



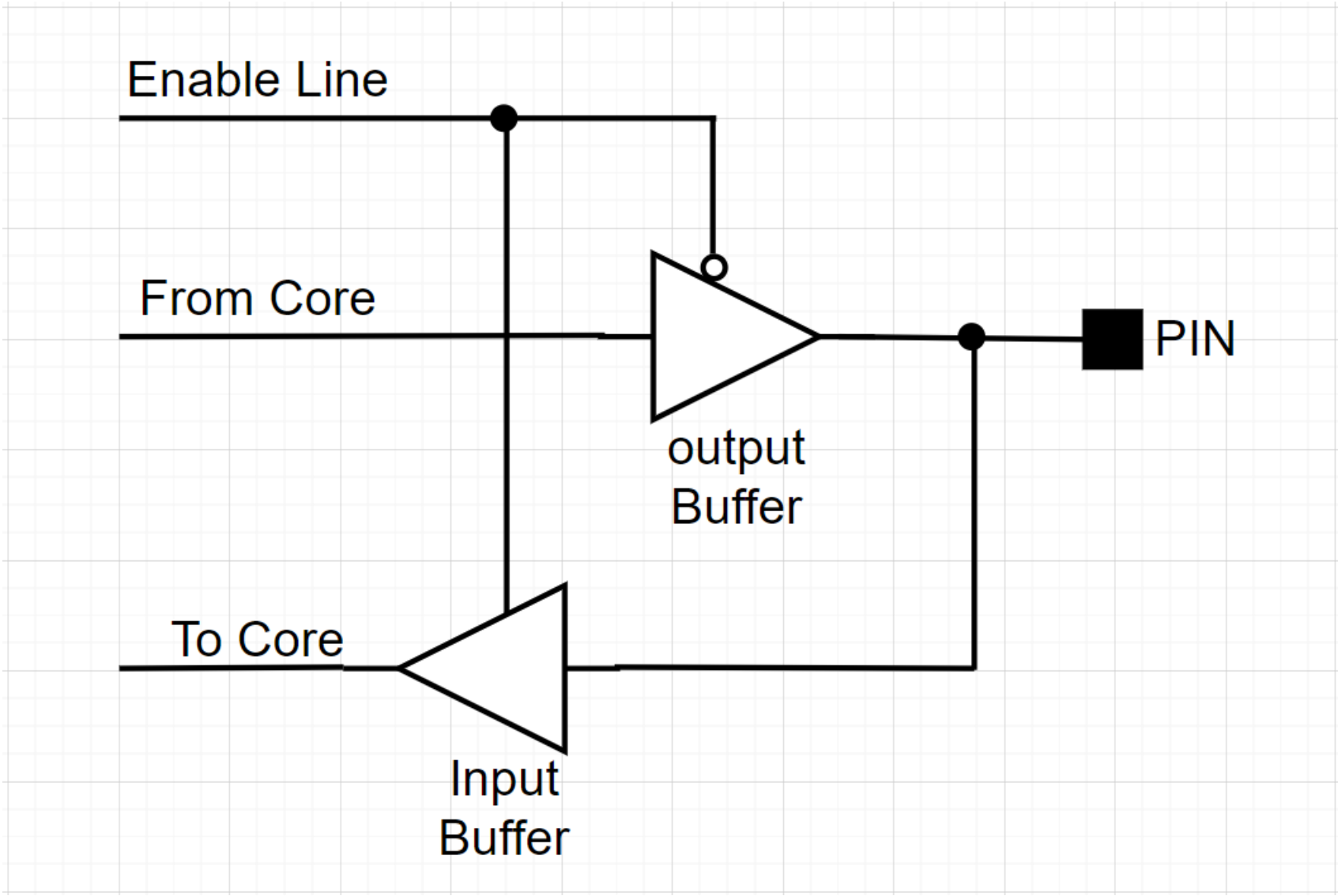

PAD

I/O

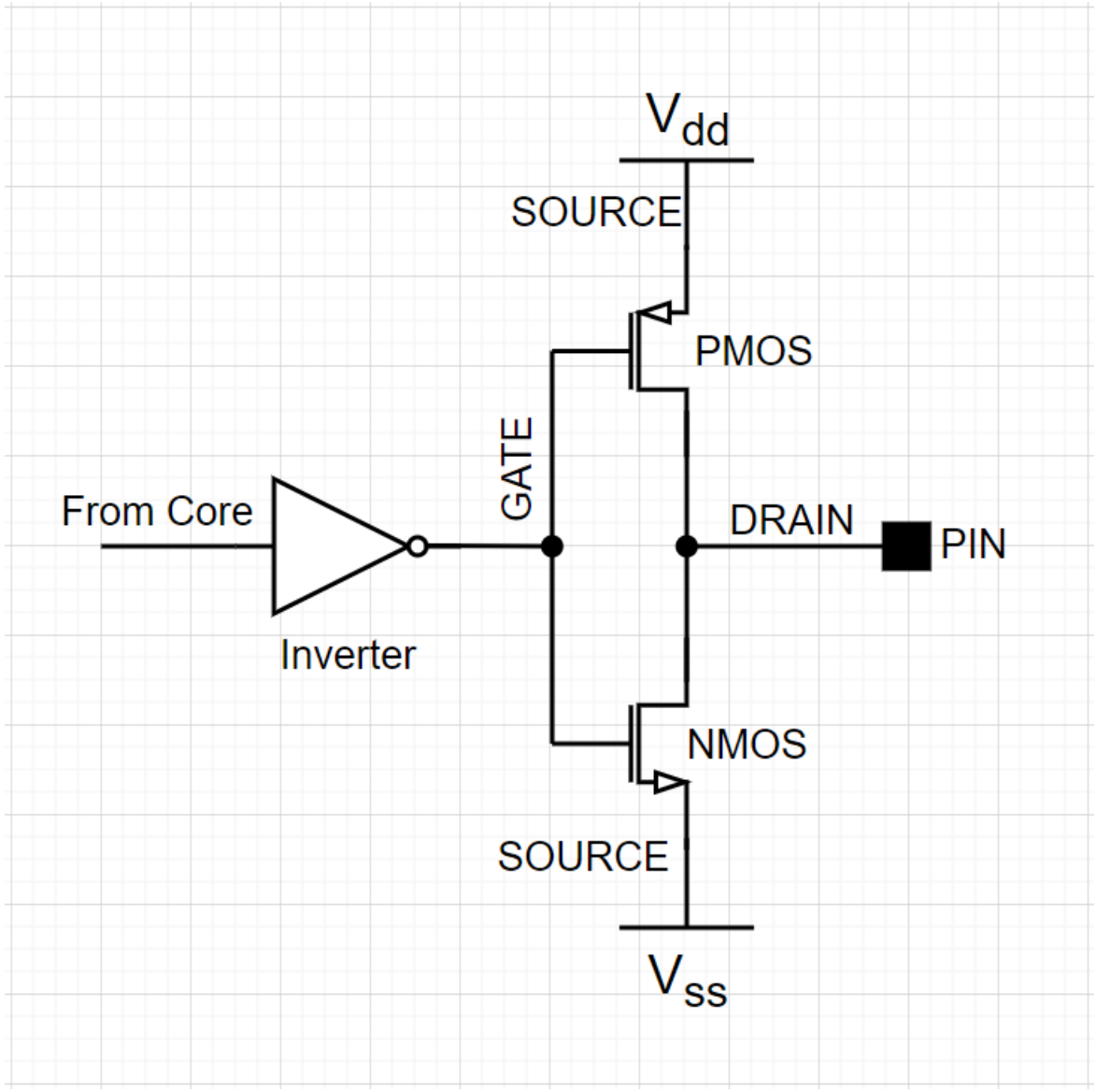
Core

# GPIO: General Purpose Input Output

- Reading digital signal
- Generating trigger
- Issuing interrupt
- GPIO is nothing but the collection of fixed number of I/O pins
- Default mode is input mode and input pin is floating
- Default output mode is push-pull



# GPIO: Output Buffer



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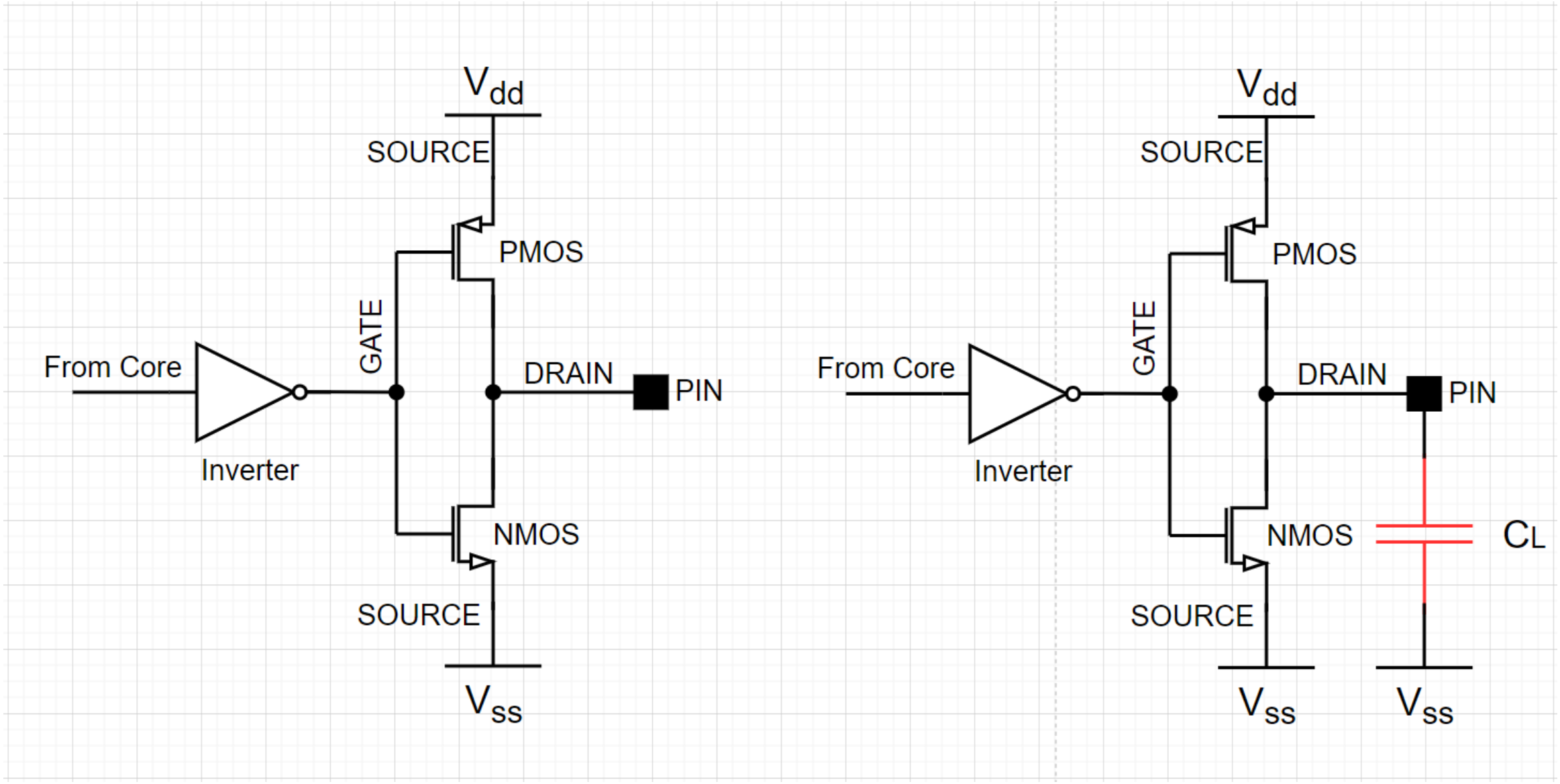
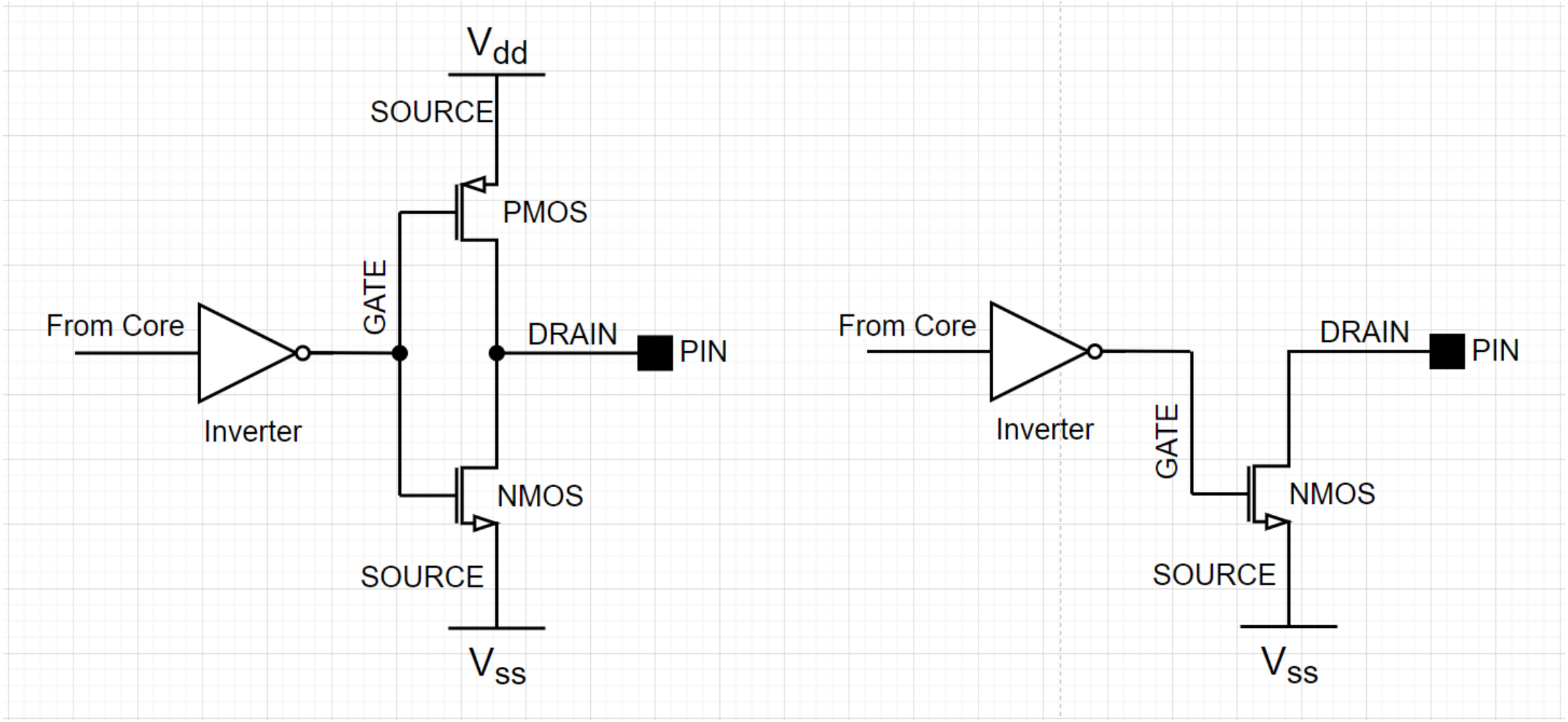
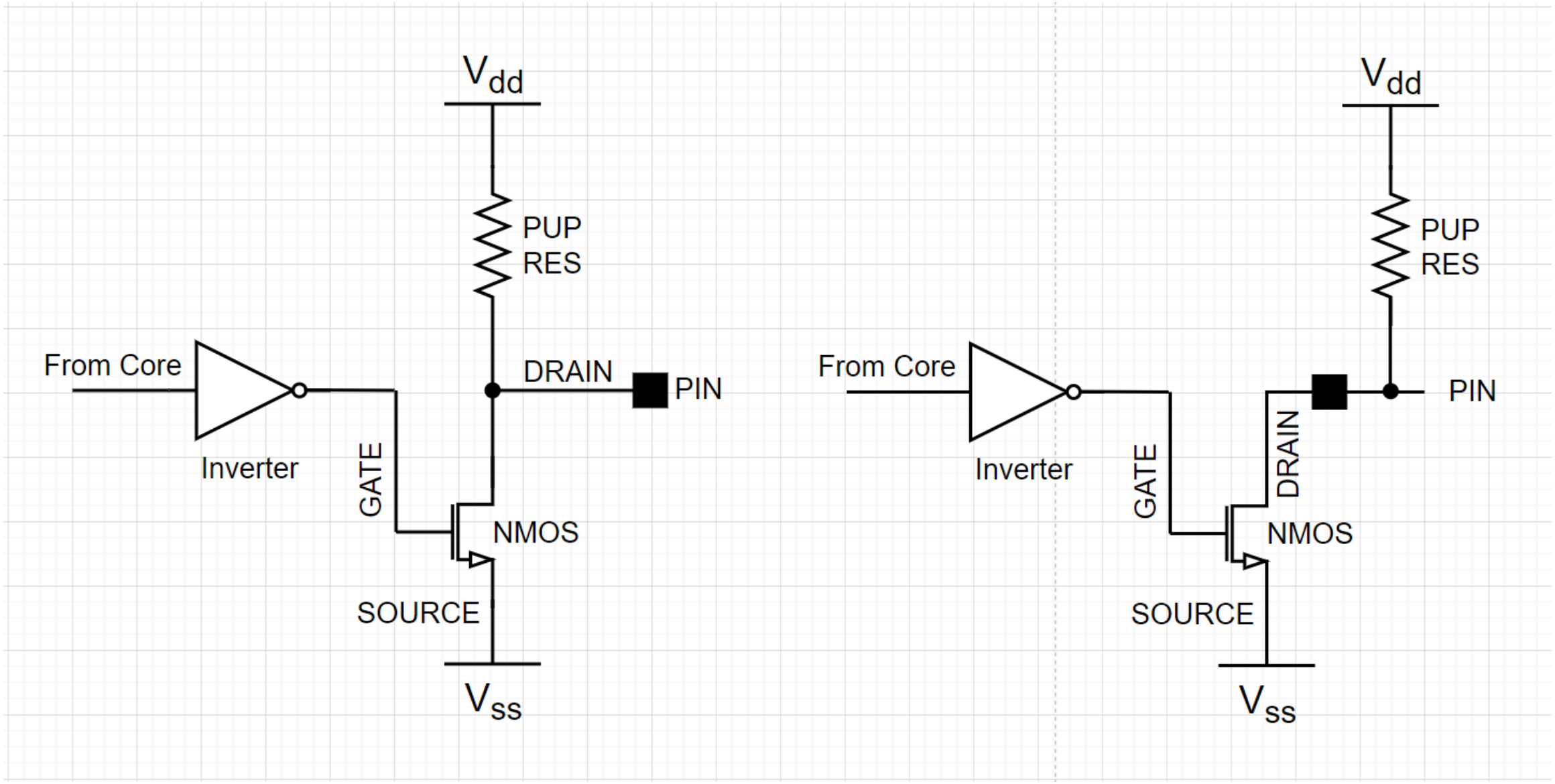


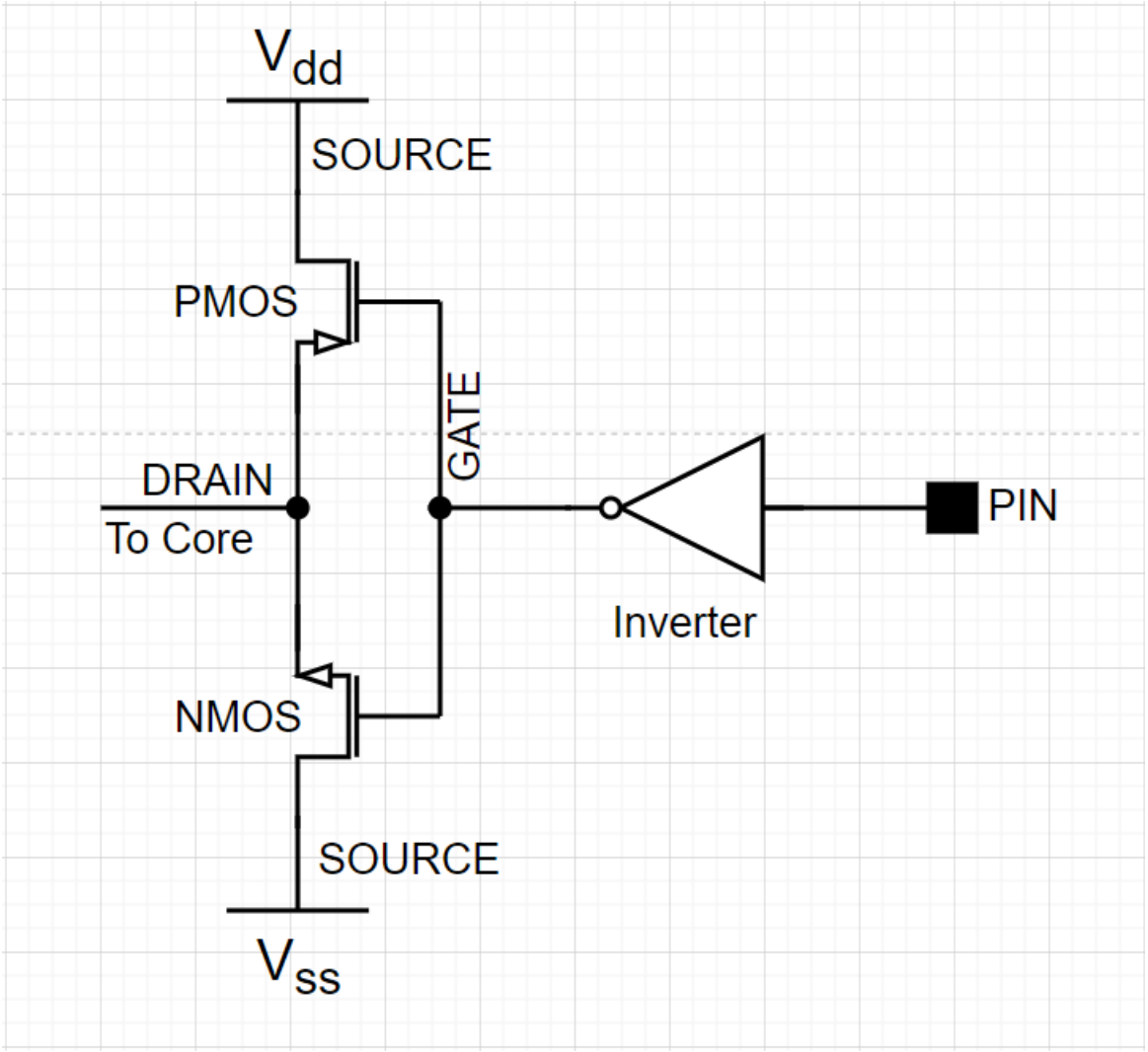
# GPIO: Output Mode-Push-pull or Open Drain



# GPIO: Output Mode-With Pull up Resistor



# GPIO: input Buffer: Floating Pin



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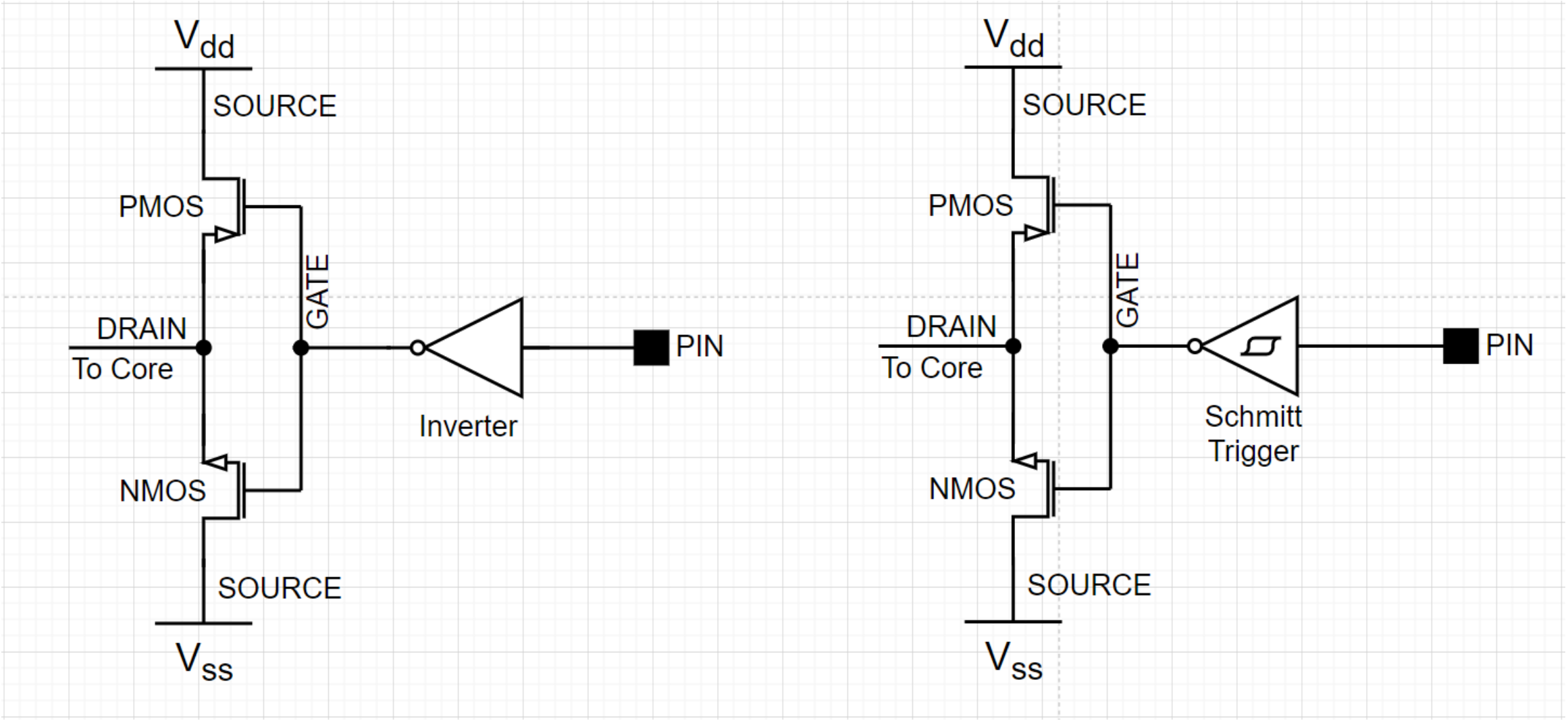
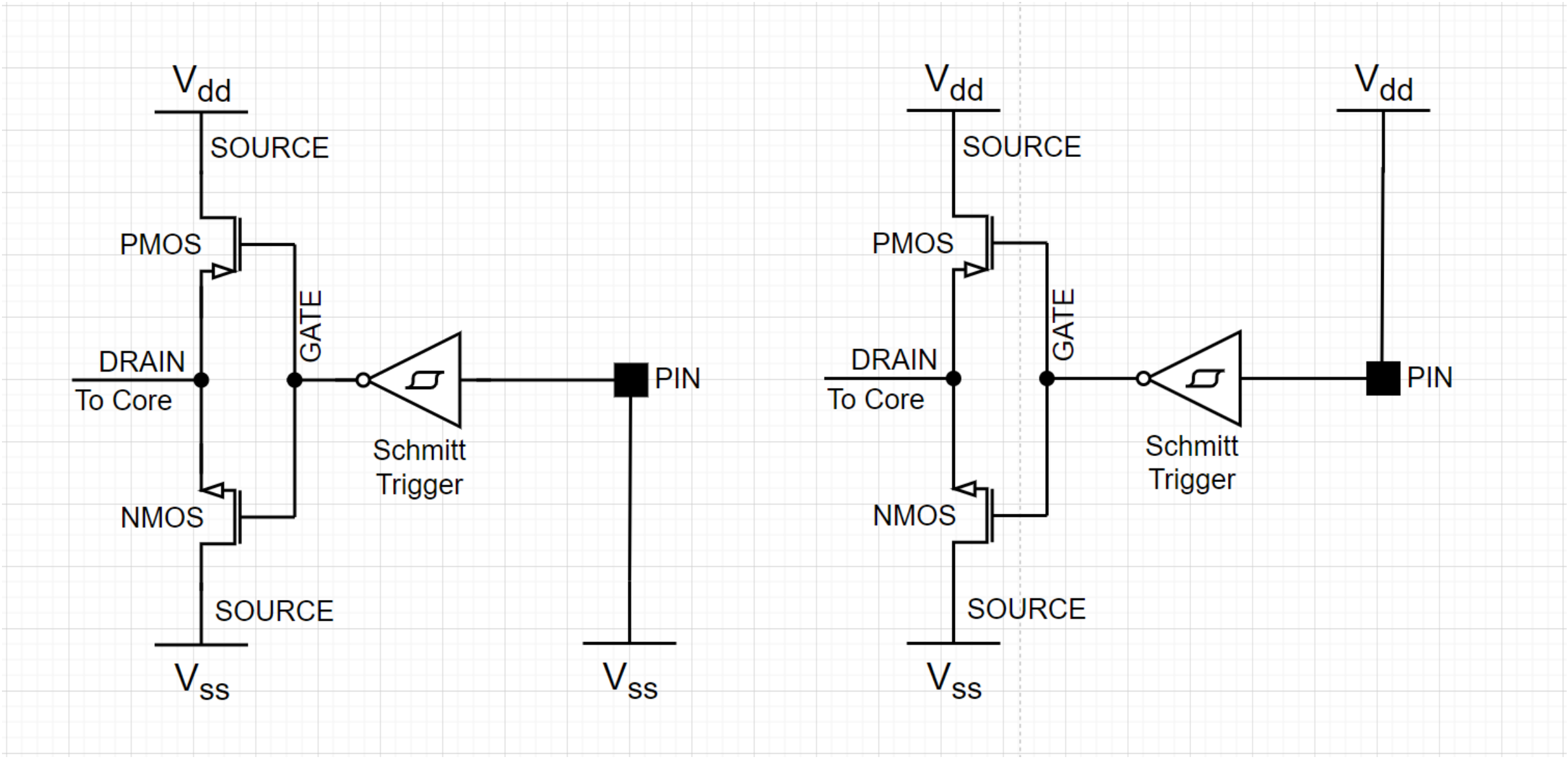
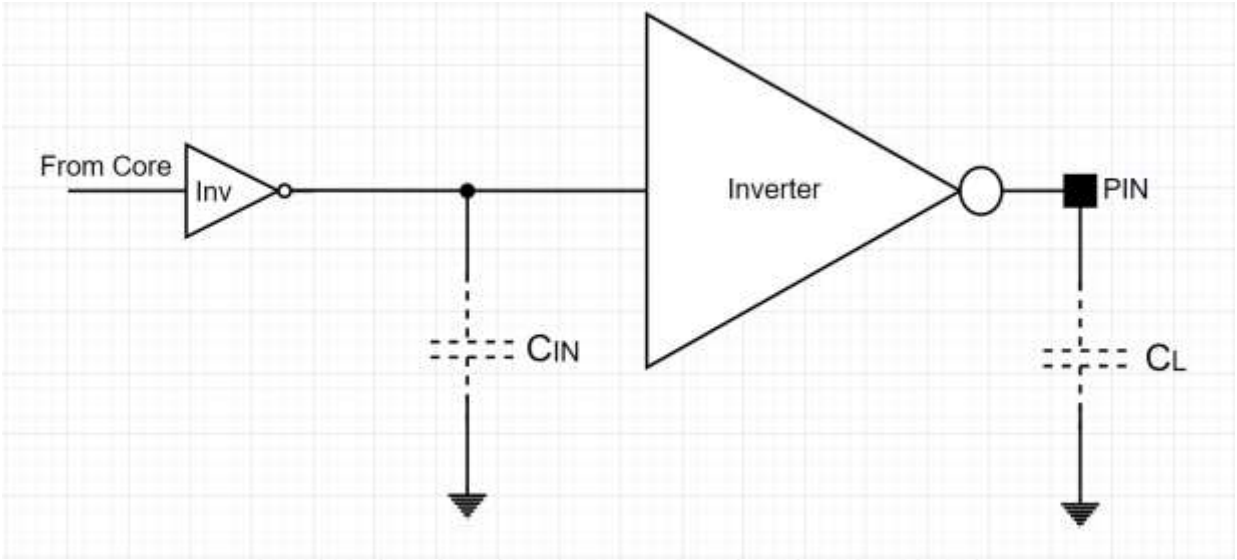
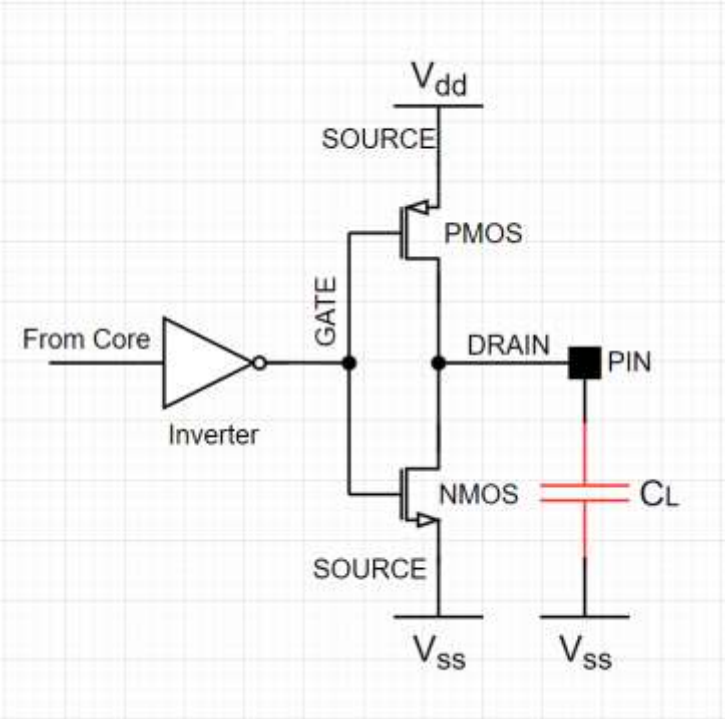


# GPIO: input Buffer: Pin Connected to Vss or Vdd



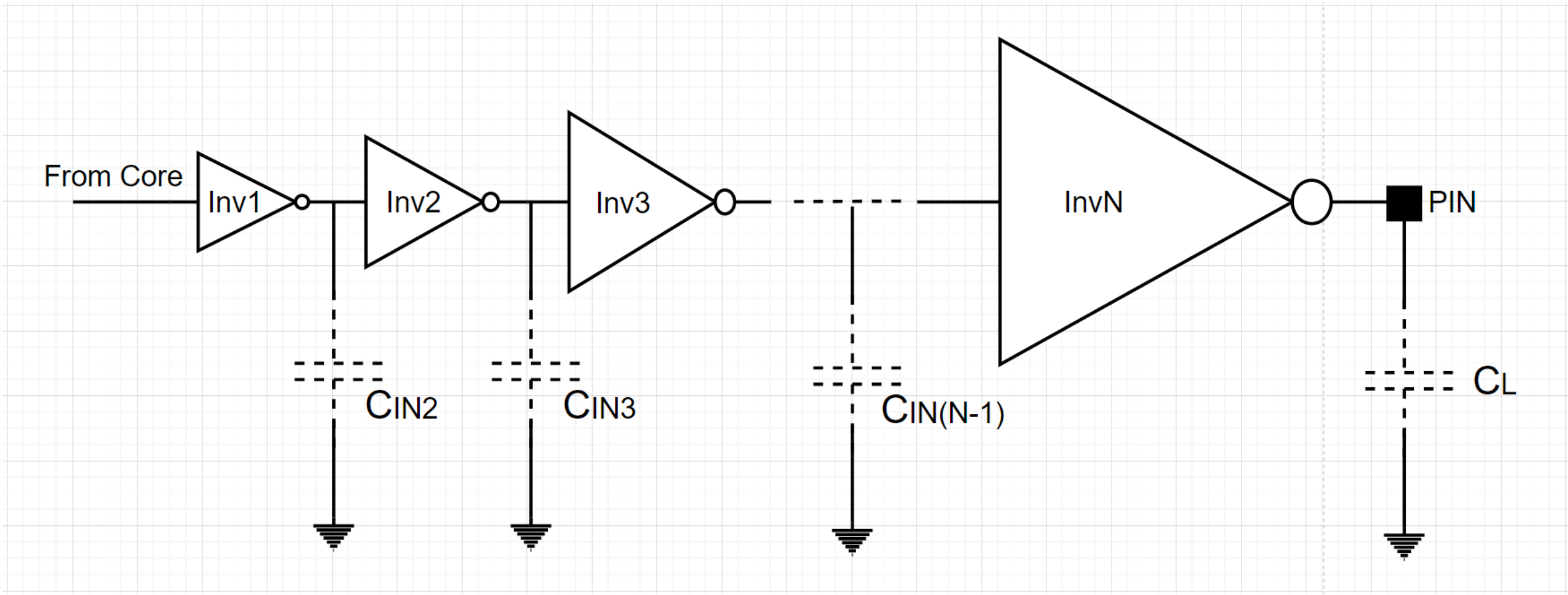
# Transmitter (TX) Driver



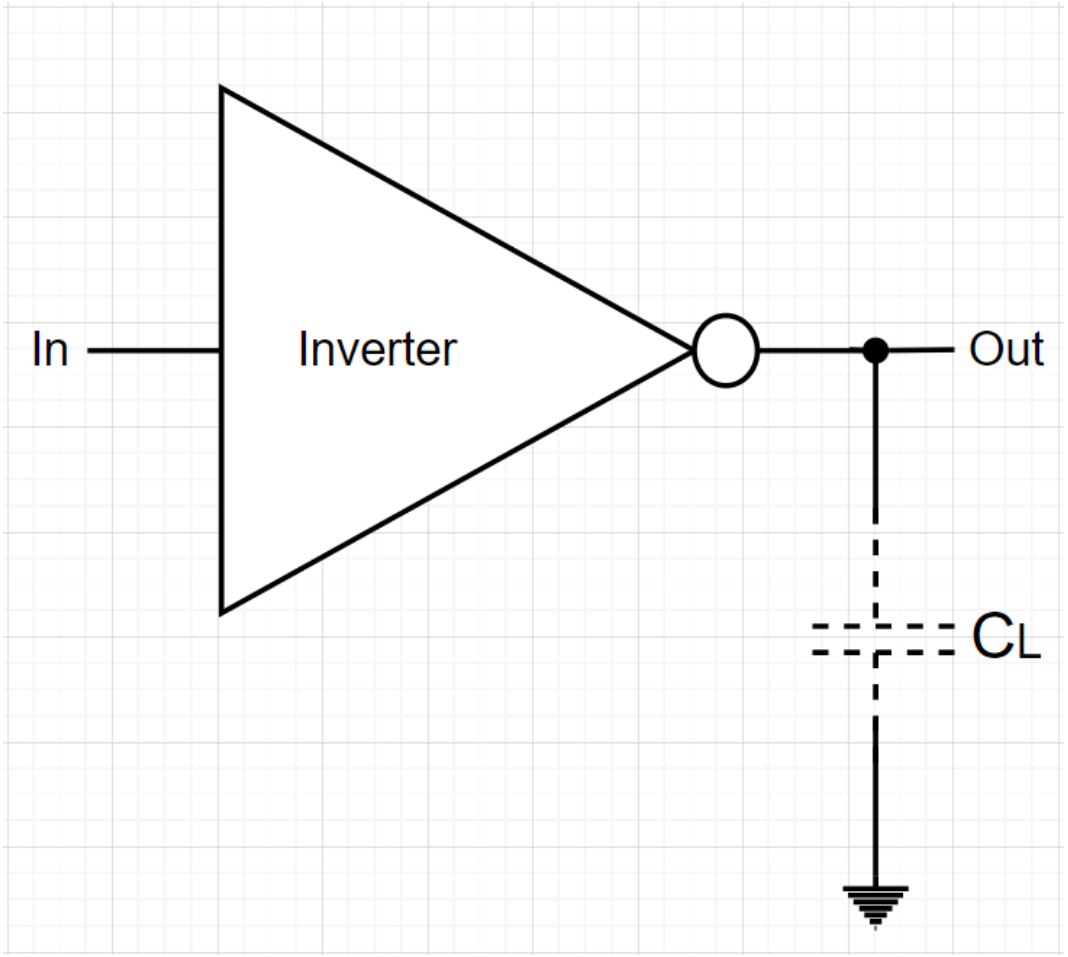




- A driver of buffer drives the output load and send signal to the output smoothly.
- As the I/O pin's physical dimension is huge compare to the core circuitry, the pin parasitic or pin capacitance is huge (10s of pF).
- To drive such a huge capacitive load a huge output current is required, which leads the output inverter size to be huge.
- The huge inverter size also creates the loading effect on the previous stage, which the degrades the signal or increases delay and not able to perform in high frequencies.
- Solution: Need Buffer chain

# Buffer Chain Design



# Sizing Inverters for Performance



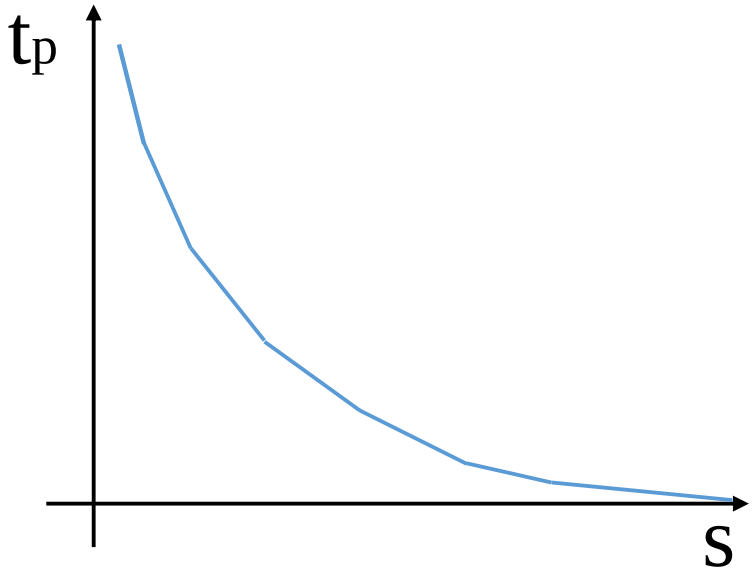

- In this analysis, we assume a symmetrical inverter, where PMOS and NMOS are sized such a way that the rise and fall delay are identical.
- $C_L = C_{int} + C_{ext}$
- $C_{int}$ represents the self-loading or intrinsic capacitance, where as $C_{ext}$ represents the external load capacitance attributable to fanout and wiring capacitance.
- Assuming that the $R_{eq}$ stands for equivalent on resistance of the gate, we can express the propagation delay as,
- $t_p = 0.69R_{eq}(C_{int} + C_{ext}) = 0.69R_{eq}C_{int}\left(1 + \frac{C_{ext}}{C_{int}}\right)$
- $t_p = t_{p0}\left(1 + \frac{C_{ext}}{C_{int}}\right)$, where $t_{p0}$ is called intrinsic or unloaded delay

# Transistor Sizes Impact The Performance

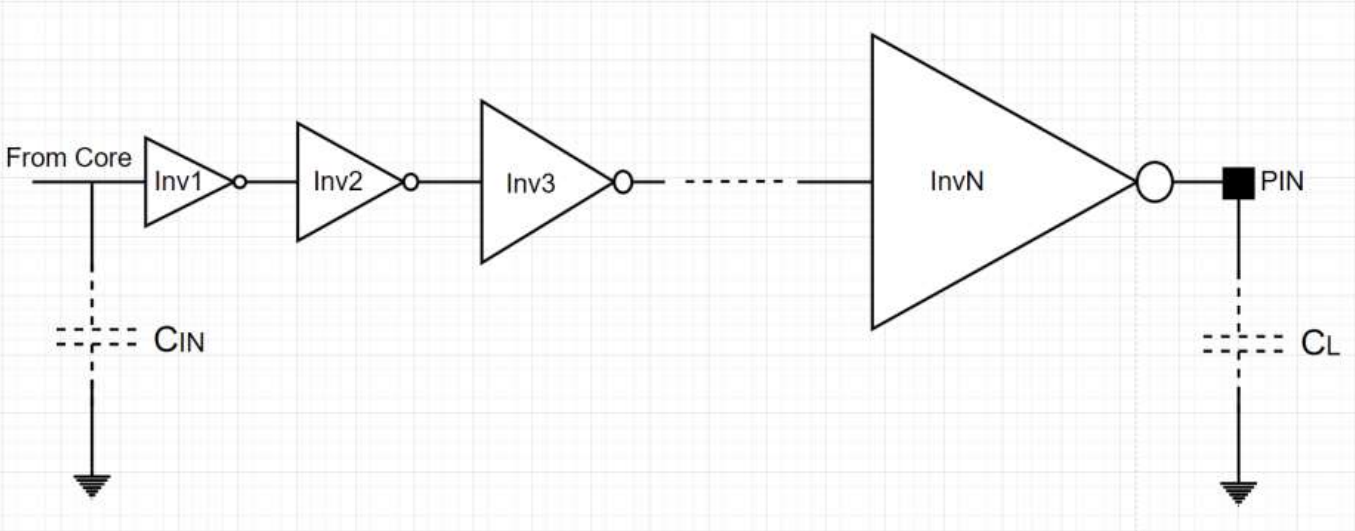
- To know how transistor sizes impact the gate performance, we must establishes the relation between the various parameters of the below equation and the sizing factor S.
  - $t_p = 0.69R_{eq}(C_{int} + C_{ext}) = 0.69R_{eq}C_{int}\left(1 + \frac{C_{ext}}{C_{int}}\right)$
- Sizing factor S relates the transistor sizes of our inverter to a reference gate- typically a minimum sized inverter.
- $C_{int} = SC_{iref}$ , where S = sizing factor and $C_{iref} = C_{int}$ of the reference gate
- $R_{eq} = \frac{R_{eq}}{S}$
- $t_p = 0.69\frac{R_{eq}}{S}SC_{iref}\left(1 + \frac{C_{ext}}{SC_{iref}}\right) = 0.69R_{eq}C_{iref}\left(1 + \frac{C_{ext}}{SC_{iref}}\right)$
- $t_p = t_{p0}\left(1 + \frac{C_{ext}}{SC_{iref}}\right)$

The above expression leads to two conclusion;

1. $t_{p0}$ is independent of inverter sizing.
2. Performance continue to increase by increasing sizing factor S.



# Sizing a Chain of Inverter




$C_{int} = \gamma C_{in}$, Where $\gamma$ is proportionality constant

$t_p = t_{p0}\left(1 + \frac{C_{ext}}{\gamma C_{in}}\right) = t_{p0}\left(1 + \frac{f}{\gamma}\right)$, where $f$ is effective fanout

The goal is the minimize the delay through the inverter chain.

- Delay expression for jth inverter stage,

$$t_{pj} = t_{p0}\left(1 + \frac{C_{in,j+1}}{\gamma C_{in,j}}\right) = t_{p0}\left(1 + \frac{f_j}{\gamma}\right)$$

- Total Delay of the chain;

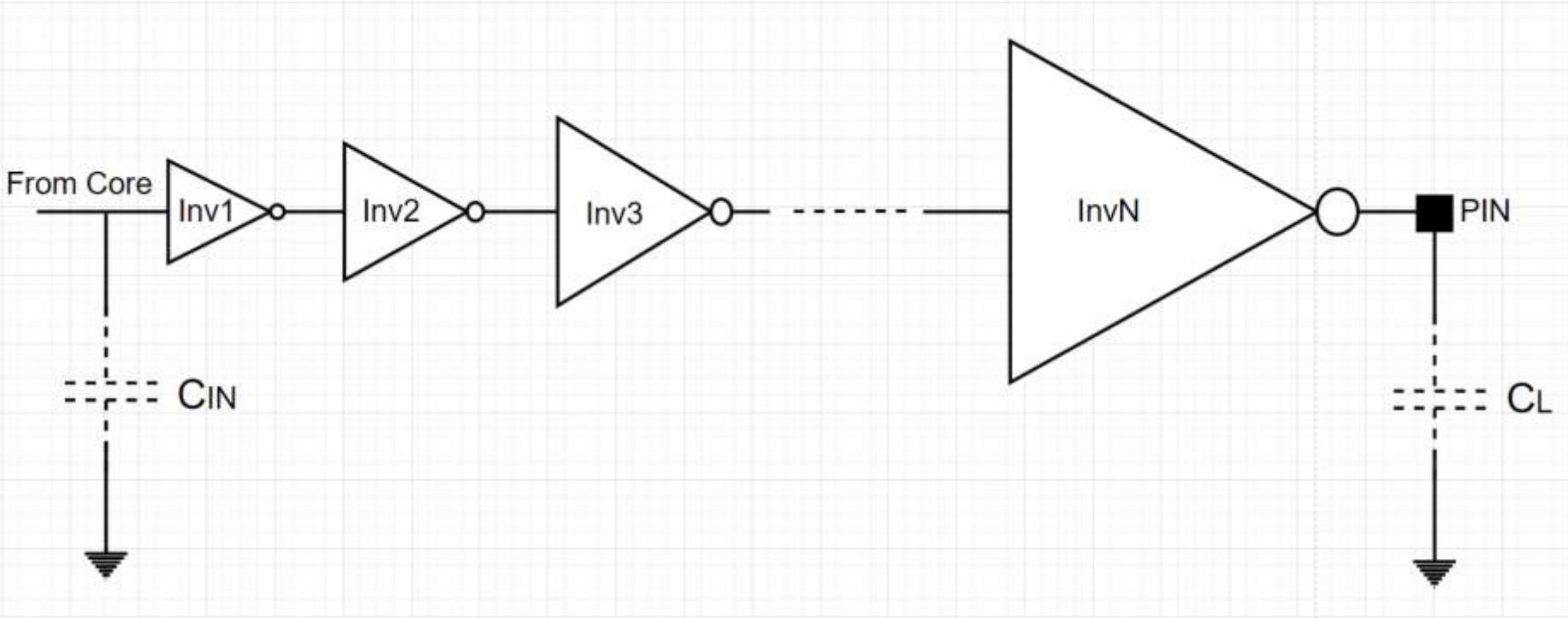
$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left\{1 + \frac{C_{in,j+1}}{\gamma C_{in,j}}\right\}$$

- The optimum size of each inverter is the geometric mean of its neighbors size;

$$C_{in,j} = \sqrt{C_{in,j-1}.\, C_{in,j+1}}$$

- This means that each inverter is sized up by the same factor $f$ with respect to the preceding gate, has the same effective fanout ($f_i = f$), hence the same delay.

# Sizing a Chain of Inverter




- With $C_{in1}$ and $C_L$ given we can derive the sizing factor;

$$f = \sqrt[N]{C_L/C_{in1}} = \sqrt[N]{F}$$

- And the minimum delay through the chain,

$t_p = Nt_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)$, where $F$ is overall effective fanout

# Choosing the Right Number of Stages

- The final $t_p$ expression reveals the trade-offs in choosing the number of stages for a given $F$ ($f^N$)

$$t_p = Nt_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)$$

- If the number of stages are too high, the first component of the expression, representing the intrinsic delay, becomes dominant.
- If the number of stages is too small, the effective fanout of each stage becomes large and the second component is dominant.
- The optimum value of N can be found by differentiating the minimum delay expression by the number of stages and setting the result to 0.

$$\frac{\partial t_p}{\partial N} = \frac{\partial}{\partial N}\left[Nt_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)\right] = 0, \qquad \Rightarrow \gamma + \left(\sqrt[N]{F}\right)\left\{1 - \frac{lnF}{N}\right\} = 0$$

- The above equation only has a close form solution for γ=0, under these simplifies condition, it is found that the optimal number of stages $N = \ln(F)$, where $F = e$=*2.71828.*
- Fanout values higher than e does not impact much on the delay but reduces number of stages. So a common practice is to select the optimum fanout of 4.

# Assignment

Design a TX Driver with the following specs

- Output Load Cap: 100pF
- Operating Frequency: 10 MHz

Design the driver, so that the delay will be minimum.

- Find the optimum number of stages,
- Fanout factor f
- Total propagation delay
- Power Consumption

# Thank You