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Broadband Microwave Amplifiers



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Foreword

Broadband microwave amplifiers are one of the key components that are employed in electronic warfare, radar, high-data-rate fiber-optic communication, and broadband instrumentation systems. The authors come from different backgrounds—industry and academia—with extensive experience in designing broadband amplifiers, as well as other microwave components and systems. They have pooled their knowledge and expertise to provide a comprehensive book that serves as an introduction to the theory, analysis, and design of this genre of amplifiers via several examples that were actually realized and characterized. This includes a step-by-step methodology from the characterization and modeling of the active devices to the design and manufacture of amplifiers. This book should be an invaluable resource to both new and experienced practitioners involved in the design of such amplifiers or the systems that employ them.

*Professor J. D. Rhodes CBE FRS FREng FIEE FIEEE
Executive Chairman of Filtronic PLC*

Preface

Microwave amplifiers designed using discrete field effect transistors (FETs) in microwave integrated circuits (MICs) or monolithic microwave integrated circuits (MMICs) are extensively used in all subsystem development for microwave wireless applications. The requirement from an amplifier design differs for different applications. For example, a wireless communications transmitter requires a radio frequency (RF) amplifier mainly to boost the power of the modulated RF signal before transmission, whereas microwave receivers require high-gain amplifiers to enhance the strength of the weak received signal without introducing any additional noise component. The configuration of microwave receivers is also highly dependent on their application. For example, communication receivers may only require narrow bandwidth ($<10\%$) but must be tunable, whereas commercial radar receivers have fixed frequency and moderate bandwidth (inversely proportional to pulse width). However, electronic warfare (EW) and optical communication systems use ultrawide bandwidths. In the case of EW systems, the ultrawide bandwidth is used to accommodate an uncertain emitter frequency, whereas in the case of fiber-optic communication systems, it enables high-data-rate communication.

This book is based on recent research work conducted by the authors dealing with broadband microwave amplifiers for EW, fiber-optic communication, and instrumentation applications. The book is unique in that it presents broadband amplifier designs through a series of design examples that were actually realized and characterized. A complete design cycle is presented, starting with the device characterization and modeling of the active devices, continuing with the modeling and optimization of the amplifier circuit, and finally culminating in the fabrication and performance measurement. Designs undertaken include the conventional broadband amplifier architectures such as the traveling wave distributed amplifier (TWDA) and feedback amplifiers, and novel broadband amplifier architectures, such as the cascaded single-stage distributed amplifier (CSSDA) and the cascaded reactively terminated single-stage distributed amplifier (CRTSSDA). Amplifier designs are provided for optimum output power and power-added efficiency performance. In addition, also included are the design, implementation, and measured performance of a novel high-dynamic-range broadband amplifier and a novel current-sharing biasing technique applied to a broadband feedback amplifier. The current-sharing biasing technique is shown to substantially reduce the current consumption by the amplifier and hence enhance its efficiency performance. The book

concludes with the design of a data modulator driver amplifier that is capable of supporting data rates of 2.5 to 20 Gbps and shows that the CSSDA architecture is amenable to MMIC technology.

Organization of This Book

Chapter 1 provides a historical perspective on the most common types of broadband amplifiers and introduces the concept of CSSDA.

In Chapter 2 the principles behind the TWDA and the novel CSSDA are discussed. In particular, the theory and a comparison between these two types of distributed amplifier architectures are presented. It is also shown how the distributed amplifier technique can be applied to other circuit functions where broadband performance is attractive, namely mixer, active circulator, multiplier, power combiner and splitter, impedance transformer, and oscillator.

Chapter 3 reviews the structure and the basic operation of gallium arsenide (GaAs) metal-semiconductor field effect transistor (MESFET), double-heterojunction pseudomorphic high-electron-mobility transistor (DPHEMT), and the single-heterojunction PHEMT (SPHEMT). The latter two devices are shown to be far more superior to the conventional GaAs MESFET device in terms of providing high-frequency performance with substantially improved gain, output power, and power-added efficiency.

Chapter 4 describes the procedure used for carrying out small-signal and large-signal device characterization, which is essential for obtaining accurate equivalent circuit device models of the active devices that are used for the design and modeling of the broadband amplifiers. The device's *hot* S-parameter data, which is obtained by biasing the devices at its nominal operating point, was used to extract the intrinsic device elements of the small-signal model. The *cold* S-parameter data of the device is obtained by biasing the device at pinch-off. This data was used to derive the extrinsic device elements of the small-signal model.

To analyze the power performance of the broadband amplifier, scattering parameters alone are insufficient because under large RF drive, a transistor exhibits considerable nonlinear behavior in C_{gs} , g_m , C_{gd} , and R_{ds} . Hence, in order to analyze the large-signal performance of the broadband amplifier, it was necessary to derive the device's large-signal model from the pulsed direct current (dc) I_{ds} - V_{ds} and I_{ds} - V_{gs} measurements. The latter measurements eliminate the dispersion effects that are shown to be very significant in the static dc I_{ds} - V_{ds} measurements.

This chapter also describes the procedure for accurately extracting the device's small-signal and large-signal equivalent circuits from the device's S-parameter and pulsed dc I - V measured data. The method used to determine the component values of the small-signal equivalent circuit is based on the process of calculating the extrinsic and intrinsic component values from two sets of S-parameter measurements. The small-signal equivalent circuit is generated using these component values, and is optimized using computer-aided design (CAD) tools. This analytical method that is

employed is far more elegant than of the conventional numerical optimization method, which requires the small-signal model to be “fitted” to a large number of measured S-parameter data at various bias settings. One of the main problems of the latter method is the determination of the starting component values for the optimization procedure. Depending on these starting values, the final values may be very different, even with low error functions, and this can result in component values that lack any physical meaning, thus leading to an inaccurate device model.

Large-signal device models are critical for accurately modeling and analyzing the broadband amplifier design for output power and power-added efficiency performance. The merits of deriving the large-signal model from the device process information and the empirical method is discussed. A semiempirical method, which is a compromise between the analytical and empirical methods, is shown to provide an accurate large-signal model, as no assumptions are referenced to the physical operation of the device and it uses the measured data of the device. The chapter also reviews the different methods of nonlinear analysis and large-signal modeling techniques. The optimum large-signal model of the devices employed was derived by “fitting” the pulsed dc I_{ds} - V_{ds} and I_{ds} - V_{gs} measured data to the theoretically predicted I_{ds} - V_{ds} and I_{ds} - V_{gs} characteristics of the large-signal models available in CAD tools.

Chapter 5 provides general analyses on the different classes of amplifier operation for broadband applications to provide an insight into how a particular class of operation may affect the amplifier’s performance in terms of power-added efficiency.

Chapter 6 describes the design, analysis, fabrication, and measured performance of different types of broadband amplifiers operating across the frequency range of 2 to 18 GHz. All of the amplifiers were fabricated using hybrid MIC technology. The amplifiers were fabricated on a high dielectric constant Alumina substrate, and all of the active devices were embedded into the circuit using chip and wire technology. The broadband amplifiers investigated include the conventional traveling wave amplifier, the feedback amplifier, novel CRTSSDAs, and a novel high-dynamic-range broadband amplifier. Finally, a novel current-sharing biasing technique is demonstrated on a feedback amplifier, which is shown to exhibit a substantial improvement in efficiency and a 50% reduction in current consumption by the amplifier.

Chapter 7 covers the practical aspects of the realization of the broadband amplifier designs in Chapter 6. The fabrication of the broadband amplifiers is implemented using the hybrid MIC technology. The active devices were mounted onto gold-plated posts, and the inductance associated with the posts was derived by the technique of shunt mounting a chip capacitor. The purpose of deriving the post inductance is to ensure that it is of a relatively small magnitude, as a large value could result in high-source inductance, which could induce instability in the active device. The inductance of the post is included in the amplifiers model to provide an accurate analysis. The characterization of the broadband chip capacitors is also presented. These capacitors are employed as dc blocks and for power supply decoupling. It is also shown how the RF choke inductance is realized, which is used for dc

biasing of the broadband amplifiers. These coils were designed to provide low insertion loss and no inband resonances. Finally, the fabrication of the test carriers, amplifier housings, and test jigs are presented. The material selected for the test carriers and amplifier housings is thermally matched to the Alumina substrate.

Chapter 8 describes the design of ultrabroadband microwave amplifiers for data modulator drivers.

Finally, Appendix A provides relevant artificial transmission line theory related to distributed amplifiers. A List of Acronyms and a List of Symbols are also included.

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Overview of Broadband Amplifiers

1.1 Historical Perspective on Microwave Amplifiers

The interest in microwave techniques for communication systems has grown immensely over recent years, and the performance of microwave active and passive circuits for wireless systems technology has become extremely advanced. One of the most critical active circuits employed in systems applications is the microwave amplifier. Because it is a highly versatile circuit function, it has always been the first to benefit from developments in the device and semiconductor technologies. Amplifiers with extremely wide bandwidths with good performance have been successfully realized in the past 2 decades in hybrid and monolithic technologies. Hence, the subject of amplifiers has been firmly established in the fields of microwave, optical communication, instrumentation, and EW.

It was from approximately the late nineteenth century to as early as 1930 that communication systems were severely limited due to the shortage of technology and sources for invention. During this spell, the triode electronic valve (tube) was used to develop amplifier and oscillator modules that were associated with very limited applications and were mainly used for civil purposes. Many experiments were conducted for radio communication; among the experimenters was A. G. Clavier, who successfully set up a radio link across the channel between England and France in 1931 [1]. Since then, the amplifier became the arena of active research carried out by many researchers. Their primary aim was to improve the performance of its gain-bandwidth product, but this was not possible because the technology was constrained at that time by the electronic valve.

This problem was extensively investigated by W. S. Percival [2], in 1935, who found that gain-bandwidth product is greatly affected by the capacitance and transconductance of the conventional electronic valve. In 1936, Percival elaborated discussion on a new type of electronic-discharge (thermionic) valve, with one or more of its electrodes made in the form of a spiral coil. This coil and the interelectrode capacitance form a distributed transmission system; therefore, he was the first to propose the idea of distributed amplification. This work was patented at that time in July 1936 under British Patent Number 460562. His publication states that if a system is terminated with appropriate characteristic impedance, a signal can propagate through the electrode and finally be absorbed by the termination line impedance. This discussion was then delineated on two-stage distributed

amplifiers using the thermionic valves (consisting of six screen grid vacuum tubes) [2]. The idea was based on separating the input and output capacitances of a series thermionic valve from their transconductance and thereby overcoming the problem of constraining the gain-bandwidth product associated with the earlier narrow bandwidth amplifiers. This is achieved by means of absorbing the input and output capacitances into artificial transmission lines, so that the distributed amplifier would behave as a low-pass filter with bandwidth set by the cut-off frequency of the input and output lines.

The potential of Percival's work was not fully appreciated until a decade later, when his idea of the distributed amplifier was further investigated and developed by Ginzton [3] and Horton [4]. They managed to realize the distributed amplifier and achieved good practical results. This area of amplifier work later became highly topical for active research, resulting in more activities and discussion on the distributed amplifier. Consequently, a number of publications and scientific articles appeared on different applications such as television broadcasting, radar systems, networking, and EW applications [1].

A spectacular technological maturity was established in the early 1960s by transferring the tube-valve technology to the junction transistor technology. Since then, the development of distributed amplification techniques has increased rapidly. For broadband amplifier technologies, new methods and techniques for broadband matching were established [5, 6]. Other types of amplifier designs in general also improved due to the advent of semiconductor diodes and transistors. Also different amplifiers (e.g., the varactor parametric amplifiers [7, 8], balanced transistor amplifier [9], traveling wave amplifier [10], and MESFET distributed amplifier [11]) could now be realized in hybrid technology.

Between 1970 and 1980, advanced GaAs FET and MESFET technologies were heavily involved in the design of hybrid microwave amplifiers and circuits [12, 13]. Later, broadband designs for preamplifiers for small signals [14, 15] and medium power amplifier for larger signals were developed [16, 17].

In the early 1980s, the technology of distributed amplification was markedly improved using advanced technologies based on MMICs, which are still currently widely applied in a wide range of applications. At that time, Archer at Siemens [18] realized hybrid GaAs FET distributed amplifiers that had gains of 12 dB, input and output return loss better than 10 dB, and noise figures of 3 to 6 dB over a bandwidth of 0.1 to 6 GHz. For the first time, a monolithic GaAs FET four-stage traveling-wave amplifier with a gain of 8.5 dB 1 dB over a bandwidth of 0.5 to 14 GHz and good input and output return losses was realized by Ayasli at Raytheon [19]. Since then, the design considerations for monolithic microwave integrated circuits based on silicon and GaAs technologies have been seriously considered as viable candidates for satellite communication, airborne radar, EW, and other applications. The properties of silicon and semi-insulating GaAs MMICs show low loss, improved reliability, small size and weight, multioctave broadband performance, circuit design flexibility, and multifunction performance on single chip transceivers. The MMICs continue to play a prominent role in improving communication systems in general, and

this is accomplished with the aid of CAD techniques [20]. In the following sections, various types of broadband amplifiers are reviewed.

1.2 Broadband Amplifiers

Broadband systems have traditionally employed TWDA, as they have been extensively investigated and firmly established as being reliable and robust devices that can be realized in MIC and MMIC technologies. This device has become very popular due to its excellent bandwidth performance. This is possible because the input and output capacitances of the active devices are absorbed in the distributed structures [21]. The resulting amplifier also exhibits very low sensitivities in process variations when realized in MMIC technology and is relatively easy to design and simulate [22].

The gain performance of a single-stage traveling wave amplifier comprising of two MESFET devices is limited to 8 to 9 dB. This is due to the gate and drain line attenuation that limits the number of FET devices in a distributed amplifier configuration. In other words, there are a certain number of devices that maximizes the gain per FET used. The limitation on the number of devices at high frequencies is mainly due to the attenuation on the gate line. The attenuation on the lines also reduces the bandwidth with an increase in the number of FETs. In practice, it is possible to improve the efficiency and power output of a distributed amplifier by tapering the drain line impedance from section to section. Impedance tapering forces the backward traveling current to zero at the termination, thus forcing all of the developed current from each FET to propagate in the forward direction only. In order to realize high gain amplifiers, a number of the single-stage traveling wave amplifiers have to be cascaded together. The major deficiencies of the latter technique, however, are those of higher manufacturing cost and a substantial reduction in the amplifier power-added efficiency (i.e., typically 7% to 14%). The improvement in efficiency demands is primarily driven by the next generation of multioctave systems, such as high-data-rate fiber-optic links and EW, which require considerably lower power dissipation. Such systems have very stringent requirements from broadband amplifiers in terms of the following attributes: high stability, high gain, high output power, and high power-added efficiency. Moreover, these amplifier designs in practice are also required to meet the high production yield and reproducibility targets necessary to minimize manufacturing cost.

1.3 Review of Various Broadband Amplifiers

Recently there has been considerable emphasis placed on the realization of solid-state power amplifiers at the L-band with power-added efficiency performance of 60% to 80% operating over bandwidths of 500 MHz. The improvement in power-added efficiency has resulted from the development of state-of-the-art DPHEMT

devices and novel efficiency-enhancing circuit concepts [23, 24]. In comparison with the narrowband power amplifier, the broadband power amplifier's power-added efficiency performance is substantially lower, typically in the range of 8% to 19%. This is because the emphasis placed on the design of such amplifiers has been achieving a maximum output power over the desired multioctave bandwidth, which comes at the expense of efficiency performance.

The most popular and well-established circuit techniques employed in the design of broadband amplifiers that are realized in hybrid and monolithic technologies are:

- Reactively matched circuit;
- Traveling wave distributed circuit;
- Feedback circuit;
- Lossy matched circuit.

The concept of cascading single-stage distributed amplifiers [25] presented in Chapters 2 and 6 has evolved to overcome the deficiencies in the TWDA's performance.

1.3.1 Reactively Matched Amplifiers

The reactively matched amplifier, shown in Figure 1.1, is also termed as the lossless matched amplifier due to the reactively matched input and output circuits. The matching circuits are used to accomplish gain compensation (i.e., to flatten the FET's gain roll off) by selectively creating reflections between the matching network and the active device. Because the matching networks are composed exclusively of reactive elements, the maximum gain, minimum noise figure, and maximum power output can be achieved for a given FET with a properly designed matching network. In practice, maximum gain can be achieved by optimizing the input matching circuit, and the output matching circuit can be optimized to achieve maximum output power and hence power-added efficiency. The disadvantage of this type of amplifier is its relatively poor impedance match, because although the lossless matching circuits provide the desired match over a narrow band of frequencies, the matching at other frequencies is degraded. This can be improved by employing isolators in the case of a single-ended design or hybrid couplers as combiners and dividers in the case of balanced amplifiers. In the single-ended case, this will result in extra cost and

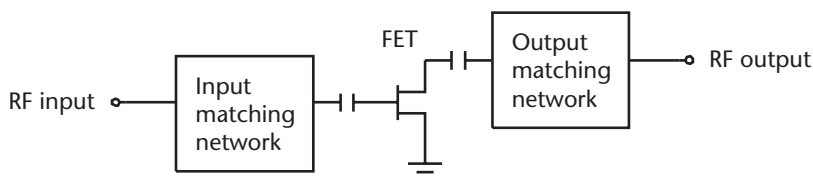


Figure 1.1 Reactively matched amplifier configuration.

an increase in the overall size of the amplifier module. The balanced-amplifier approach results in an increase in output power of 3 dB; however, this comes at expense of double the dc power consumption.

Tserng, et al. [26], reported the first reactively matched 2- to 18-GHz power amplifier employing GaAs MESFET devices. The amplifier was designed using wideband impedance transformers realized in MIC, and it achieved average power-added efficiency in the range of 8% to 15% with an output power of 23 dBm. The main deficiency of this amplifier design was that the terminal voltage standing wave ratios (VSWRs) were very poor under small-signal conditions. Palmer, et al. [27], produced the first reactively matched MMIC multioctave power amplifier operating over the frequency range of 6 to 18 GHz. The amplifier achieved an output power of 27 dBm with an average power-added efficiency of 19%. This was a two-stage amplifier employing a driver stage and an output stage, which had two power devices connected in a parallel configuration in order to decrease the source inductance and to diffuse heat concentration in the devices.

The design of amplifiers capable of high output powers require FET devices with large gate peripheries that enable high channel current densities to be achieved from the FETs. Unfortunately, a large gate width simply increases the device's parasitics, especially the gate-source capacitance and the gate resistance. Although it is possible to decrease the gate resistance by changing the geometry of the FET, the gate resistance of a FET usually cannot be reduced in proportion to the increase in gate width, so gain decreases as gate width increases; consequently, power FETs usually have relatively low gain. It was found that the size of the GaAs MESFETs could not be increased indefinitely because of crosstalk, phasing, and stability problems. In an effort to minimize these effects, designers have developed divider/combiner circuits [28]. Other designs use the *cluster cell matching* concept, where input matching is achieved at the level of the individual *cell clusters*, which are then partially matched at their outputs prior to combining via quarter wavelength lines [29]. The operating bandwidth of the latter circuits is limited to an octave.

1.3.2 TWDAs

The traveling wave concept has been well researched and established, hence it is immensely popular in the design of amplifiers operating across multioctave bandwidths. In a GaAs MESFET distributed amplifier, the input and output lines are two transmission lines with a number of GaAs MESFETs connected between them, as shown in Figure 1.2. The gate and drain impedance of the MESFETs is absorbed into the lossy artificial transmission lines formed by using lumped inductors that are terminated into a characteristic impedance. As the signal travels down the gate line, each transistor is excited by the traveling voltage wave and transfers the signal to the drain line through its transconductance. The signals on the drain line add in the forward direction as they arrive at the output. The waves traveling in the reverse direction are not in phase, and any uncanceled signal is absorbed by the drain-line termination. As a result, the characteristic impedance tends to provide a constant

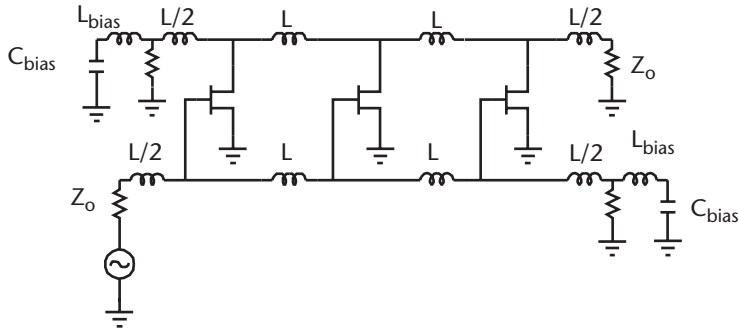


Figure 1.2 TWDA configuration.

input and output resistance, thus achieving a very wide bandwidth (e.g., 2 to 18 GHz) performance. This type of amplifier eases the difficulties associated with broadband matching of the FET input and output impedances, as the input and output capacitances of the FETs are absorbed into the input gate and output drain transmission lines, respectively. The major application of this type of amplifier has been in EW, radar, and broadband communication systems, as well as in measurement instrumentation. The main advantages of the amplifier are its very wide bandwidth and inherent circuit stability characteristics. The major disadvantages of the amplifier are its relatively poor output power and therefore low power-added efficiency performance, in addition to the need for multiple active devices in its implementation, which results in increased complexity and manufacturing cost.

The distributed amplifier employing solid-state GaAs MESFET devices was first investigated by Moser in 1967 [30] and by Jutzi in 1969 [31]. They realized an amplifier that used hybrid lumped element circuit technology and demonstrated its potential for providing a relatively high gain bandwidth product. In 1982, the first 1- to 13-GHz monolithic traveling wave amplifier was presented by Ayasli, et al. [32]. In the following year a practical design approach for both lumped element and transmission line element traveling wave amplifiers was formalized by Niclas, et al. [33]. It was later that the expressions for the gain and bandwidth of the distributed amplifier in terms of the input and output propagation constant and the cut-off frequency were developed by Beyer, et al. [34].

Ayasli, et al. [22], reported 2- to 20-GHz decade band amplification with 30-dB gain with GaAs FETs in monolithic form. He also investigated the power-limiting mechanisms in a GaAs FET traveling wave amplifier and described a circuit approach that decreases the effect of some of these limiting mechanisms [21]. He basically used two traveling wave amplifiers that had a common drain line. The input power was split into the two gate lines, each employing four 150- μm FETs, using a Wilkinson divider. The FETs excited from the two gate lines are combined on the single drain line, effectively giving four 300- μm drain periphery. Thus, the total gate periphery is doubled without affecting the loading on the gate lines. Also, the load line impedance is halved, as there is twice the drain periphery on the output

line. Because gain per stage is not significantly affected, the efficiency of the amplifier is effectively doubled. This amplifier produced 0.25 W of output power across 2 to 20 GHz with power-added efficiencies in the range of 7% to 14%.

Kim and Tserng [35] described a novel concept of reducing the gate line losses by using series capacitors with the GaAs MESFET devices. Their concept was to increase the gate periphery of the GaAs MESFET devices, resulting in an increased broadband output power performance. An output power of 0.5 W was achieved with 4-dB small-signal gain over 2- to 21-GHz bandwidth. The average power-added efficiency achieved across the bandwidth was approximately 7%.

Prasad, et al. [36], described the quantitative procedures for the design of GaAs MESFET distributed amplifiers using series capacitors in the device gate circuits. They showed that the choice of series capacitors allows the designer to trade gain for bandwidth while maintaining a given gain-bandwidth product. It was also shown that the input power capability could be increased by the use of series capacitors when the device pinch-off is the power-limiting factor. Furthermore, they also showed how the addition of series capacitors enables the gate periphery of an amplifier to be increased, which results in an increase in power-bandwidth product. Ayasli, et al. [37], followed a similar concept where they *capacitively coupled* the individual GaAs MESFETs to the gate input line through discrete series capacitors. One watt of output power was achieved over 2 to 8 GHz with power-added efficiency in the range of 5% to 7%.

Paoloni, et al. [38], describe an innovative topology of a distributed amplifier based on input and output broadband Lange couplers. The modified operation mechanism of the new configuration, in comparison with the conventional distributed amplifier, establishes a remarkable improvement of the output power, power-added efficiency, and small-signal gain. The performance of a 2- to 18-GHz conventional distributed amplifier is presented with power-added efficiency in the range of 8% to 15%. The newly configured amplifier design achieves power-added efficiency in the range of 13% to 19%, which is a significant improvement when compared with the conventional distributed amplifier case.

Shapiro, et al. [39], have described a novel traveling wave power amplifier topology, which employs power-combining techniques. Conventional distributed amplification techniques have allowed for high gain and bandwidth to be achieved at the expense of low efficiency. The decreased efficiency is primarily due to the existence of an actively loaded artificial transmission line at the output, resulting in backward wave propagation. Using the same traditional input line distributed techniques to achieve high bandwidth, their research explored the use of a delay line, including a combining output topology, to improve the efficiency at large signal by eliminating the backward waves. A broadband output combiner transforms the amplifier load impedance to that of an optimum load for each device, thus realizing a traveling wave power amplifier. The novel amplifier, designed to operate over the frequency range of 1 to 9 GHz, achieves an efficiency of 25% across the entire bandwidth. The conventional traveling wave amplifier, however, achieves 5% to 10% across the same bandwidth.

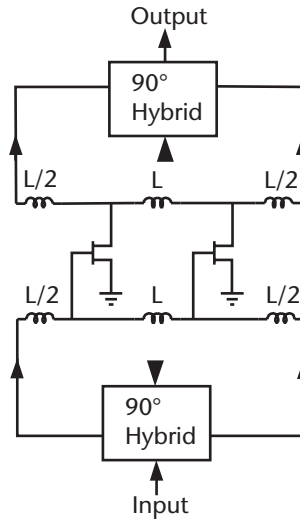


Figure 1.3 The dual-fed distributed amplifier.

Aitchison, et al. [40, 41], proposed a novel amplifier based on the TWDA, which they referred to as a dual-fed distributed amplifier. This was because the input signal is fed to both ends of the gate line by means of a hybrid coupler. In addition, because superposition applies, the benefit of gain is obtained in both directions. Both amplified signals are collected by means of a second hybrid, as illustrated in Figure 1.3. The use of a 90° hybrid results in forward and reverse gain benefit being obtained at the output port so that there is a 6-dB increase in gain above that obtained from the same amplifier circuit used unidirectionally. This benefit is obtained up to at least half of the cut-off frequency. Thus, 6 dB of gain is obtained from only two FETs. In addition, the input power for 1-dB compression is increased by 3 dB, and hence the 1-dB gain compression power is 3 dB higher than for the corresponding unidirectional amplifier. Measurements also show that a carrier to third-order intermodulation product ratio (C/I) of 25 dB can be achieved with an input power back off of 9 dB for conventional power distributed amplifier, while the corresponding figure for the dual-fed distributed amplifier is 6 dB, an improvement of 3 dB. There is also a noise figure improvement of about 2 dB, which diminishes with increase in frequency.

More recently ultrabroadband traveling wave amplifiers operating at up to 180 GHz have been realized by Agarwal, et al. [42]. This amplifier exhibited a gain of 5 dB across the 180-GHz bandwidth. Agarwal and his team also reported traveling wave amplifiers having 1- to 112-GHz bandwidth with 7-dB gain, and 1- to 157-GHz bandwidth with 5-dB gain. All of these amplifiers were fabricated using a $0.1\text{-}\mu\text{m}$ gate length InGaAs/InAlAs HEMT MMIC technology.

1.3.3 Broadband Feedback and Lossy Matched Amplifiers

The amplification of microwave signals employing amplifiers, which only require a single device to achieve the multioctave bandwidth, was proposed by Niclas, et al.

[43, 44]. These amplifiers are defined as the *feedback* and *lossy matched*. The feedback amplifier, shown in Figure 1.4, employs shunt feedback between the gate and drain of the active device used in the circuit. The major advantages of the feedback amplifier are:

- The circuit is less complex compared with the reactively matched and traveling wave amplifier circuits and therefore is easier to realize.
- The amplifier can provide higher power-added efficiency performance when compared with the conventional traveling wave amplifiers.
- The amplifier offers a cost-effective multioctave bandwidth amplifier design.
- It has excellent performance in achieving flat gain and unconditional stability, and it provides very good input and output match.
- The amplifier can be realized in hybrid MIC and MMIC circuit technologies.
- It provides lower distortion and sensitivity to active device variations.

The main disadvantage of this type of amplifier is the erosion of the its output power and noise figure over the lower end of the frequency band due to loss associated with the feedback resistor.

The feedback path consists of three elements (i.e., resistor R_{fb} , inductor L_{fb} , and the capacitor C_{fb}). The value of the feedback resistor R_{fb} controls the gain and bandwidth of the amplifier. The gate inductance L_g , the drain inductance L_d , and the feedback inductance L_{fb} can be optimized to extend the amplifier's bandwidth [43]. The feedback inductance L_{fb} reduces the effectiveness of the negative feedback with increasing frequency. The drain inductance L_d is selected to compensate for the intrinsic drain-source capacitance of the device up to the cut-off frequency. The dc block capacitor C_{fb} is used to isolate the gate from the drain bias supply. The capacitor C_{fb} and bias inductors $L1$ and $L2$ also determine the amplifier's bandwidth performance, which has to be resonance free across the desired bandwidth. The feedback amplifier can be very sensitive to frequency when implemented in hybrid technology; hence, its implementation dominates in MMIC technology.

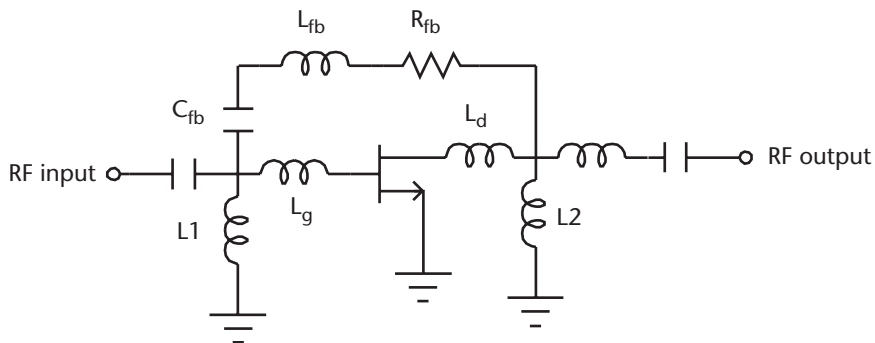


Figure 1.4 Feedback amplifier configuration.

The lossy matched amplifier employs resistors $R1$ and $R2$ at the input and output matching circuits, respectively, as illustrated in Figure 1.5. These resistors are used to provide gain equalization (i.e., flat gain response) by introducing high attenuation at low frequencies and low attenuation at high frequencies, while maintaining a good input and output match over the desired broad bandwidth. This fact makes the amplifier suitable for cascading without the need for isolators to improve interstage matching, as is the case for the reactively matched amplifier. Therefore, they are relatively smaller and have lower power consumption. The amplifiers provide broad bandwidth performance at the expense of low gain, low output power, high noise figure, and poor power-added efficiency [43]. This is mainly due to losses in the resistors, which are used in the input/output matching and interstage networks.

1.3.4 CSSDAs

Although the TWDA has the desirable attributes of flat gain and good terminal match over a wide frequency range, it is deficient in terms of gain and output power, and it requires multiple devices leading to a relatively large gain module. These drawbacks stimulated work for improving the design of conventional distributed amplifiers in terms of realizing a more compact circuit using fewer devices to produce high levels of gain. Minnis [45] described for the first time the principles of cascable amplifiers. His simulation results indicate that the single-stage distributed amplifier employing $800\text{-}\mu\text{m}$ FET is capable of delivering a 6-dB gain over 7 to 14 GHz and occupies less than 1 mm^2 of GaAs. Later in the same year, Moazzam and Aitchison [40] described a single-stage distributed amplifier that is based on the dual-fed distributed amplifier. Figure 1.6 illustrates this amplifier. In this configuration, the input and output line idle ports are reactively terminated, which results in a significant improvement in gain and power-added efficiency over that available from a conventional TWDA and dual-fed distributed amplifier. The signal at the input port travels down the gate line and is reflected at the open circuit so that the gate voltage is double the input voltage. Similarly, the output current in the drain line load is due to current reflected from the drain open circuit as well as the direct drain current. Moazzam and Aitchison theoretically analyzed this configuration, and their simulation results show that the single-stage distributed amplifier with open-circuited terminations have a relative flat gain response of 9.5 dB up to 5 GHz beyond which it gradually diminishes. The gain response is approximately the same up to 5 GHz for a four-stage conventional distributed amplifier. The power-added

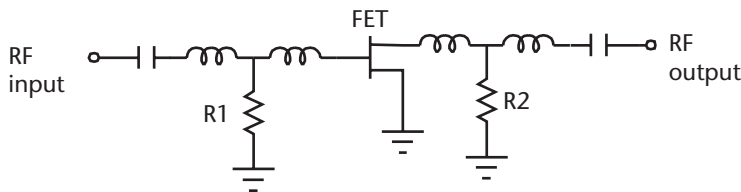


Figure 1.5 Lossy matched amplifier configuration.

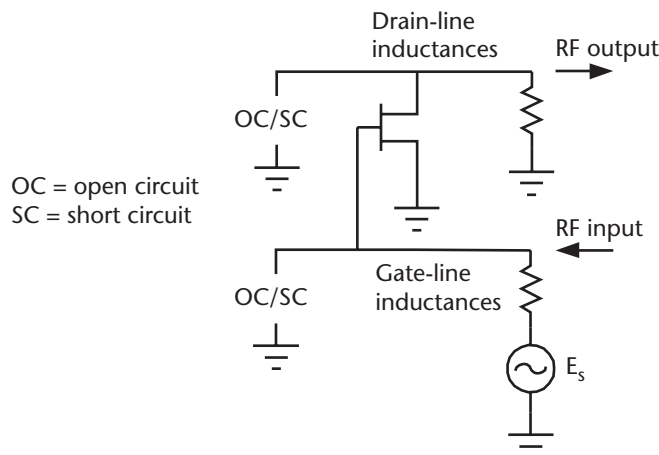


Figure 1.6 Single-ended dual-fed distributed amplifier.

efficiency of the single-stage distributed amplifier is more than quadrupled in comparison with that of the four-stage distributed amplifier. But, using short-circuited terminations in the single-stage distributed amplifier results in a bandpass-like gain response with a maximum gain occurring at its center. This gain response can be shifted from one end of the band to the other by changing the phase of the reflecting terminations (e.g., by terminating the idle ports with inductors or capacitors). The drawback of the single-stage distributed amplifier is its poor input and output match, and its 3-dB bandwidth is approximately half that of a conventional distributed amplifier.

Figure 1.7 shows how the single-stage distributed amplifier, with some modification, can be used as a tunable oscillator [40]. The output of the amplifier is connected to the input through a length of line to provide an appropriate phase change of 180° at the required frequency of oscillation. The frequency of oscillation is tunable over a broad bandwidth by means of adjusting the terminating reactances.

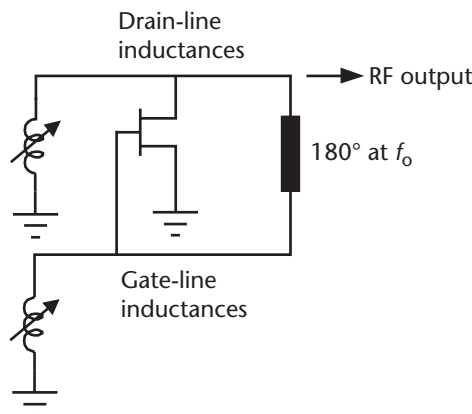


Figure 1.7 Single-ended dual-fed distributed amplifier used as a tunable oscillator.

Liang and Aitchison [46] extended the concept of a single-stage distributed amplifier by transforming the configuration into a cascade of n single-stage distributed amplifiers (n -stage CSSDA), where n is the number of devices, as is illustrated in Figure 1.8. In this configuration, the idle drain/gate termination is omitted for stages other than the first and last. With no idle drain/gate termination, the voltage swing across the input gate of the active device is increased, which consequently enhances the amplifier's gain. A series feedback is included in the amplifier configuration as an external inductance added to the source terminal of the FET at each stage. In this configuration, the input signal power is coupled and amplified via the transconductance of the FETs, and it emerges from the drain line. The simulation results of this amplifier show that a cascade of four single-stage distributed amplifiers provides a 20-dB flat gain performance and return loss better than 14 dB. The conventional four-stage distributed amplifier configuration employing the same FETs provides a gain of 9 dB over the same bandwidth. This clearly shows the superiority of the cascaded single-stage distributed amplifier over the conventional distributed amplifier.

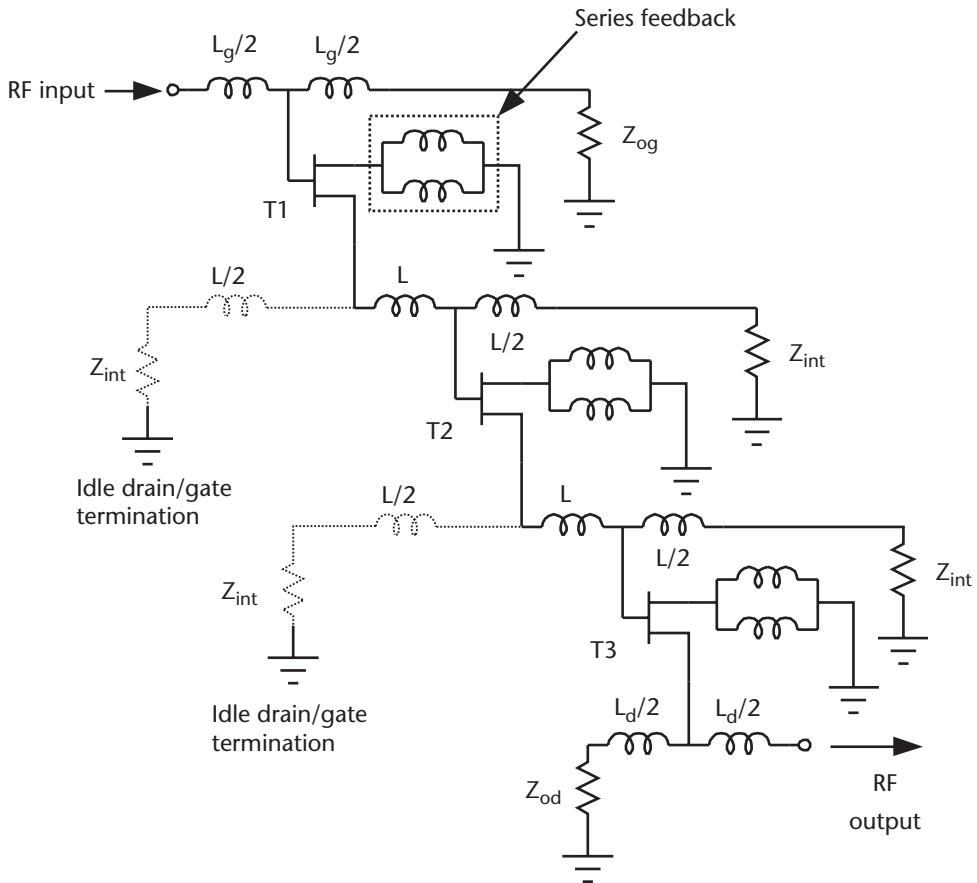


Figure 1.8 Schematic diagram of the cascaded single-stage distributed amplifier.

The CSSDA design proposed by Liang and Aitchison [46] is difficult to realize in practice because:

- The series feedback is difficult to realize, especially in hybrid form using packaged active devices.
- The series feedback is very sensitive at high frequency and may drive the amplifier into oscillation (instability) at some stage across the wide bandwidth.
- The design requires transistors with high transconductance greater than 50 mS to compensate for losses caused by the series feedback.

Despite these shortcomings, the series feedback can be a useful technique for modifying the input impedance (usually increasing it) or in some cases for improving the noise figure.

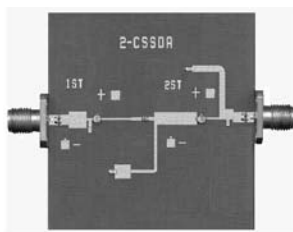
Stability can be more of an issue with the CSSDA configuration than in an ordinary distributed amplifier, other than due to the series feedback element. This is because the high gain associated with the cascaded distributed amplifier may result in excessive coupling between the input and output ports, which can lead to instability. Coupling between the input and output of the individual cascaded devices may also erode the amplifier's stability. Hence, in the CSSDA design, careful consideration must be exercised in order to ensure stable operation over its frequency bandwidth.

Banyamin, et al. [47], improved the single-stage distributed amplifier circuit by eliminating the series feedback network and its detrimental effect of eroding the gain potential of the amplifier. Banyamin realized the amplifier in two-, three-, and four-cascaded single-stage distributed amplifier using packaged heterojunction FET devices and showed that the new CSSDA amplifier provides useful gain response over a bandwidth of 2 to 10 GHz as well as providing stable operation. The comparison between the CSSDA with the conventional traveling wave amplifier realized using the same active devices is given in Table 1.1. It can be seen that a four-stage CSSDA provides a gain of 37 dB, compared with 10 dB obtained from the conventional traveling wave amplifier realized using the same devices achieved across the same bandwidth [48]. The prototypes of the amplifier are shown in Figure 1.9.

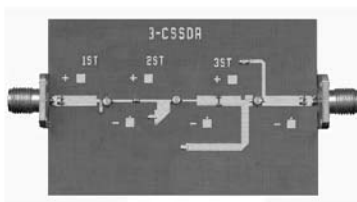
The CSSDA configuration is discussed further in Chapter 2.

Table 1.1 Measured Performance of the CSSDA

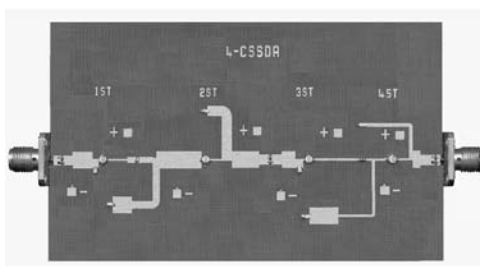
<i>CSSDA Number of Stages</i>	<i>Available Power Gain (dB)</i>	<i>Return Loss (dB)</i>
2	20	>10
3	30	>10
4	37	>10
<i>TWDA Number of Stages</i>	<i>Available Power Gain (dB)</i>	<i>Return Loss (dB)</i>
2	6	>10
3	10	>10
4	10	>10



Two-stage CSSDA



Three-stage CSSDA



Four-stage CSSDA

Figure 1.9 Hybrid prototypes of CSSDA.

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Principles and Applications of Distributed Amplifiers

2.1 Introduction

This chapter describes the principles behind the conventional TWDA and the CSSDA. A lossless cascade of two single-stage distributed amplifier (two-stage CSSDA) design using a simplified unilateral FET model is investigated. The effect of the interstage characteristic impedance on the available power gain and the influence of intrinsic FET elements on the CSSDA performance are analyzed. A comparison is provided between the conventional TWDA and CSSDA designed using identical devices. Finally, it is shown that the distributed amplifier is not only applicable to wideband multioctave amplifiers, it can also be applied to other circuit functions where broadband performance is needed.

2.2 Heterojunction Field Effect Transistor

The active device employed in the design and analysis of the CSSDA presented in this chapter is the heterojunction field-effect transistor (HJ-FET) (NE32584C) [1]. The choice of this device was made arbitrarily; however, it has an excellent low noise of 0.45 to 0.55 dB and high associated gain of 12.5 dB at 12 GHz. Its simplified unilateral equivalent circuit is shown in Figure 2.1. The gate and drain

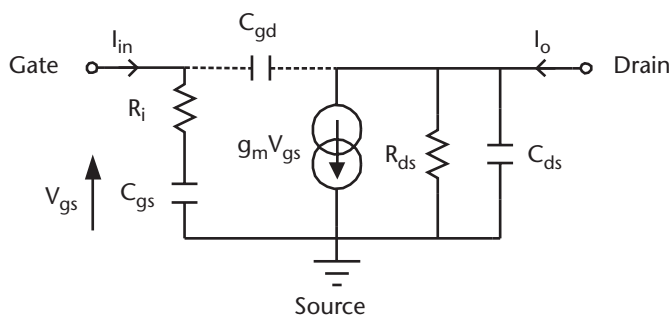


Figure 2.1 Simplified unilateral model of the HJ-FET.

channels have parasitic reactance C_{gs} and C_{ds} , respectively. The feedback capacitance C_{gd} represented by the dotted line is usually ignored in the simplified device model. The transconductance g_m is a voltage-controlled current source that governs the magnitude of the current flowing through the device. The transconductance is controlled by the voltage swing V_{gs} across the FET's input gate capacitance C_{gs} .

In reality, the FET's small-signal equivalent circuit is complicated, as illustrated in Figure 2.2. The elements enclosed by the dotted line box are referred to as the intrinsic elements. The remaining parts are referred to as extrinsic elements or parasitic elements, where resistors R_g , R_d , and R_s represent the bond-wire resistances at the gate, drain, and source terminals, respectively. The inductors L_g , L_d , and L_s are bond-wire inductances at the gate, drain, and source terminals, respectively. The feedback capacitance C_{gd} is responsible for reverse gain or isolation, S_{12} . This capacitance is used to differentiate whether the device is classified as unilateral or nonunilateral. A FET with a high value of C_{gd} is nonunilateral, while one with low C_{gd} is unilateral. The isolation S_{12} of this HJ-FET is very small (typically, its magnitude varies between 0.025 to 0.098 dB across 2 to 18 GHz). Therefore, it is assumed to be unilateral. This implies that the transistor die has a negligible internal feedback. Packaged HJ-FETs normally have associated external parasitic capacitances caused by the packaging of the device. These capacitances are represented by C_{gdp} that exists between the gate and drain channels, C_{gsp} that exists between the gate and source channels, and C_{dsp} that exists between the drain and source channels. Their values are relatively small and depend entirely on the packaging type.

The element values in the small-signal equivalent circuit model for this HJ-FET were obtained using a commercial simulation tool and are given in Table 2.1.

Considering the circuit diagram in Figure 2.1, the input I_{in} and output I_o currents are given by

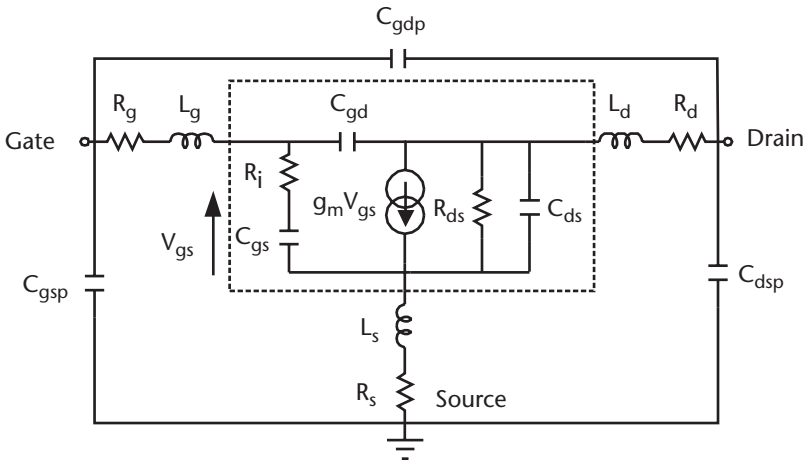


Figure 2.2 Full nonunilateral model of the HJ-FET.

Table 2.1 Equivalent Circuit Parameters of the HJ-FET (NE32584C)

<i>Intrinsic Elements</i>		<i>Extrinsic Elements</i>	
R_i	5Ω	R_g	3Ω
C_{gs}	0.25 pF	L_g	0.3 nH
C_{gd}	0.01 pF	R_d	1Ω
g_m	60 mS	L_d	0.4 nH
C_{ds}	0.1 pF	R_s	1Ω
R_{ds}	243Ω	L_s	0.1 nH
		C_{gdp}	0.01 pF
		C_{dsp}	0.01 pF
		C_{gsp}	0.01 pF

$$I_{in} = j\omega C_{gs} V_{gs} \quad (2.1)$$

$$I_o = g_m V_{gs} \quad (2.2)$$

where $\omega = 2\pi f$

From (2.1) and (2.2), the current gain $|h_{21}|$ is given by

$$|h_{21}| = I_o / I_{in} = g_m / \omega C_{gs} \quad (2.3)$$

The maximum power gain transfer from the input to the output terminal of the transistor is given by [2]

$$\text{Maximum power gain} = \left(\frac{I_o}{I_{in}} \right)^2 \frac{R_{ds}}{4R_i} = \left(\frac{f_t}{f} \right)^2 \frac{R_{ds}}{4R_i} \quad (2.4)$$

where f_t is the maximum cut-off frequency.

The maximum cut-off frequency (i.e., the frequency at which the short-circuit current gain of the transistor drops to unity) is defined as the gain-bandwidth product, which can be obtained from (2.3) and is given by

$$f_t = g_m / 2\pi C_{gs} \quad (2.5)$$

The maximum frequency of oscillation f_{max} (i.e., the frequency at which the available gain power of the transistor is unity) is obtained from (2.4) and is represented by

$$f_{max} = \frac{f_t}{2} \sqrt{\frac{R_{ds}}{R_i}} \quad (2.6)$$

From the small-signal equivalent circuit element values given in Table 2.1, f_t and f_{max} of the HJ-FET are found to be 38.2 GHz and 133 GHz, respectively.

2.3 Conventional TWDA

As mentioned in Chapter 1, the TWDA is associated with two artificial transmission lines, one that makes up the input gate line and another that forms the drain output line. The artificial lines basically consist of a ladder network of series inductance and shunt capacitances, hence the formation of two constant- k transmission lines that have different cut-off frequencies and attenuation characteristics. The shunt capacitors of the gate line are supplied by the gate capacitance C_{gs} of the FETs, whereas the drain-line shunt capacitors are supplied by the FET's drain capacitance C_{ds} . Lengths of transmission line are used to form the series inductances. Figure 2.3 shows the circuit diagram of the TWDA, in which four identical active devices are connected in parallel. Each stage can be considered a T-section network connected in parallel. The purpose of the artificial transmission lines is to effectively remove the gate and drain capacitances associated with the active device by absorbing them within an artificial line. Such an ideal artificial line has the property that power can be propagated along the line from a matched generator to a matched load up to the cut-off frequency of the line, at which point propagation ceases and all power is reflected. In practice, the cut-off frequency is limited by the gate capacitance of the FET and the gate-line inductance.

In the distributed amplifier, the input signal propagates down the gate line, with each FET tapping off some of the input signal. The input voltage that appears at the gate of each FET is amplified via the FET's transconductance, producing current in the drain line. For the distributed amplifier to produce useful gain, it is essential that these drain currents add in phase as the signal propagates along the drain line toward the amplifier's output. This means that the phase shift between FETs along the drain line must be exactly the same as the phase shift between FETs along the gate line. This is achieved by carefully choosing the propagation constants and lengths of the gate and drain lines for constructive phasing of the output signals. The termination impedances on the lines serve to absorb waves traveling in the reverse directions. Unfortunately, as the artificial lines are heavily loaded by the FET's

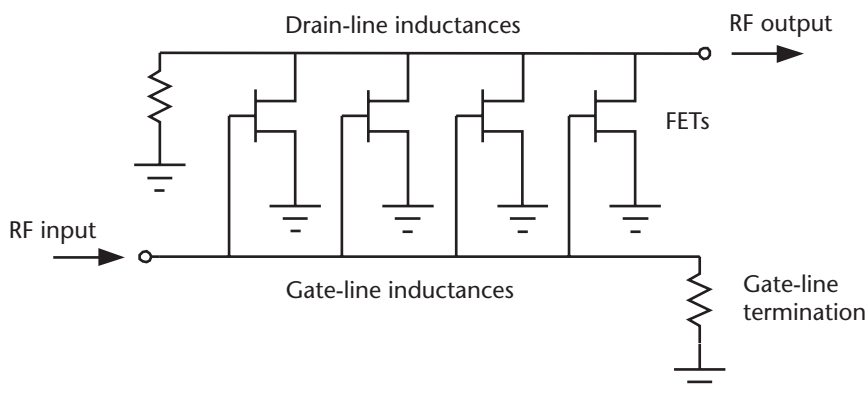


Figure 2.3 Schematic diagram of the conventional TWDA.

resistances, the number of active device sections cannot be added indefinitely. This is because the attenuation along the transmission lines will eventually exceed the gain obtained by adding an additional active device.

2.3.1 Available Gain of a TWDA

The forward gain of a traveling wave amplifier comprised of n active devices can be derived by using the simple amplifier model of Figure 2.4. Essentially, the FET is considered to be loss free and to consist of a gate capacitance C_{gs} and a drain current generator I_n with associated drain capacitance C_{ds} . Other elements in the more general equivalent circuit are neglected to simplify the analysis presented here. Similarly, the artificial transmission lines, which form the input gate-line inductance L_g and the output drain-line inductance L_d , are considered to be loss-free lumped components. The gate and drain lines are terminated in their characteristic impedances Z_g and Z_d , respectively. It is assumed that the external source and load impedances Z_g and Z_d are purely real (i.e., 50Ω).

In the amplifier circuit, a wave from the gate generator propagates down the gate line with a phase constant β_g per section and is dissipated entirely in the right-hand gate load. The voltage across each input gate capacitor C_{gs} causes the corresponding current generator to produce current $g_m V_{gs}$ in the drain line, which flows in both directions with a phase constant of β_d per section. Thus, the power will be dissipated in both of the drain loads. Hence, we need to consider the forward gain to the right-hand drain load and the reverse gain to the left-hand drain load.

The expression for the forward small-signal available gain can be obtained by considering that the FET current generators have a magnitude I_1, I_2, \dots, I_n . Then the total current I_d in the load Z_d is the superposition of the drain line currents given by [3]

$$I_d = \frac{1}{2} \left\{ I_1 e^{-jn\beta_d} + I_2 e^{-j(n-1)\beta_d}, \dots, I_n e^{-jn\beta_d} \right\} \quad (2.7)$$

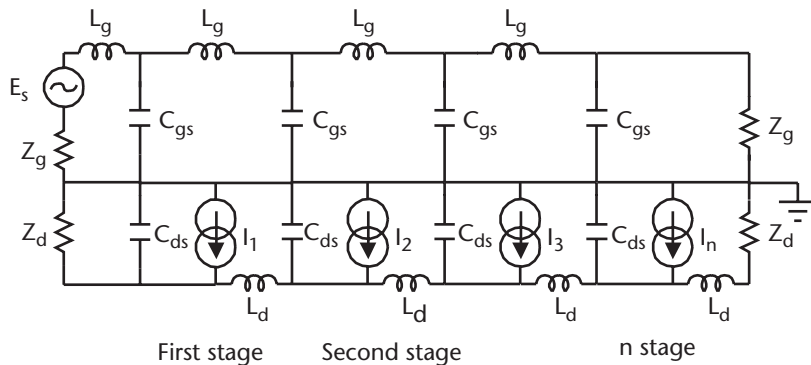


Figure 2.4 Equivalent circuit of TWDA with n sections.

The voltage wave propagating down the gate line due to E_s produces voltages V_1, V_2, \dots, V_n across each input gate capacitor. If the voltage across the input terminal of the amplifier is V_{in} , then

$$V_1 = V_{in} e^{-j\beta_g}, V_2 = V_{in} e^{-2j\beta_g}, \dots, V_n = V_{in} e^{-nj\beta_g} \quad (2.8)$$

Now

$$I_1 = g_m V_1, I_2 = g_m V_2, \dots, I_n = g_m V_n \quad (2.9)$$

Because we have assumed the gate line to be loss free, the following applies

$$|V_1| = |V_2| = |V_n| = |V_{in}| \quad (2.10)$$

and

$$|I_1| = |I_2| = |I_n| = |I_{in}| \quad (2.11)$$

Therefore,

$$I_d = \frac{1}{2} V_{in} g_m \left\{ e^{-j(n\beta_d + \beta_g)} + e^{-j((n-1)\beta_d + 2\beta_g)} + \dots + e^{-j(\Delta\beta_d + n\beta_g)} \right\} \quad (2.12)$$

This expression simplifies to

$$I_d = \frac{1}{2} V_{in} g_m \left\{ \frac{1 - e^{-j+1n(\beta_d - \beta_g)}}{1 - e^{j\Delta(\beta_d - \beta_g)}} \right\} e^{-j(n+1\beta_d + \beta_g)} \quad (2.13)$$

However, V_{in} is equal to $E_s/2$ for a matched line, so (2.13) can be written as

$$|I_d| = \frac{1}{4} E_s g_m \left| \frac{\sin \frac{n}{2} (\beta_d - \beta_g)}{\sin \frac{1}{2} (\beta_d - \beta_g)} \right| \quad (2.14)$$

The power dissipated in the load Z_d is therefore given by

$$\frac{E_s^2}{16} g_m^2 \left\{ \frac{\sin \frac{n}{2} (\beta_d - \beta_g)}{\sin \frac{1}{2} (\beta_d - \beta_g)} \right\}^2 Z_d \quad (2.15)$$

Because the power available from the generator is given by

$$\frac{E_s^2}{4Z_d} \quad (2.16)$$

The forward available gain is given by

$$G_{twa} = \frac{g_m^2 Z_d Z_g}{4} \left\{ \frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right\}^2 \quad (2.17)$$

The function in the braces can be simplified in the limiting case as $\beta_g \rightarrow \beta_d$. The sine function can be represented by the following series:

$$\sin x = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \dots \quad (2.18)$$

so

$$\begin{aligned} \lim_{(\beta_d - \beta_g) \rightarrow 0} \left\{ \frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right\}^2 &= \left\{ \frac{\frac{n}{2}(\beta_d - \beta_g) - \left[\frac{n}{2}(\beta_d - \beta_g) \right]^3 / 3! + \dots}{\frac{1}{2}(\beta_d - \beta_g) - \left[\frac{1}{2}(\beta_d - \beta_g) \right]^3 / 3! + \dots} \right\}^2 \\ &= \lim_{(\beta_d - \beta_g) \rightarrow 0} \left\{ \frac{n - n^3(\beta_d - \beta_g)^2 / 4 \times 3! + \dots}{1 - (\beta_d - \beta_g)^2 / 4 \times 3! + \dots} \right\}^2 = n^2 \end{aligned}$$

Then the forward available gain can be represented by this simplified expression

$$G_{twa} = \frac{1}{4} n^2 g_m^2 Z_d Z_g \quad (2.19)$$

This expression is significant in that it is frequency independent up to the cut-off frequency of the artificial transmission line. The cut-off frequency of the two transmission lines can be altered by the appropriate selection of β_d and β_g . It indicates that the gain can be increased without limit by simply increasing n while maintaining a constant bandwidth; however, this only applies in an ideal loss-free case.

In practice, the gain of the amplifier does not increase monotonically with n because of losses in the gate and drain lines. A more accurate gain expression is given by [4, 5]

$$G_{twa} = \frac{1}{4} g_m^2 Z_d Z_g \left[\frac{e^{-A_g n} - e^{-A_d n}}{A_g - A_d} \right]^2 \quad (2.20)$$

where

A_g is the gate-line attenuation

A_d is the drain-line attenuation

The optimum number of devices N_{opt} that maximizes gain at a given frequency is given by the expression [6]

$$N_{opt} = \frac{\ln\left(\frac{A_d}{A_g}\right)}{A_d - A_g} \quad (2.21)$$

The expressions for the gate- and drain-line attenuation factors are derived from the propagation function for a constant k line and are given by

$$A_g = \frac{\left(\frac{\omega_c}{\omega_g}\right)\left(\frac{\omega}{\omega_c}\right)^2}{\sqrt{\left\{1 - \left[1 - \left(\frac{\omega_c}{\omega_g}\right)^2\right]\left(\frac{\omega}{\omega_c}\right)^2\right\}}} \quad (2.22)$$

$$A_d = \frac{\left(\frac{\omega_d}{\omega_c}\right)}{\sqrt{\left\{1 - \left(\frac{\omega}{\omega_c}\right)^2\right\}}} \quad (2.23)$$

where

ω is the midband radian frequency

ω_c is the radian cut-off frequency

$$\omega_g = \frac{1}{R_i C_{gs}} \quad (2.24)$$

$$\omega_d = \frac{1}{R_{ds} C_{ds}} \quad (2.25)$$

$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d C_{ds}}} \quad (2.26)$$

These equations allow us to determine the optimum number of devices required to realize a traveling wave amplifier. These expressions indicate that the frequency response of the amplifier is determined primarily by the gate line, as it exhibits a

substantially larger attenuation factor than the drain line and has a lower cut-off frequency. The gain performance is also limited by the gate-line attenuation factor because the gate-line attenuation will eventually exceed the added gain obtained by increasing the number of amplifier sections. The former constraints usually limit the gain and bandwidth attainable with practical realizations.

The effect of the number of amplifier stages on the gain and bandwidth for a typical FET distributed amplifier is shown in Figure 2.5. This analysis shows improvement in gain as the number of amplifier stages is increased; however, the gain increase begins to become negligible for n greater than 5. In addition, the flatness of the bandwidth response deteriorates as the number of amplifier stages is increased. However, in practice, the flatness can be improved slightly by optimizing the artificial transmission-line terminations.

The expression of the reverse available gain for power dissipated in the left-hand drain load can be determined in a similar fashion to the forward available gain described earlier. The current flowing through the left-hand drain load is given by

$$I_d = \frac{1}{2} \{ I_1 + I_2 e^{-j\beta_d}, \dots, I_n e^{-j(n-1)\beta_d} \} \quad (2.27)$$

The relationships given in (2.8)–(2.11) apply, so that

$$I_d = \frac{1}{2} V_{in} g_m \left\{ e^{-j\beta_g} + e^{-j(2\beta_g + \beta_d)} + \dots + e^{-j(n\beta_g + (n-1)\beta_d)} \right\} \quad (2.28)$$

This expression simplifies to

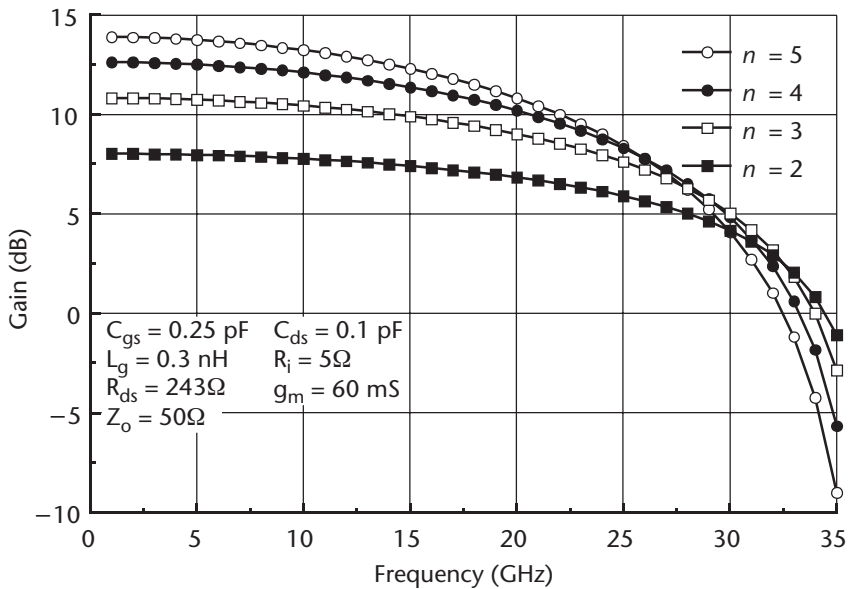


Figure 2.5 Gain of a distributed amplifier as a function of the number of amplifier stages.

$$I_d = \frac{1}{2} V_{in} g_m \left\{ \frac{1 - e^{-jn(\beta_g + \beta_d)}}{1 - e^{-n(\beta_g + \beta_d)}} \right\} e^{-j\beta_g} \quad (2.29)$$

Because V_{in} is equal to $E_s/2$ for a matched line, (2.29) becomes

$$|I_d| = \frac{1}{4} E_s g_m \left| \frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right| \quad (2.30)$$

Therefore the power dissipated in the left-hand drain load Z_d is given by

$$\frac{E_s^2}{16} g_m^2 \left\{ \frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right\}^2 Z_d \quad (2.31)$$

and the reverse available gain is given by

$$G_{rtwa} = \frac{g_m^2 Z_d Z_g}{4} \left\{ \frac{\sin \frac{n}{2}(\beta_g + \beta_d)}{\sin \frac{1}{2}(\beta_g + \beta_d)} \right\}^2 \quad (2.32)$$

For maximum forward gain, $\beta_d = \beta_g = \beta$; then (2.32) becomes

$$G_{rtwa} = \frac{g_m^2 Z_d Z_g}{4} \left\{ \frac{\sin n\beta}{\sin \beta} \right\}^2 \quad (2.33)$$

The value of the function in the braces $\{\sin n\beta/\sin\beta\}^2$ is small except when $n\beta$ is close to 0 or π when the function approaches n and the forward and reverse available gains are identical.

It can be concluded that the forward gain can be made as large as is desired by simply increasing the number of stages, while the reverse gain becomes negligible except at those frequencies at which $n\beta \rightarrow 0$ or π .

2.3.2 Advantages of TWDA

The advantages of TWDA include:

1. Providing a good input match, so gain modules can readily be cascaded.
2. Its isolation from output to input is good (typically – 40 dB) and this coupled with the nonresonant nature of the input and output impedance results in a stable amplifier configuration with no oscillatory tendency on module cascading.

3. Providing more options for the design of the input and output matching networks than the single-stage amplifier.
4. Providing a higher power level than amplifiers with a single stage, as the current generated by each active device is vectorially combined at the output drain line.
5. Being versatile, as its configuration allows the implementation of other functions, such as the power combiner, power splitter, circulator, multiplier, mixer, impedance transformer, and oscillator (see Section 2.5).
6. Being relatively insensitive to the tolerance of passive and active device characteristics.
7. Being relatively insensitive to temperature.
8. Its noise figure can be reduced by increasing the number of active devices [7].

2.3.3 Disadvantages of TWDA

The disadvantages of TWDA include:

1. Phase velocity equalization is necessary because the total output current is dependent on the phase coherence of the individual current generators. The phase velocity equalization requires adding extra capacitance to the drain line in parallel with C_{ds} at each stage to equalize the input and output capacitances of the active device. This adds complexity and may cause difficulties for realizing the amplifier.
2. As the input signal propagates down the gate line, each active device receives a reduced amount of input voltage than the previous one because the energy is dissipated by the device's gate-source resistance. This effect is a function of frequency.
3. The amplifier's gain is limited by the gate-line attenuation, which will eventually exceed the added gain obtained by increasing the number of active devices.
4. Failure of any stage in the gain module will seriously affect the performance of the amplifier, as the gain is determined by the behavior of several FETs whose contributions are added rather than multiplied. It therefore follows that the effect of failure of one FET will be to cause the gain to be reduced rather than eliminated. Thus, the distributed amplifier possesses the property of graceful degradation.

2.4 CSSDA

The distinguishing features that make the distributed amplifier attractive are its flat gain and good terminal match over a broad range of frequencies. However, in the worst-case design scenario, its architecture can squander up to 50% of the available output current from the FETs by allowing current to flow in the reverse direction along the drain line toward the idle drain load end. This substantially reduces

both the efficiency and the output power per FET that could otherwise be achieved if all of the current flowed toward the required output load. In practice, we can direct more drain current toward the output drain load by simply tapering the impedance of the artificial transmission lines [8]. However, in the extreme case when the drain line is severed on the inner side of the last device, this would make it impossible for any current to flow in the reverse direction along the drain line. This approach effectively makes all preceding devices redundant, leaving what is essentially a single-stage distributed amplifier, as the device is connected between two artificial transmission lines. By connecting n of these amplifiers, cascaded in series, the overall gain module is referred to as *n -stage cascaded single-stage distributed amplifier* (n -stage CSSDA). In the analysis presented next, this amplifier configuration is shown to exhibit higher levels of gain and power-added efficiency using the same number of FETs as a conventional distributed amplifier over the same frequency bandwidth.

2.4.1 Lossless CSSDA

The CSSDA topology shown in Figure 2.6 uses the simplified small-signal equivalent model of the FET. A signal generator connected at the input of this network will result in a voltage swing across the input gate capacitor C_{gs} at the first stage. The

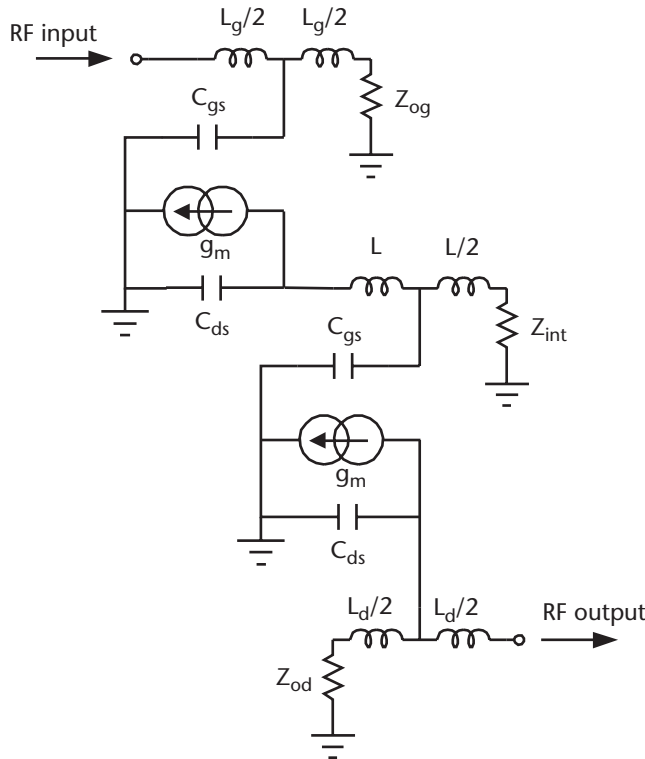


Figure 2.6 CSSDA.

signal is amplified via the FET's transconductance to produce a current flow at its drain port, which is terminated by the interstage impedance Z_{int} . This current will in turn develop a voltage at the gate of the next stage to be amplified by the corresponding FET, producing a current at its drain port. Thus, the signal will be amplified by the gain of the successive stages. Hence, the available power gain can be significantly increased by increasing the number of device stages n , as confirmed by the analysis in the next section. In this design, only the characteristic impedance of the input gate and output drain ports of the active device need to be equalized at each stage. This indicates the ease of the cascaded distributed amplifier design over the conventional distributed amplifier, as no phase equalization between successive stages in the drain and gate lines is necessary.

Based on this technique, a two-stage CSSDA was designed. Figure 2.7 shows the simulated performance of the lossless two-stage CSSDA module. The available power gain S_{21} is 25 ± 1 dB; input S_{11} and output S_{22} return losses are better than 10 dB across a 10-GHz bandwidth. Noise figure (NF) is about 3 dB across this bandwidth.

2.4.2 Available Power Gain of the Lossless CSSDA

The expression representing the available power gain of the lossless n -stage CSSDA is obtained using the schematic diagram in Figure 2.8. For convenience, the FET is considered to be loss free and is represented by a simple equivalent circuit model. This diagram represents the first stage of the n -stage CSSDA and neglects the associated biasing circuitry. As shown, a sinusoidal signal generator having voltage amplitude of E_s is connected at the input of the n -stage CSSDA.

The output voltage V_{o1} for the first stage of the amplifier is given by

$$V_{o1} = g_m V_{gs1} Z_{int} \quad (2.34)$$

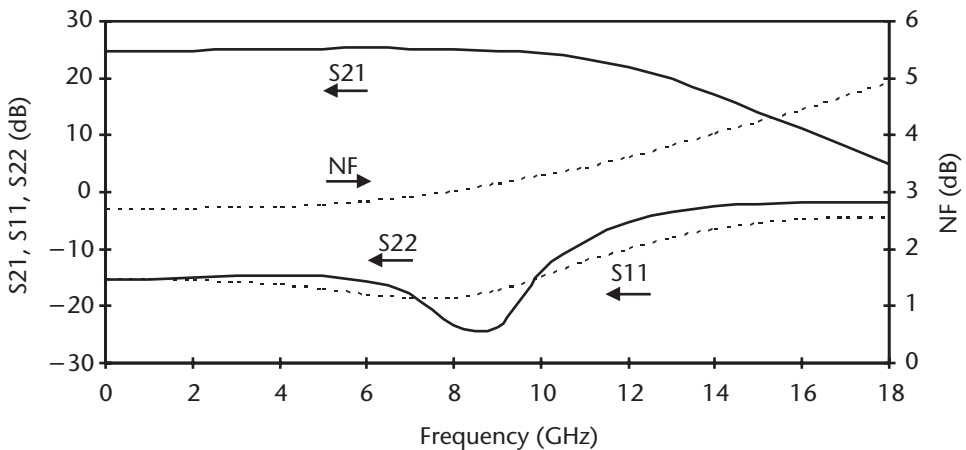


Figure 2.7 Available power gain S_{21} , return losses S_{11} and S_{22} , and NF of a lossless two-CSSDA.

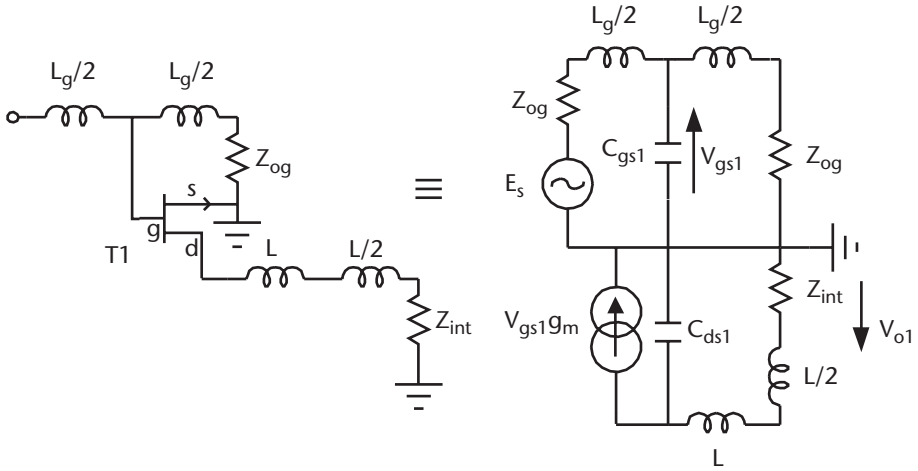


Figure 2.8 Schematic diagram representing the first stage of CSSDA.

Because the amplifier is matched to the generator, the voltage swing at the input gate capacitance C_{gs} of the first stage is given by

$$V_{gs1} = E_s / 2 \quad (2.35)$$

From (2.34), V_{o1} can be written as

$$V_{o1} = g_m Z_{int} E_s / 2 \quad (2.36)$$

Now, by considering the second stage of the n -stage CSSDA, illustrated in Figure 2.9, the output voltage of this stage is given by

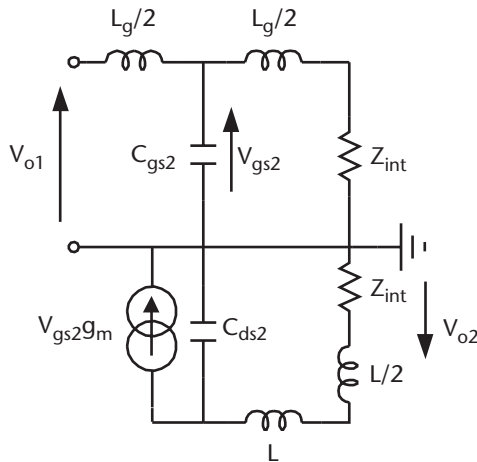


Figure 2.9 Diagram representing the second stage of CSSDA.

$$V_{o2} = g_m V_{gs2} Z_{int} \quad (2.37)$$

It is clear from Figure 2.9 that $V_{o1} = V_{gs2}$ and therefore V_{o2} can be written as

$$V_{o2} = g_m^2 Z_{int}^2 E_s / 2 \quad (2.38)$$

For the $(n - 1)$ stage, the output voltage $V_{o(n-1)}$ is given by

$$V_{o(n-1)} = g_m^{(n-1)} Z_{int}^{(n-1)} E_s / 2 \quad (2.39)$$

Figure 2.10 shows the last stage of an n -stage CSSDA. It is clear that for a matched output load, the current emerging from the drain port of the last stage will split equally into the idle drain load on the left-hand side of the artificial transmission line and the output drain load on the right-hand side.

Hence, for the n th stage, the voltage across the output drain load is given by

$$V_{on} = g_m (V_{o(n-1)} / 2) Z_{od} \quad (2.40)$$

Substituting $V_{o(n-1)}$ from (2.39) into (2.40) gives

$$V_{on} = g_m (g_m^{(n-1)} Z_{int}^{(n-1)} E_s / 4) Z_{od} = g_m^n Z_{int}^{(n-1)} E_s Z_{od} / 4 \quad (2.41)$$

The output power P_o dissipated in the load Z_{od} is given by

$$P_o = V_{on}^2 / Z_{od} \quad (2.42)$$

Therefore, the output power dissipated in the load can be written as

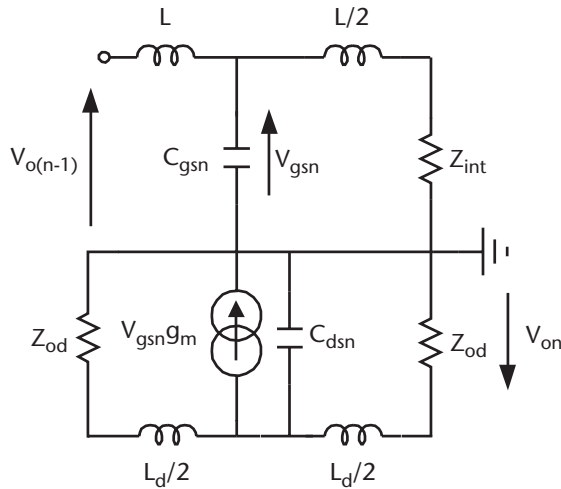


Figure 2.10 Diagram representing the last stage of CSSDA.

$$P_o = g_m^{2n} Z_{int}^{2(n-1)} E_s^2 Z_{od} / 16 \quad (2.43)$$

The input power delivered by the signal generator is

$$P_{in} = \left(\frac{E_s}{2} \right)^2 / Z_{og} = E_s^2 / 4Z_{og} \quad (2.44)$$

where Z_{og} is the characteristic impedance of the gate line. The available power gain of an amplifier is defined as

$$G = \frac{\text{Power delivered to load}}{\text{Power delivered by generator}} \quad (2.45)$$

From (2.43) and (2.44), the available power gain of n -stage cascaded distributed amplifier is

$$G_{cssda} = g_m^{2n} Z_{int}^{2(n-1)} Z_{od} Z_{og} / 4 \quad (2.46)$$

This equation can be expressed as

$$G_{cssda} = g_m^{2n} Z_{int}^{2(n-1)} (Z_{ext})^2 / 4 \quad (2.47)$$

where $Z_{ext} = \sqrt{Z_{od} Z_{og}}$

It can be noted that G_{cssda} is an exponential function of the number of devices n and Z_{int} . In other words, for a given number of devices, the gain can be significantly increased as Z_{int} is optimized for higher values. Increasing Z_{int} would boost the voltage swing across the interstages and therefore generate more current at the output drain of each FET.

The power-added efficiency η of an amplifier is defined as

$$\eta = (1 - 1/G) P_{out} / P_{in} \quad (2.48)$$

where P_{out} is the output power dissipated in the load, P_{in} is the amplifier's dc power consumption, and G is the amplifier gain. From this equation, it is clear that a low-gain amplifier will have a reduced power-added efficiency.

2.4.3 Analysis of Interstage Characteristic Impedance on the Lossless CSSDA

The equivalent circuit diagram representing the two-stage CSSDA using a simplified FET model is shown in Figure 2.11. The interstage characteristic impedance network is represented by the dotted lumped elements. These elements include the output drain-source capacitance C_{ds} of the first active device and input gate-source capacitance C_{gs} of the second active device. Other lumped elements represent the internal artificial transmission line terminated by the load impedance Z_{int} .

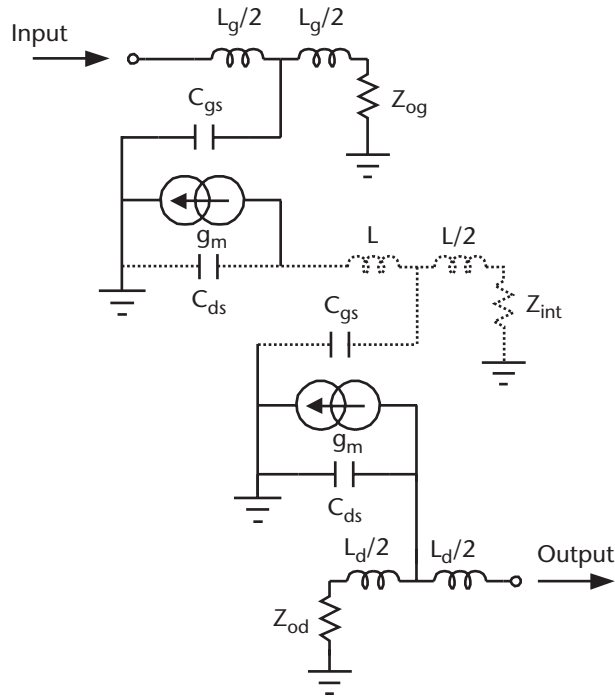


Figure 2.11 CSSDA.

Figure 2.12(a) illustrates the interstage characteristic impedance network of the cascaded distributed amplifier. This network is delineated into an L-section and T-section network, as shown in Figure 2.12(b). It can be shown that if the output impedance of the T section is terminated by its characteristic impedance Z_{oT} , then the impedance looking into the input of the T section will also appear to be Z_{oT} . Then the L section will transform its input impedance Z_{in} to the impedance Z_{oT} , which terminates the output T section (property of the L section, see Appendix A). The overall network is now terminated properly by its characteristic impedance. However, in practice this is not completely achievable, as C_{ds} and C_{gs} are unequal.

Figure 2.13 shows the simulated performance of the interstage impedance Z_{in} as a function of frequency. The magnitude of this impedance tends to fall with an increase in frequency above 4 GHz from 80Ω to 20Ω at 18 GHz. This impedance can be optimized to its maximum value to boost the voltage swing at the gate input of the active device at each interstage, thus enhancing the overall gain of the amplifier. The impedance should introduce enough positive gain roll-up slope to compensate for the active device's negative gain roll-off slope.

2.4.4 Output Current of the CSSDA

When signal power is applied at the input gate terminal of the active device, the voltage appearing across its gate capacitance C_{gs} will result in the device's

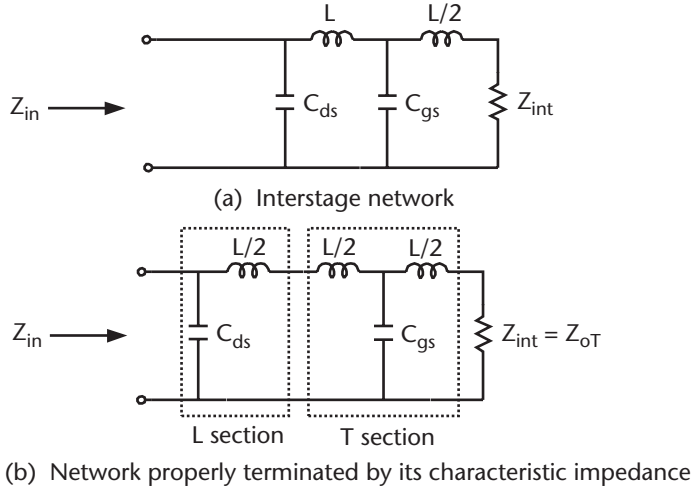


Figure 2.12 The interstage characteristic impedance of the CSSDA.

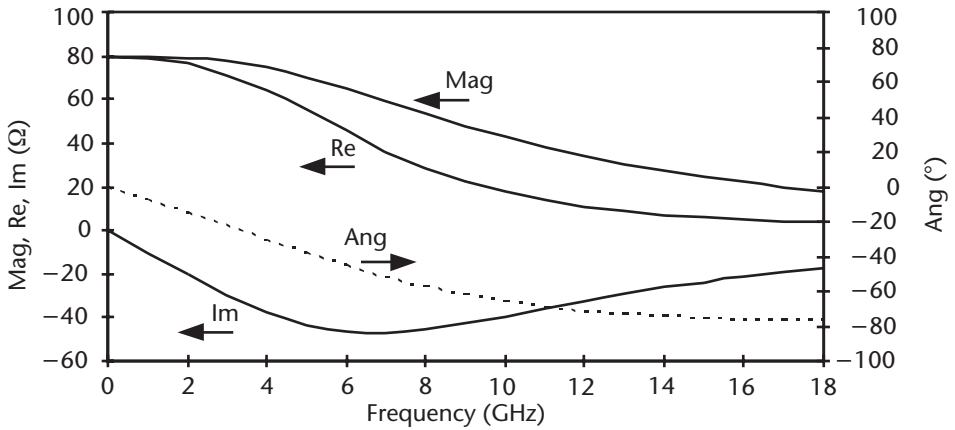


Figure 2.13 Performance of the interstage characteristic impedance.

transconductance g_m , generating current at the drain terminal. The magnitude of this current, at any instant in time, is proportional to the instantaneous voltage across C_{gs} . However, some of the injected voltage will drop across the parasitic elements of the gate terminal. This is detrimental, especially at high frequencies, as the reactance of C_{gs} becomes negligible and the losses dictated by R_i become dominant. Hence, the gain-bandwidth product of the amplifier will tend to be suppressed.

For the n -stage CSSDA, the current will extensively increase as the stage number n is increased, and this is mainly dependent on the optimized value of Z_{int} . The current at stage 1 (see Figure 2.8) can be represented by

$$I_{o1} = g_m V_{gs1} \quad (2.49)$$

At stage 2 (see Figure 2.9), Z_{int} causes the output current to be boosted, as given by

$$I_{o2} = g_m V_{gs2} = g_m^2 Z_{int} E_s / 2 \quad (2.50)$$

Because $V_{gs2} = V_{o1}$

For the n th stage (see Figure 2.10), the output current is given by

$$I_{on} = g_m^n Z_{int}^{(n-1)} E_s / 2 \quad (2.51)$$

The output current delivered to a matched load is half the total current produced by the last stage of the CSSDA. The other half is completely dissipated by the left-hand termination Z_{od} . Equation (2.51) indicates that the output current increases as an exponential function of the number of devices n .

Figure 2.14 shows the relative magnitudes and phase relationship of current waveforms in the two-stage CSSDA. The currents I_{o1} , I_{o2} , and I_{o3} represent the current signal at the input, intermediate, and output stages, respectively. As can be seen, the input current is significantly boosted by the successive stages of the amplifier.

2.4.5 Output Voltage of the CSSDA

Voltage swings at the gate terminals of the active devices in the CSSDA are created by $Z_{in} \times I_n$ established at each stage. These voltage signals traveling through the various stages of the amplifier will suffer ohmic losses in the FET and the artificial transmission line. Figure 2.15 shows the voltage waveform propagating through the two-stage CSSDA. Voltages V_{o1} , V_{o2} , and V_{o3} represent the voltage signal at the input, intermediate, and last stage, respectively.

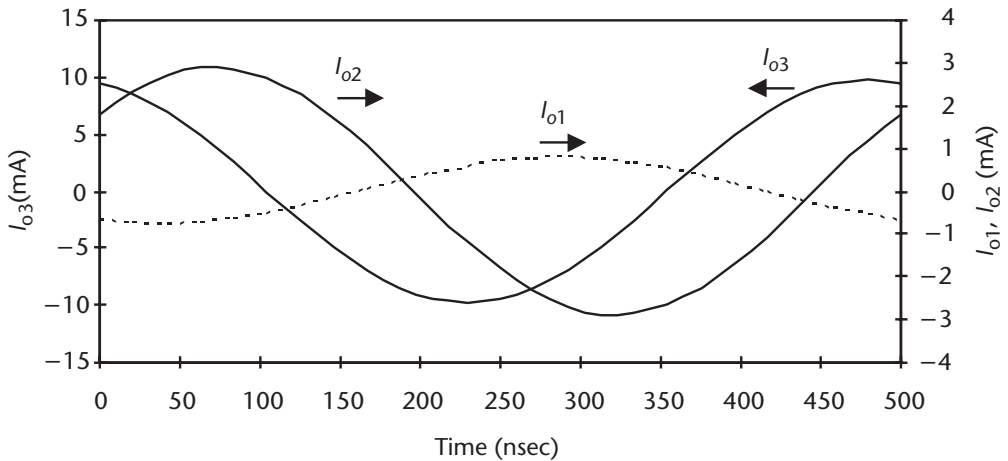


Figure 2.14 Relationship of the current signals in the two-stage CSSDA.

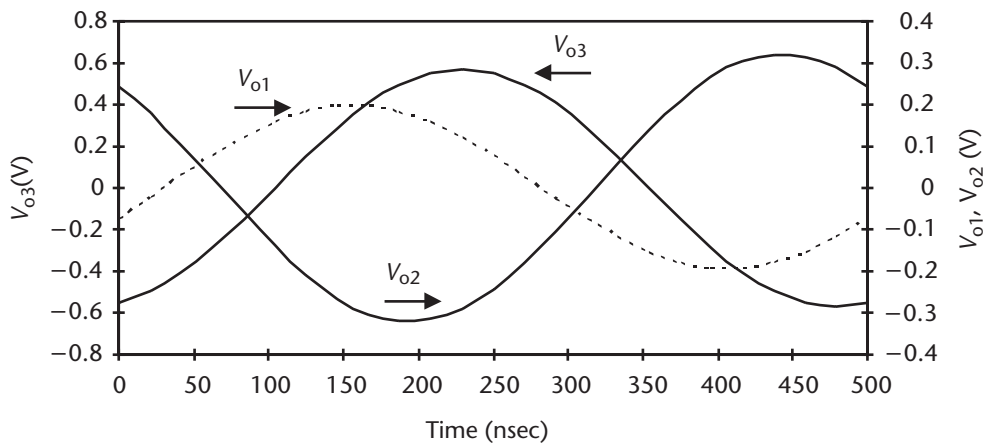


Figure 2.15 Relationship of the voltage signals in the two-stage CSSDA.

The waveforms shown in Figures 2.14 and 2.15 are not fully representative of the actual signals in the amplifier, as a linear small-signal equivalent circuit model representing the FET is used in the analysis.

2.4.6 Lossy CSSDAs

In Section 2.4.2, the lossless CSSDA was analyzed in terms of the simplified unilateral model of the FET. The results of this analysis, in practice, will not accurately predict the performance of the amplifier in terms of available power gain and bandwidth, especially at higher frequencies, as the parasitic losses associated with the active devices and the artificial lines become dominant.

As an example, the full model of the nonunilateral HJ-FET (NE32584C), presented in Section 2.2, is now used in the design of a two-stage CSSDA. The

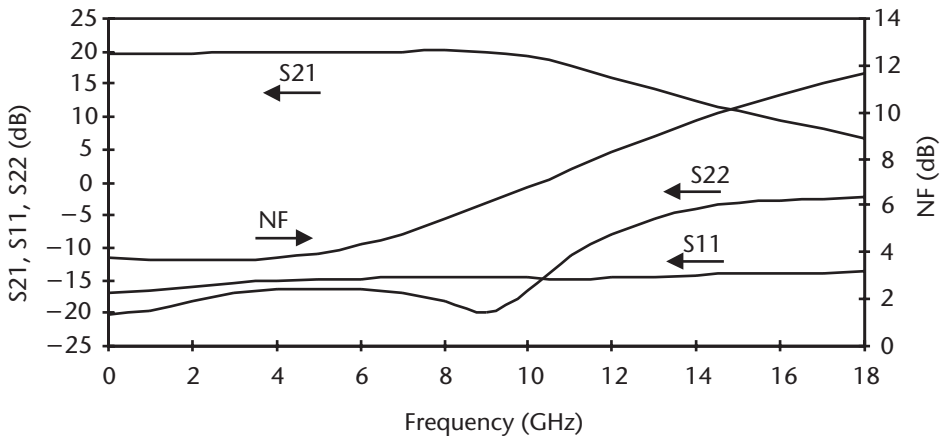


Figure 2.16 Performance of the two-stage CSSDA using full nonunilateral HJ-FET model.

performance of this amplifier is shown in Figure 2.16. In comparison with the previous result of the lossless two-stage CSSDA (see Figure 2.7), S_{21} is about 5 dB lower. This shows the real effect of the parasitic elements of the HJ-FET on the performance of the CSSDA.

In this section, the effect of the three most significant elements of the active device (i.e., R_i , R_{ds} , and C_{gd}) on the two-stage CSSDA are examined in terms of the available power gain S_{21} , input return loss S_{11} , output return loss S_{22} , and NF.

2.4.6.1 Effect of the Input Gate-Source Resistance

The input gate-source resistance R_i is the intrinsic active device element on the gate line, which mainly affects the amplifier's available power gain. Its effect is frequency dependent due to the reactance of the input gate-source capacitance C_{gs} . The magnitude of this capacitance is high at low frequencies and low at high frequencies, which causes most of the input signal voltage to drop across R_i at high frequencies. As the output drain current $g_m V_{gs}$ depends on the device's transconductance and signal voltage drop across C_{gs} , this means that the device's available power gain will progressively degrade as more and more of the input signal voltage drops across R_i . The effect of R_i on the two-stage CSSDA is characterized by the simulation results in Figure 2.17. As shown, at high frequency the available power gain S_{21} of the amplifier decreases as R_i increases. This effect appears to be very small at low frequencies, whereas at high frequencies, its effect becomes more significant. It also indicates that as R_i decreases, the amplifier bandwidth increases until it is limited by the cut-off frequency of the transmission lines.

The input gate-source channel resistance R_i also affects the return loss S_{11} at certain high frequencies. This is because it mainly influences the input matching of the device so that the gate terminating impedance Z_{og} no longer perfectly terminates the gate line. R_i has negligible effect on output return loss S_{22} . The typical value of R_i for low noise devices is constrained to 1–10 Ω .

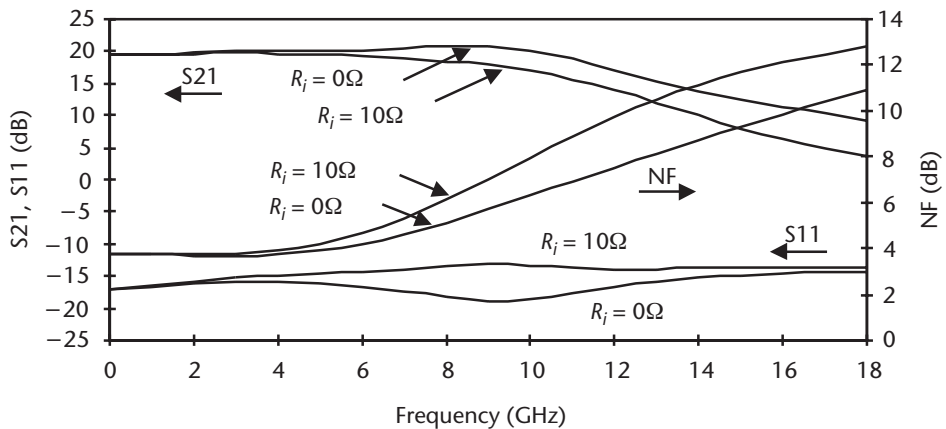


Figure 2.17 Effect of the input gate-source resistance on two-stage CSSDA.

2.4.6.2 Effect of the Output Drain-Source Resistance

The output drain-source resistance R_{ds} acts as a shunt loss across the output of the active device. R_{ds} is frequency independent, and it mainly affects the output drain current, such that if R_{ds} reduces, more current will be diverted away from the output drain terminal to therefore suppress the output signal. Figure 2.18 shows the effect of R_{ds} on the two-stage CSSDA. It shows that the available power gain response for the two R_{ds} values shown varies almost uniformly with one another over the entire 0- to 18-GHz frequency bandwidth. R_{ds} has a negligible effect on the input match of the active device; however, it affects the output return loss S_{22} of the amplifier because it influences the amplifier's output matching network. The typical value of R_{ds} for low noise devices is constrained to 100–200 Ω .

2.4.6.3 Effect of the Feedback Gate-Drain Capacitance

The gate-drain channel capacitance C_{gd} exists between the input gate terminal and output drain terminal. This capacitance feeds back some of the output current $g_m V_{gs}$ into the input gate terminal. It causes gain variations with increasing frequency. This capacitive element is frequency dependent, and it severely affects the amplifier's performance, especially at high frequencies. Figure 2.19 shows the effect of C_{gd} on forward and reverse gain. Figure 2.20 shows the effect of C_{gd} on input and output return loss, and Figure 2.21 shows the effect of the C_{gd} on the noise figure of the two-stage CSSDA. The effects of the other parasitic elements, such as inductances L_g , L_s , and L_d , are negligible compared to the above parasitic elements R_i , R_{ds} , and C_{gd} .

2.4.7 Characteristic Features of CSSDA

From the above analyses, we can deduce several advantages and disadvantages of the CSSDA.

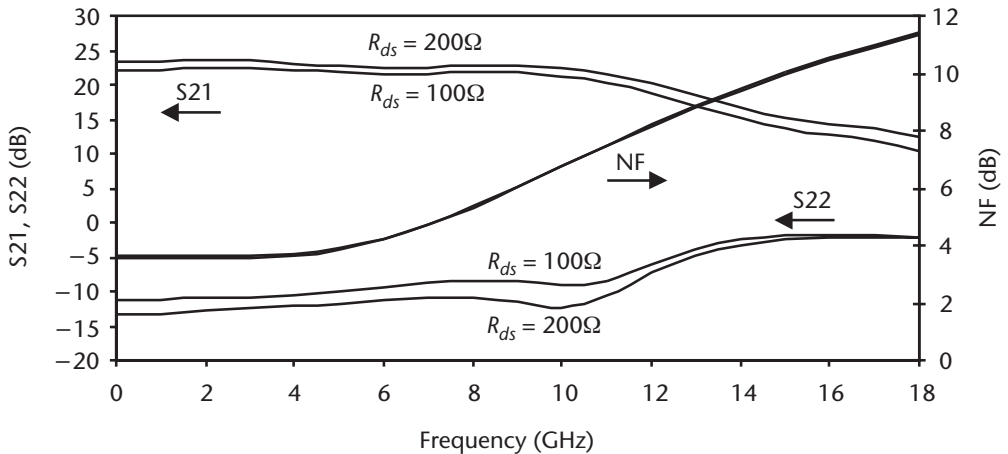


Figure 2.18 Effect of the input drain-source resistance on the two-stage CSSDA.

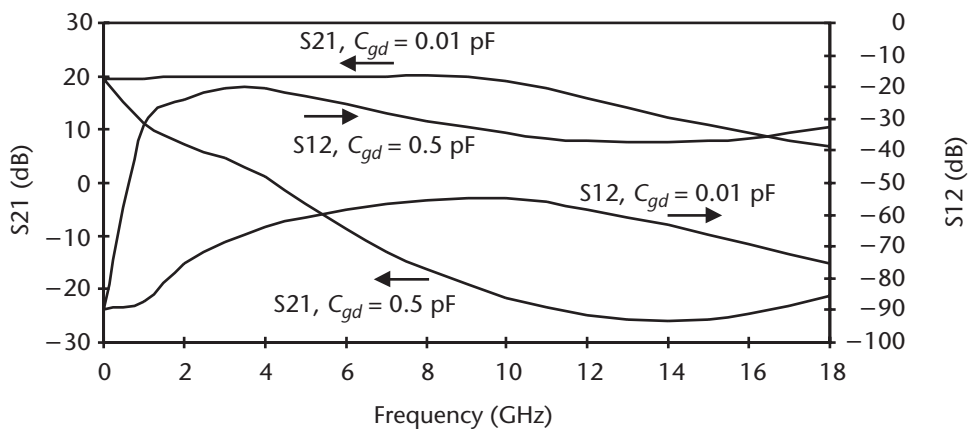


Figure 2.19 Effect of the feedback gate-drain capacitance on the forward and reverse gain of the two-stage CSSDA.

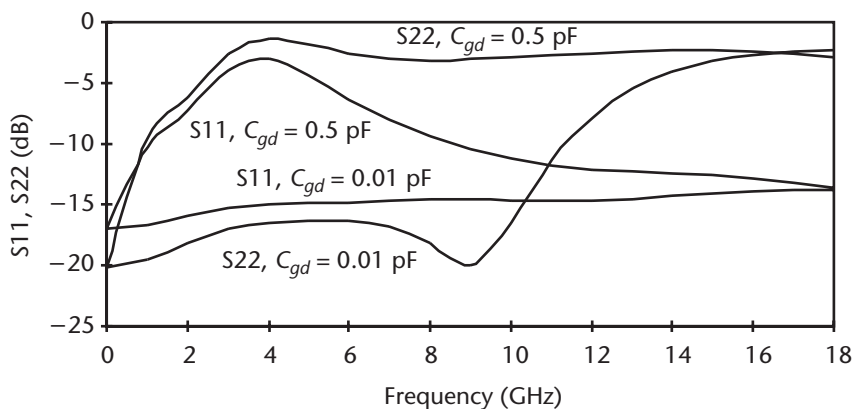


Figure 2.20 Effect of the feedback gate-drain capacitance on the input and output return loss of the two-stage CSSDA.

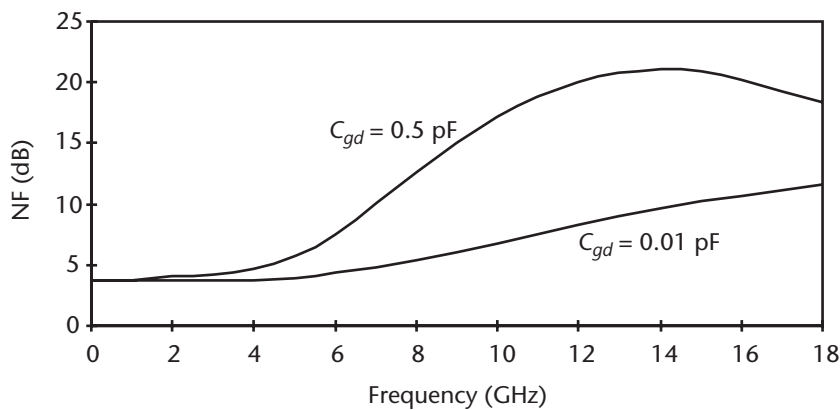


Figure 2.21 Effect of the feedback gate-drain capacitance on noise figure of the two-stage CSSDA.

2.4.7.1 Advantages

The advantages of the CSSDA include:

1. The available power gain G_{cssda} of the CSSDA configuration is significantly higher than that produced by the TWDA using the same number of active devices. The gain can be increased by increasing the number of devices n , and, unlike the TWDA, the CSSDA is not restricted to an optimum number of active devices.
2. With the CSSDA configuration, a flat gain, good input-output isolation, good input/output return loss, and good group delay is achievable for broad bandwidth performance.
3. Unlike the TWDA, the phase velocity equalization is unnecessary for the CSSDA because the total output current is independent of the phase coherence of the individual current generators.
4. The CSSDA module costs less than the TWDA, as fewer active devices are needed to achieve a given gain requirement.
5. The CSSDA is relatively simple to implement in practice.
6. The CSSDA boasts ease of matching, as it only requires matching of the first stage to the $50\text{-}\Omega$ source impedance and the last stage to the $50\text{-}\Omega$ load impedance. In addition, the interstages do not require $50\text{-}\Omega$ matching. Therefore, the device can be optimized to boost the overall available power gain of the amplifier.
7. The CSSDA configuration does not require isolators in order to cascade subsequent amplifier stages, as is the case in broadband amplifiers such as the reactively matched amplifier.

2.4.7.2 Disadvantages

The disadvantages of the CSSDA include:

1. Unlike the TWDA, this particular CSSDA configuration is incapable of delivering a good output power level because some of the power delivered by the last stage is dissipated by the idle drain termination impedance. However, this limitation is overcome by the reactively matched CSSDA configuration described in Chapter 6.
2. The CSSDA circuit is relatively sensitive to component tolerances, either active or passive.
3. It requires complicated biasing networks, as each stage has to be isolated and biased individually.
4. It is very sensitive and prone to oscillation, especially when designed for very high gain levels due to coupling occurring between the adjacent stages. This problem can be avoided by employing a substrate of high dielectric constant to minimize the coupling between the stages, as the majority of the electromagnetic field will be confined within the microstrip medium.

These limitations of the CSSDA configuration are overcome by employing reactive matching, as described in Chapter 6. This configuration is referred to as CRTSSDA.

2.5 Other Applications of Distributed Amplifiers

The versatility of the TWDA and CSSDA configurations makes this genre of amplifiers useful for performing several other circuit functions.

2.5.1 Applications of TWDA

2.5.1.1 Power Combiner and Splitter

Levy, et al. [9], proposed and practically demonstrated an active power combiner using a distributed amplifier concept. The circuit was comprised of two gate lines and a common drain line actively coupled by FETs, as illustrated in Figure 2.22(a). This combiner operates across a band of 2 to 18 GHz. The gain per channel

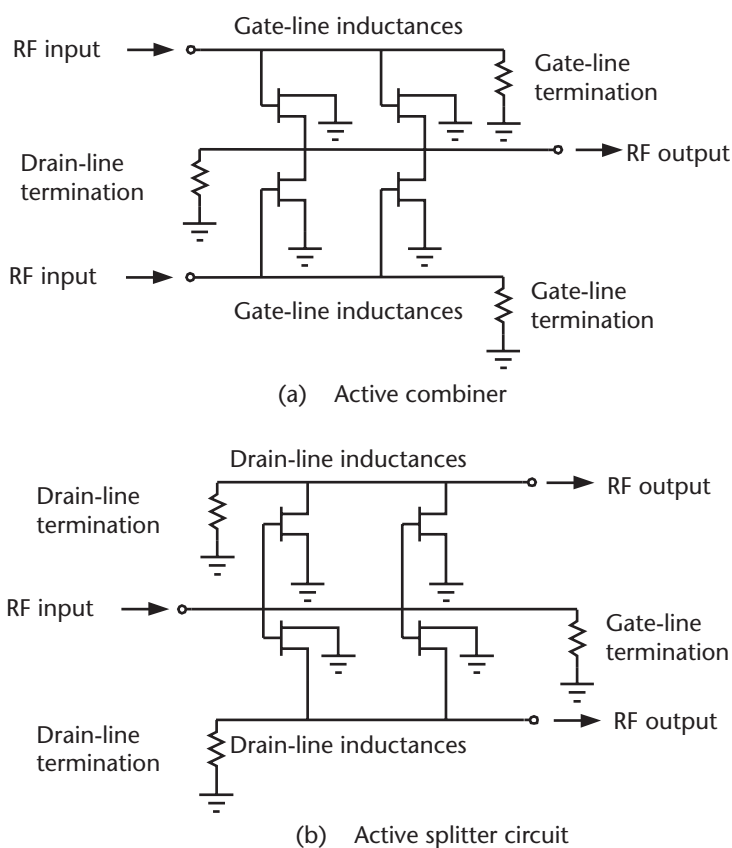


Figure 2.22 Basic diagram of active combiner and splitter circuits.

achieved was 2 dB for a configuration with four FETs with about 20-dB channel-to-channel isolation and a noise figure of about 9 dB. The same technique was used by Robertson and Aghvami [10].

It is similarly possible to create a distributed active power splitter, as illustrated in Figure 2.22(b). Like the combiner, the splitter consists of two independent distributed amplifiers that have a common input realized as constant- k filter network. In this case, the common input is the gate line. Each channel of the distributed power splitter shown uses two FETs. Ito [11] has described a similar wideband device whose input gate line is formed using a bridged-T lowpass filter network, as illustrated in Figure 2.23. This network has the added advantage of providing variable characteristic impedance without affecting the cut-off frequency by simply changing the central bridging inductance. This feature can be used to improve the gain and input VSWR without eroding the bandwidth. The distributed power splitter exhibited a gain of about 1.8 dB and input/output VSWR of less than 2:1 over 0.5 to 26.5 GHz. The active combiner and splitter provide an attractive alternative to the conventional Wilkinson or other planar power dividers in terms of gain, isolation, and size.

2.5.1.2 Circulator

In Section 2.3.1, it was shown that the distributed amplifier, in addition to providing forward gain, also has the property whereby some of the power is coupled to the idle drain port, which gives rise to reverse gain. In a well-designed distributed amplifier, the reverse gain is much less than unity over almost all of the bandwidth, and the distributed amplifier can be considered a four-port active directional coupler with the usual directional coupler property of fourth-port isolation. Thus, this device can be used as an active circulator, as illustrated in Figure 2.24. The operation of the active circulator is quite simple, as signal power fed into port 1 emerges from port 3 after forward amplification and isolation is provided

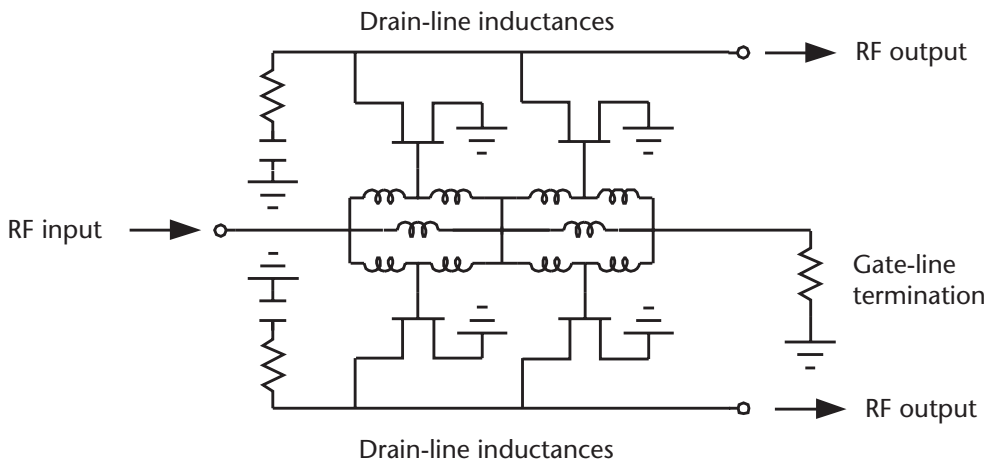


Figure 2.23 Two-way distributed active power splitter.

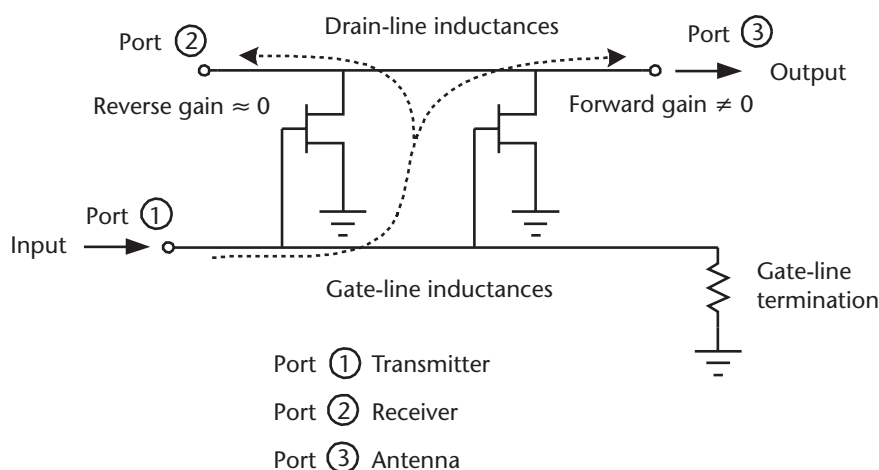


Figure 2.24 Basic diagram of an active circulator.

between port 1 and port 2. Power fed into port 3 is fed directly to port 2. As an example, a transmit signal could be connected to port 1, an antenna to port 3, and a receiver to port 2. A matched termination is connected to port 4. Leisten, et al. [12], first showed the feasibility of using a distributed amplifier in a duplexer/circulator role across the S band. Useful gain of about 6 dB was measured in the S_{34} direction, and 7.5 dB was measured in the S_{21} direction, with 10-dB isolation between S_{31} . The same principle has been extended by Byrne and Beyer [13] using CAD techniques. They have optimized the performance to give a directivity of greater than -30 dB over the 2.5- to 6.5-GHz band; however, no experimental results are provided.

2.5.1.3 Active Frequency Multiplier

Pavio, et al. [14], have demonstrated the concept of a frequency multiplier using the distributed amplifier. The design is based on a balanced drain line output, which effectively suppresses the fundamental frequency. The multiplier, illustrated in Figure 2.25, was realized in monolithic form using four FETs, where one pair of FETs is connected in a common gate configuration while the other pair is connected in a common source configuration. This arrangement provides the required 180° phase difference at the fundamental, which transforms to 360° at the second harmonic. The common input transmission line of impedance Z_o is connected to the source and gate of each pair of devices. The two output drain lines of impedance $2Z_o$ are summed at a common node to cancel the fundamental signal and maximize the second harmonic. This relationship is maintained over an octave. With an input power of 18 dBm over the 5- to 9-GHz band, the second harmonic output (10 to 18 GHz) varied from 8 to 6 dBm while the fundamental output change was only 0 to 3 dBm.

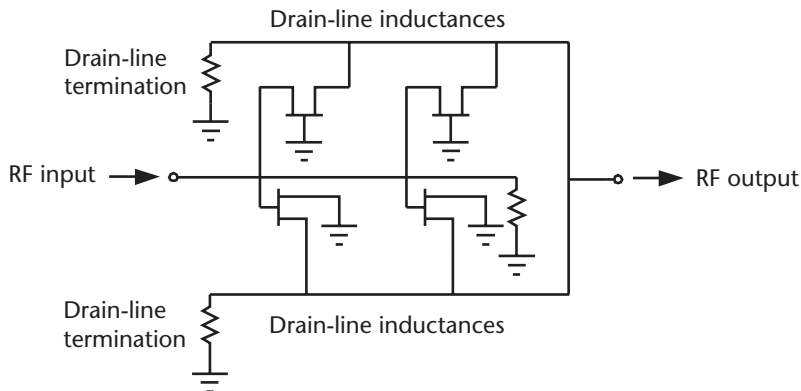


Figure 2.25 Basic diagram of an active frequency multiplier.

2.5.1.4 Active Mixer

The principle of using a distributed amplifier as a distributed mixer was first suggested by Tang and Aitchison [15, 16]. They combined the local oscillator (LO) and radio frequency (RF) signals into the same input by using an external coupler. Both LO and RF signal are propagated down the gate line, whereas the intermediate frequency (IF) propagates along the drain line. It is necessary to arrange the phase constant at the IF frequency in the drain line to be equal to the difference between the phase constants of the signal and local oscillator frequency in the gate line. This yields a very broadband mixer with some gain. With only two MESFETs, the input signal was converted to an IF of 10 MHz over the 2- to 10-GHz signal band with a conversion gain of 1 dB. Increasing the IF to 1.5 GHz reduced this to -4 dB over the same signal band. This approach, however, is not practical in many systems, as the size of the broadband coupler outweighs any size reduction obtained by the mixer. In addition, it requires more LO power to overcome coupling losses and exhibits degraded LO to RF isolation performance, compared to other designs.

The same technique has been investigated by other workers. For example, Howard and Pavio [17] used the inherent isolation in a dual-gate FET to overcome the need for the external coupler and obtained similar broadband mixing performance. This is an attractive technique for implementing the mixer using MMIC, but the noise figures achieved have been unsatisfactory. An improved conversion gain performance was obtained by Robertson and Aghvami [10], who obtained a 3-dB conversion gain over the 2- to 12-GHz band with an 11-dB NF at an IF between 100 MHz and 1 GHz. The technique used here is to employ an active distribute signal combiner at the input of a single-gate FET mixer, as illustrated in Figure 2.26. The active combiner consists of two distributed amplifiers sharing a common drain line. In this configuration, the RF and LO current generators pass independent currents into the drain line, and in small-signal conditions the signals add by superposition. The measured third-order two-tone intermodulation products output intercept point is -10 dBm, and the conversion gain 1-dB compression point occurs at -4 dBm

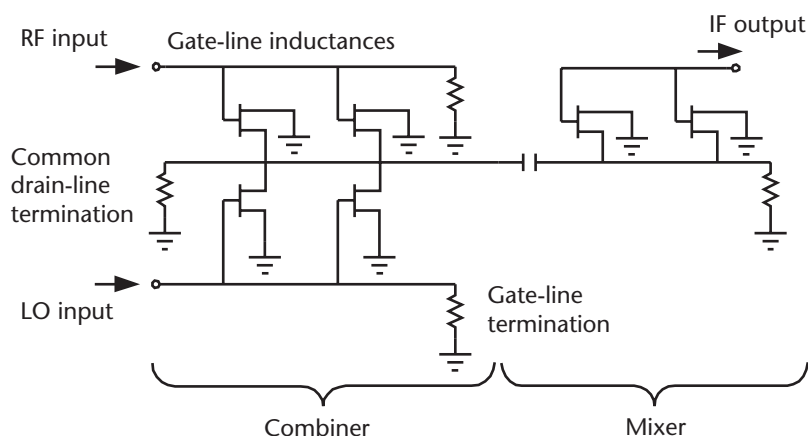


Figure 2.26 Basic diagram of an active mixer.

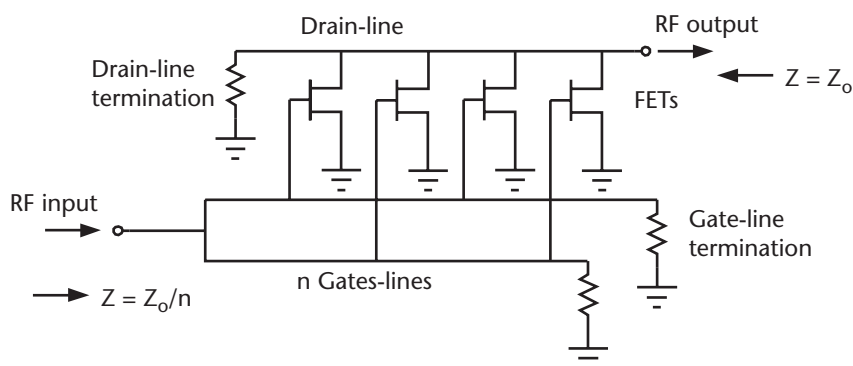
IF output. These levels are comparable to conventional double-balanced diode mixers using the same LO power. A major advantage of this active combiner approach is that the combiner gain lowers the overall noise figure. Also, the output impedance at the IF frequency is reasonably low and easier to match.

2.5.1.5 Active Impedance Transformer

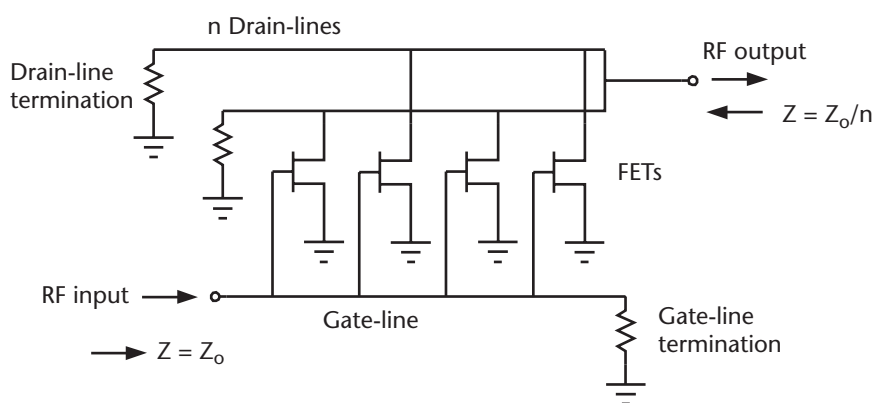
Cioffi [18] showed that the distributed amplifier can be used as an impedance transformer. Thus, to transform from $50/n\Omega$ to 50Ω , he proposed that n 50Ω gate lines in parallel feed the one 50Ω drain line via the FETs, as illustrated in Figure 2.27(a), thereby achieving a wideband transformation from a low impedance to 50Ω . As shown, each gate line feeds the input signal to an alternate FET. Conversely, impedance reduction from 50Ω downwards can be obtained by using one 50Ω gate line that feeds n 50Ω drain lines via the FETs, as illustrated in Figure 2.27(b). Here, the drain terminal of the successive FETs is attached to alternate drain lines. The output drain lines are paralleled to give an output impedance of $50/n\Omega$. He describes the results of a distributed amplifier transformer, which transforms from 50Ω at the input to 25Ω at the output. The structure operates from 2 to 20 GHz and has a gain of 10 dB with input return loss of better than 10 dB and output return loss (with respect to 25Ω) of 10 dB.

2.5.1.6 Multidecade Oscillator

Skvor, et al. [19], first proposed a way to modify the distributed amplifier into a tunable oscillator. This was achieved by omitting the idle drain load and connecting the drain line directly to the amplifier's input, as illustrated in Figure 2.28. This approach makes use of the distributed amplifier's reverse gain to form an oscillation loop. The proposed arrangement had seven active devices in a nine-stage configuration to provide a decade-wide electronically tunable range. This was only possible



(a) From low impedance to 50Ω



(b) From 50Ω to low impedance

Figure 2.27 Basic diagram of an active impedance transformer.

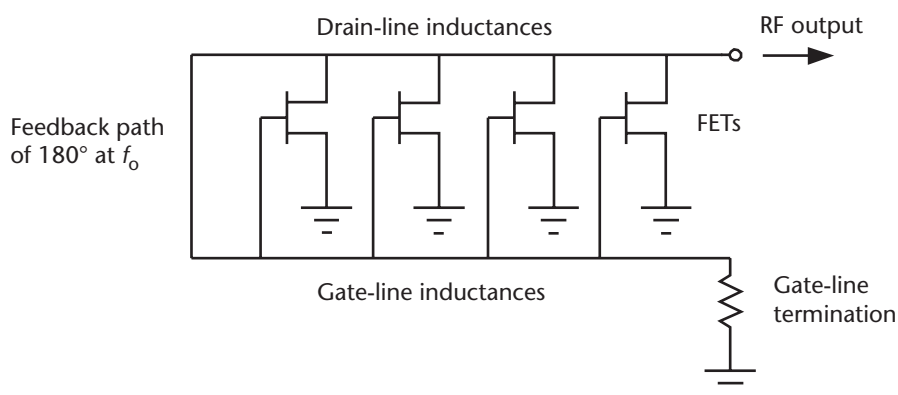


Figure 2.28 Basic diagram of the distributed oscillator.

by differentially biasing in a sequence one pair of FETs. Divina and Skvor [20] experimentally verified the distributed oscillator at 4 GHz. The oscillator was capable of being tuned over the range 1 to 3.5 GHz with output power variation of 3 to 11 dBm. The oscillator exhibited a very good spectral purity and very good suppression of second and third harmonics.

2.5.1.7 Power-Distributed Amplifier

A power-distributed amplifier is simply a distributed amplifier in which power GaAs MESFET devices are used instead of the small-signal GaAs MESFET devices. A characteristic of power GaAs MESFETs is that the gate to source capacitance is larger than that of small signal GaAs MESFETs; hence, an artificial transmission line constructed from power devices will have a lower cut-off frequency for a given size chip. In practice, power GaAs MESFETs are likely to be arrays of lower power devices and consequently will be physically larger than the small signal device; again, this results in a reduction in cut-off frequency.

The power-distributed amplifier also needs to have high power-added efficiency as well as a good C/I. The expression in (2.48) indicates that operating an amplifier at low gain will reduce the power-added efficiency.

The carrier-to-intermodulation product ratio is determined by the intermodulation behavior of the amplifier. As the transconductance nonlinearity predominates in the distributed amplifier, an improved output is obtained by subdividing the gate line into two halves while maintaining a common drain line, as demonstrated by Ayasli, et al. [4]. He obtained 25 dBm with 4 dB of gain over the 2- to 18-GHz band with a monolithic distributed amplifier. The power-added efficiency varied between 7% and 14% and the third-order modulation intercept point was 34 dBm. Ayasli, et al. [21], also proposed an alternative technique, which reduced the effect of gate-line loss and nonlinearity, whereby the MESFETs are coupled to the gate line through series capacitors, as illustrated in Figure 2.29. The advantage of this arrangement is that the gate is more loosely coupled to the gate line, so the gate line

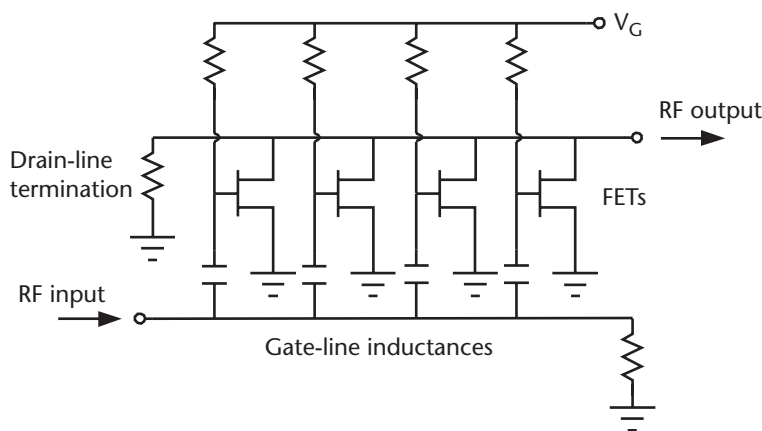


Figure 2.29 Distributed amplifier with gate capacitors.

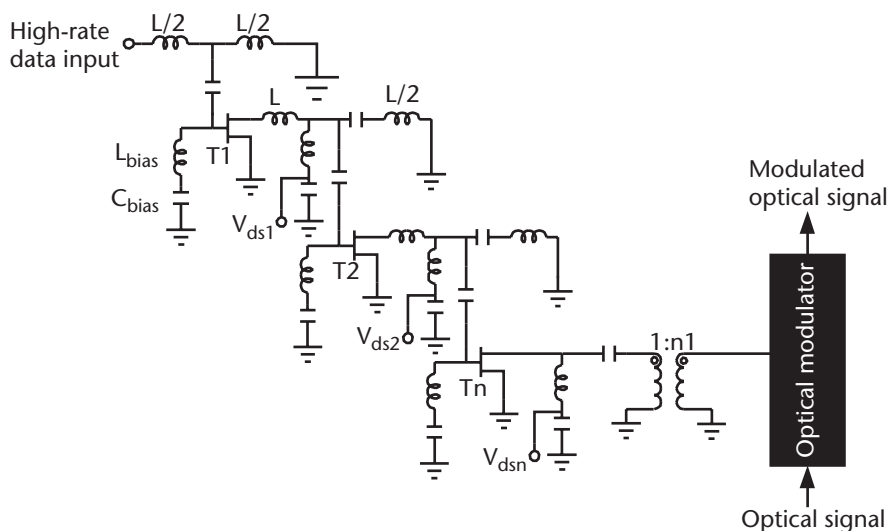


Figure 2.31 CSSDA as driver amplifier for optical modulators.

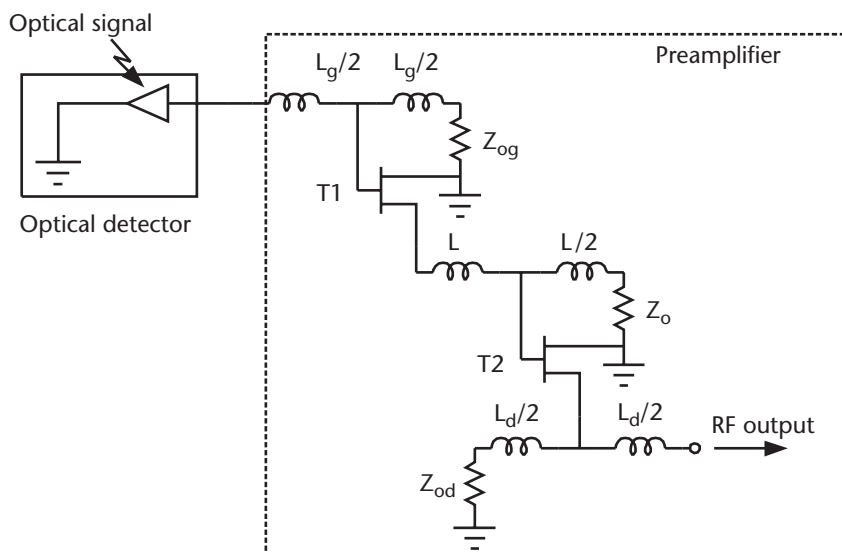


Figure 2.32 Schematic diagram of an optical receiver using CSSDA as a preamplifier.

and the preamplifier. The CSSDA configuration is capable of being used as a preamplifier, as it can offer high gain (making an optical receiver very sensitive to weak signals) as well as good phase linearity and low noise figure. The two elements have to be matched to the $50\text{-}\Omega$ input and output impedance. The bandwidth for such a preamplifier has to be extended down to low frequency (30 kHz). In this case, a special biasing technique is implemented so that the alternating current (ac) signal is isolated at low frequency as well as at high frequency.

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Device Structure and Mode of Operation

3.1 Introduction

The development of high-performance multioctave microwave amplifiers is directly related to the availability of suitable active devices. Advances in semiconductor materials and fabrication technology, combined with the stringent requirements of the commercial and military microwave systems market for increased frequency, efficiency, power, and lower noise performance, have resulted in the dramatically improved active devices available today. The two most important and commonly used active devices for broadbandwidth applications are the GaAs MESFET and the high-electron mobility transistor (HEMT). The current generation of the state-of-the-art pseudomorphic high-electron-mobility transistors (PHEMTs) bears only a faint resemblance to the GaAs MESFETs that are available today. In particular, the DPHEMT structure is capable of delivering high current densities of 300 to 325 mA/mm, possess transconductance of 350 mS/mm, and provide power density of up to 1 W/mm and power-added efficiencies of 50% up to 18 GHz. A typical 28-dBm DPHEMT device exhibits a power gain of more than 1-dB compression point at a frequency of 18 GHz. This chapter briefly reviews the structure and the basic operation principles of these devices. It provides the necessary background information that is important for the understanding of these devices and their inherent limitations.

3.2 The GaAs MESFET—Structure and Operation

The cross-sectional view of the GaAs MESFET is shown in Figure 3.1, where the chief attribute is the use of a metal-semiconductor Schottky contact for the gate, rather than a metal-oxide-semiconductor (MOS) structure, which is used in the MOSFET device. This “oxideless” approach minimizes the device’s gate-to-source capacitance, which would otherwise degrade the high-frequency gain performance. The Schottky contact’s built-in voltage, with the application of a bias voltage on the gate and drain contacts, creates a depletion region below the gate contact, which is shown by the shaded area in Figure 3.1. This region, which is depleted of the majority-carrier electrons, modulates the drain-source channel current to give rise to the transconductance effect, which is described by [1]

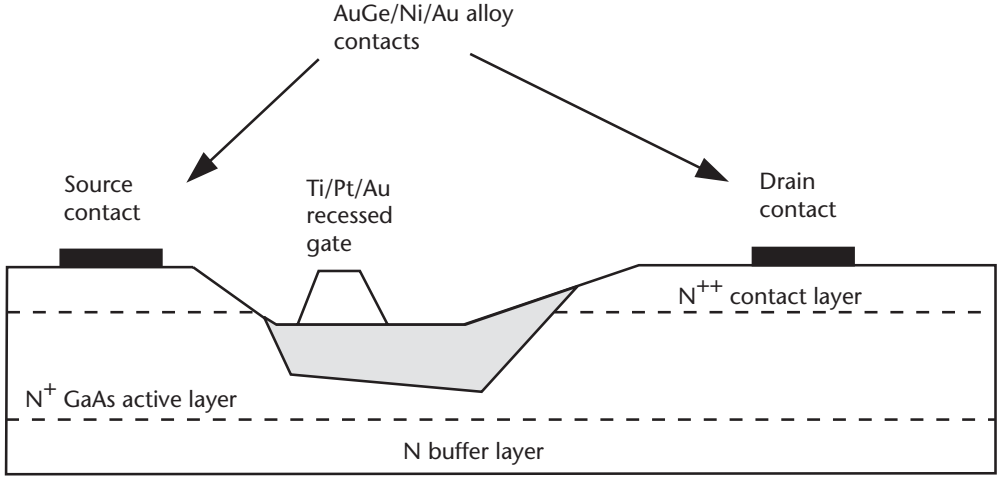


Figure 3.1 Cross-sectional view of the GaAs MESFET structure shows the depletion region below the gate.

$$g_m = w\epsilon_s v_{sat}/h_d \quad (3.1)$$

where

- g_m = intrinsic device transconductance;
- h_d = depletion-layer depth;
- w = gate width;
- ϵ_s = semiconductor dielectric constant;
- v_{sat} = saturated carrier velocity.

As with the MOSFET nomenclature, gatewidth w is defined as being perpendicular to the current flow while the gate length l_g is the shortest gate dimension, which is parallel to the current flow. For high-frequency amplifier applications, a useful figure of merit is the unity-current-gain frequency f_T . For the MESFET, this parameter is given by

$$f_T = g_m/2\pi C_{gs} \quad (3.2)$$

where C_{gs} = gate to source capacitance

At frequencies above f_T , the current through C_{gs} is greater than that produced by the transconductance; therefore, f_T represents a fundamental high-frequency limit.

The gate-source capacitance is given by the expression [1]:

$$C_{gs} \cong w\epsilon_s l_g/h_d \quad (3.3)$$

Therefore, f_T can be expressed in terms C_{gs} and g_m as

$$f_T = v_{sat}/2\pi l_g \quad (3.4)$$

For optimum high-frequency performance, the device designer must either increase the saturated carrier velocity or decrease the gate length. The saturated carrier velocity is a fundamental attribute of the semiconductor that cannot be significantly increased unless a different semiconductor material is used. The gate length can be reduced; however, after a certain point, the advanced lithography-process technologies and their inherent costs become the limiting design factor.

Optimization of the MESFET for maximum RF output power requires the device to be capable of sustaining large peak-voltage and current amplitudes. A typical MESFET current versus voltage (I-V) characteristic shown in Figure 3.2 illustrates that with a positive gate bias, the MESFET can conduct current levels of 15% to 20% above the saturated drain-source current I_{dss} . This maximum current is denoted as I_{dssm} , whereas I_{dss} is measured at zero gate-source bias. The transition from the linear operating region to the current saturation region occurs at drain-to-source voltage above the *knee* voltage V_k . The highest voltage that can exist between the drain and the source is the gate-to-drain breakdown voltage V_{gdb} minus the pinch-off voltage V_p . This maximum voltage will be reached only as the drain current approaches zero. The drain-to-source voltages below V_k should be avoided because they imply high microwave losses in the nonsaturation region.

Load-line analysis, based on this family of characteristic curves, can be used to determine the dc quiescent operating point and hence the mode in which the device is operated (see Chapter 5 for further information). The load line connects the point of maximum operating current (at $V_{ds} = V_k$ and $I_{ds} = I_{dss}$) to the point of maximum voltage (at $V_{ds} = V_{gdb} - V_p$, and $I_{ds} = 0$), as shown in Figure 3.2. Hence, the corresponding RF output power is approximately [2]

$$P_{RF} = I_{pp} V_{pp} / 8 \quad (3.5)$$

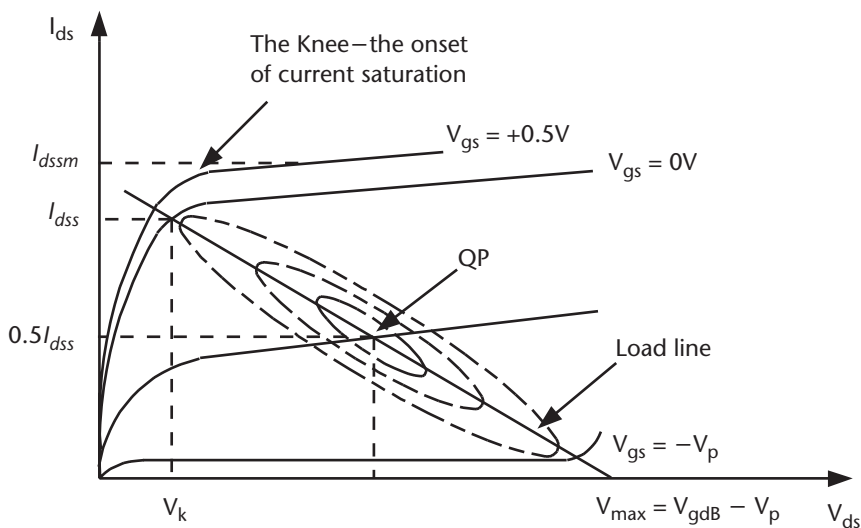


Figure 3.2 GaAs MESFET drain-source current versus drain-source voltage characteristics.

where

I_{pp} is the peak-to-peak current amplitude (I_{dssm})
 V_{pp} is the peak-to-peak voltage amplitude ($V_{gdB} - V_p$)

The RF output power obtainable from this device can be increased by increasing the doping in the active-layer in order to raise I_{dss} and I_{dssm} . However, by doing this the breakdown voltage is decreased, which makes the device vulnerable to failure more easily. Consequently, the only option is to scale the MESFET so that it has a large total gate width. The scaling of MESFET in order to achieve high output power results in the increase of the device's intrinsic parasitics, and this is the main factor causing the degradation of the bandwidth, power-added efficiency, and gain performance [3]. A typical MESFET capable of delivering 1-W output power at the 1-dB gain compression point has a total gate periphery of 2,800 to 3,200 μm with an I_{dss} of 600 to 800 mA.

3.3 HEMT-based Devices—Structure and Operation

3.3.1 HEMT

The HEMT device, which was first introduced about the mid 1970s [4, 5], retains the basic external design attributes of the traditional MESFET. However, the intrinsic physics and electrical characteristics of these two devices are dramatically different. The HEMT device achieves superior high-frequency performance by not only employing alternate semiconductor materials, but by also using the semiconductor heterojunction [6]. Prior to 1980, most semiconductor devices used single-material structures formed with either silicon or GaAs. Advances in material-growth technology, such as molecular-beam-epitaxy (MBE) systems, led to the fabrication of devices composed of different combinations of semiconductors. The junction formed between two semiconductors [7] in intimate contact possesses special qualities, one of which is the ability to confine charge carriers (electrons, in this case) in an extremely thin sheet. Under certain conditions, the confined electron layer will exhibit quantum effects and the term *two-dimensional electron gas* (2-DEG) is sometimes used to describe this confined-carrier layer. Figure 3.3 shows a simplified HEMT structure that is formed by using an AlGaAs/GaAs heterojunction.

The charge carrier confinement phenomenon can be explained by observing Figure 3.4. The valence band is omitted for simplicity, as the HEMT structure is a majority (electron) carrier device. The energy-band diagram is shown along a line drawn from the gate electrode into the device substrate. The Fermi level is the energy level in which the probability of finding an electron is exactly one-half, and because carriers do not exist below the conduction band, the separation of the conduction band from the Fermi level indicates the relative electron density. It can be noted in Figure 3.4 that the AlGaAs layer in contact with the gate electrode is depleted of

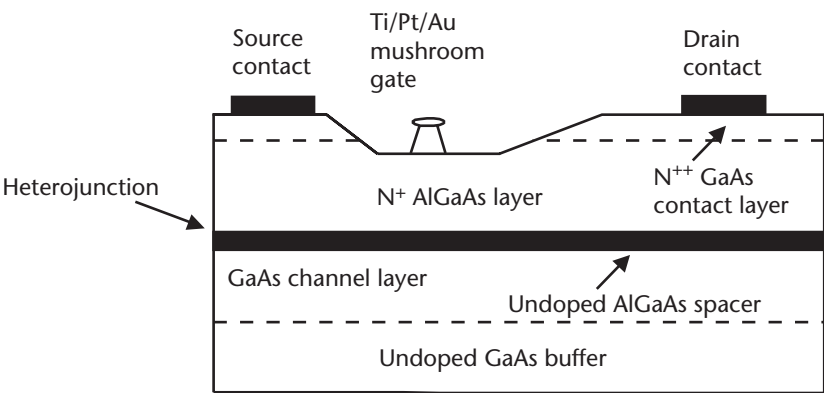


Figure 3.3 Cross-sectional view of the HEMT structure.

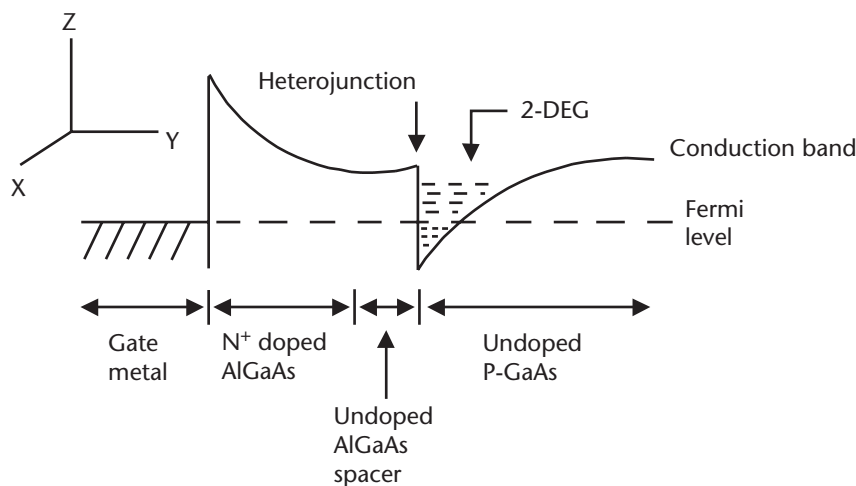


Figure 3.4 The HEMT’s conduction-band discontinuity supports an accumulation of electrons in a thin sheet adjacent to the heterojunction. This accumulation layer is the 2-DEG, while the drain-source current flows in the x direction.

carriers (the conduction band above the Fermi level), while there is a large accumulation of carriers on one side of the heterojunction (the conduction band below the Fermi level).

The large conduction-band discontinuity at the heterojunction is due to the difference in bandgap energy between AlGaAs and GaAs. In practice, HEMT devices are fabricated with a 20% to 30% aluminum mole fraction (instead of pure AlGaAs) in order to avoid excessive crystalline mismatch effects. With this concentration of Al, the conduction-band discontinuity is approximately 0.2 to 0.3 eV.

The HEMT structure exhibits higher intrinsic transconductance g_m for two reasons. First, the current flow occurs in undoped GaAs, which has higher mobility and greater saturated carrier velocity. Second, the carriers are much closer to the

gate electrode. As a further refinement, there is a thin undoped AlGaAs layer on one side of the heterojunction in order to physically isolate the 2-DEG from the ionized dopant atoms in the AlGaAs. The HEMT represents an improvement over the MESFET, as demonstrated by the device performance shown in Table 3.1.

The transconductance expression for a HEMT is similar to that of a MESFET, except for the substitution of the depletion layer depth h_d with the term $(d + \Delta d)$, which represents the total thickness of the AlGaAs layer, and is given by [7]

$$g_m \cong v_{sat} w \epsilon_s / (d + \Delta d) \quad (3.6)$$

The HEMT could be improved further because these devices still have a number of unresolved problems [8]. For example, the electrons have to surmount the heterojunction energy barrier in order to flow into the ohmic contacts. This produces additional parasitic resistance, which decreases the extrinsic device transconductance. In the HEMT, the 2-DEG layer charge density is partially determined by the doping in the AlGaAs layer below the gate. Higher current density in the 2-DEG requires greater doping density, with the subsequent degradation of the device's breakdown voltage.

In a HEMT, as in a MESFET, the gate length greatly influences the maximum operating frequency of the device. Gate lengths of $0.15 \mu\text{m}$ allow operation up to frequencies as high as 94 GHz, but for lower frequency applications, a large gate periphery is required. A compromise is made between the improved performance of short gates and higher yields possible with longer gates. For most applications of up to 20 GHz, for example, gates of 0.25 to $0.5 \mu\text{m}$ lengths are preferred. While reduced gate length is needed for best high-frequency performance, care must be taken to ensure that the gate series resistance remains acceptably low. One solution to lower gate series resistance is the use of a *mushroom* structure gate, as shown in Figure 3.3. The mushroom gate has another benefit as well, that is under RF drive, appreciable gate current can flow through the device. If the current density is excessive, electromigration of the gate metal will occur, but the large cross-sectional area of the mushroom gate reduces the gate current density.

3.3.2 SPHEMT

A wide range of alternative semiconductor materials and combinations has been studied over the last decade in an effort to optimize the device performance. One of

Table 3.1 Summary of Materials-Related Device Performance

Device Type	Gate Length (μm)	Saturation Velocity (cm/s)	I_{dss} (mA/mm)	I_{dssm} (mA/mm)	Device Transconductance g_m (mS/mm)	f_t (GHz)
GaAs MESFET	0.5	6.9×10^6	170	200	250	22
HEMT	0.5	7.5×10^6	120	180	290	30
HEMT	0.25	6.3×10^6	220	380	320	40
SPHEMT	0.25	7.8×10^6	200	450	500	50
DPHEMT	0.25	7.8×10^6	310	600	425	35

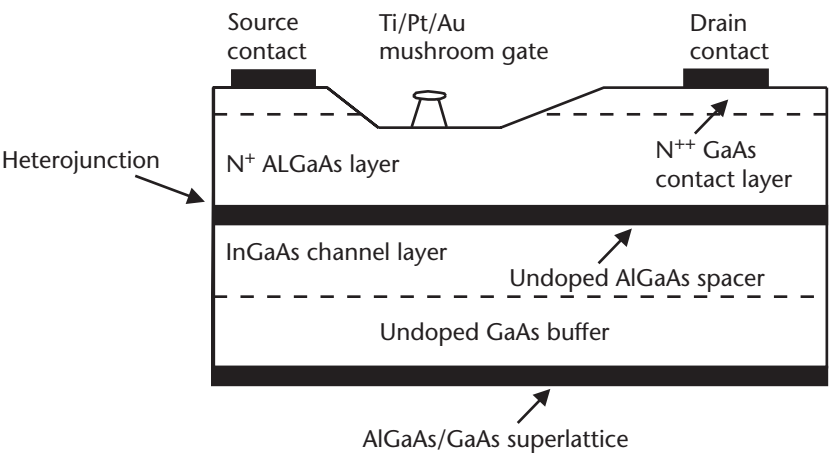


Figure 3.5 The SPHEMT structure is formed with a combination of AlGaAs and InGaAs layers.

the best materials that has emerged is the AlGaAs/InGaAs combination [9], as shown in Figure 3.5. The use of the InGaAs as the conducting or channel layer provides an even larger conduction band discontinuity, which maximizes electron transfer from the AlGaAs layer into the 2-DEG. In addition, the undoped InGaAs layer exhibits very high saturation velocity (i.e., as fast as 1.0×10^7 cm/s, versus 5×10^6 to 7×10^6 cm/s for the MESFET). The InGaAs and GaAs crystalline structures are slightly mismatched by approximately 1% so that the channel layer is kept thin. Due to this mismatch, the term SPHEMT is used. A thin sheet of dopant atoms deposited in the AlGaAs layer can be optimized for higher breakdown voltage. The basic SPHEMT energy band diagram shown in Figure 3.6 is similar to that of the HEMT containing a single 2-DEG layer.

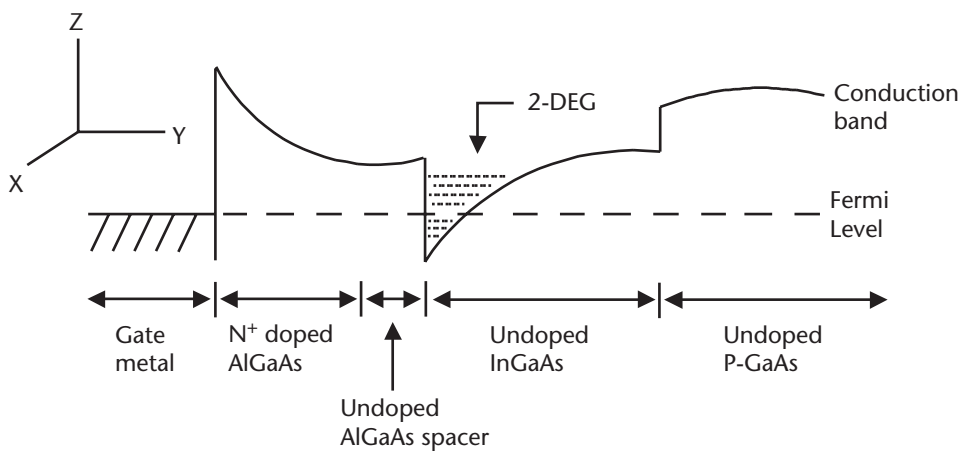


Figure 3.6 The SPHEMT's energy band diagram demonstrates the device's AlGaAs/InGaAs bandgap energy difference, which permits a larger conduction band discontinuity than that of the HEMT.

3.3.3 DPHEMT

In order to enhance the current and power density, the SPHEMT structure is modified to make use of both heterojunctions, which is accomplished by adding another AlGaAs doping layer, as shown in Figure 3.7. In this configuration, the gate electrode modulates two parallel conducting 2-DEG layers. The DHEMT [10, 11] is the basis of a new class of much improved high-performance device, in terms of power, gain, and efficiency.

In the DPHEMT, the carriers are introduced into the InGaAs channel by doping the AlGaAs on both sides of the InGaAs. This results in high channel current and hence high power-handling capability. Planar doping, or the placement of a thin plane of silicon dopant atoms, at the upper AlGaAs/InGaAs heterojunction provides additional electrons to the channel. This also allows lower doping to be used in the AlGaAs donor layer, which enhances breakdown voltage.

A comparison of the related material parameters of these devices, given in Table 3.1, clearly shows that the DPHEMT device provides a substantial improvement in I_{ds} and I_{dssm} characteristics over other devices. In particular, this class of devices is capable of achieving typically 1 W/mm power density with a nominal operating drain source voltage of $V_{ds} = 8V$. The additional advantage of the DPHEMT device is that in low-voltage-power applications, such as 3V, high current density can still be achieved.

The enhanced power density has other performance implications. For example, smaller gate width devices can be employed to achieve a desired output power, as the input impedance is higher. Higher input impedance permits a lower transformation ratio in the matching circuit, which results in a higher gain bandwidth product.

In order to realize high output power from the DPHEMT device, a large number of gate fingers are required to be combined [12]. The topology of the large power DPHEMT devices is critical, as it determines not only the RF performance but also

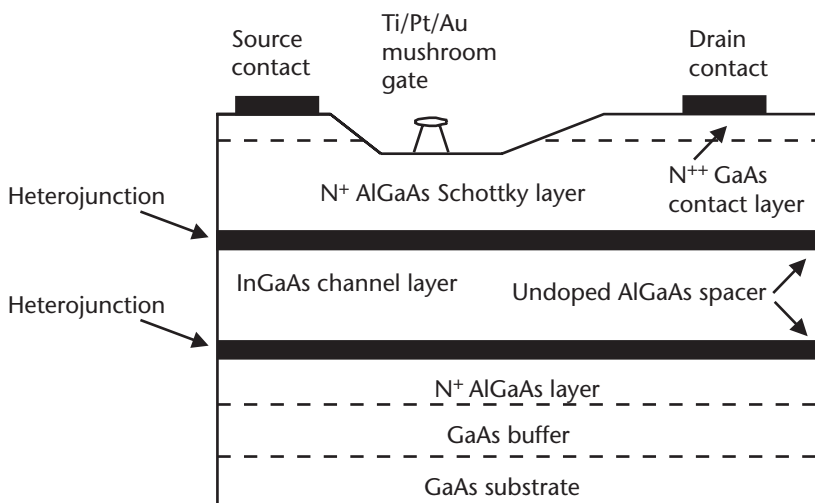


Figure 3.7 The DPHEMT contains dual 2-DEG layers on opposite sides of the InGaAs channel.

the thermal characteristics, and hence the long-term reliability of the device. For a large-power DPHEMT device, the topology design depends on the following considerations. The power requirement, from which the total gate width can be determined, is based on the power density expected for that channel design. An interdigitated device layout with many parallel gate fingers is the most space-efficient layout. In general, the gate finger lengths are made to be as long as possible, in order to minimize the number of fingers and resulting overall device width.

Table 3.2 highlights the typical performance comparisons between the GaAs MESFET, SPHEMT, and the DPHEMT devices and shows the higher output power capability of the DPHEMT devices.

The fundamental current control mechanism in the DPHEMT differs significantly from that of the GaAs MESFET [13]. The two devices, in fact, exhibit many extrinsic similarities, but there are several important differences. The main ones are the device I–V and transconductance characteristics. Figure 3.8 shows the I–V characteristics for the DPHEMT device. The most striking attribute of the DPHEMT is that the device’s I_{dssm} is typically twice the I_{dss} value. By contrast, the MESFET might exhibit an I_{dssm} that is 15% to 20% greater than I_{dss} under the same forward gate bias. With both devices, the maximum forward gate bias that can be applied is approximately +1.0V (to avoid driving the gate into forward conduction). Therefore, for accurate first-order predictions of power performance, optimum load line,

Table 3.2 Device Performance Comparisons

Device Type	Gate Length (μm)	Power-Added Efficiency (%)	Power Gain (dB)	Power Density (W/mm)
GaAs MESFET	0.5	25–40	3–5	0.35
SPHEMT	0.25	50–70	10–12	0.4–0.6
DPHEMT	0.25	60–70	8–10	0.85–1.0

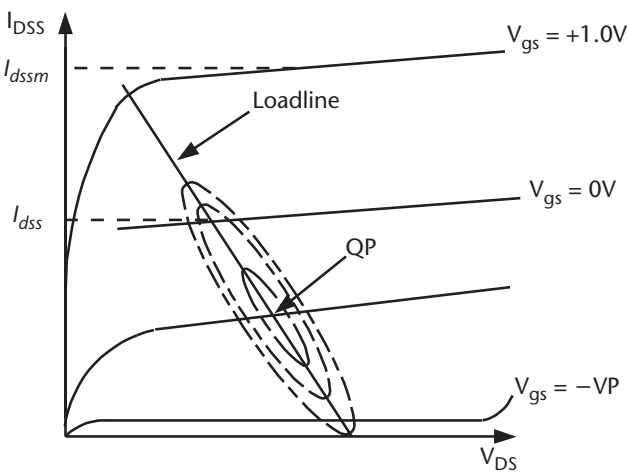


Figure 3.8 DPHEMT drain-source current versus drain-source voltage characteristics.

and selection of a suitable quiescent bias point, the user of the power DPHEMT devices should observe the relationship $I_{dssm} \cong 2I_{dss}$.

Figure 3.9 shows the optimum RF output load impedance required in order to achieve the maximum output power and hence efficiency from a particular device. The arrows point to the I_{dss} current corresponding to the device. It must be noted that as the output power depends on the RF load presented, and the RF load is a function of the operating frequency, hence there are instances when the output power may be lower than the expected maximum case [14–17].

Table 3.3 shows a comparison of the device performances of some common commercially available and compatible devices. It clearly indicates the superior performance that is achievable, in terms of gain, power-added efficiency, and upper operating frequency, with the first four devices (i.e., LPS200, LPD200, LP6836, and LP6872). However, LP1500 and LP3000 outperform the other devices in terms of power. The LPS200 is a 200- μm gate width SPHEMT device designed for low noise amplifier applications. The DPHEMT device LPD200 (200 μm), LP6836 (360 μm), LP6872 (720 μm), LP1500 (1,500 μm), and LP3000 (3,000 μm) are designed for power amplifier applications. The LP1500 and LP3000 devices are designed for applications of up to an octave, whereas the LPS200, LPD200, LP6836, and LP6872 have been designed for multioctave bandwidth applications. All of these devices have gate lengths of 0.25 μm . Hence, the following devices were selected for the broad bandwidth amplifier designs presented in Chapter 6: LPS200, LPD200, LP6836, and LP6872.

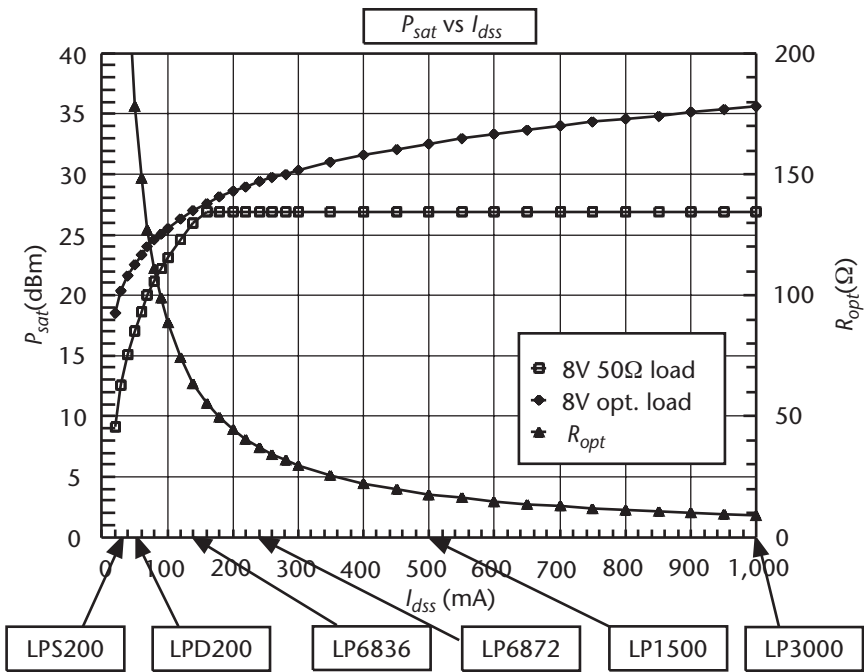


Figure 3.9 Plot of output power and RF load characteristics.

Table 3.3 Device Performance Characteristics

Device Type	Frequency Range (GHz)	Gain (dB)	Power (dBm)	Power-Added Efficiency (%)	Manufacturer
LPS200	1–35	8.5 ¹	10	N/A	Filtronic
LPD200	1–40	11.0 ²	21	60	Filtronic
LP6836	1–30	8.0 ²	25	55	Filtronic
LP6872	1–35	8.0 ²	27	55	Filtronic
LP1500	1–25	7.0 ²	31.5	50	Filtronic
LP3000	1–25	4.0 ²	33.5	45	Filtronic
FHX35X	1–20	7.0 ¹	13	25	Fujitsu
CF003-02	1–26	4.0 ²	20	20	Celeritek
CF003-03	1–26	5.0 ²	20	20	Celeritek
MWT-3	1–26	7.0 ²	20	30	Microwave technology
MWT-6	1–18	6.0 ²	26	30	Microwave technology
MWT-9	1–18	6.0 ²	26	30	Microwave technology
MWT-15	1–26	6.0 ²	24	30	Microwave technology

1. Associated gain at optimum NF, measured at 18 GHz.

2. Power gain, device tuned for optimum power at 18 GHz.

3.4 Summary

The SPHEMT and DPHEMT devices are far more superior to the conventional GaAs MESFET devices in terms of providing high-frequency performance amplifiers with substantially improved gain, output power, and power-added efficiency. The pseudomorphic HEMT structures utilize the AlGaAs/InGaAs heterojunction, rather than the AlGaAs/GaAs combination that is employed in the case of the HEMT device.

The DPHEMT devices exhibit I–V characteristics that are quite different from the conventional GaAs MESFET device I–V characteristics. In particular, the maximum drain-source current I_{dssm} is twice the value of I_{dss} (drain-to-current ratio at $V_{gs} = 0V$). This phenomenon can greatly affect the quiescent point biasing of the device and the first-order prediction of the RF load line for optimizing the amplifier's output match in order to realize maximum output power.

From this discussion, the devices deemed suitable for improving the amplifier's gain and output power performance across a multioctave bandwidth are the following SPHEMT and DPHEMT devices: LPS200, LPD200, LP6836, and the LP6872. These devices were used in the amplifier designs presented in Chapter 6.

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Device Characterization and Modeling

4.1 Introduction

This chapter describes the characterization of SPHEMT and DPHEMT devices in terms of their scattering parameters and the pulsed dc I–V characteristics. The characterization methods described here, however, can be applied to other transistors. It is then shown how the measured S-parameter and the pulsed dc I–V data is used to derive the device’s small-signal and large-signal equivalent circuit models. In particular, the device’s *hot* and *cold* deembedded S-parameter measurements enable the determination of the intrinsic and extrinsic element values constituting the small-signal model. The large-signal device model is determined by using the semiempirical method, as it uses the measured pulsed dc I–V data of the device and no assumptions are made relating to the physical operation of the device itself. This approach is shown to provide an accurate large-signal model. The device models are highly dependent on the accuracy of the measurement techniques employed to characterize the device, as this will ultimately impact the accuracy of the amplifier’s design and hence its performance.

4.2 Device Characterization

The S-parameters are measured on a vector network analyzer, and the accuracy of these measurements is largely dependent on the quality of the analyzer’s calibration. The calibration of this instrument should remove unwanted and repeatable information, such as the effects of nonideal transmission lines, connectors, and circuit parasitic. If all of the unwanted information has been removed, then the measurements should represent the device under test perfectly. However, in practice, this is not totally possible, and some tiny amount of error will inevitably remain uncanceled.

In practice, a major problem encountered when making network analyzer measurements in microstrip or other noncoaxial media is the need to separate the effects of the transmission medium, in which the device is embedded for testing purposes, from the device characteristics. While it is desirable to predict how a device will behave in the environment of its final application, this is very difficult to measure in situ. The accuracy of the device measurements depends on the availability of

quality calibration standards. Unlike coaxial measurements, a set of three distinct impedance standards is often impossible to produce for noncoaxial transmission media. Hence, the thru-reflect-line (TRL) [1, 2] technique is usually preferable, as it relies only on the characteristic impedance of a short transmission line.

This section describes how the physical structure of the TRL standards is established for characterizing active devices. It also includes a brief description on how the standards are used in the two-port calibration procedure prior to the small-signal S-parameter measurements.

4.2.1 Basis of Calibration

The characterization of active devices described in this chapter was carried out using the HP8510 vector network analyzer, shown in Figure 4.1. This instrument measures the amplitude ratio and the relative phase of two broadband swept signals. By using dual directional couplers, the instrument is able to separate the incident and reflected waves in a transmission line, thereby enabling the measurement of the impedance and the gain of RF and microwave circuits. The network analyzer measurements are based on S-parameter principles that are the accepted standards in the high frequency industry [3]. The errors associated with the S-parameter measurements on a network analyzer can affect the measurement accuracy. These errors are attributed to systematic and random errors [4].

Systematic errors are those that are stable and repeatable and can be identified, characterized, and removed from the measurement system. For a full two-port set of

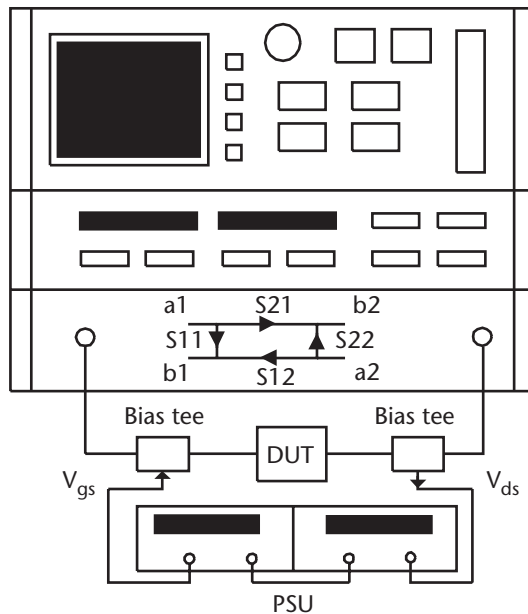


Figure 4.1 Test set up for device characterization and measurements employing the HP8510 vector network analyzer.

S-parameters, such errors include coupler directivity, source and load mismatch, transmission and reflection tracking, and finite port isolation. These errors can be measured then removed from the measurement with the built-in error-correction techniques of the network analyzer.

Random errors are those that are random in nature and cannot be characterized and removed, such as noise, drift, and connector repeatability. The noise encountered in any measurement system is mainly due to low level (system noise floor) and phase noise of the source (or high-level noise). The drift error is largely due to temperature variations in the measurement environment. Although these errors cannot be entirely removed, they can be minimized by averaging the measurements, reducing the IF bandwidth or recalibrating the network analyzer.

Two-port components are generally measured in test fixtures, which add complexity to the measurement system. A calibration at the coaxial ports of the network analyzer removes the effects of the network analyzer and any cables or adapters before the test fixture. However, the effects of the test fixture are not accounted for. To eradicate completely the effects of the test fixture from the measurement, the method of *in-fixture calibration* provided by the TRL method of calibration needs to be employed [5].

The TRL is a two-port calibration procedure that relies on transmission lines rather than a set of discrete impedance standards. The key advantages of using transmission lines as reference standards are:

- Transmission lines are among the simplest elements to realize in many non-coaxial media.
- The impedance of transmission lines can be accurately determined from the physical dimensions and materials.
- Transmission lines have traditionally been used as standards and are well understood.

The basic TRL calibration procedure consists of three steps, *thru*, *reflect*, and *line*. The thru step is performed when the test ports are directly mated together. This allows the measurement of the transmission response and the port match in both directions over the frequency range of interest. In the reflect step, a short or open circuit is connected to each of the test ports, and the reflection coefficient is measured. The final line step involves the measurement of the frequency response and port match with a short transmission line inserted between the test ports.

4.2.2 Microstrip Test Fixture and Calibration Standards

In order to carry out the TRL calibration in microstrip, a custom-made test fixture is needed whose design is based on the *split-block* approach. This is necessary, as one of the main requirements in the calibration process is the need to insert the test device and the calibration standards, which are of dissimilar physical lengths between the two halves of the test fixture. Figure 4.2 shows the test fixture, where

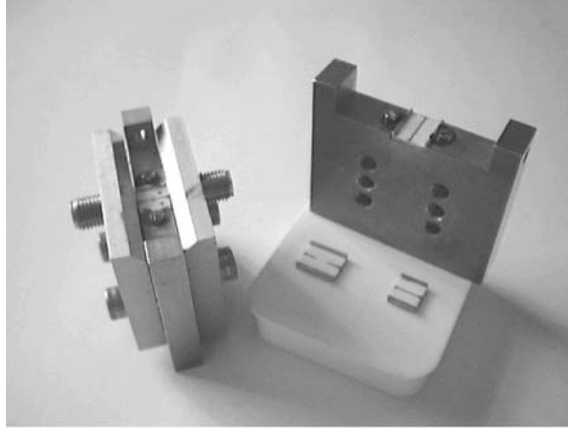


Figure 4.2 TRL calibration fixture and calibration pieces.

the TRL calibration standards shown were fabricated on Alumina substrate with dielectric constant of 9.8, substrate thickness of 0.381 mm, and a gold-plated thickness of 5 μm . When the test fixture is calibrated, adequate separation between the coaxial and microstrip launchers is essential during the thru and line measurements to prevent the generation of the dominant and higher order modes. Otherwise, the coupling of these higher order modes between the launchers will produce spurious variations during the error-corrected measurements. In practice, a minimum of two wavelengths is necessary between the launchers.

As the signal propagating through the microstrip is approximated to a quasi-TEM wave, some of the signal will be supported by the electric fields above the microstrip surface. Hence, if the electric fields in the fixture are perturbed between the calibration and measurement process, then the propagation characteristics of the microstrip transmission line will alter, too. Consequently, nonsystematic errors are introduced, which cannot be removed through the analyzer's error-correction techniques. Therefore, in order to minimize this effect, the test environment should be the same during calibration and device measurement.

The sidewalls of the test fixture need to be considered, too, as the sidewalls could behave as a resonant cavity, which can affect the measurements. To prevent propagation of unwanted modes, the size of the cavity is made small enough so that the resonant frequency is above the range of the measurement. For resonance-free operation under dielectric loading, the width of the cavity can be calculated using

$$w_c = c/2f\epsilon_{eff} \quad (4.1)$$

where

- c = speed of light (m/s);
- f = upper frequency of the calibration range (Hz);
- ϵ_{eff} = effective dielectric constant of the substrate.

The various calibration standards are shown in Figure 4.3. The thru standard is specified as having a zero phase delay, so that the reference plane is established at the middle of the thru. Test devices that are mounted on center blocks are connected directly at this calibration plane. The length chosen for the thru is 5.94 mm with a line width of 0.36 mm corresponding to 50- Ω line fabricated on a 0.381-mm-thick Alumina substrate with a dielectric constant of 9.8. The most simple standard is the reflect, as this is an open circuit; however, a short circuit could be employed if significantly more energy is radiated than reflected at the open circuit. The line standard is a short microstrip line whose length is calculated to be the thru line length plus the optimal length of one quarter wavelength relative to the thru at the center frequency of the measurement range. An additional requirement in the calibration is that the insertion phase difference between the thru and the line should be 20° to 160° [5]. As the frequency range for calibration and device measurement is 2 to 20 GHz, the guide wavelength λ_g at the center frequency can be calculated using

$$\lambda_g = c/f\sqrt{\epsilon_{eff}} \quad (4.2)$$

where

c = speed of light 3×10^8 m/s;

f = center frequency of the calibration frequency range (Hz);

ϵ_{eff} = effective dielectric constant of the substrate.

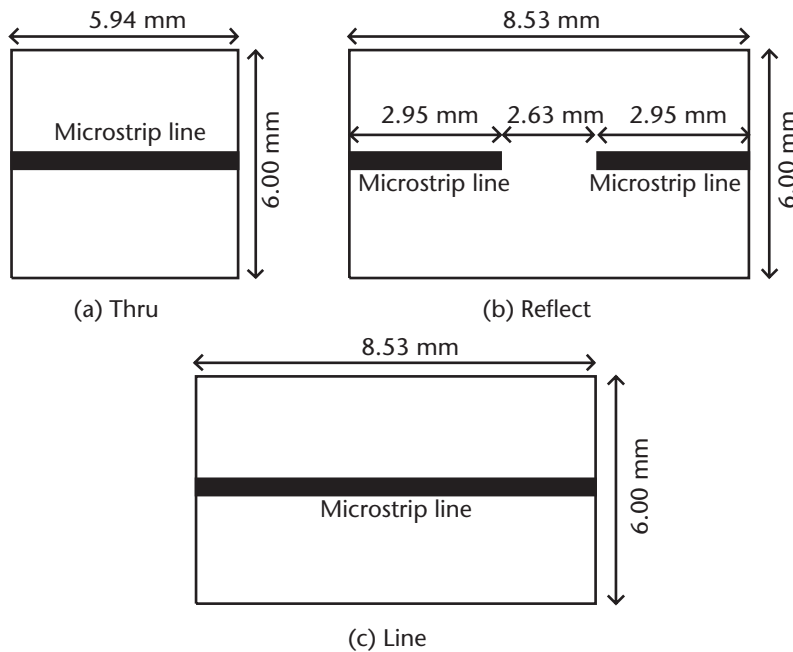


Figure 4.3 TRL calibration standards: (a) Thru, (b) reflect, and (c) line.

For the specified Alumina substrate ($\epsilon_r = 9.8$ and $h = 0.381$ mm), $\epsilon_{eff} = 6.693$, so $\lambda_g/4 = 2.63$ mm. Therefore, the electrical delay τ associated with this length is calculated to be 22.68 ps using

$$\tau = \lambda_g \sqrt{\epsilon_{eff}} / 4c \quad (4.3)$$

The phase associated with the length 2.63 mm is given by

$$\theta = (360 \times 2.63) / \lambda_g \quad (4.4)$$

The guide wavelength calculated using (4.2) at 2 GHz and 20 GHz are 58.81 mm and 5.69 mm, respectively. Therefore, the corresponding phase at 2 GHz is 16.10° , and at 20 GHz, it is 166.4° . Although the insertion phase difference is slightly outside the required range for TRL calibration, it is still within the practically acceptable limit. The reflect standard consists of two open-circuit transmission lines of length 2.95 mm, which are separated by 2.63 mm, as shown in Figure 4.3(b). The physical line length of the line standard is set to 8.53 mm, as shown in Figure 4.3(c).

Once the TRL calibration standards are established, the HP8510 vector network analyzer can then be calibrated by changing the definitions of the analyzer's calibration kit. A mathematical description [5] of each of the standards derived here is entered into the network analyzer. Each of the standards must be defined in terms of the coefficients required by the *standard definition table*. After defining the standards, each of the standards must be assigned to a class. Thereafter, the TRL calibration procedure can then be performed using the test fixture, shown in Figure 4.2.

4.2.3 Small-Signal Measurements

The S-parameters of an active device were measured using a custom-made device test carrier, shown in Figure 4.4, which was constructed from copper-tungsten material that is gold plated. The input and output of the test carrier consists of 50- Ω lines fabricated on Alumina substrate, which is attached onto the carrier using gold/tin (composition 80/20) solder. The device itself is soldered onto a gold-plated mounting post that is positioned in the middle of the test carrier. The mounting post is designed to accommodate the device and the associated source decoupling capacitors. Figure 4.5 shows the assembled test carrier with the DPHEMT device LP6872.

The HP8510 vector network analyzer set up for measuring the S-parameters, shown in Figure 4.1, comprised of the TRL test fixture and the device test carrier. The gate-source and drain-source bias is supplied through broadband bias tees, using a dual power supply. The active device's S-parameters were measured at the reference planes indicated in Figure 4.4, having first calibrated the analyzer, as described earlier. As these measurements include the gate and drain bond wires, the small-signal equivalent model will also include the device's extrinsic elements.

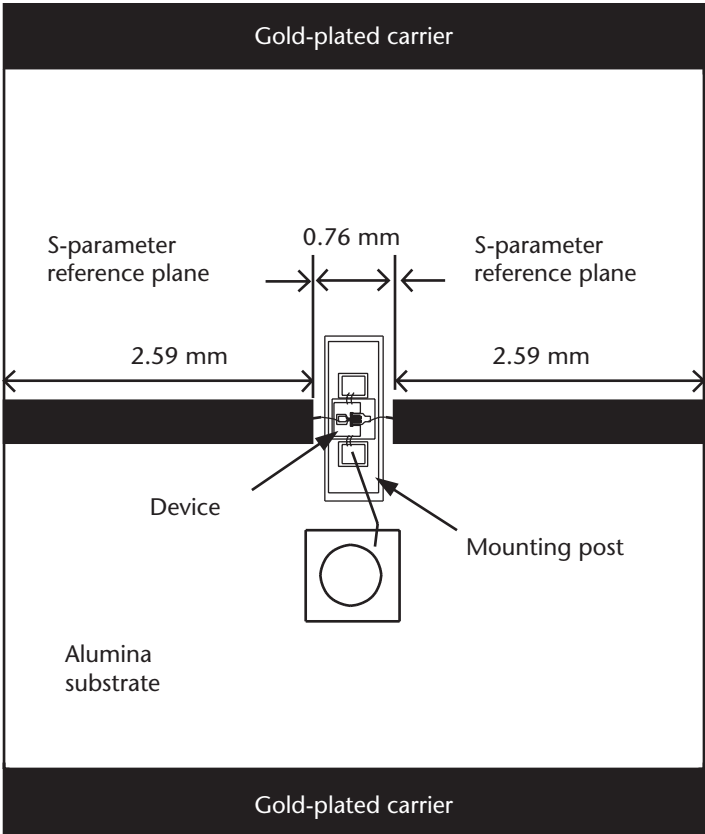


Figure 4.4 Device test carrier.

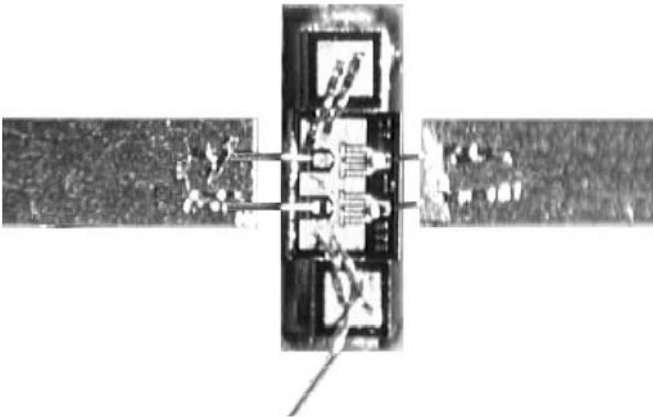


Figure 4.5 Device LP6872 assembled test carrier.

Hot S-parameter measurements [6] were made over the frequency range of 2 to 20 GHz at specific bias points (i.e., $V_{ds} = 3\text{V}$ at $0.5I_{dss}$ for LPS200; $V_{ds} = 4\text{V}$ at $0.5I_{dss}$ for LPD200; $V_{ds} = 8\text{V}$ at $0.5I_{dss}$ for LP6836; and $V_{ds} = 8\text{V}$ at $0.5I_{dss}$ for LP6872. The S_{11} , S_{22} , and S_{21} measurements for these devices, shown in Figures 4.6– 4.13, enable the intrinsic elements of the small-signal equivalent model to be determined.

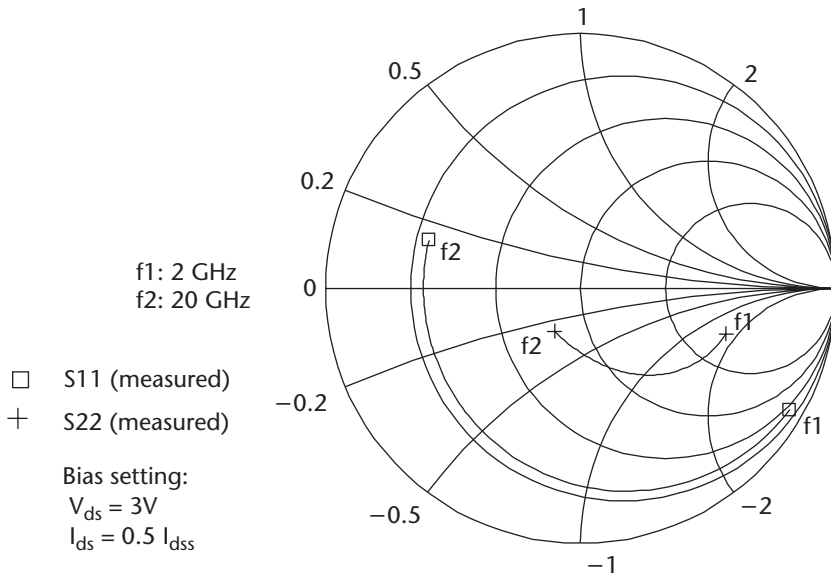


Figure 4.6 Device LPS200 measured hot S_{11} and S_{22} .

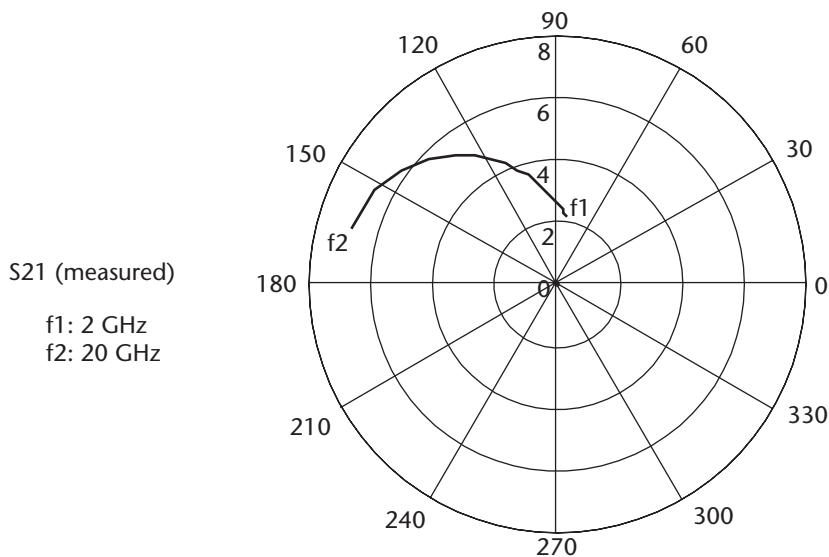


Figure 4.7 Device LPS200 measured hot S_{21} .

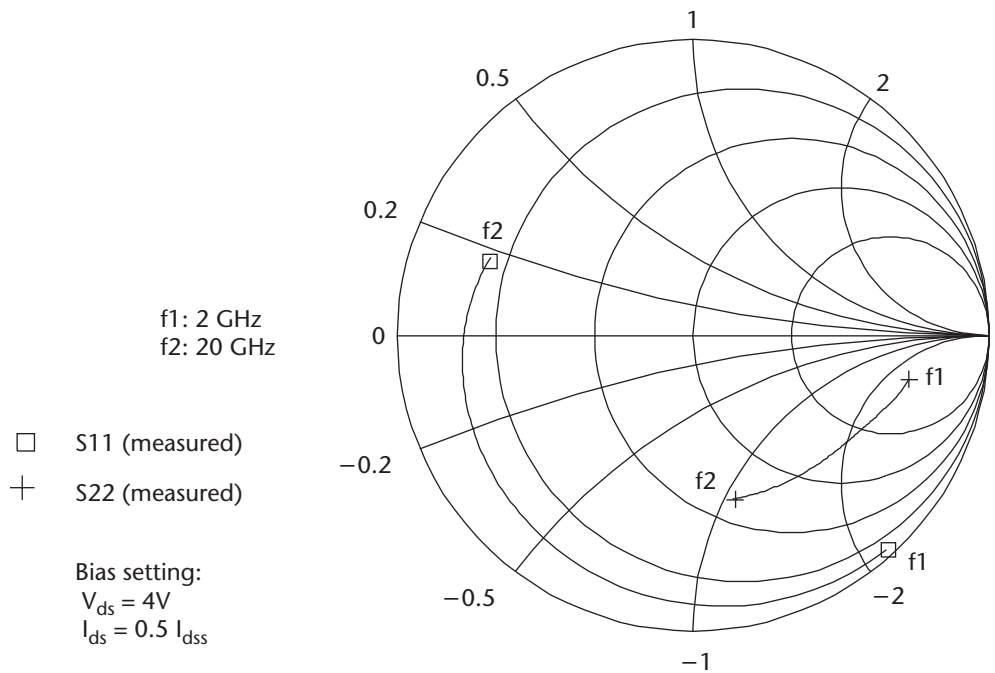


Figure 4.8 Device LPD200 measured hot S_{11} and S_{22} .

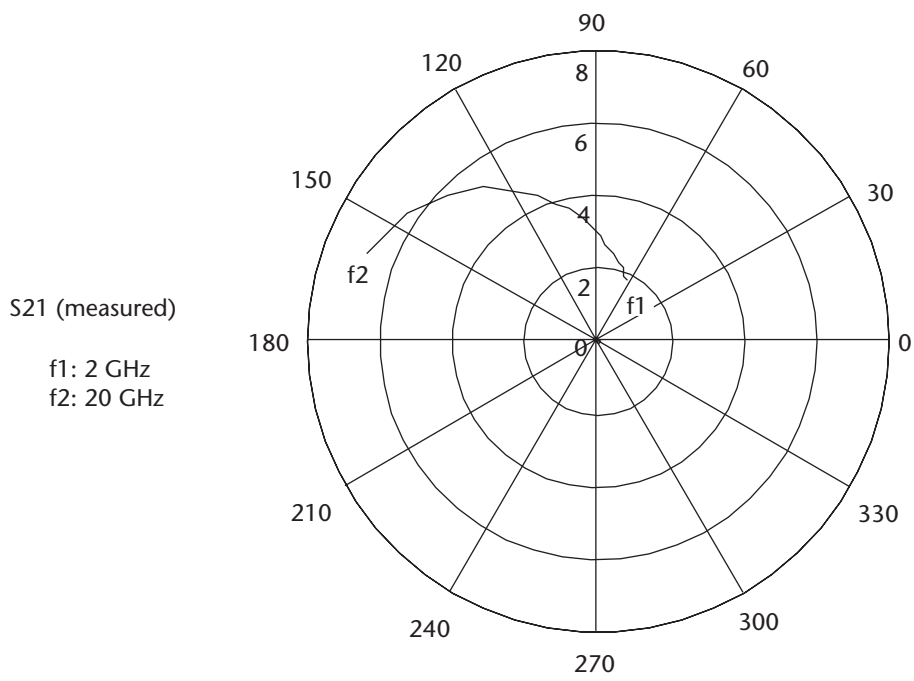


Figure 4.9 Device LPD200 measured hot S_{21} .

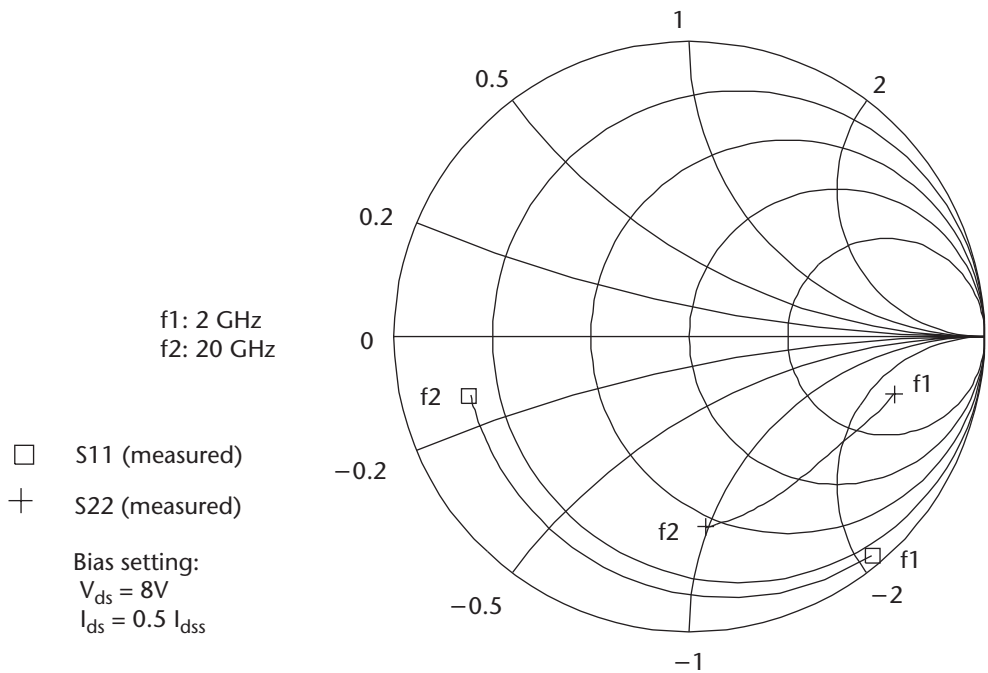


Figure 4.10 Device LP6836 measured hot S_{11} and S_{22} .

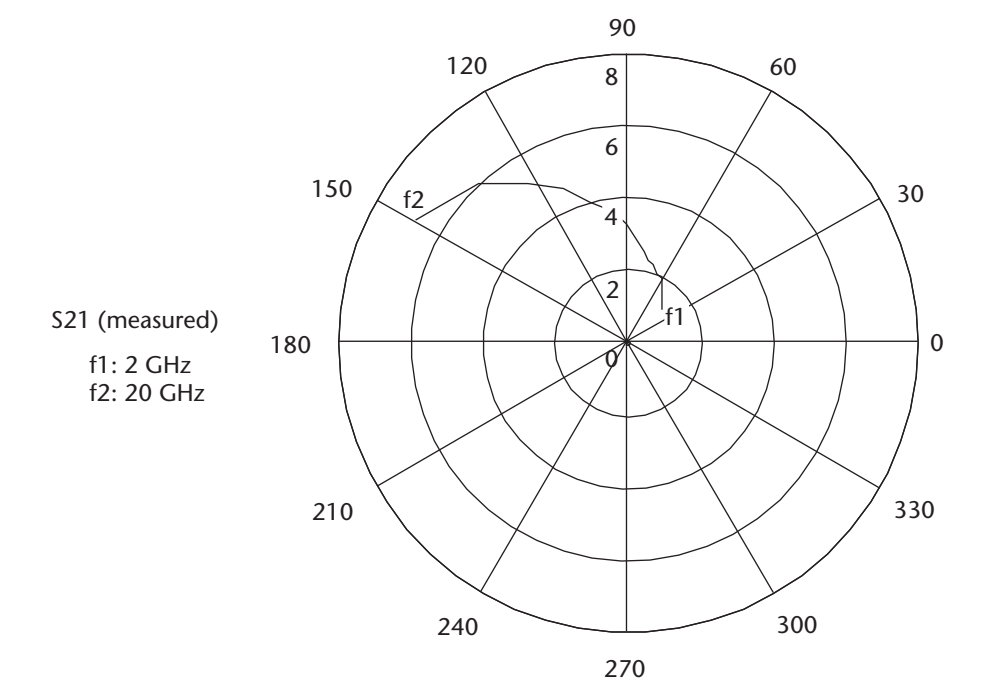


Figure 4.11 Device LP6836 measured hot S_{21} .

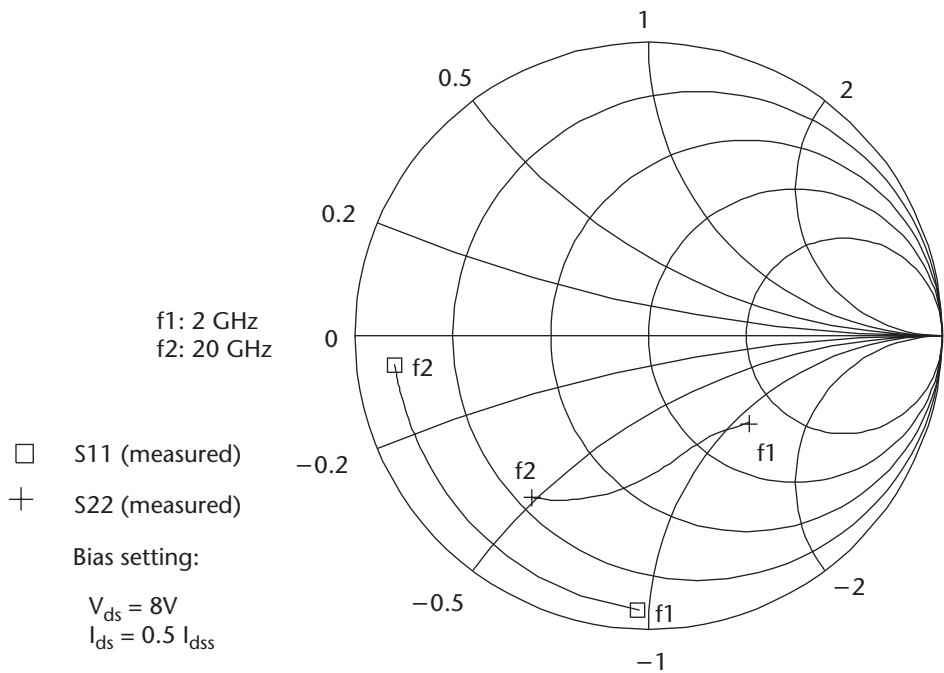


Figure 4.12 Device LP6872 measured hot S_{11} and S_{22} .

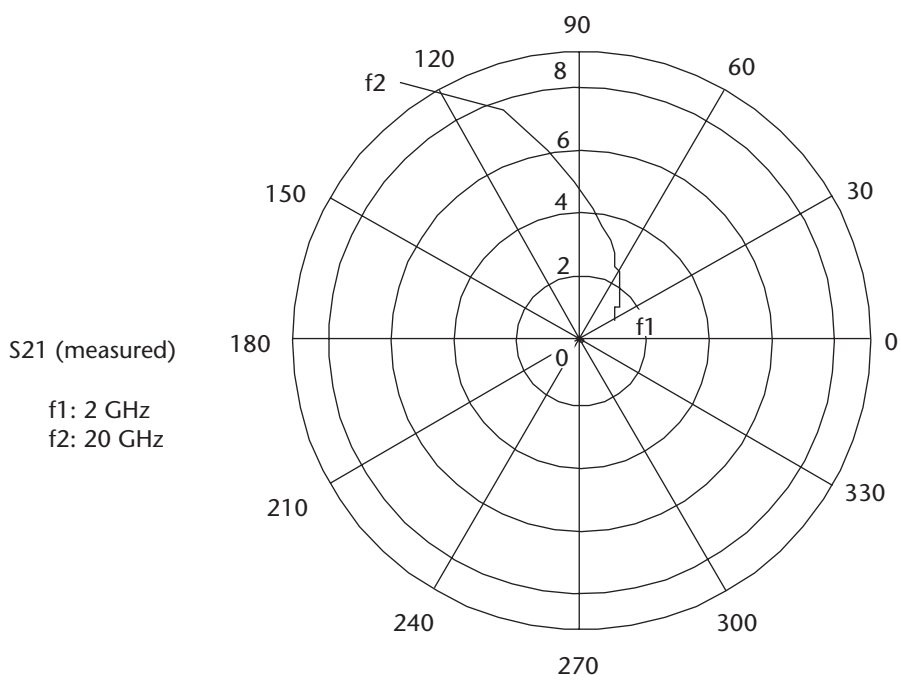


Figure 4.13 Device LP6872 measured hot S_{21} .

Cold S-parameter measurements [7, 8] were also made over the same frequency range with the devices biased at the drain-source voltage V_{ds} of 0V, and the gate-source voltage V_{gs} set at the device's pinch-off (i.e., -3V). This condition enables the extrinsic elements of the small-signal equivalent model to be ascertained. The measured S_{11} and S_{22} of LPS200, LPD200, LP6836, and LP6872 devices are shown in Figures 4.14 to 4.17.

4.2.4 Pulsed dc I-V Measurements

The large-signal model, which is extracted from the measured static dc I-V data, does not fully describe the behavior of the device characterized at RF. This is because the temperature and dispersion effects introduce a discrepancy between the dc and RF transconductance as well as the output conductance. A common explanation of this is due to traps and surface states [9, 10] in the semiconductor that affect the performance of the device. However, a better large-signal model can be extracted when the dc characteristics are obtained by using pulsed measurements [11]. This is valid as long as the pulses are kept short and the pulse period is shorter than the mean lifetime of the traps, so that the device characteristics are not affected by the traps.

The dc pulsed $I_{ds}-V_{ds}$ and $I_{ds}-V_{gs}$ measurements were performed on the devices LPD200, LP6836, and LP6872 by using the HP4145B parameter analyzer. The block diagram of the pulsed set up is as shown in Figure 4.18. The devices were pulsed for a short period of 1 μ s into the active region and were then held in the

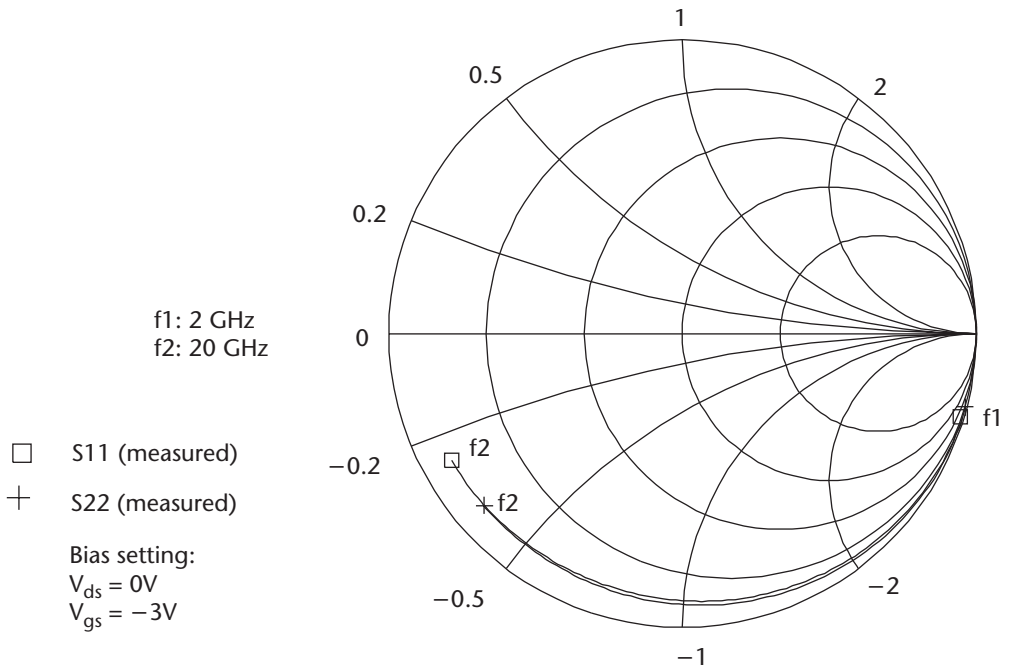


Figure 4.14 Device LPS200 measured cold S_{11} and S_{22} .

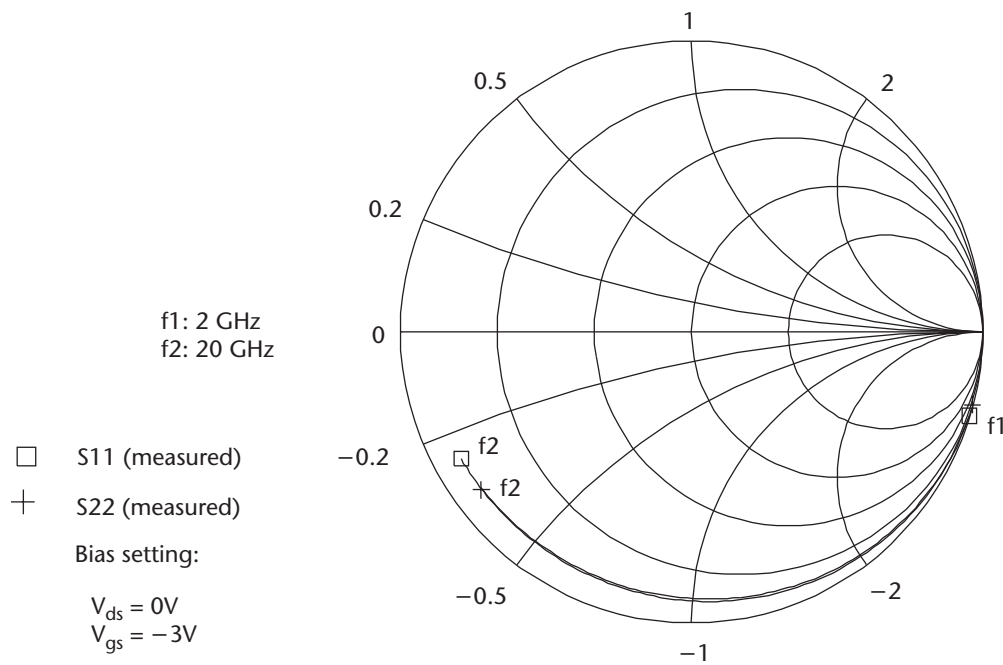


Figure 4.15 Device LPD200 measured cold S_{11} and S_{22} .

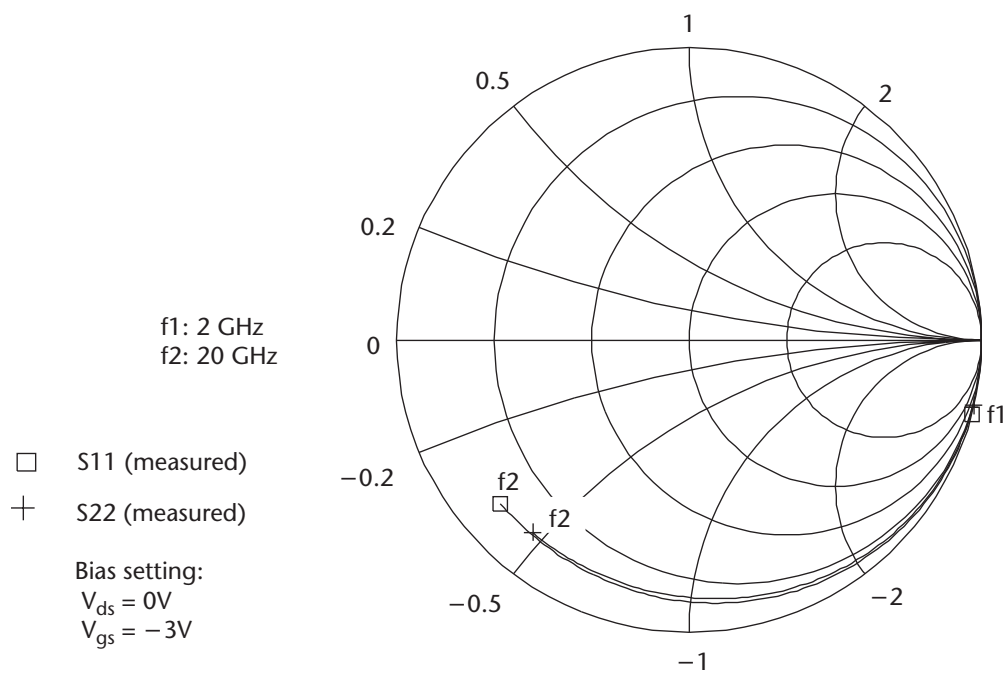


Figure 4.16 Device LP6836 measured cold S_{11} and S_{22} .

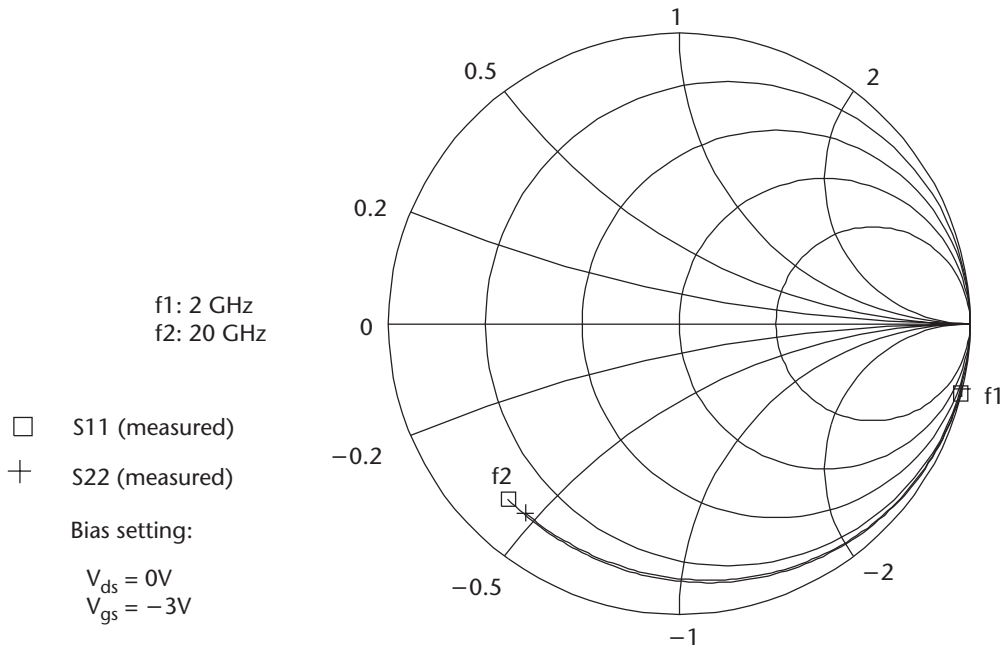


Figure 4.17 Device LP6872 measured cold S_{11} and S_{22} .

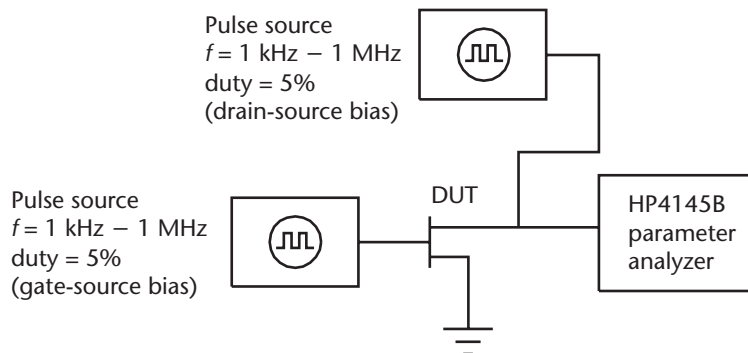


Figure 4.18 Pulsed $I_{ds}-V_{ds}$ and $I_{ds}-V_{gs}$ measurement setup.

passive cut-off region for the rest of the period, typically 1 ms. In the measurement set up, a 5-sec pause was used between each measured trace in order to allow cooling of the device between the sweeps. The pulsed dc isothermal $I_{ds}-V_{ds}$ and $I_{ds}-V_{gs}$ characteristics measured for these three devices are shown in Figures 4.19–4.24. The measured characteristics exhibit a positive output conductance over the entire bias range considered.

The dc static $I_{ds}-V_{ds}$ measurements were also performed on these devices. The measured results for these devices, shown in Figures 4.25–4.27, indicate significant distortion in the form of drooping in the dc curves at high gate-source voltages V_{gs} .

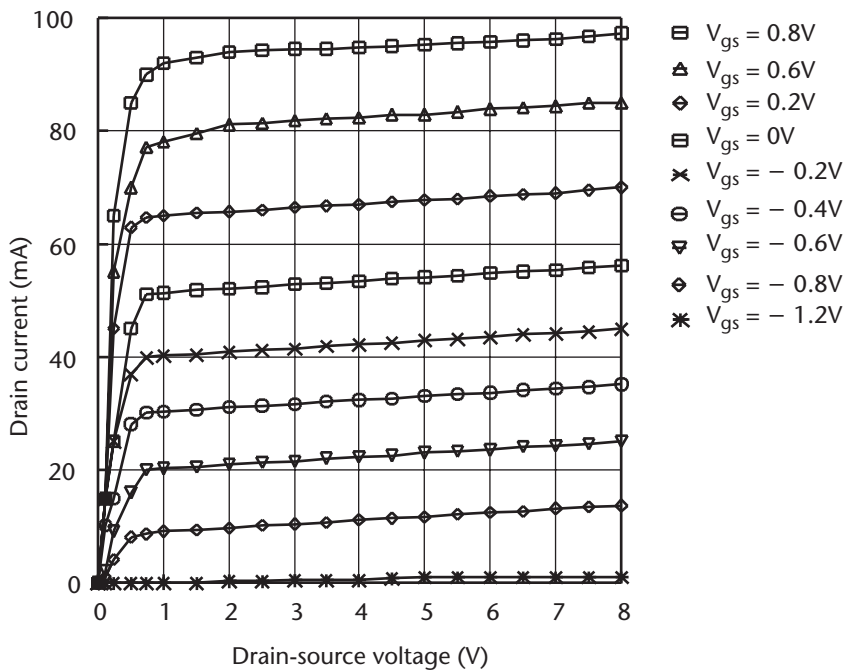


Figure 4.19 Measured pulsed dc I_{ds} - V_{ds} of device LPD200.

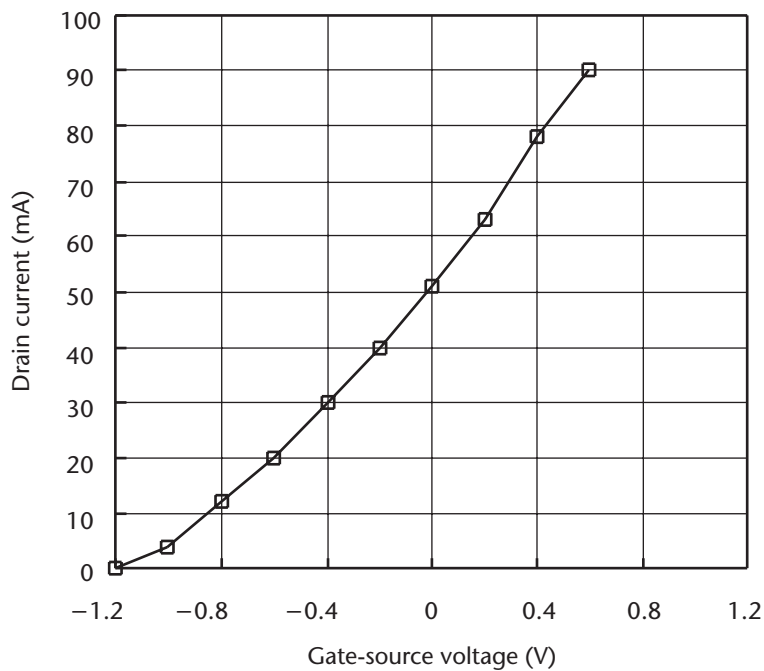


Figure 4.20 Measured pulsed dc I_{ds} - V_{gs} of device LPD200.

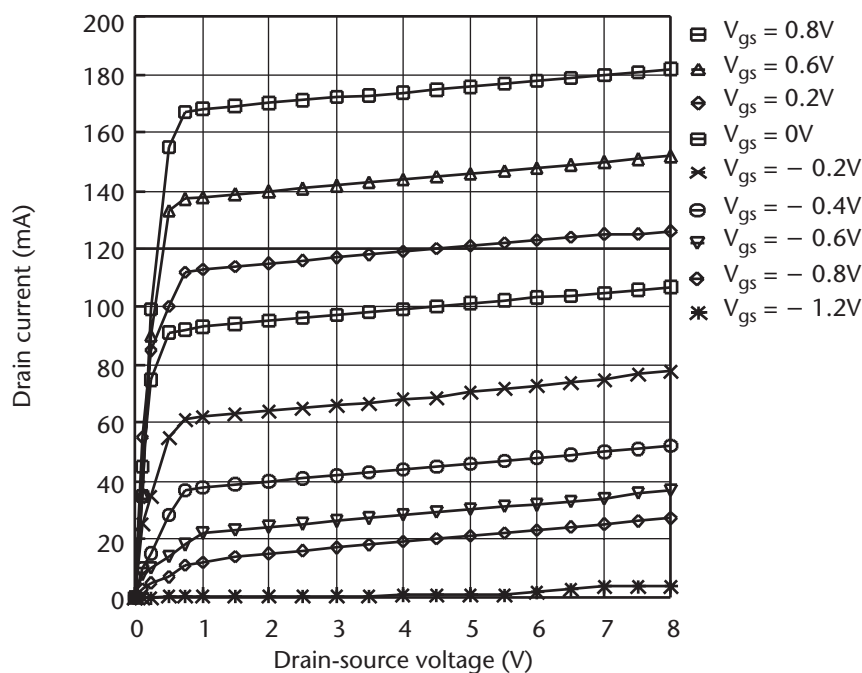


Figure 4.21 Measured pulsed dc I_{ds} - V_{ds} of device LP6836.

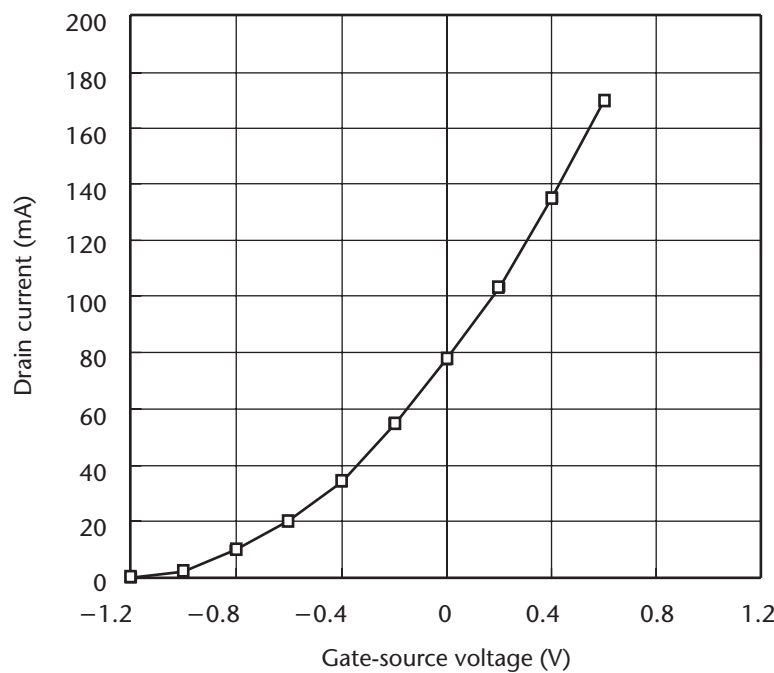


Figure 4.22 Measured pulsed dc I_{ds} - V_{gs} of device LP6836.

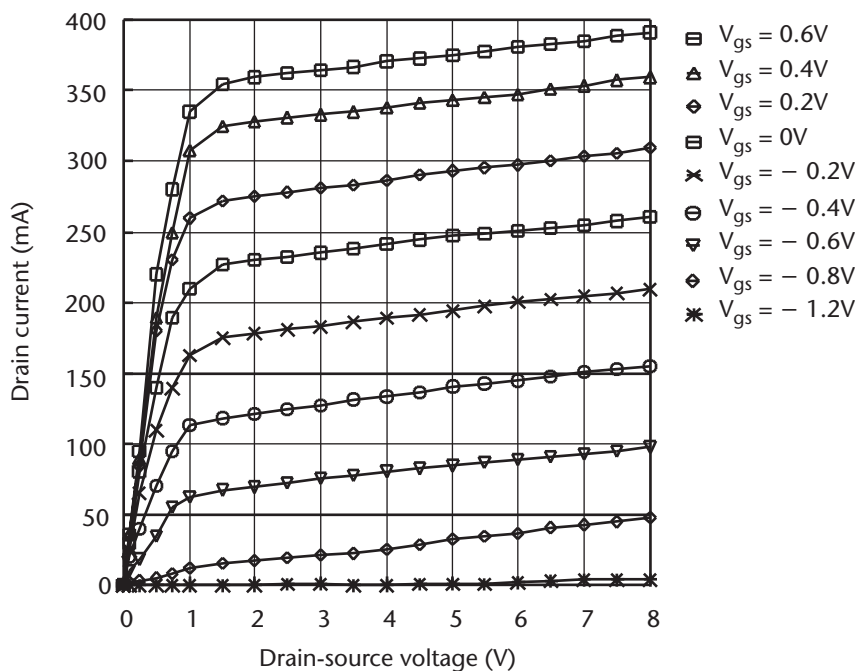


Figure 4.23 Measured pulsed dc I_{ds} - V_{ds} of device LP6872.

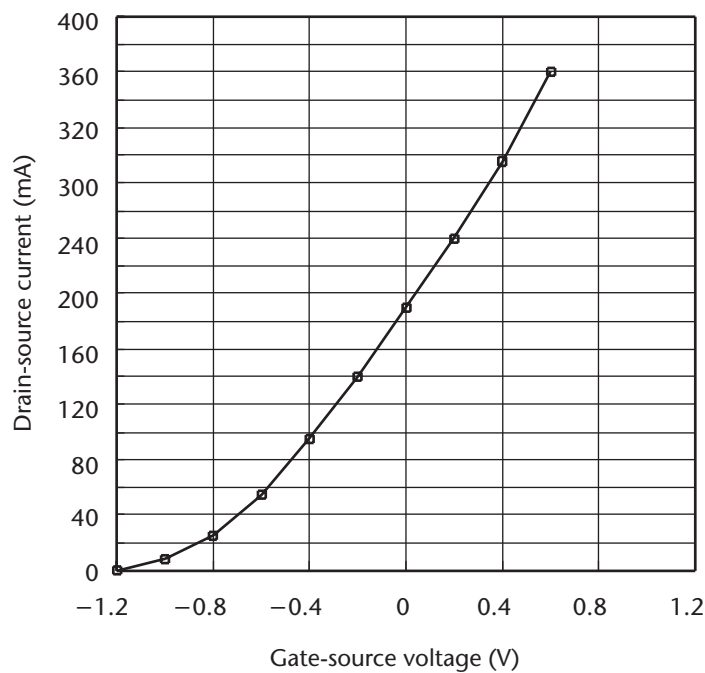


Figure 4.24 Measured pulsed dc I_{ds} - V_{gs} of device LP6872.

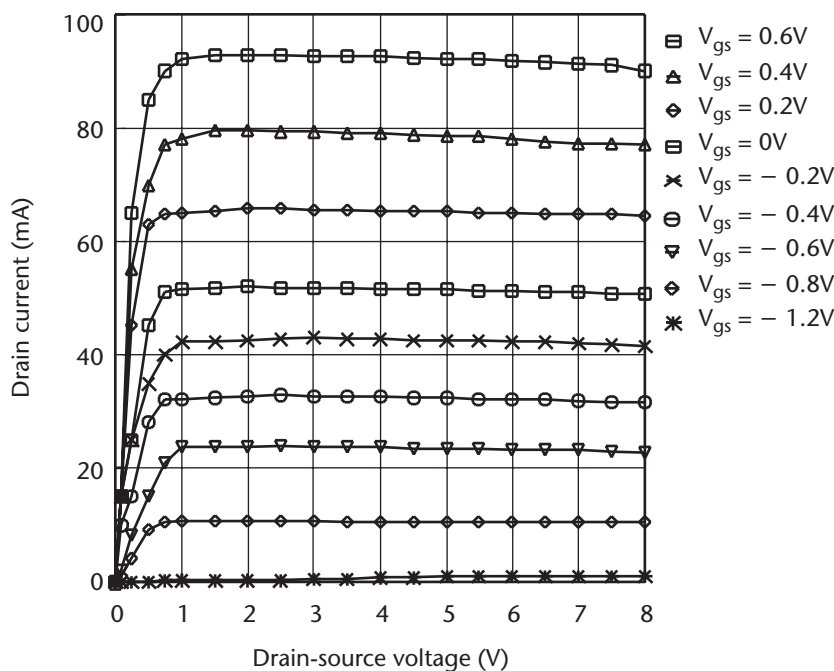


Figure 4.25 Measured static dc I_{ds} - V_{ds} of device LPD200.

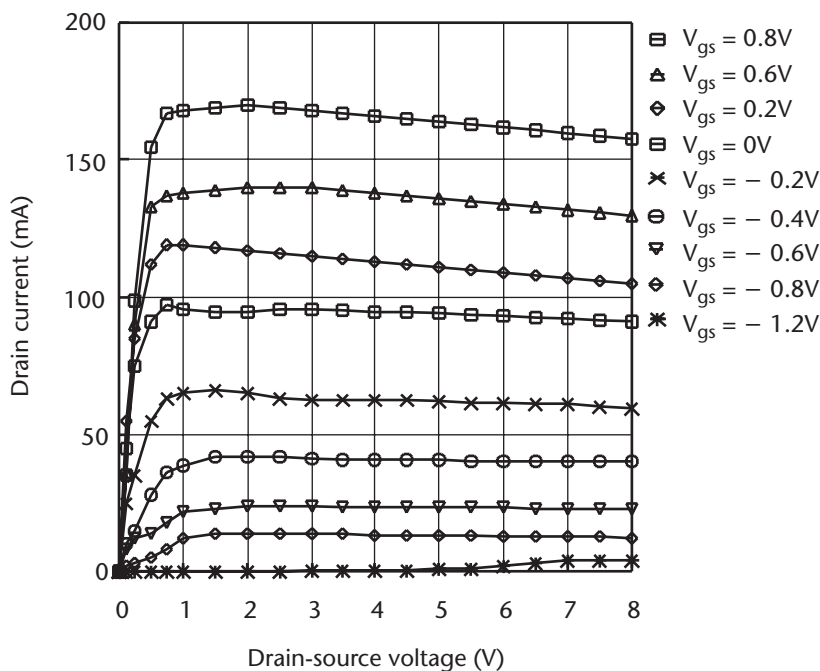


Figure 4.26 Measured static dc I_{ds} - V_{ds} of device LP6836.

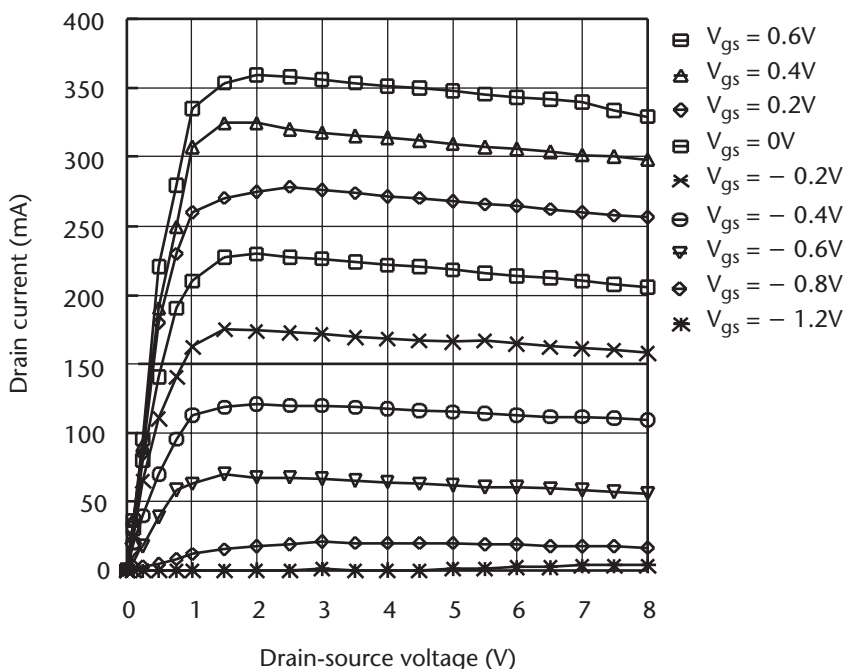


Figure 4.27 Measured static dc I_{ds} - V_{ds} of device LP6872.

due to thermal effects. This gives rise to negative output conductance values, and if this data is used to obtain the large-signal equivalent circuit model, significant error will result in the amplifier design. Therefore, for greater accuracy, the measured pulsed dc I_{ds} - V_{ds} and I_{ds} - V_{gs} data is used to achieve a best fit with the appropriate large-signal model available in standard microwave CAD packages, which is described in Section 4.4. This large-signal model is essential to accurately analyze and optimize the amplifier design.

4.3 Small-Signal Device Modeling

This section describes how the small-signal equivalent circuit model representing the SPHEMT (LPS200) and DPHEMT (LPD200, LP6836, and LP6872) devices were obtained using the S-parameter data measured in the last section. The analytical method employed provides a simple and practical means of extracting the device's intrinsic element values from the hot S-parameter measurements and the extrinsic element values from the cold S-parameter measurements. The model derived is then optimized so that it fits to the measured data as accurately as possible using a commercial microwave CAD package. The accuracy of the model is paramount to analyze and optimize the amplifier design for broadbandwidth performance.

4.3.1 Principle of Model Extraction Procedure

The procedure for obtaining the small-signal model is shown in the flowchart of Figure 4.28. The process begins with measurement of the hot and cold S-parameters, which are deembedded from the test fixture in order to obtain the device S-parameters. The deembedded hot and cold device S-parameters are used to calculate the intrinsic and extrinsic component values of the small-signal equivalent circuit model representing the device. The model is optimized using a microwave CAD package to achieve an accurate fit to the deembedded device S-parameters.

Determination of the small-signal equivalent circuit is the first step for obtaining the device model. The accuracy of the model is based on minimizing the error function used in the CAD optimization [12] to match the S-parameters of the equivalent circuit model with the actual measurements over the required frequency range. The optimization can be implemented either numerically [12–14] or analytically [14–21]. Unlike the analytical method, one of the main problems encountered with the numeric method is the determination of suitable starting values for the optimization. Depending on these starting values, the final equivalent circuit values may lack any physical meaning, even with low optimization error functions (e.g., the extrinsic resistance values can often tend to vanish independent of their starting values).

Two types of equivalent circuit models are commonly used to represent an intrinsic device: the seven-element model [13, 17] and the eight-element model [12, 18–21]. Contrary to the eight-element model, the seven-element model does not account for the observed positive reverse transfer conductance, which may occur

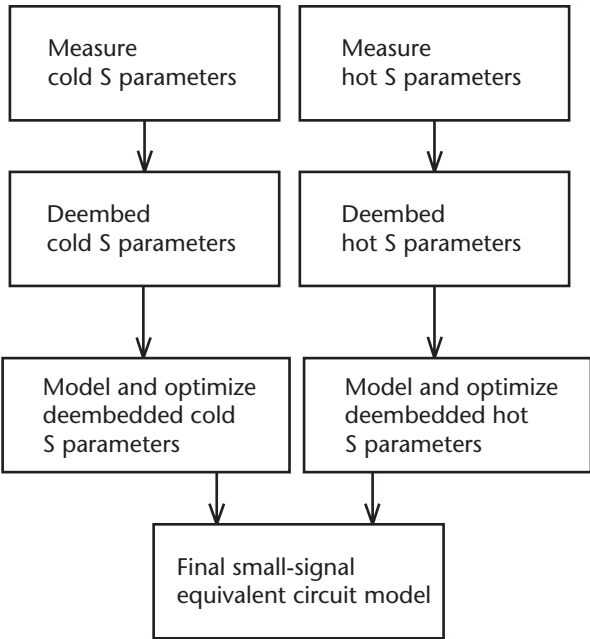


Figure 4.28 Small-signal device modeling procedure.

due to the lack of a gate-to-drain channel feedback capacitance. The eight-element model is further categorized into model 1 and model 2. In model 1, sometimes called the Curtice model [12], the control voltage V_g is defined across C_{gs} and R_i , while in model 2, V_g is defined across just C_{gs} . The analytical parameter extraction method [20, 21] also takes into account the gate and drain bond-pad capacitance (C_{pg} and C_{pd}) in the modeling process.

The equivalent device circuit model, shown in Figure 4.29, consists of 16 elements in total, comprising of eight intrinsic and eight extrinsic elements. The intrinsic parameters include t , g_m , C_{gs} , C_{gd} , R_i , R_{ds} , C_{ds} , and C_{dc} . The dipole layer capacitance C_{dc} is represented with a dotted line, as it is normally omitted in the model due to its negligible value. The extrinsic parameters include C_{gp} , C_{dp} , L_g , L_d , R_g , R_s , and R_d .

4.3.2 Extraction of Cold Component Values

The extrinsic component values of the small-signal model can be analytically obtained from the measured deembedded cold S-parameters. The analytical equivalent circuit [20, 21] of the device biased in the pinched-off condition (i.e., cold device) is represented by Figure 4.30. The capacitors C_a , C_b , and C_c represent the

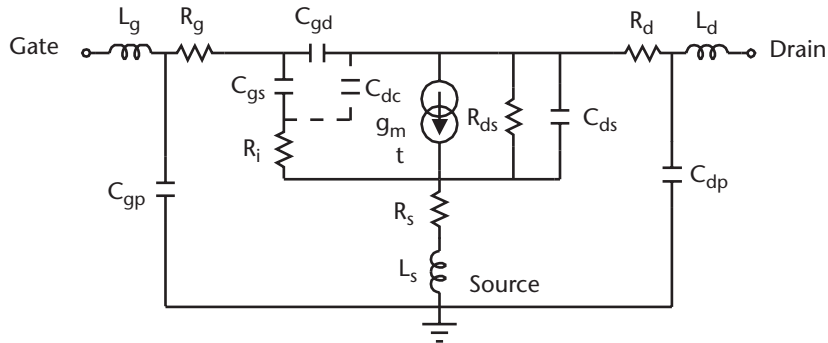


Figure 4.29 Small-signal model.

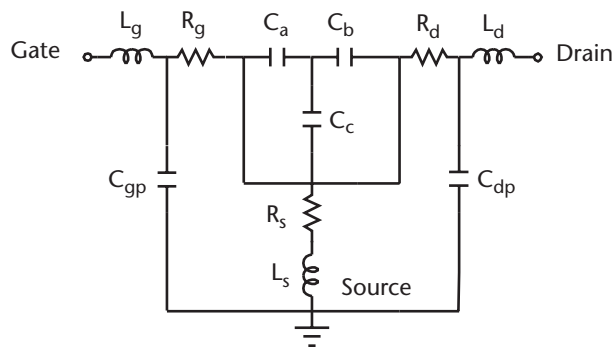


Figure 4.30 Cold small-signal model.

fringing capacitance due to depletion layer extension at each side of the gate. Inductors L_g and L_d represent the inductance associated with the bond-wire connection at the gate and drain, respectively. Resistors R_g and R_d represent the device's gate and drain resistance, respectively. The source resistance and inductance are represented by R_s and L_s , respectively. This circuit preserves the symmetry of the device when viewed from the gate and drain sides of the device. The Z-parameters Z_{cij} corresponding to the device's deembedded cold S-parameters are represented by

$$Z_{C11} = R_g + R_s + j[\omega(L_g + L_s) + 1/\omega C_{ab}] \quad (4.5)$$

$$Z_{C12} = Z_{C21} = R_s + j[\omega L_s - 1/\omega C_b] \quad (4.6)$$

$$Z_{C22} = R_d + R_s + j[\omega(L_d + L_s) - 1/\omega C_{bc}] \quad (4.7)$$

where

$$C_{ab}^{-1} = C_a^{-1} + C_b^{-1} \text{ and } C_{bc}^{-1} = C_b^{-1} + C_c^{-1} \quad (4.8)$$

From (4.5)–(4.7) we then have

$$R_g = \text{Re}(Z_{C11} - Z_{C12}) \quad (4.9)$$

$$R_s = \text{Re}(Z_{C12}) \quad (4.10)$$

$$R_d = \text{Re}(Z_{C22} - Z_{C12}) \quad (4.11)$$

$$\omega \text{Im}(Z_{C11}) = \omega^2 (L_g + L_s) - 1/C_{ab} \quad (4.12)$$

$$\omega \text{Im}(Z_{C12}) = \omega^2 L_s - 1/C_b \quad (4.13)$$

$$\omega \text{Im}(Z_{C22}) = \omega^2 (L_d + L_s) - 1/C_{bc} \quad (4.14)$$

Equations (4.9)–(4.11) enable the component values of R_g , R_s , and R_d to be determined at each of the measured frequencies from the Z-parameters. Table 4.1 gives these extrinsic component values, which are valid across the 2- to 18-GHz frequency range, for devices LPS200, LPD200, LP6836, and LP6872.

Equations (4.12)–(4.14) enable the inductances corresponding to L_g , L_d , and L_s to be computed from the gradients of $\omega \text{Im}(Z_{C11})$, $\omega \text{Im}(Z_{C12})$, and $\omega \text{Im}(Z_{C22})$ against

Table 4.1 Extracted Component Values R_g , R_d , and R_s

Extrinsic Component	LPS200	LPD200	LP6836	LP6872
R_g	2.52Ω	0.22Ω	1.43Ω	1.20Ω
R_d	0.95Ω	4.85Ω	0.52Ω	0.64Ω
R_s	0.95Ω	0.11Ω	1.86Ω	0.27Ω

ω^2 plots, as well as the capacitors C_a , C_b , and C_c . These component values for devices LPS200, LPD200, LP6836, and LP872, which are valid across the 2- to 18-GHz frequency range, are given in Table 4.2.

4.3.3 Extraction of Hot Components Values

The intrinsic component values of the small-signal model representing the active device is analytically obtained from the measured deembedded hot S-parameters. The analytical equivalent circuit of the device biased at the nominal operating point is shown in Figure 4.31.

Therefore the Y-parameters Y_{cij} corresponding to the hot device are

$$Y_{11} = R_i C_{gs}^2 \omega^2 / D + j\omega (C_{gs} / D + C_{gd}) \quad (4.15)$$

$$Y_{12} = -j\omega C_{gd} \quad (4.16)$$

$$Y_{21} = g_m e^{-j\omega\tau} / (1 + j\omega R_i C_{gs}) - j\omega C_{gd} \quad (4.17)$$

$$Y_{22} = g_{ds} + j\omega (C_{ds} + C_{gd}) \quad (4.18)$$

where

$$D = 1 + R_i C_{gs}^2 \omega^2 \quad (4.19)$$

Table 4.2 Extracted Extrinsic Component Values

Extrinsic Component	LPS200	LPD200	LP6836	LP6872
C_a, C_b, C_c	0.21 pF	0.21 pF	0.32 pF	0.55 pF
L_g	0.095 nH	0.095 nH	0.0181 nH	0.0102 nH
L_d	0.095 nH	0.095 nH	0.053 nH	0.028 nH
L_s	0.039 nH	0.039 nH	0.041 nH	0.042 nH

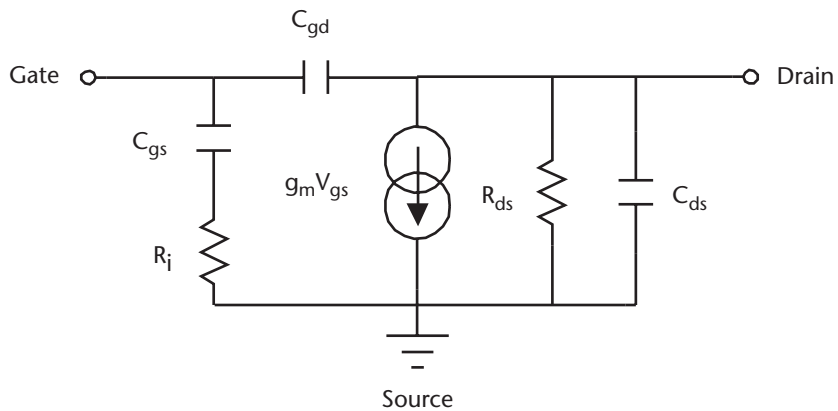


Figure 4.31 Hot small-signal model.

Equations (4.15)–(4.18) can be separated into their real and imaginary parts, thus allowing the components values of the hot small-signal model to be determined analytically as follows:

$$C_{gd} = -Im(Y_{12})/\omega \quad (4.20)$$

$$C_{gs} = \frac{Im(Y_{11}) - \omega C_{gd}}{\omega} \left\{ 1 + \frac{[Re(Y_{11})]^2}{[Im(Y_{11}) - \omega C_{gd}]^2} \right\} \quad (4.21)$$

$$R_i = [Re(Y_{11})] / \left\{ [Im(Y_{11}) - \omega C_{gd}]^2 + Re(Y_{11})^2 \right\} \quad (4.22)$$

$$g_m = \sqrt{[Re(Y_{21})]^2 + [Im(Y_{11}) - \omega C_{gd}]^2 [1 + \omega^2 C_{gs}^2 R_i^2]} \quad (4.23)$$

$$t = (1/\omega) \sin^{-1} \left\{ [-\omega C_{gd} - Im(Y_{21}) - Re(Y_{21})\omega C_{gs} R_i] / g_m \right\} \quad (4.24)$$

$$C_{ds} = [Im(Y_{22}) - \omega C_{gd}] / \omega \quad (4.25)$$

and

$$R_{ds} = 1/Re(Y_{22}) \quad (4.26)$$

The measured hot S-parameters need to be first transformed into their equivalent Y-parameters, before (4.20)–(4.26) can be used to calculate the intrinsic component values in the small-signal model. The intrinsic component values for the various devices are given in Table 4.3. These values are valid across the frequency range of 2 to 18 GHz, and for drain voltages greater than 0V.

4.3.4 Small-Signal Modeling

The intrinsic and extrinsic component values calculated here were used in ADS[®] by Agilent Technologies to generate the small-signal models for the following devices: LPS200, LPD200, LP6836, and LP6872. These models were optimized so that they fit as accurately as possible to the measured deembedded S-parameter data.

Table 4.3 Extracted Intrinsic Component Values

<i>Intrinsic Component</i>	<i>LPS200</i>	<i>LPD200</i>	<i>LP6836</i>	<i>LP6872</i>
C_{gd}	0.033 pF	0.0175 pF	0.0225 pF	0.0508 pF
C_{gs}	0.280 pF	0.3800 pF	0.6630 pF	1.0300 pF
R_i	3.4Ω	4.1Ω	0.763Ω	0.965Ω
g_m	95 mS	80 mS	101 mS	198 mS
t	0.66 pS	2.1 pS	2.40 pS	2.51 pS
C_{ds}	0.031 pF	0.031 pF	0.0562 pF	0.132 pF
R_{ds}	187Ω	373Ω	296Ω	155Ω

Tables 4.4–4.7 show that excellent agreement is obtained between the calculated and optimized small-signal model elements. The simulated and measured S-parameter characteristics for the device LPS200, shown in Figures 4.32 and 4.33, validates the accuracy of this model across the required 2- to 18-GHz bandwidth. These results clearly demonstrate the excellent accuracy that can be achieved by using the device parameter extraction procedure employed here to derive the device's small-signal equivalent model.

As LPS200 is a low-noise device, it was therefore necessary to model the effect of the noise generated within this device. The value of the current generator in the

Table 4.4 LPS200 Calculated and Optimized Component Values

<i>Intrinsic and Extrinsic Components</i>	<i>Calculated Value</i>	<i>Optimized Value</i>
C_{gd}	0.033 pF	0.032 pF
C_{gs}	0.28 pF	0.27 pF
R_i	3.4 Ω	3.5 Ω
g_m	95 mS	100 mS
t	0.66 pS	0.685 pS
C_{ds}	0.031 pF	0.03 pF
R_{ds}	187 Ω	190 Ω
C_{pg}	0.022 pF	0.023 pF
C_{dp}	0.033 pF	0.034 pF
C_b	0.21 pF	0.22 pF
L_g	0.095 nH	0.1 nH
L_d	0.095 nH	0.1 nH
R_d	0.95 Ω	1.0 Ω
R_s	0.95 Ω	1.0 Ω
R_g	2.52 Ω	2.6 Ω
L_s	0.039 nH	0.04 nH

Table 4.5 LPD200 Calculated and Optimized Component Values

<i>Intrinsic and Extrinsic Components</i>	<i>Calculated Value</i>	<i>Optimized Value</i>
C_{gd}	0.0175 pF	0.0176 pF
C_{gs}	0.38 pF	0.39 pF
R_i	4.1 Ω	4.2 Ω
g_m	80 mS	82 mS
t	2.1 pS	2.2 pS
C_{ds}	0.031 pF	0.032 pF
R_{ds}	373 Ω	375 Ω
C_{pg}	0.022 pF	0.023 pF
C_{dp}	0.032 pF	0.034 pF
C_b	0.21 pF	0.22 pF
L_g	0.095H	0.1 nH
L_d	0.095H	0.1 nH
R_d	4.85 Ω	5.0 Ω
R_s	0.105 Ω	0.11 Ω
R_g	0.215 Ω	0.20 Ω
L_s	0.039 nH	0.04 nH

Table 4.6 LP6836 Calculated and Optimized Component Values

<i>Intrinsic and Extrinsic Components</i>	<i>Calculated Value</i>	<i>Optimized Value</i>
C_{gd}	0.0225 pF	0.0229 pF
C_{gs}	0.663 pF	0.665 pF
R_i	0.763 Ω	0.768 Ω
g_m	101 mS	103 mS
t	2.4 pS	2.33 pS
C_{ds}	0.0562 pF	0.056 pF
R_{ds}	296 Ω	301 Ω
C_{pg}	0.067 pF	0.07 pF
C_{dp}	0.054 pF	0.0556 pF
C_b	0.32 pF	0.34 pF
L_g	0.0181 nH	0.0186 nH
L_d	0.053 nH	0.055 nH
R_d	0.52 Ω	0.54 Ω
R_s	1.86 Ω	1.88 Ω
R_g	1.43 Ω	1.45 Ω
L_s	0.041 nH	0.04 nH

Table 4.7 LP6872 Calculated and Optimized Component Values

<i>Intrinsic and Extrinsic Components</i>	<i>Calculated Value</i>	<i>Optimized Value</i>
C_{gd}	0.0508 pF	0.050 pF
C_{gs}	1.03 pF	1.05 pF
R_i	0.965 Ω	0.95 Ω
g_m	198 mS	200 mS
t	2.51 pS	2.56 pS
C_{ds}	0.132 pF	0.133 pF
R_{ds}	155 Ω	158 Ω
C_{pg}	0.0208 pF	0.022 pF
C_{dp}	0.053 pF	0.055 pF
C_b	0.55 pF	0.59 pF
L_g	0.0102 nH	0.01 nH
L_d	0.028 nH	0.03 nH
R_d	0.64 Ω	0.65 Ω
R_s	0.27 Ω	0.283 Ω
R_g	1.2 Ω	1.22 Ω
L_s	0.042 nH	0.0405 nH

device's model is determined from the low-frequency noise-power method [22], which basically involves the measurement of the device's short-circuit noise power. The measured noise power is then used to calculate the spectral noise power density, and this value (for LPS200, it is 1,400 (pA)²/Hz) is used in the device's model. As shown in Figure 4.34, the device's small-signal model incorporates a current generator defined by I_{Noise} ; the magnitude of current noise, per sqrt (Hz). Figure 4.35 shows excellent agreement obtained between the measured and simulated noise figure and small-signal gain performance for this device.

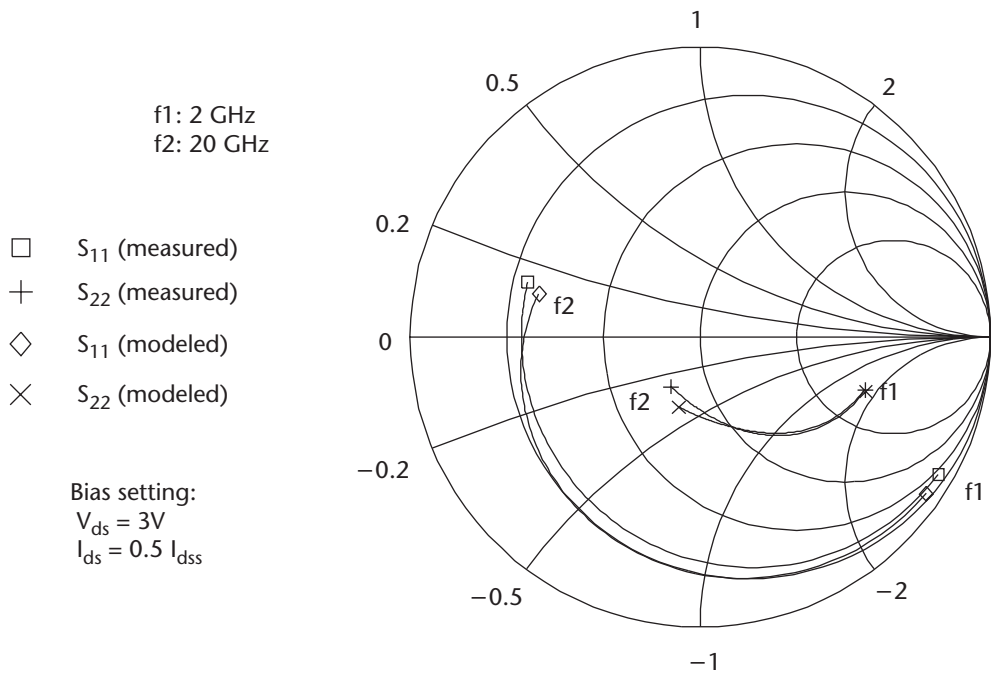


Figure 4.32 LPS200 measured and modeled S_{11} and S_{22} .

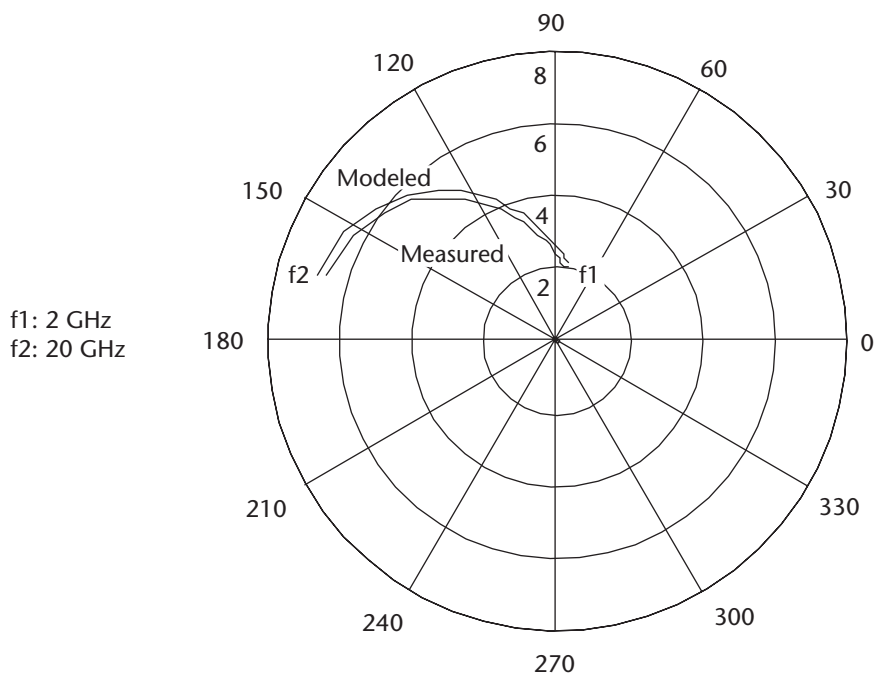


Figure 4.33 LPS200 measured and modeled S_{21} .

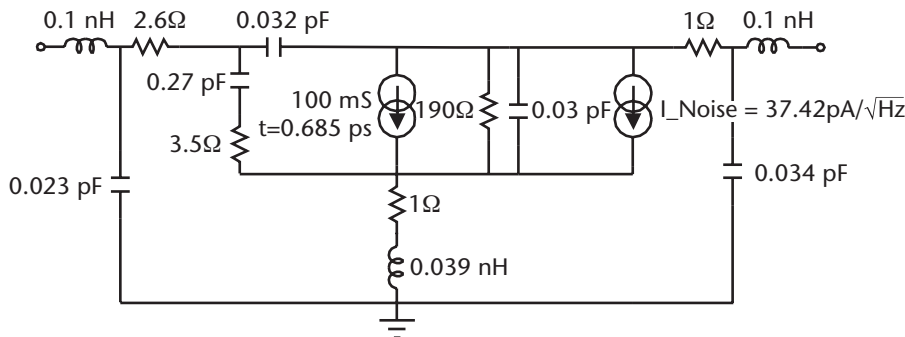


Figure 4.34 LPS200 optimized small-signal model.

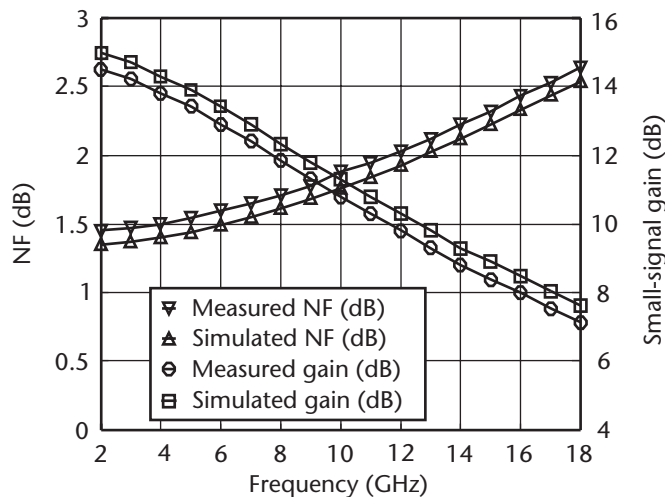


Figure 4.35 LPS200 noise and small-signal gain modeling.

4.4 Large-Signal Device Modeling

The basic small-signal model can be adapted to represent the device's nonlinearities, which give rise to the large-signal effects. This large-signal model can be derived from one of two basic approaches (i.e., from theoretical considerations based on process parameters, such as device geometry and carrier concentrations, or from its measured I–V characteristics). The latter approach is preferable, as no reference to process information is needed in the empirical model. In addition, it is shown that the empirical model leads to an accurate large-signal model.

This section describes how the large-signal equivalent circuit model of an active device is determined, as this is critical in the nonlinear analysis of the amplifier performance. First, a brief review is given of the various nonlinear analysis and large-signal modeling techniques currently available. It is then shown how the

large-signal model of a DPHEMT device is derived, which is based on fitting the theoretical model to the device's pulsed dc $I_{ds} - V_{ds}$ and $I_{ds} - V_{gs}$ characteristics.

4.4.1 Large-Signal Device Model

The device models described in Section 4.3 are valid for small-signal device operation where the signal voltages are small compared with the static operating point. However, as the signal voltage rises, the signal deviates from its static operating point, therefore changing the device's performance characteristics [23]. The elements in the small-signal model that change with bias conditions are termed *nonlinear elements*, which include the gate-drain capacitance C_{gd} , gate-source capacitance C_{gs} , transconductance g_m , transit time t , drain-source capacitance C_{ds} , and the drain-source resistance R_{ds} , as indicated in Figure 4.36.

The large-signal model also has to take into account the breakdown effects [24] that occur at high voltage levels or by forward biasing the gate-source Schottky diode. In particular, the gate-drain avalanche breakdown current occurs at a high value of V_{gd} and the forward gate-source breakdown current occurs when a positive voltage is applied to the DPHEMT device's gate. Both of these effects severely alter the characteristics of the active device. Hence, to obtain a realistic large-signal model that takes into account these effects, the model needs to incorporate diodes [25].

4.4.2 Nonlinear Analysis Techniques

The nonlinear behavior of any circuit can be defined where the output varies with the input and cannot be described by a linear expression. Linear circuits are generally solved in the frequency domain, but this is not suitable for nonlinear characterization. The four different types of nonlinear analysis are:

- Time domain;
- Harmonic balance;
- Volterra series;

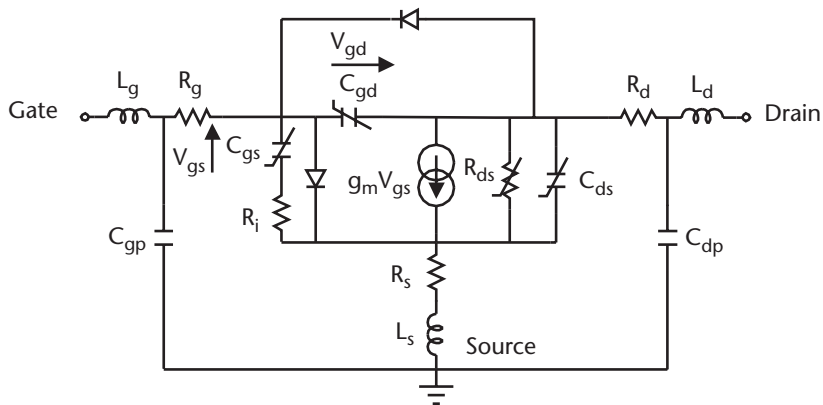


Figure 4.36 Large-signal model at a nominal operating bias.

- Describing functions.

The time-domain analysis [26] involves a system of nonlinear equations with respect to time. The relationship between voltage and current in the time domain is specified for each circuit element, which is solved using Kirchhoff's laws. Solutions are found over a transient period in steps of δt , where the size of δt is inversely proportional to the total solution time and the accuracy. The speed of solution is also affected by the complexity of the nonlinear circuit. The disadvantage of time-domain analysis is that all of the transients must be calculated to reach a solution, whereas in many cases only the steady-state solution is required. Often, the transient settling time (e.g., of the bias circuit) can be many orders of magnitude greater than the basic RF period, leading to lengthy calculations. Another problem may occur where, for a given time step, a solution of Kirchhoff's law cannot be found and the solution fails to converge, usually caused by poorly defined nonlinear expressions.

Harmonic-balance analysis [27] is performed in both the time and frequency domains. The circuit is divided into linear and nonlinear sections: the linear section is solved quickly in the frequency domain for each of N harmonics, and the nonlinear section is solved separately in the time domain. Results are passed between the two sections by means of Fourier and inverse-Fourier transforms. Normally, simulation begins with an analysis of the linear system from the initial conditions. The solution of this analysis is used to perform an analysis of the nonlinear system, and the results are passed back to the linear system once again. This iterative process continues until the error function between the two systems drops to an acceptably small level. The speed efficiency of the harmonic-balance method depends on the type of nonlinear circuit, the partitioning into linear and nonlinear blocks, the initial conditions, and the number of harmonics that must be considered. It is usually quicker than the time-domain analysis but can become very complicated in applications where signals with more than one frequency are considered. Several improvements to the harmonic balance method have been proposed [27], which have reduced the number of time domain calculations needed and increased the number of harmonics that can be considered.

The Volterra series [28] is useful in systems that are only weakly nonlinear and where the input signal consists of a number of different frequencies. It is particularly useful in circuits where higher harmonics can be ignored, although analysis becomes rather complicated in systems where this approximation cannot be made.

The describing function [29] is used to analyze systems where the level of nonlinearity is low. The nonlinear system is converted to a number of linear systems (usually linear filters) that can be simply analyzed in the frequency domain. The accuracy of the method is largely dependent on the error that exists between the nonlinear and equivalent linear systems. The main disadvantage of this method is that it can be difficult to transpose a nonlinear circuit into a number of linear circuits, especially when the nonlinearity is more pronounced.

4.4.3 Large-Signal Modeling Techniques

There are many ways to derive large-signal models for active devices, depending on the available data, the CAD tool, and the theoretical approach chosen [30]. The four different methods commonly used are listed next, although a particular method may involve a combination of two or more of these methods.

- Empirical models are derived from the device's S-parameters, dc pulsed I–V measurements.
- Semiempirical models require some characterization measurements and some information on the process parameters, such as the DPHEMT gate dimensions and the channel doping concentration. These are most commonly used commercial nonlinear models and are regarded as *industry standard*.
- Analytical models are calculated from mathematical equations, which describe the device physics, where certain assumptions have been made to simplify the calculations. Compared with empirical and semiempirical models, the analytical models to date have been less accurate, mainly because the physical mechanisms controlling charge transport in the DPHEMT are not yet fully understood. The accuracy of the analytical model is also undermined by the assumptions and approximations that are made during derivation of the equations.
- Numerical models employ the most complicated type of analysis. This type of modeling is computationally more intensive and requires detailed information about the material properties and device geometry.

Semiempirical models result from a compromise between the empirical and analytical approaches. As these models offer the advantage of simplicity and computer efficiency, they are employed in this section to obtain the large-signal model of the DPHEMT device. These models are based on fitting the dc I_{ds} – V_{ds} and I_{ds} – V_{gs} characteristics of the DPHEMT to equations, which are derived from analytical expressions. The equations may include process-controlled parameters, such as the pinch-off voltage and the built-in voltage; however, all of the equations contain arbitrary parameters (e.g., α , β , γ) that are used to fit the equation to dc measurements.

The most important nonlinear element in the large-signal model is the current equation, and many semiempirical expressions have been proposed for it [31–34]. The general slopes of these equations are similar, including a linear region rising to a *knee* point and a saturation region. The flowchart of Figure 4.37 shows the procedure for deriving the large-signal model based on the semiempirical model.

The harmonic balance technique that is available in microwave CAD package such as ADS® by Agilent Technologies uses the following semiempirical large-signal models: the Curtice Quadratic Model [31], the Curtice-Ettenberg Model [32], the Statz Model [33], and the TOM Model [34]. It is important to select the appropriate model so that it fits as accurately as possible to the measured pulsed I–V data

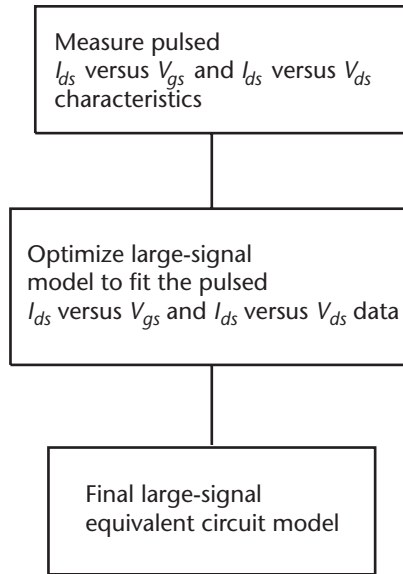


Figure 4.37 Large-signal modeling procedure.

of the device, as this model will be used to analyze and optimize the amplifier incorporating this device. These models are now reviewed.

4.4.3.1 The Curtice Quadratic Model

The Curtice Quadratic large-signal model was introduced in 1980 [31] and assumes a square-law dependence of drain-source current I_{ds} on gate-source voltage V_{gs} based on the following analytical function

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} + |V_p|)^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (4.27)$$

Where β is a transconductance scaling parameter, $|V_p|$ is pinch-off voltage, λ defines the dc value of R_{ds} , and α adjusts the knee of I_{ds} versus V_{ds} . The square-law portion of (4.27) is adopted from the Shichman-Hodges junction field-effect transistor (JFET) model [35], and Curtice augmented this model with the $\tanh(\alpha V_{ds})$ function. The hyperbolic tangent \tanh is a continuous function that provides versatility in fitting the knee of the I_{ds} versus V_{ds} characteristics and has been adopted for all of the popular, empirical large-signal device models. At $V_{ds} = 0V$, both \tanh and its approximation have a slope of α . The $(1 + \lambda V_{ds})$ term in (4.27) models the dc output conductance slope of the I_{ds} versus V_{ds} curves in the saturated region. In addition, the square-law model for the g_m nonlinearity means only second harmonics can be generated by g_m (i.e., g_m does not contribute to third-order harmonic and intermodulation distortion). Therefore, in simulating class A amplifiers, this model can be expected to underestimate third-harmonic and third-order intermodulation

distortion (IMD) output power. The model is also the least accurate of all models in fitting pinch-off and g_m bias dependency, but the merit of the quadratic model is its simplicity, which leads to quick computations and good convergence qualities.

4.4.3.2 The Curtice-Ettenberg Model

The Curtice-Ettenberg model, introduced in 1985 [32], employs a third-order polynomial to fit the I_{ds} versus V_{gs} characteristic and is often referred to as the cubic model. It is defined by the following function:

$$I_{ds}(V_{gs}, V_{ds}) = (A_o + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) \tanh(\alpha V_{ds}) \quad (4.28)$$

where

$$V_1(V_{gs}, V_{ds}) = V_{gs} [1 + \beta(V_{dso} - V_{ds})] \quad (4.29)$$

In (4.29), β controls the change in pinch-off voltage with V_{ds} , and V_{dso} is the drain-source voltage at which the A_i coefficients are evaluated. The function is capable of replicating the curvature more accurately by sacrificing the fit accuracy along other regions of the I–V curve. In particular, the model achieves a best fit along the major portion of the I_{ds} versus V_{ds} curve; however, the fit is poor at the region of curvature close to pinch-off. For large-signal class A amplifiers, the fit of the model near the pinch-off region is usually less important than the fit along the quasi-linear I_{ds} – V_{gs} region surrounding the quiescent bias point. However, for class AB amplifier design, the accurate fitting of the pinch-off region is important in order to produce realistic simulations of the output power and power-added efficiency as a function of the input drive signal. Therefore, employing this model in this case could result in less accurate simulations.

This cubic model can be expected to be capable of more accurate simulations of the third-order harmonic and intermodulation distortion in class A operation than the other popular dc I–V fitting functions. The coefficient A_3 in (4.28) controls the magnitude of the third-order distortion. Ideally, the extraction of A_3 would be made through a fitting between third partial derivatives $\delta^3 I_{ds} / \delta V_{gs}^3$ for the data and the cubic function.

4.4.3.3 The Statz Model

The Statz model [33] introduced two important advances over previous device models. First, the model incorporates an improved analytical dc I–V formulation, and, second, the model offers an improved charge model representation of C_{gs} and C_{gd} as functions of both V_{gs} and V_{ds} . The Statz model modifies Curtice's formulation, (4.27), by replacing the more computationally intensive hyperbolic tangent function with a truncated series representation. The Statz I_{ds} equation then becomes:

$$I_{ds}(V_{gs}, V_{ds}) = \beta (V_{gs} + |V_p|)^2 (1 + \lambda V_{ds}) \times \left\{ 1 - [1 - (\alpha V_{ds})/3]^3 \right\} / [1 + b(V_{gs} + |V_p|)] \quad (4.30)$$

for $0 < V_{ds} < 3/\alpha$
and

$$I_{ds}(V_{gs}, V_{ds}) = \beta (V_{gs} + |V_p|)^2 (1 + \lambda V_{ds}) / [1 + b(V_{gs} + |V_p|)] \quad (4.31)$$

for $V_{ds} \geq 3/\alpha$

where $\{1 - [1 - (\alpha V_{ds})/3]^3\}$ is the truncated series representation of $\tanh(\alpha V_{ds})$ and β is a model parameter. The equations provide unusually good control over the contour in the transition of $I_{ds} = f(V_{gs})$ as it goes from square-law to linear behavior. As long as the quantity $b(V_{gs} + |V_p|)$ is < 1 , as it is when V_{gs} is close to pinch-off, then the behavior is square law, as $I_{ds} = \beta(V_{gs} + |V_p|)^2$. However, when $b(V_{gs} + |V_p|) \gg 1$, then the expression is nearly linear, as I_{ds} approaches $I_{ds} = \beta(V_{gs} + |V_p|)/b$. The coefficient β is easily evaluated for any choice of b because

$$I_{ds} = \beta |V_p|^2 / (1 + b|V_p|) \quad (4.32)$$

and

$$\beta = I_{dss} (1 + b|V_p|) / |V_p|^2 \quad (4.33)$$

The Statz function described here allows broad latitude in the I_{ds} versus V_{ds} fitting by performing adjustments of the coefficients b and β . It can accommodate I_{ds} versus V_{ds} behavior that varies from totally square law throughout ($b = 0$) to totally linear throughout (very large b).

The Statz model allows each of the Schottky barrier junction capacitances, C_{gs} and C_{gd} , to vary as functions of both V_{gs} and V_{ds} . Most conventional models represent C_{gs} and C_{gd} as simple diode junction capacitances, each of which varies as a function of a single voltage. The simple diode capacitance representation causes contradictions in defining that $C_{gs} = C_{gd}$ when $V_{ds} = 0$ V. Similarly, the simple diode junction capacitance dependency improperly models C_{gs} and C_{gd} when V_{ds} is negative. Statz [33] introduced an improved way of representing the charge distribution in the devices in order to assure continuity of charge. By first defining a total charge under the gate electrode and then apportioning this into a C_{gs} charge and a C_{gd} charge, continuity is assured over all conditions of device operation. The improved capacitance equations are of the form:

$$C_{gs} = C_{gs0} \times f_1(V_{gs}, V_{gd}) + C_{gd0} \times f_2(V_{gs}, V_{gd}) \quad (4.34)$$

$$C_{gs} = C_{gs0} \times f_3(V_{gs}, V_{gd}) + C_{gd0} \times f_4(V_{gs}, V_{gd}) \quad (4.35)$$

Where f_1 , f_2 , f_3 , and f_4 , are functions of both V_{gs} and V_{gd} . The Statz improved capacitance formulations can be expected to simulate amplitude modulation (AM) and phase modulation (PM) effects in amplifiers more accurately than does the simple diode capacitance function.

4.4.3.4 The TOM Model

The TOM model (TriQuint's own model) [34] merges some key features of the models described earlier to create a model that consequently fits a broad range of device I–V characteristics. The model is unusual in that it can produce device dc I–V families of curves, and the curves cover V_{gs} ranging from pinch-off to just beyond forward biasing the device. The main features of the TOM model are:

- A simple and widely controllable means for fitting g_m as a function of V_{gs} as the device changes from square-law dependence on V_{gs} toward a linear dependence;
- A soft or gradual pinch-off characteristic (i.e., a pinch-off voltage V_p' whose magnitude increases with increasing V_{ds});
- A simple means for modeling the dependence of R_{ds} on V_{gs} , V_{ds} , and channel temperature.

The pinch-off voltage is a function of V_{ds} given by:

$$V_p' = |V_p| + \gamma V_{ds} \quad (4.36)$$

The flattening of the slope in the drain current I_{ds} versus drain-source voltage V_{ds} as characteristic V_{gs} increases is fitted using

$$I_{ds} = I_{ds0} / (1 + \delta V_{ds} I_{ds0}) \quad (4.37)$$

where

$$I_{ds0} = \beta (V_{gs} + |V_p| + \gamma V_{ds})^Q K \tanh(\alpha V_{ds}) \quad (4.38)$$

TOM recognized that not all device behavior is well predicted by the square-law assumption, so the exponent in the expression $\beta(V_{gs} + |V_p| + \gamma V_{ds})^Q$ is changed from a constant 2 to the variable Q . The model also uses the parameter δ to model the decreased drain conductance at low gate-source bias and allows for scaling of $|V_p|$ to account for drain-source voltage dependence.

4.4.4 Modeled and Measured Results

The large-signal modeling process described here was carried out using ADS[®] by Agilent Technologies; however, Microwave Office[®] by Advanced Wave Research, Inc., or any other equivalent CAD package may be used. The fundamental large-signal models used by this software are the Curtice Quadratic Model [31] (defined as the Curtice Asymmetric Model), as shown in Figure 4.38, and the Curtice-Ettenberg Model [32] (defined as the Curtice Symmetric Model), shown in Figure 4.39. The Statz [33] and TOM [34] models in the software are based on these two models, with the necessary theoretical modifications. The components shown in Figures 4.38 and 4.39 are defined in Table 4.8. When carrying out the large-signal modeling,

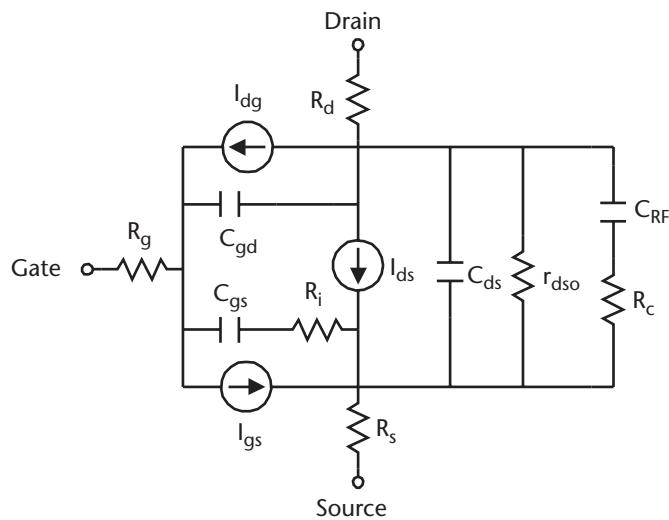


Figure 4.38 Curtice Asymmetric model.

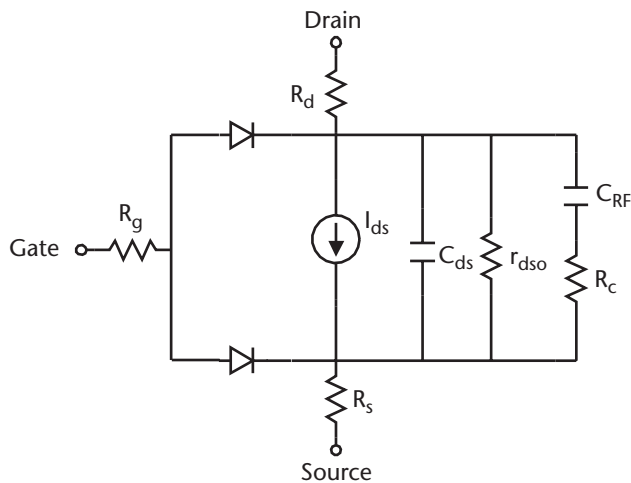


Figure 4.39 Curtice Symmetric model.

Table 4.8 Large-Signal Components

R_g	Gate ohmic resistance
I_{dg}	Reverse breakdown drain-gate current
R_d	Drain resistance
C_{gd}	Gate-drain capacitance
I_{ds}	Drain-source current
C_{ds}	Drain-source capacitance
R_i	Gate-source resistance
I_{gs}	Forward gate-source current
R_s	Source resistance
r_{dso}	Zero bias drain-source resistance
C_{RF}	Capacitance to model frequency dependency of output conductance
R_C	Resistance to model frequency dependency of output conductance

it is crucial that the model accurately fits the measured dc bias characteristics of $I_{ds}-V_{ds}$ and $I_{ds}-V_{gs}$, as these define the trajectory of the optimum load line for maximum output power and power-added efficiency [36, 37].

The measured and modeled $I_{ds}-V_{gs}$ characteristics of the device LPD200 is shown in Figure 4.40. This shows that the Curtice Quadratic model agrees with the measured data at only two V_{gs} points, namely at pinch-off when $V_{gs} = -1.2\text{V}$ and at I_{dssm} when $V_{gs} = 0.6\text{V}$. Therefore, the model can only provide a compromised fit to the measured data. The Statz and TOM models provide an improvement, as the fit is

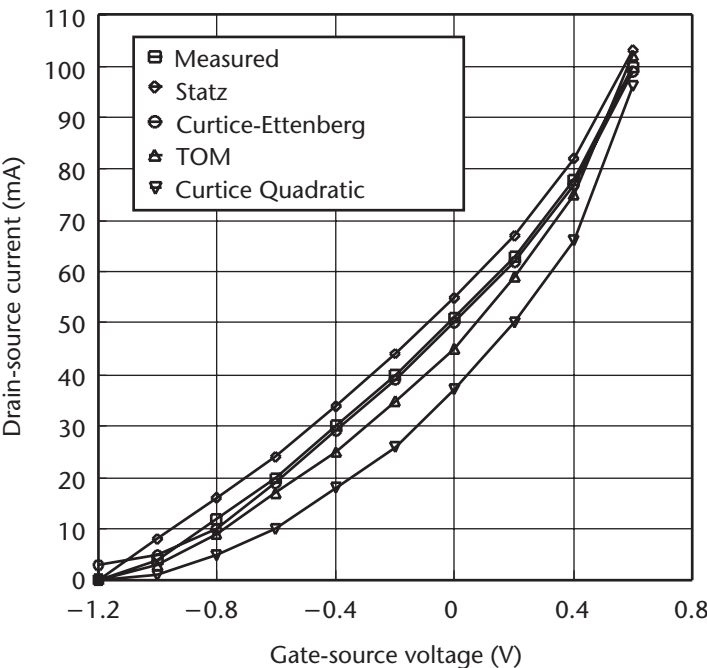


Figure 4.40 Measured and modeled $I_{ds}-V_{gs}$ characteristics of device LPD200.

better long the measured the $I_{ds}-V_{gs}$ curve, including the curvature close to pinch-off. Therefore, this model is the ideal candidate to use in the analysis and design of class AB amplifiers. Figure 4.40 shows that the Curtice-Ettenberg model achieves optimum fit along most of the $I_{ds}-V_{gs}$ measured characteristics, except at the pinch-off point. This model would be appropriate in the analysis and design of class A amplifiers, as the accuracy of the model near the device's pinch-off is usually less important than at the quasi-linear $I_{ds}-V_{ds}$ region surrounding the quiescent bias point. As shown in Figure 4.41, the Curtice-Ettenberg model exhibits good agreement between the measured and modeled $I_{ds}-V_{ds}$ characteristic of the device LPD200.

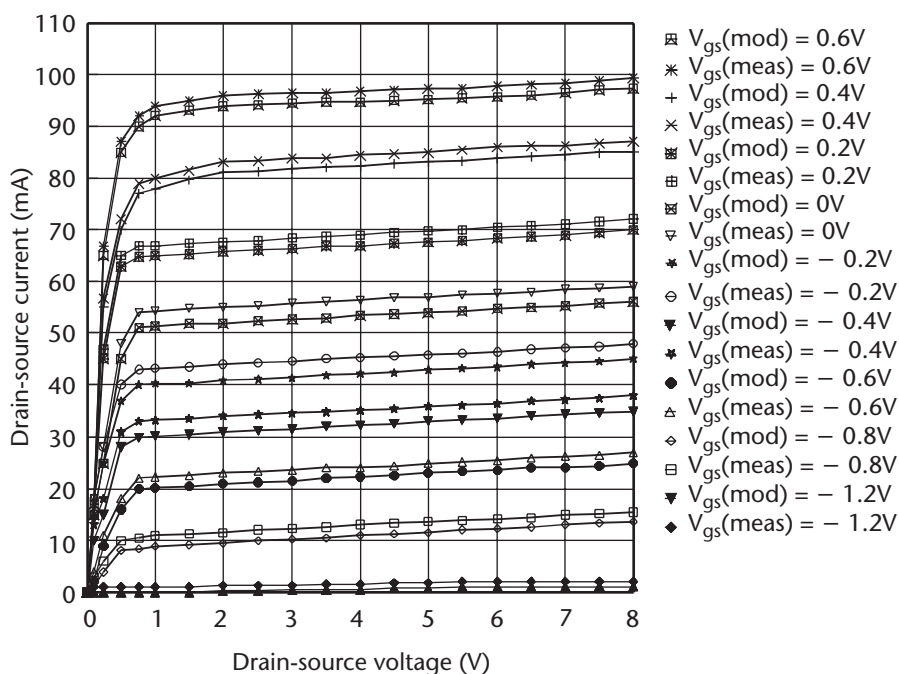


Figure 4.41 Measured and modeled (Curtice-Ettenberg) $I_{ds}-V_{ds}$ characteristics of device LPD200.

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Amplifier Class of Operation

5.1 Introduction

An important factor that needs to be addressed in any amplifier design is the selection of the dc quiescent point for the active device, which determines in what class the amplifier will operate. The various classes of device operation typically employed at microwave frequencies are defined as A, B, AB, C, D, E, and F. The selection of the class depends primarily on the particular application that is intended for the amplifier. For example, for broadband microwave amplifier designs, class A, B, or AB is selected. A bias network is used to provide the appropriate quiescent point for the active device under the specified operating conditions, and it maintains a constant setting irrespective of transistor parameter variations and temperature fluctuations.

In this chapter, a general analysis is presented of the different classes of amplifier operation relevant for broadband microwave application in order to provide an understanding of how a particular class may affect the amplifier's performance in terms of power-added efficiency.

5.2 Class A Amplifiers

The class A amplifier is defined as the mode in which the active device is conducting over the entire 360° cycle of the waveform, as illustrated in Figure 5.1. The Q-pt is the device's dc quiescent bias point, V_k is the knee voltage, and V_{max} is defined by $(V_{gdB} - |V_p|)$ [1], where V_{gdB} is the gate-to-drain breakdown voltage and V_p is the device pinch-off voltage.

This mode is the most linear of all the classes, as the amplifier's output waveform is a perfect replica of the input wave. If the active device is biased, as illustrated in Figure 5.2, where the gate bias circuitry has been omitted for simplicity, then the maximum efficiency that is available from the amplifier operating in class A mode can be determined by applying *Fourier expansion*.

In the following analysis on the class A amplifier, it is assumed that the device has a linear transfer characteristic, as shown in Figure 5.3. A periodic signal of period T is applied at the input of the amplifier, resulting in the device generating an output current $I_d(t)$ that can be described by the Fourier expansion

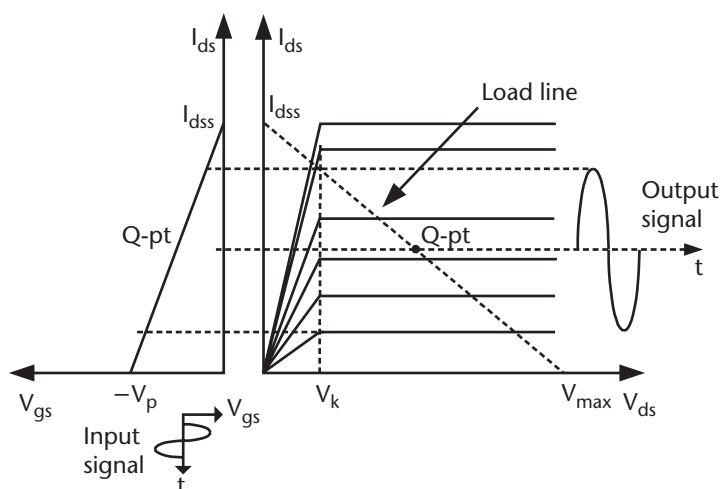


Figure 5.1 Waveform showing the class A mode of operation.

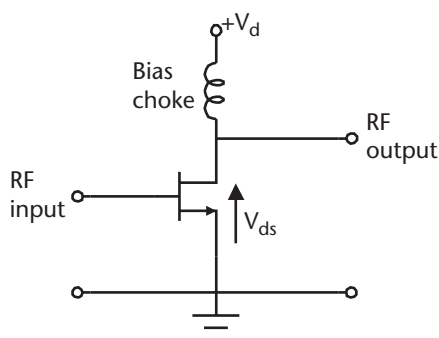


Figure 5.2 Simple FET biasing circuit.

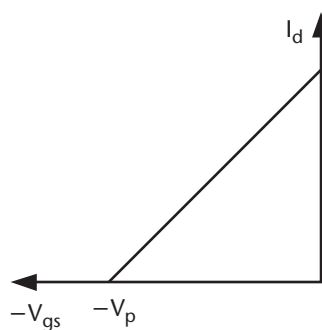


Figure 5.3 Device with linear transfer characteristic.

$$I_d(t) = I_o/2 + \sum_{n=1}^{\infty} [A_n \cos 2n(\pi/T)t + B_n \sin 2n(\pi/T)t] \quad (5.1)$$

where

$$A_n = \frac{2}{T} \int_0^T I_d(t) \cos(2n\pi t/T) dt \quad (5.2)$$

and

$$B_n = -\frac{2}{T} \int_0^T I_d(t) \sin(2n\pi t/T) dt \quad (5.3)$$

Equation (5.1) can be written as

$$I_d(t) = I_o/2 + \sum_{n=1}^{\infty} I_n \cos(\theta_n + \phi_n) \quad (5.4)$$

where

$$\begin{aligned} I_n &= \sqrt{A_n^2 + B_n^2} \\ \theta_n &= 2n\pi t/T \\ \phi_n &= \tan^{-1}(B_n/A_n) \end{aligned}$$

The Fourier expansion of the signal shows that the first three terms of the output current comprise a dc component ($n = 0$) of amplitude $I_o/2$, a fundamental component ($n = 1$) of amplitude I_1 (which represents the output signal), and an infinite series of harmonics of amplitude I_n for $n > 2$. The dc component represents the current drawn by the device from the power supply when using the bias arrangement in Figure 5.2. The dc power supplied to the device is the product of the average voltage and the average current. That is,

$$P_{dc} = V_{av} I_{av} \quad (5.5)$$

or

$$P_{dc} = V_{dsQ} I_o/2 \quad (5.6)$$

where V_{dsQ} represents the quiescent point drain-source voltage. The output voltage waveform of the device that is developed across the load resistor R_L is

$$V_d(t) = V_{dsQ} - \left[\sum_{n=1}^{\infty} I_n \cos(\theta_n + \phi_n) \right] R_L \quad (5.7)$$

The negative sign in (5.7) accounts for the 180° phase inversion of the output wave. From (5.4)

$$\sum_{n=1}^{\infty} I_n \cos(\theta_n + \phi_n) = I_d(t) - I_o/2 \quad (5.8)$$

and, therefore, (5.7) can be written as

$$V_d(t) = V_{dsQ} - R_L [I_d(t) - I_o/2] \quad (5.9)$$

In order to obtain maximum output power, the voltage swing at the output of the device must be maximized. This condition is achieved when $V_d(t)$ is set to zero, as $I_d(t)$ tends to I_{dss} . That is,

$$0 = V_{dsQ} - R_L [I_{dss} - I_o/2] \quad (5.10)$$

Therefore, the value of the load resistor for maximum output power is given by

$$R_L = V_{dsQ} / [I_{dss} - I_o/2] \quad (5.11)$$

This equation assumes that all of the harmonic voltages are present and terminated by the load resistor R_L . If all of the harmonics are short circuited, then the only voltage signal developed across the load is due to the fundamental component. In this case, for maximum power, the load resistor is given by

$$R_L = V_{dsQ} / I_1 \quad (5.12)$$

The efficiency of the device is defined as

$$\text{Device efficiency} = \frac{\text{RF output power}}{\text{dc input power}} \times 100\% \quad (5.13)$$

For a sinusoidal current output of amplitude I_n , the RF power is given by

$$P_n = I_n^2 R_L / 2 \quad (5.14)$$

Thus, the output efficiency of each harmonic is given by

$$\eta_n = I_n^2 R_L / V_{dsQ} I_o \quad (5.15)$$

We can now consider the efficiencies for two cases, one with all of the harmonics present and the other with all harmonics except for the fundamental short circuited.

- Case (1): All harmonics present.

$$\eta_n = I_n^2 \left[V_{dsQ} / (I_{dss} - I_o / 2) \right] / V_{dsQ} I_o = I_n^2 / I_o (I_{dss} - I_o / 2) \quad (5.16)$$

- Case (2): All harmonics short circuited except for the fundamental.

$$\eta_1 = I_1^2 (V_{dsQ} / I_1) / V_{dsQ} I_o = I_1 / I_o \quad (5.17)$$

In this analysis, the class A amplifier is considered to have a linear transfer characteristic so that the output waveform from the device is a sinusoid, as there are no harmonics present. Also, $I_o = I_{dss}$, and the quiescent bias point is given by $I_1 = I_{dss}/2$. Then, from (5.17), the theoretical maximum efficiency achievable in class A mode of operation is $\eta_1 = 50\%$. However, the power-added efficiency will be less than this value, as the power-added efficiency is defined as

$$\text{Power-added efficiency} = \frac{(\text{RF output power} - \text{RF input power})}{\text{DC input power}} \times 100\% \quad (5.18)$$

The theoretical maximum output power achievable in class A mode of operation in this case is given by

$$P_1 = \frac{1}{2} I_1^2 R_L = \frac{1}{2} \left(\frac{I_{dss}}{2} \right)^2 \frac{V_{dsQ}}{I_{dss}/2} = \frac{1}{4} I_{dss} V_{dsQ} \quad (5.19)$$

This analysis assumes an ideal-case scenario; however, in practice the device will have a finite gain G , knee voltage V_k , gate-to-drain breakdown voltage V_{gdb} , and pinch-off voltage V_p . Therefore, for a realistic case, the optimum power-added efficiency of an amplifier operating in class A is given by [1]

$$\eta_{\max} = (1 - 1/G) [(1 - \alpha) / 2(1 + \alpha)] \quad (5.20)$$

where

$$\alpha = V_k / (V_{gdb} - |V_p|) \quad (5.21)$$

Equation (5.20) indicates that for a very large gain device operating in class A and which has a very low knee voltage, the maximum power-added efficiency will approach the theoretical limit of 50%, as shown in Figure 5.4. This result applies to an impractical device; however, in the case of a typical power GaAs MESFET device with $G = 12$ dB, $V_k = 1.6$ V, $V_{gdb} = 28$ V, $V_p = 0.7$ V and $V_{ds} = 3.2$ V, then $\alpha = 0.06$ and the maximum power-added efficiency is calculated to be 41%. A much more drastic reduction in power-added efficiency occurs with low-gain devices (e.g., a device with only 6-dB small-signal gain will achieve a maximum efficiency of only 32% at the bias point of $0.5I_{dss}$). Allowing for practical effects such as circuit loss, nonoptimum load impedance, and the imperfection of the matching network

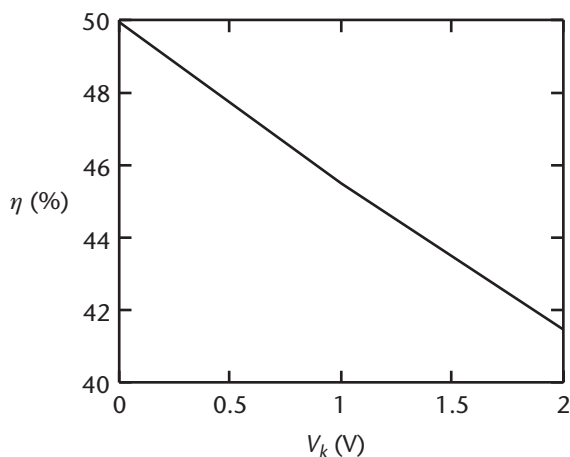


Figure 5.4 Power-added efficiency versus knee voltage for class A operation.

employed, the amplifier's efficiency will erode further to anywhere between 25% to 30%. The efficiency can also be compromised by the device's bias point. If the device is operated at a low value of I_{dss} , such as $0.2I_{dss}$, then the gain and the power-added efficiency of the amplifier will be severely degraded.

A comparison of the transconductance of a conventional GaAs MESFET and a DPHEMT device is shown in Figure 5.5. This graph indicates that the transconductance of the DPHEMT device rises steeply for low gate-source bias V_{gs} values,

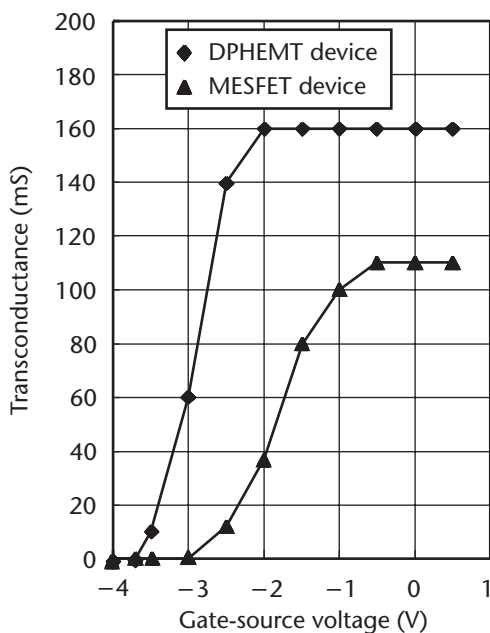


Figure 5.5 Comparison of transconductance variation with gate-source voltage for a DPHEMT and GaAs MESFET device.

reaching a constant value of 160 mS at V_{gs} of $-2V$. However, the maximum transconductance that is achievable by a typical GaAs MESFET device is limited to about 110 mS at a V_{gs} of $-0.5V$. This suggests that the DPHEMT device offers substantially higher gain at the low bias point of 0.15 to $0.25I_{dss}$ compared to the GaAs MESFET device. Hence, the DPHEMT device will therefore enable higher levels of power-added efficiency to be achieved.

5.3 Class B Amplifiers

Class B amplification is defined as the mode in which the active device amplifies during one half of the input signal's period (180°), as illustrated in Figure 5.6. As will be shown in the following analysis, class B has a major advantage over class A in terms of providing a higher drain efficiency, as there is a significant lowering of dc input power and heat dissipation by the active device.

The optimum efficiency achievable in class B mode can be easily analyzed if it is assumed that the device has a linear transfer characteristic. The output waveform in this mode is a half-wave rectified sinusoid, as shown in Figure 5.7. For this mode of operation V_{max} is defined by $(V_{gdb} - 2|V_p| - V_\phi)$, where V_{gdb} is the gate-to-drain breakdown voltage and V_ϕ is the forward gate-source voltage.

The Fourier expansion of this output waveform can be described by

$$I_d(t) = 2I_{AV} \left\{ \frac{1}{2} + \frac{\pi}{4} \cos \left[2\pi \left(\frac{1}{T} \right) t \right] - \sum_{n=1}^{\infty} \frac{(-1)^n}{(4n^2 - 1)^{-1}} \cos \left[2\pi \left(\frac{2n}{T} \right) t \right] \right\} \quad (5.22)$$

where

$$I_{AV} = I_{dss} / \pi$$

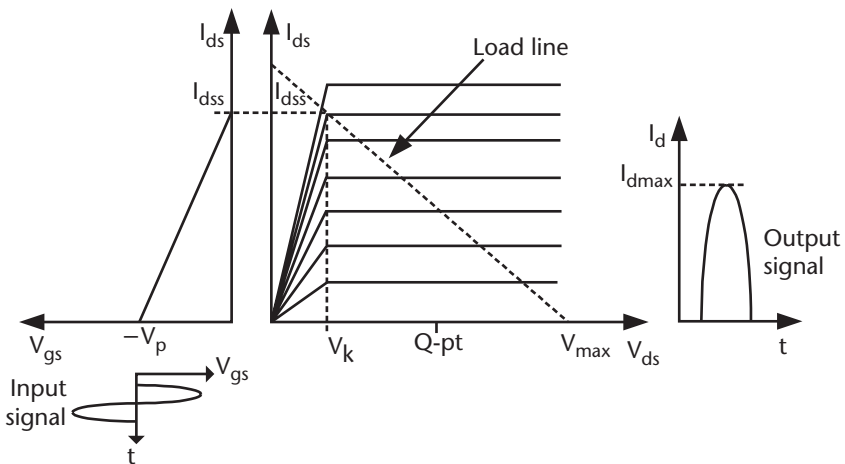


Figure 5.6 Waveform showing class B mode of operation.

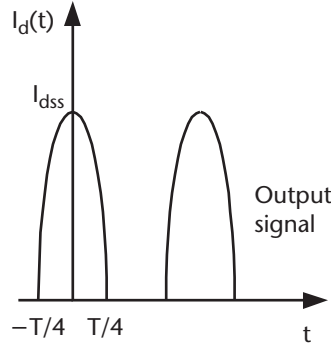


Figure 5.7 Output waveform showing class B mode of operation.

The components of the Fourier expansion are

$$\text{dc component:} \quad I_o = I_{dss} / \pi \quad (5.23)$$

$$\text{Fundamental:} \quad I_1 = I_{dss} / 2 \quad (5.24)$$

$$\text{Second harmonic:} \quad I_2 = 2I_{dss} / 3\pi \quad (5.25)$$

$$\text{Fourth harmonic:} \quad I_4 = -2I_{dss} / 15\pi \quad (5.26)$$

It must be noted that there are no odd harmonics present. The load resistance R_L with all of the harmonic components present is given by

$$R_L = V_{dsQ} / (I_{dss} - I_o) \quad (5.27)$$

The efficiency of each harmonic can then be calculated using

$$\eta_n = I_n^2 R_L / 2V_{dsQ} I_o \quad (5.28)$$

By substituting R_L from (5.27) into (5.28), the following efficiency expression is obtained

$$\eta_n = I_n^2 / 2I_o (I_{dss} - I_o) \quad (5.29)$$

Then the efficiency of the fundamental component is

$$\eta_1 = \frac{I_1^2}{2I_o (I_{dss} - I_o)} = \frac{(I_{dss}/2)^2}{(2I_{dss}/\pi)(I_{dss} - I_{dss}/\pi)} = 57.6\% \quad (5.30)$$

Similarly, the efficiency of the second and fourth harmonic terms are $\eta_2 = 10.4\%$ and $\eta_4 = 0.43\%$, respectively. The output power of each of these harmonics is given by

$$P_n = I_n^2 R_L / 2 \quad (5.31)$$

where R_L is defined in (5.27). Then the output power of the first three harmonic modes are

$$P_1 = 0.18 V_{dsQ} I_{dss} \quad (5.32)$$

$$P_2 = 0.033 V_{dsQ} I_{dss} \quad (5.33)$$

$$P_4 = 0.00132 V_{dsQ} I_{dss} \quad (5.34)$$

A comparison of the power level of the second and fourth harmonics with respect to the fundamental is

$$\frac{\text{Power of second harmonic}}{\text{Power of fundamental}} = 0.183 = -7.4 \text{ dBc}$$

$$\frac{\text{Power of fourth harmonic}}{\text{Power of fundamental}} = 0.0073 = -21.3 \text{ dBc}$$

If all harmonics except for the fundamental are short circuited, then the load resistor R_L is given by

$$R_L = V_{dsQ} / I_1 \quad (5.35)$$

It must be noted that the value of the load resistor in this analysis is the same as for class A mode of operation. Then from (5.28), the maximum efficiency in class B mode of operation is given by

$$\eta_1 = I_1^2 R_L / 2 V_{dsQ} I_o = I_1^2 (V_{dsQ} / I_1) / 2 V_{dsQ} I_o = I_1 / 2 I_o \quad (5.36)$$

so $\eta_n = (I_{dss} / 2) / (2 I_{dss} / \pi) = 78.54\%$

The theoretical maximum output power achievable in class B mode of operation can be calculated if one knows the device's I_{dss} and V_{dsQ} . That is,

$$P_{out} = \frac{I_1^2 R_L}{2} = \frac{I_1^2}{2} \frac{V_{dsQ}}{I_1} = \frac{I_1 V_{dsQ}}{2} = \frac{(I_{dss} / 2) V_{dsQ}}{2} = \frac{1}{4} I_{dss} V_{dsQ} \quad (5.37)$$

The output power is the same as that achievable in class A mode of operation, although a much higher efficiency is attained.

In order to realize a higher efficiency in class B mode of operation, the RF voltage swing across the input of the active device needs to be much larger, and this puts considerable strain on the breakdown voltage. In fact, in class B mode of operation, the RF input voltage swing for a given RF output is twice that for a device operating in class A mode, as illustrated in Figure 5.8. In class A mode, the maximum gate voltage swing required is given by

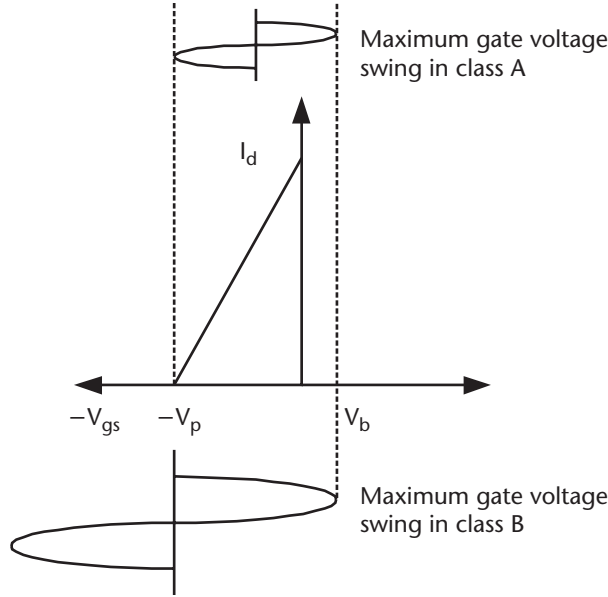


Figure 5.8 Maximum gate voltage swings in classes A and B.

$$V_b + |V_p| \quad (5.38)$$

In class B mode, the maximum gate voltage swing is

$$2(V_b + |V_p|) \quad (5.39)$$

Because the power dissipated is proportional to the voltage square (i.e., V^2), for the same output power, the input power for

- Class A is proportional to $(V_b + |V_p|)^2$;
- Class B is proportional to $4(V_b + |V_p|)^2$;

This analysis assumes an ideal case; however, in practice, the device is associated with finite gain G , knee voltage V_k , gate-to-drain breakdown voltage V_{gdB} , pinch-off voltage V_p , and forward gate-source voltage V_ϕ . Therefore, for a realistic case, the optimum power-added efficiency of an amplifier operating in class B is given by [1]

$$\eta_{\max} = (\pi/4)(1 - 1/G)[(1 - \beta)/(1 + \beta)] \quad (5.40)$$

where

$$\beta = V_k / (V_{gdB} - 2|V_p| - V_\phi)$$

Equation (5.40) indicates that a very high gain device with a very low knee voltage operating in a class B mode will yield a power-added efficiency approaching the theoretical maximum limit of 78.5%, as shown in Figure 5.9. In practice, however, a device will have a finite gain and knee voltage, and if the same GaAs MESFET device is employed, as described in Section 5.2 for the class A condition ($G = 12$ dB, $V_k = 1.6$ V, $V_{gdB} = 28$ V, $V_\phi = 0.7$ V, and $V_p = 3.2$ V), then $\beta = 0.076$ and the power-added efficiency is 63%.

In practice, high output power and efficiency are possible by overdriving the class B mode amplifier; however, this will be to the detriment of the amplifier's gain. This is because the device's transconductance falls dramatically as the gate-to-source voltage V_{gs} approaches pinch-off, leading to a substantial reduction of the small-signal gain. Also, by overdriving the amplifier in class B mode, the RF voltage swing across the device will be large, putting severe strain on the device's breakdown voltage. In addition, its bias point will be such that the device spends a considerable period in the depletion layer edge very close to the active layer/substrate interface, which will inevitably lead the device to failure. Therefore, this mode of operation is considered inappropriate for broadband microwave amplifier designs intended for high power and hence high-efficiency performance.

5.4 Class AB Amplifiers

A device operated in class AB mode is defined as having a dc quiescent drain current of 0.1 to $0.2I_{dss}$, as shown in Figure 5.10. The maximum theoretical efficiency of an amplifier operating in class AB can be easily derived using a simplified analysis where the sinusoidal current of amplitude I_m through the load for a conduction angle θ_o has a waveform shown in Figure 5.11. The drain line current I_d of the device

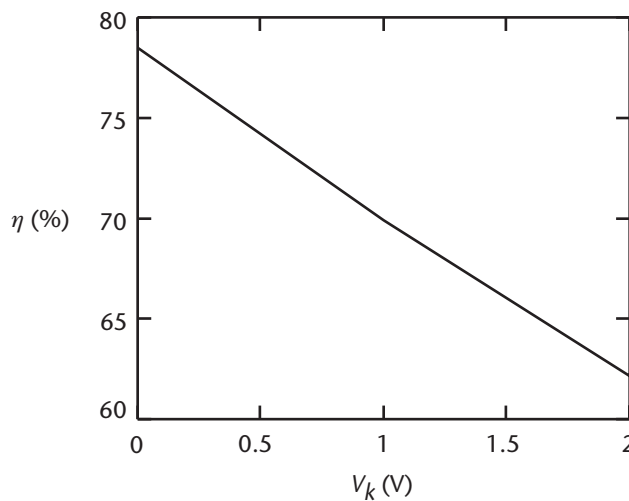


Figure 5.9 Power-added efficiency versus knee voltage for class B operation.

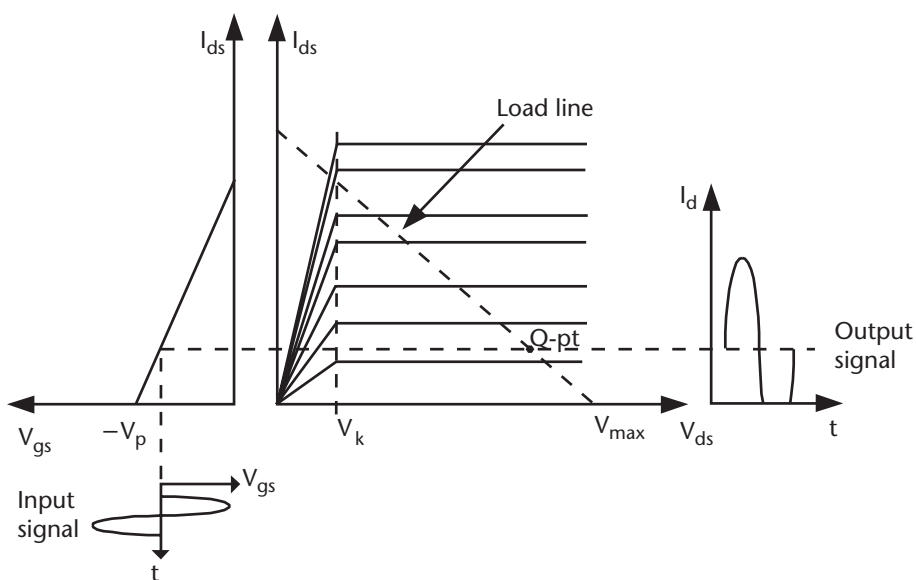


Figure 5.10 Waveform showing class AB mode of operation.

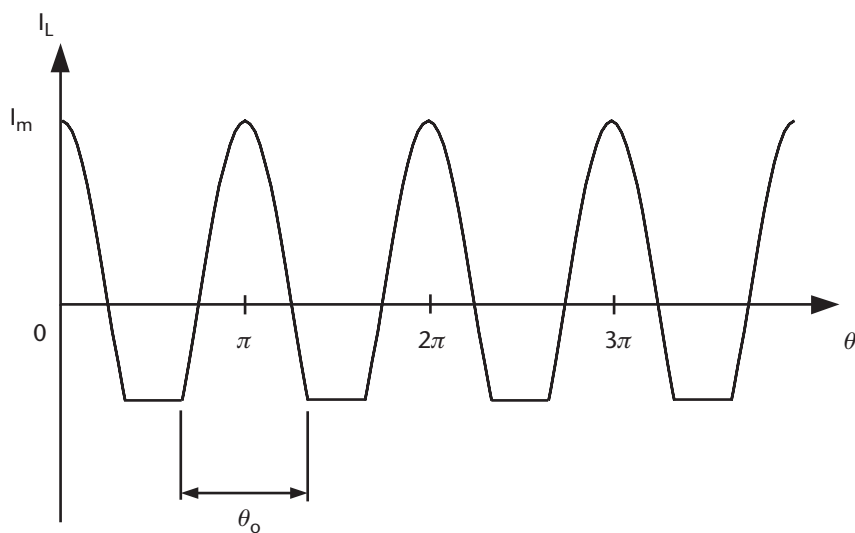


Figure 5.11 Load current waveform as a function of conduction angle.

consists of the input current of maximum value I_m and the dc quiescent current I_Q , given by

$$I_d = I_Q + I_m \cos \theta \quad (5.41)$$

The value of the quiescent current for a specified conduction angle θ_o is found from (5.41) by equating I_d to zero at $\theta = \theta_o/2$, so

$$I_Q = -I_m \cos(\theta_o/2) \quad (5.42)$$

The average drain line current is then found by integrating over the conduction angle (in radians) between the limits of $\theta = -\theta_o/2$ and $\theta = \theta_o/2$,

$$\overline{I_d} = \frac{1}{2\pi} \int_{-\theta_o/2}^{+\theta_o/2} I_d d\theta = -\frac{I_m}{2\pi} \left[\theta_o \cos\left(\frac{\theta_o}{2}\right) - 2 \sin\left(\frac{\theta_o}{2}\right) \right] \quad (5.43)$$

Thus, the average power from the power supply is

$$P_{av} = V_{av} \overline{I_d} = -\frac{I_m V_{av}}{2\pi} \left[\theta_o \cos\left(\frac{\theta_o}{2}\right) - 2 \sin\left(\frac{\theta_o}{2}\right) \right] \quad (5.44)$$

where V_{av} is the supply voltage.

Because the voltage in the load changes together with the current, the average power is an integral of the product of the load current and load voltage, given by

$$P_L = \frac{1}{2\pi} \int_{-\theta_o/2}^{+\theta_o/2} I_m V_{av} \cos^2 \theta d\theta = \frac{I_m V_{av}}{4\pi} (\theta_o - \sin \theta_o) \quad (5.45)$$

The amplifier's efficiency is then obtained by dividing (5.45) by (5.44), which gives

$$\eta = -\frac{\theta_o - \sin \theta_o}{2[\theta_o \cos(\theta_o/2) - 2 \sin(\theta_o/2)]} \quad (5.46)$$

For class AB, the conduction angle θ_o can be anywhere between 180° and 360° . If $\theta_o = 300^\circ$, then the theoretical maximum efficiency $\eta = 55\%$.

The discussion in this Section indicates that if a GaAs MESFET microwave amplifier is operated at a dc quiescent drain current of 0.1 to $0.2 I_{dss}$ then the amplifier's performance in terms of gain and power-added efficiency will be severely eroded. However, Itoh, et al. [2], have reported excellent results for a balanced reactively matched amplifier operating in class AB mode over 5 to 10 GHz (one octave bandwidth). The amplifier achieved an average power-added efficiency of 25% biased at $0.3 I_{dss}$. By employing an output matching circuit that simultaneously provides a short circuit to all even harmonics and an open circuit to all odd harmonics, the efficiency can be further enhanced, as proposed by Snider [3]. The amplifier achieved 1 -W output power over 3.7 to 4.2 GHz with an 11 -dB gain and 54%

efficiency over the entire bandwidth with the devices biased at $0.1I_{dss}$. This performance was achieved using a GaAs MESFET device that was selected for its high gain of 6 dB at 14 GHz, low pinch-off voltage of 1.5V, high breakdown voltage of 17V, and low knee voltage of 1V to ensure minimal efficiency degradation in class AB. The selection of low pinch-off and knee voltages ensures a low value for β defined in (5.40), in order to maintain the efficiency high.

The latter discussion proves that high efficiency can be achieved by employing GaAs MESFET devices in microwave amplifiers by properly selecting the devices for low pinch-off voltage, a high breakdown voltage, a low knee voltage, and by ensuring that the devices have significant gain at high frequencies. However, devices such as the PHEMT, DPHEMT, and HFETs have an advantage over the GaAs MESFET devices, as they are fabricated to have a near-constant transconductance of typically 160 mS at relatively low gate-source bias voltage than for GaAs MESFET devices, as shown in Figure 5.12, and a high maximum channel current density I_{max} of typically 435 mA/mm. The high breakdown voltage allows these devices to be operated with a relatively high drain voltage of up to 8V, and the near-constant transconductance characteristics close to pinch-off voltage gives the devices high gain in class AB mode of operation. These properties result in a marked improvement in efficiency performance obtainable from these devices compared to GaAs MESFET devices.

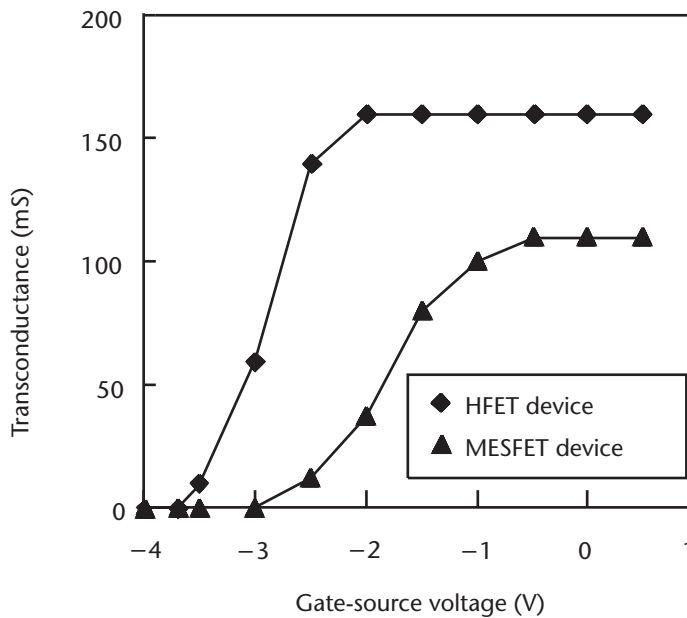


Figure 5.12 Comparison of transconductance variation with gate-source voltage for HFET and GaAs MESFET devices.

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- [2] Itoh, Y., et al., “A 5–10 GHz 15 W GaAs MESFET Amplifier with Flat Gain and Power Responses,” *IEEE Trans. on Microwave and Guided Wave*, Vol. 5, No. 12, 1995, pp. 454–456.
- [3] Snider, D. M., “Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier,” *IEEE Trans. on Electron Devices*, Vol. ED-14, December 1967, pp. 851–857.

Design of Broadband Microwave Amplifiers

6.1 Introduction

This chapter describes the design, fabrication, and the measured performance of high-gain microwave amplifiers for multioctave performance. The amplifier's small-signal and large-signal performance was analyzed using a commercially available microwave CAD package. Simulation tools such as Agilent's ADS® or Applied Wave Research's Microwave Office® are indispensable for such analysis. The device's small-signal and large-signal models extracted from the measured S-parameters and the pulsed dc I-V characteristics, as described in Chapter 4, were used for the design and modeling of the broadbandwidth amplifiers. In particular, the small-signal simulations enable the optimization of the small-signal gain and input/output return loss, whereas the large-signal simulations enable the optimization of the output power and power-added efficiency.

In this chapter the design of the following broadband microwave amplifiers are presented:

- TWDA;
- Feedback amplifier;
- CRTSSDA;
- Feedback amplifier using current sharing concept;
- High dynamic range amplifier.

The traveling wave and feedback amplifiers are the traditional workhorses in broadband systems such as EW, instrumentation, and high-data-rate light-wave communications. The major drawback of the traveling wave and feedback amplifiers is poor output power and power-added efficiency. In this chapter, it is demonstrated that the CRTSSDA concept overcomes the performance deficiencies of the traveling wave and feedback amplifiers. This chapter also describes a novel current-sharing concept, which is implemented on a dual-stage broadband feedback amplifier. The current-sharing concept is shown to substantially reduce the current consumption of the amplifier by 50% and hence significantly improve its power-added efficiency performance. Finally, this chapter describes the design and

implementation of a novel high dynamic range amplifier for broadband receiver applications. The high dynamic range amplifier is realized by integrating a CRTSSDA configuration with a low noise feedback amplifier module.

6.2 Multistage Broadband Amplifier Design

Traditionally, the multistage amplifier design is implemented by cascading together a series of balanced single-stage gain blocks [1], which comprise of reactively matched amplifiers that are configured into a balanced stage using 3-dB Lange couplers [2]. The approach allows for ease of design, as the balanced configuration improves the input and output match and allows the amplifier to be cascaded with other amplifiers. However, the amplifier's bandwidth is limited to about one-and-a-half octaves due to the Lange couplers, the dc consumption is twice that of a single-stage gain block, and it requires twice the number of active devices as that for a single-stage amplifier. Presently, the design philosophy is shifting toward the direct cascade of gain stages. This is partly due to the industry's demand for smaller and more efficient circuits and partly due to the availability of accurate device characterization and modeling techniques, as well as accurate microwave CAD tools.

The design topology of a reactively matched two-stage amplifier, illustrated in Figure 6.1, consists of the input, interstage, and output networks. The input and output networks are designed to provide an appropriate impedance transformation between the active device and the external system. The interstage network is used to provide the necessary gain shaping to compensate for the 6-dB/octave roll off of each FET, and the FET's output-matching network is designed to maximize power transfer to the load.

For large-signal applications, the output-matching network must be designed to terminate the active device with the optimum load impedance at the fundamental and harmonic frequencies [3]. Unfortunately, harmonic terminations are not always possible in broadband designs because the harmonics can easily fall within the operating bandwidth of the amplifier. Also, when the output network is designed for large-signal performance, the amplifier's small-signal output return loss or VSWR will tend to be poor.

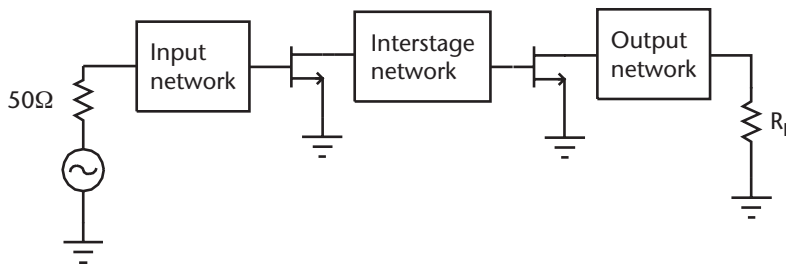


Figure 6.1 Representative two-stage amplifier.

The design of the interstage network is similarly hampered, as it must be designed for both gain shaping and maximum power transfer between the two amplifier stages [4–6]. This is necessary especially at the upper frequency band edge, where the active device's gain is at its lowest value, and therefore sufficient drive power must be delivered to the input of the next device by the preceding device. Fortunately, this is not a problem at the lower frequency band edge as the output device exhibits a higher gain, hence requiring less drive power. If, however, the interstage network is designed to provide gain shaping by mismatching the output of the first driver device and the input of the second device, this may load the driver device in such a manner as to prevent it from delivering sufficient drive power. Even if the mismatch loss from the interstage network is small (less than 1 dB), the power transfer loss can easily be several decibels, as the driver device is not terminated with an impedance approaching the optimum large-signal impedance Z_{opt} .

A variety of network synthesis techniques [1, 7] are available that are very useful for synthesizing matching networks. These techniques, which are based on either a lowpass or bandpass approach, provide gain-sloped responses and generate matching networks for complex-to-real or complex-to-complex load impedances. The synthesized networks are usually of lumped-element form, which need to be converted to their equivalent distributed form. The real-frequency technique proposed by Carlin [7] or the bandpass-synthesis technique described by Mellor [1] provides excellent flat gain performance for small-signal amplifier operation. Although synthesis techniques produce networks with the required transfer function to achieve the amplifier's desired frequency response, the element values are often unrealizable. The terminal impedances are also unconstrained; thus, the resulting amplifier may exhibit poor output power performance. However, broadband synthesis techniques do provide excellent starting values for matching network elements.

It is shown in this chapter that the use of the synthesis techniques is unnecessary for multioctave amplifier designs using either the TWDA, feedback amplifier, or CRTSSDA, as these topologies provide inherent input-output match.

6.3 Output Power and Power-Added Efficiency

The use of load line analysis to estimate the large-signal load impedance of a DPHEMT amplifier can be misleading. Analysis [8, 9] of the device dc I–V characteristics suggest that the optimal load impedance for an amplifier can be estimated by observing the maximum drain current I_{dssm} and gate-drain breakdown voltage V_{gdb} . Ideally, maximum RF output power should be obtained by promoting the maximum peak-to-peak swing of the drain voltage and current. Therefore, the load impedance should produce a load line within the dc I–V plane similar to that shown in Figure 6.2.

As indicated in Figure 6.2, the peak drain voltage occurs at the pinch-off breakdown voltage V_{gdb} . The minimum drain voltage V_k is at the knee of the dc I–V

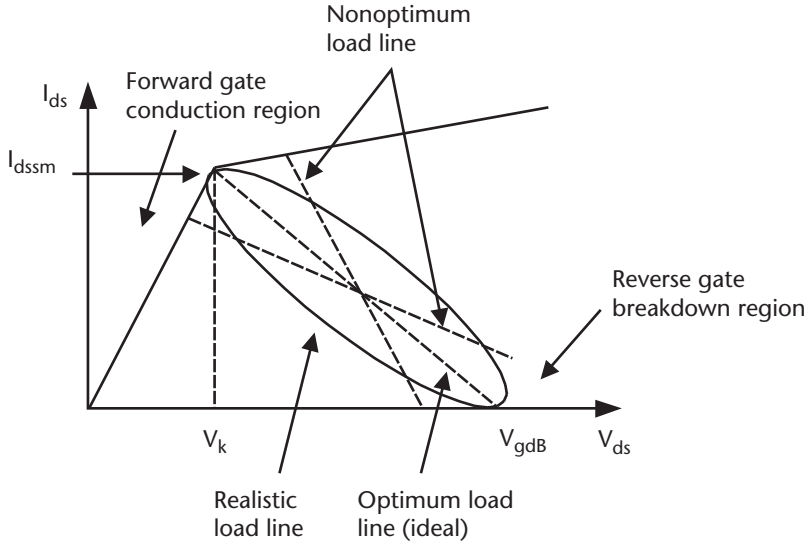


Figure 6.2 Optimum and nonoptimum RF load lines.

characteristic, where the drain current is maximum. Assuming that the amplifier can achieve an RF output power P_o and maximum drain current I_{dssm} per millimeter of gate periphery, with a supply voltage of V_B , then the maximum power-added efficiency of an amplifier can be shown to be given by [10]

$$\eta = (1 - 1/G) P_o / P_{dc} \quad (6.1)$$

where

- η = power-added efficiency;
- P_o = output power;
- P_{dc} = dc power consumption;
- G = gain at P_o .

Therefore, in order to maximize the power-added efficiency of an amplifier, the dc power consumption must be minimized while the gain and output power must be maximized. The output power is maximized by presenting the optimum large-signal load impedance to the device. The load line analysis does not account for the complex behavior of the active device under large-signal operation. Therefore, in order to accurately predict the amplifier's large-signal performance, it is necessary to use the device's large-signal model in the simulation analysis.

Under large-signal conditions, it is found that the load line for the active device deviates from the ideal conditions, as indicated in Figure 6.2. In fact, the load line in practice tends to exhibit an elliptical shape, which results from the reactance associated with the drain-source capacitance C_{ds} , with the device operating into a 50- Ω circuit. Optimal RF performance [10] is obtained when the drain and gate are

biased at the center of the load line such that the onset of saturation is caused by the simultaneous and balanced interaction of the load with the breakdown and forward gate conduction regions of the RF-IV characteristics for a particular DPHEMT.

6.4 Design of TWDAs

Two TWDAs designed to operate over the frequency range of 2 to 18 GHz consist of a single-stage traveling wave amplifier (SSTWA) and a high gain traveling wave amplifier that comprised of three cascaded single-stage traveling wave amplifiers (three-stage SSTWA). The optimum number of devices required for the SSTWA design is calculated using (2.21)–(2.26) in Chapter 2. Table 6.1 shows the optimum number of devices needed in the realization of a traveling wave amplifier design using the DPHEMT devices (LPD200, LP6836, and the LP6872) and for comparison purposes using a typical GaAs MESFET device (MWT-3).

The minimum number of devices needed to realize a traveling wave amplifier is obtained by rounding up of N_{opt} in Table 6.1. For a given gain, a minimum of two DPHEMT devices (LPD200, LP6836, or LP6872) are needed; however, the design requires a minimum of four GaAs MESFET devices. The main reason for this is that for a given cut-off frequency, the DPHEMT devices offers a lower $R_i C_{gs}$ and $R_{ds} C_{ds}$ compared to a typical GaAs MESFET. Based on this result, the design of the SSTWA is comprised of two LP6836 devices.

Having established the number of devices required, the next stage is to calculate the gate- and drain-line inductances, which form a constant- k lowpass filter structure [11]. The characteristic impedance and the cut-off frequencies of the gate and drain lines were made equal, but this can only be done if an external capacitance C_p is added to the output of each of the devices, as C_{gs} is not equal to C_{ds} . The external capacitance is calculated using

$$C_p = C_{gs} - C_{ds} \quad (6.2)$$

The value of gate-line inductance L_g is calculated with (2.26) in Chapter 2 using the device's gate-source capacitance C_{gs} and, for a given cut-off frequency, ω_c , which in this case is 18 GHz. The calculated values of L_g and C_p for the LP6836 are 0.4 nH and 0.6068 pF, respectively.

Table 6.1 Optimum Number of Devices

Device Type	R_i	C_{gs}	R_{ds}	C_{ds}	N_{opt}
LPD200	4.1 Ω	0.38 pF	373 Ω	0.031 pF	1.95
LP6836	0.763 Ω	0.663 pF	296 Ω	0.0562 pF	1.76
LP6872	0.965 Ω	0.103 pF	155 Ω	0.132 pF	1.65
MWT-3	0.8 Ω	0.5 pF	350 Ω	0.12 pF	4

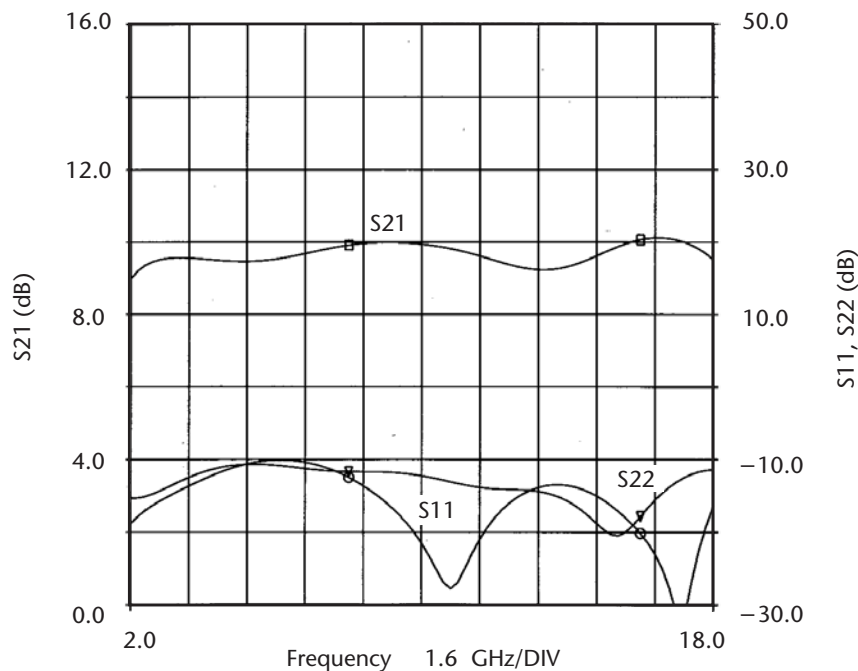


Figure 6.4 Optimized small-signal gain simulation of the SSTWA.

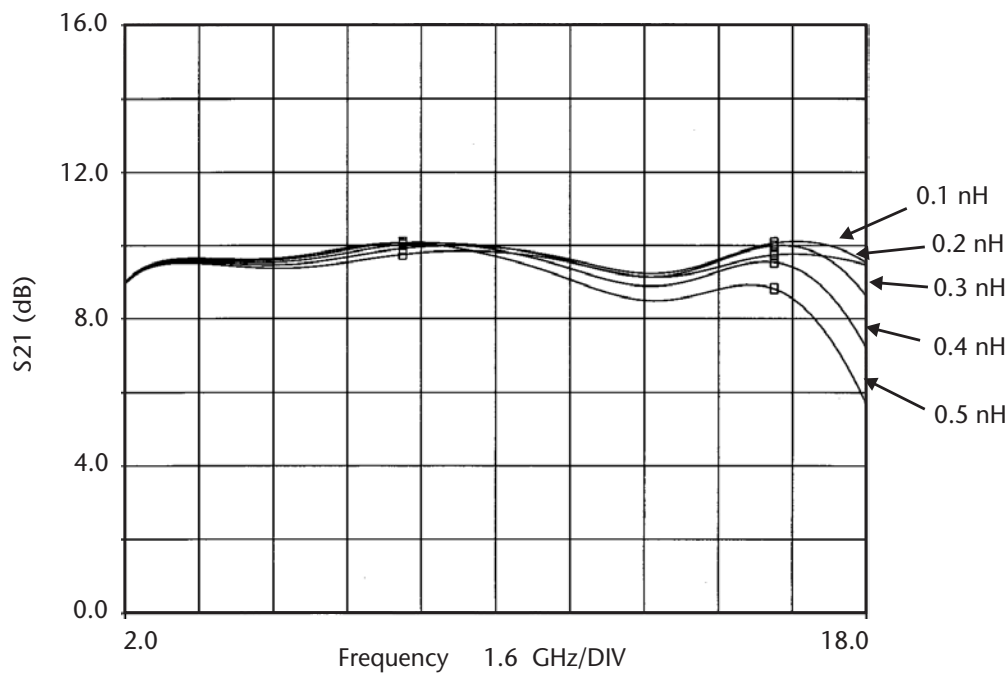


Figure 6.5 Effect of input gate inductance on the small-signal gain.

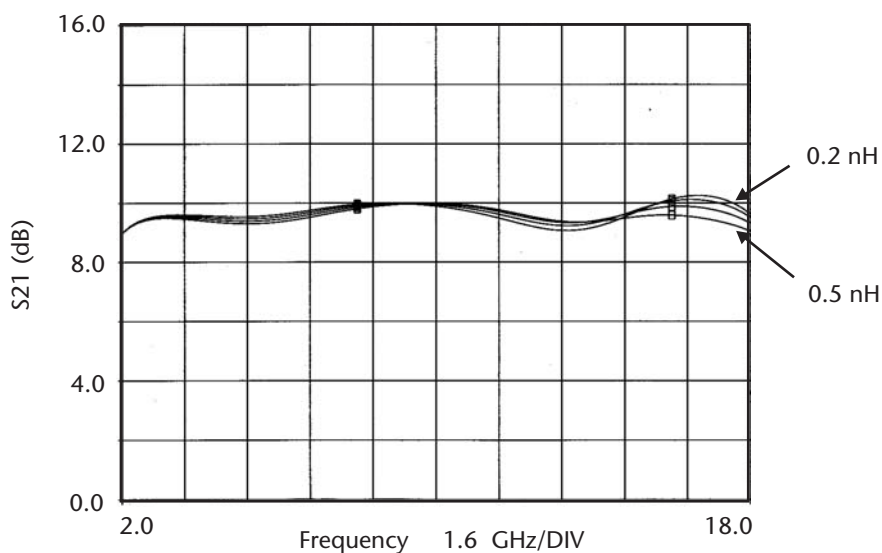


Figure 6.6 Effect of output drain inductance on the small-signal gain.

The stability factor (K) of the SSTWA amplifier, shown in Figure 6.7, confirms that the amplifier is unconditionally stable over the entire 0- to 40-GHz frequency range. Three of the SSTWAs were cascaded together to realize the high-gain three-stage SSTWA. The schematic diagram of this circuit is shown in Figure 6.8. The optimized small-signal simulation response of this amplifier is shown in Figure 6.9.

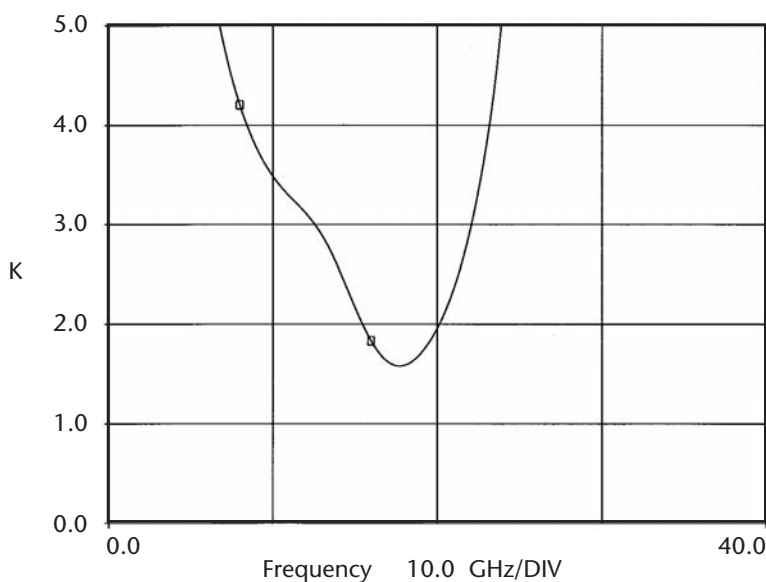


Figure 6.7 Stability factor of the SSTWA.



Figure 6.8 Schematic diagram of the three-stage SSTWA circuit.

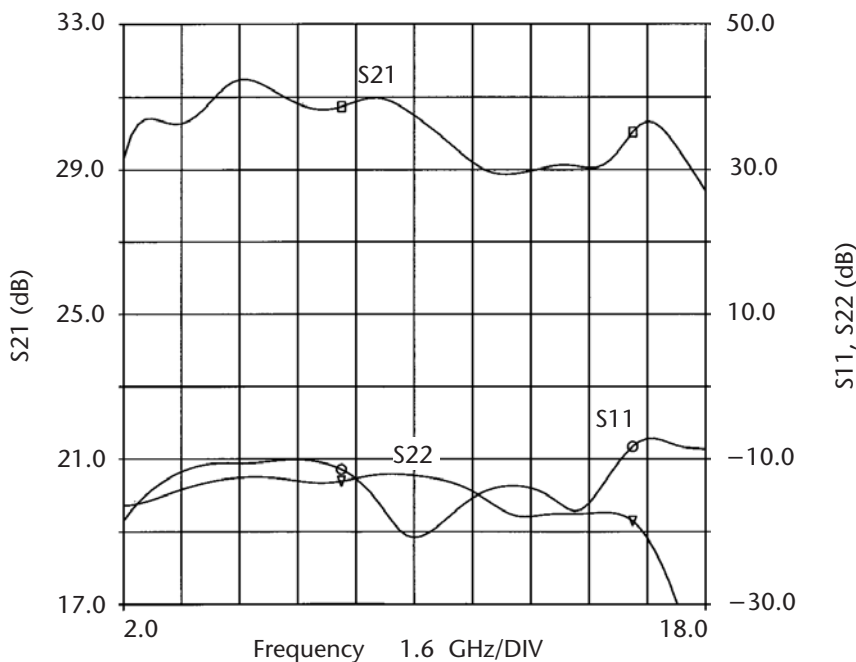


Figure 6.9 Optimized small-signal transmission and return loss response of the three-stage SSTWA.

A gain level of 30 ± 1.25 dB is predicted with input and output return loss of better than about 10 dB across 2 to 18 GHz.

The output stage of the three-stage SSTWA was analyzed under large-signal conditions by using the large-signal model of the LP6836 device. Figure 6.10 shows the variation of the load line on the drain-source current versus drain-source voltage characteristic curves. The reactive part of the RF load, as seen by the device's current source, contributes to reactive power dissipation, which transforms the actual load curve into an ellipse [12]. As the device is matched to 50Ω at the output port, the device load line deviates from the optimum load line trajectory. This causes a nonoptimum large-signal match at the output device and consequently results in low output power and hence low power-added efficiency performance. The value of the resistive RF load, obtained from Figure 3.9 in Chapter 3, is 74Ω for optimum output power performance. However, the actual value of the RF load is 33.5Ω , which corresponds to the reciprocal of the gradient of the nonoptimum load line in Figure 6.10.

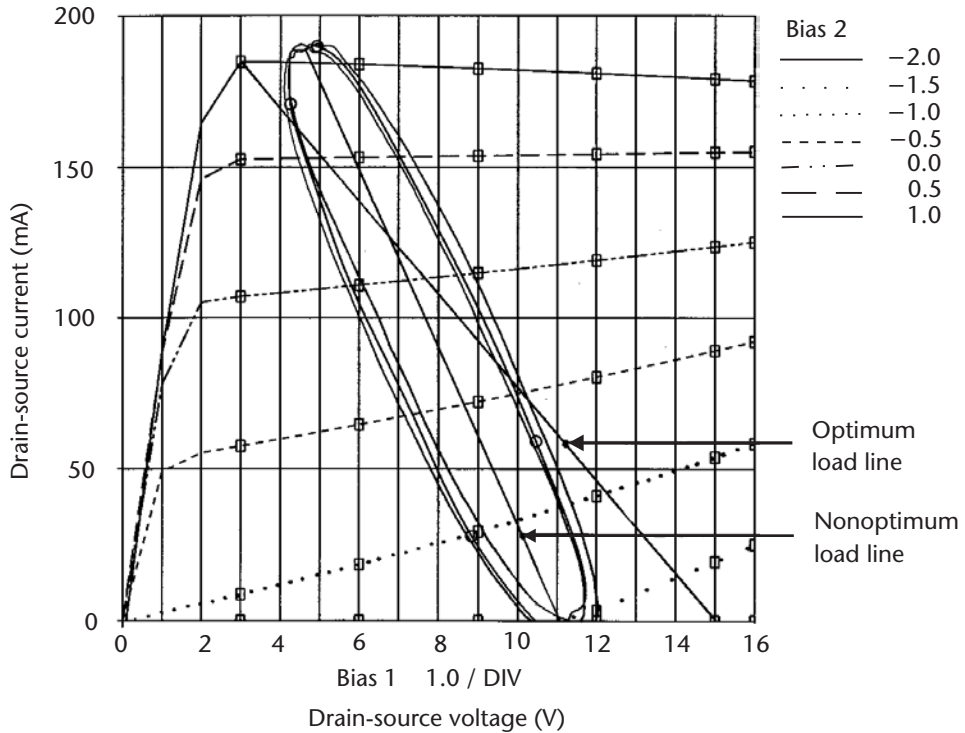


Figure 6.10 Simulated output load line response of the three-stage SSTWA at 2 GHz, 10 GHz, and 18 GHz.

6.4.1 Fabrication of TWDAs

The SSTWA and the three-stage SSTWA circuits were realized using the conventional MIC thin-film fabrication technology. The practical design considerations and fabrication techniques of these amplifiers are discussed in detail in Chapter 7. The amplifier circuits were realized on Alumina substrate with a dielectric constant of $\epsilon_r = 9.8$ and substrate thickness of $h = 0.381$ mm. All of the resistors on the circuit were processed thin-film resistors fabricated as part of the nichrome layer. All of the DPHEMT devices and components were epoxy attached and cured at a temperature of 150°C . The circuit interconnections were carried out using 0.7-mil gold bond wires, whose lengths were calculated to correspond to the values of the bond-wire inductances required. The substrate was soldered onto a gold-plated copper/tungsten carrier, and the completed amplifier was placed inside aluminum housing. The assembly drawing for the SSTWA and three-stage SSTWA modules is shown in Figures 6.11 and 6.12, respectively. The fabricated amplifiers are shown in Figures 6.13 and 6.14.

6.4.2 Measured Response of TWDAs

The SSTWA and three-stage SSTWA were mounted on custom-made test jigs (see Chapter 7), and the LP6836 devices in the amplifiers were biased to operate at a

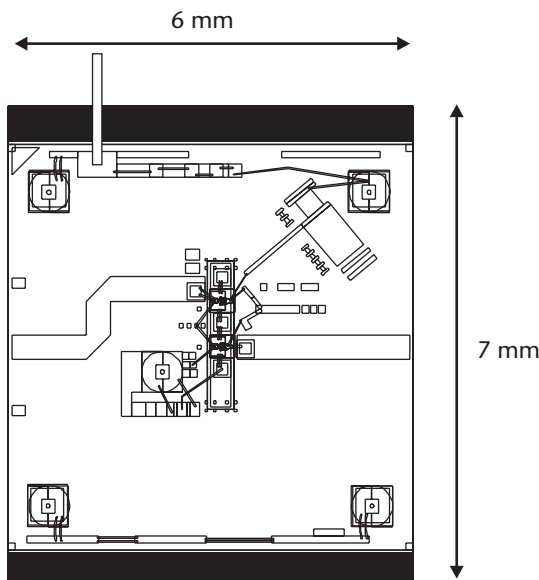


Figure 6.11 SSTWA assembly.

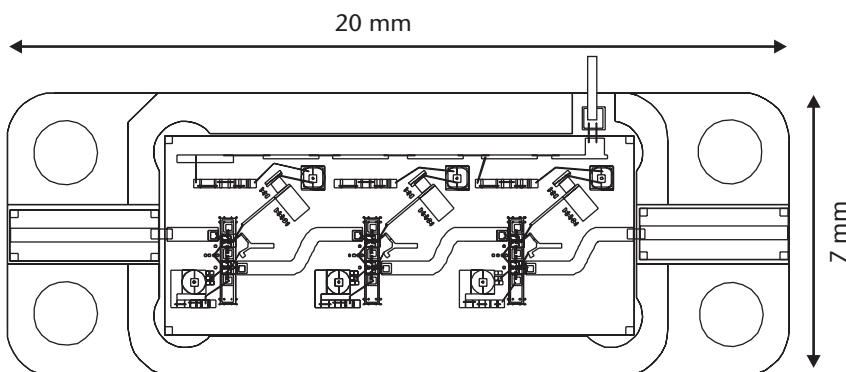


Figure 6.12 Three-stage SSTWA assembly.

drain-source voltage $V_{ds} = 8\text{V}$ at $0.5 I_{dss}$. The measured small-signal response of the SSTWA across 2 to 18 GHz is shown in Figure 6.15. This amplifier achieved a small-signal gain level of 8 ± 1 dB and its input and output return loss is better than 9.5 dB. The measured small-signal response of the 3-stage SSTWA over 2 to 18 GHz is shown in Figure 6.16. This amplifier provided a small-signal gain of 29 ± 1 dB, and its input and output return loss is better than 9.5 dB. The small-signal performance measurements for both of these amplifiers are in excellent agreement with the predicted performance in Figures 6.4 and 6.9.

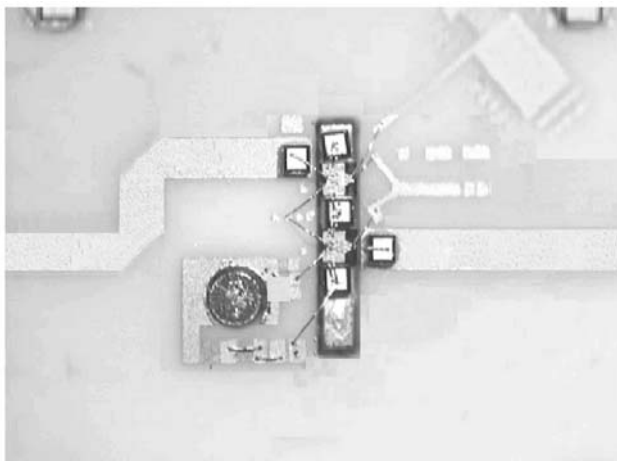


Figure 6.13 Fabricated SSTWA circuit.

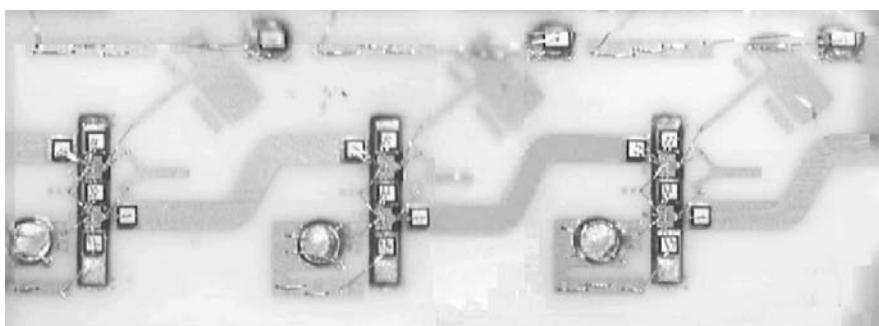


Figure 6.14 Fabricated three-stage SSTWA circuit.

The predicted and measured output power and power-added efficiency performance of the three-stage SSTWA module at 18 GHz is shown in Figure 6.17. The amplifier provides an output power of 21 dBm at the 2-dB compression point with a power-added efficiency of about 5%. Figure 6.18 shows the amplifier's output power, and the efficiency performance is maintained almost constantly across the entire 2- to 18-GHz bandwidth. The agreement between the simulated and measured nonlinear performance shown in these figures is excellent, indicating the accuracy of the characterization and modeling of the devices described in Chapter 4.

6.5 Broadband Feedback Amplifiers

6.5.1 Principles of Broadband Feedback Amplifiers

The principle of the negative feedback amplifier [13–16] is based on the near-ideal voltage-controlled current-source characteristics of the microwave FET device

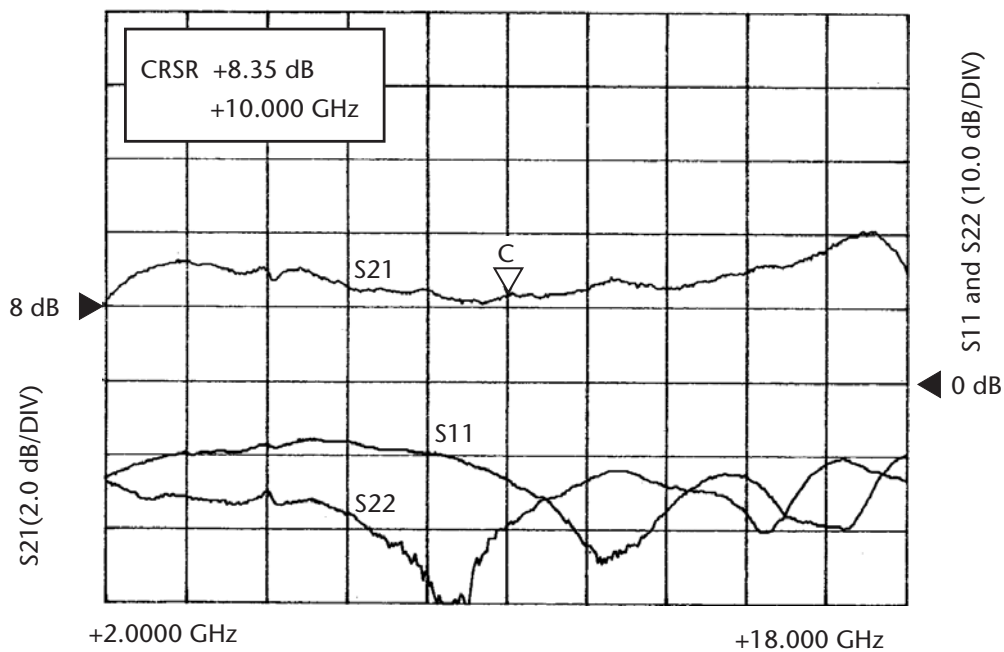


Figure 6.15 Measured small-signal gain response of the SSTWA.

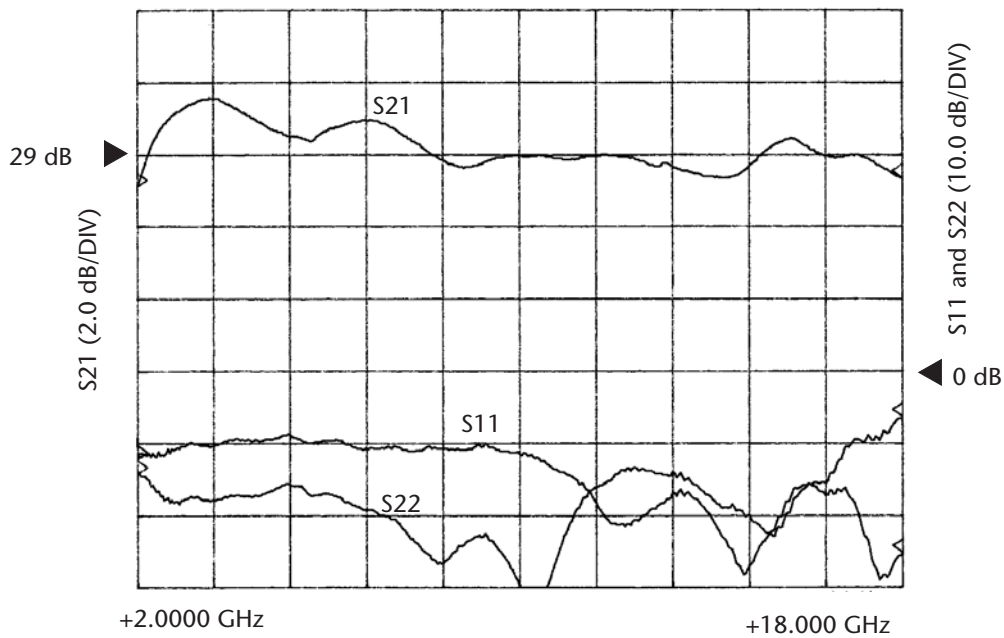


Figure 6.16 Measured small-signal response of the three-stage SSTWA.

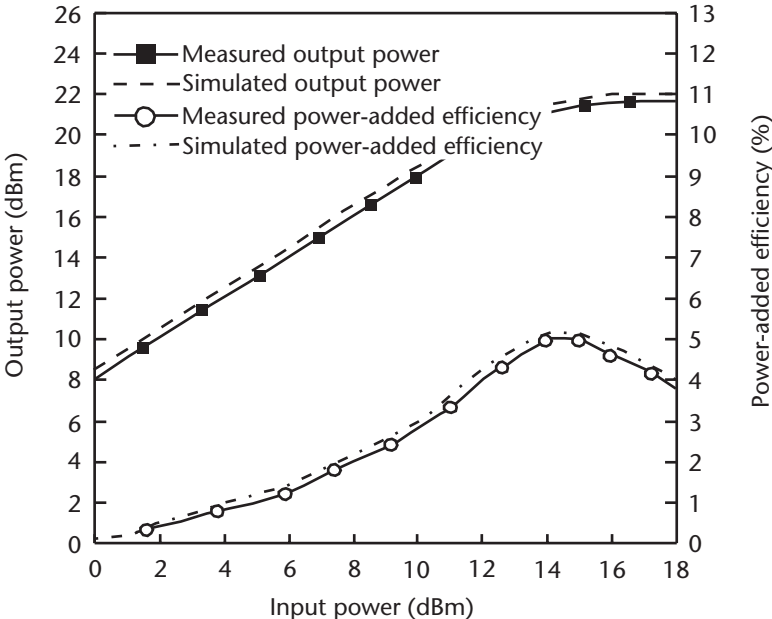


Figure 6.17 Simulated and measured output power and power-added efficiency as a function of input power of the three-stage SSTWA at 18 GHz.

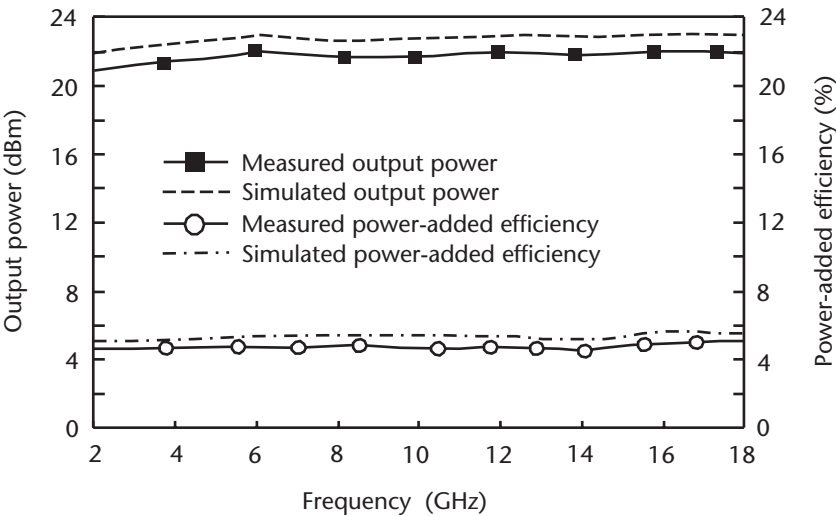


Figure 6.18 Simulated and measured output power and power-added efficiency response of the three-stage SSTWA over 2 to 18 GHz.

operated at low frequencies. Application of series and shunt resistive feedback, as illustrated in Figure 6.19, is an effective way of simultaneously achieving flat gain and good input and output match, as the following analysis shows.

In the analysis, the FET is represented by the equivalent circuit shown in Figure 6.20, where the effects of the gate-source capacitance C_{gs} and parasitic

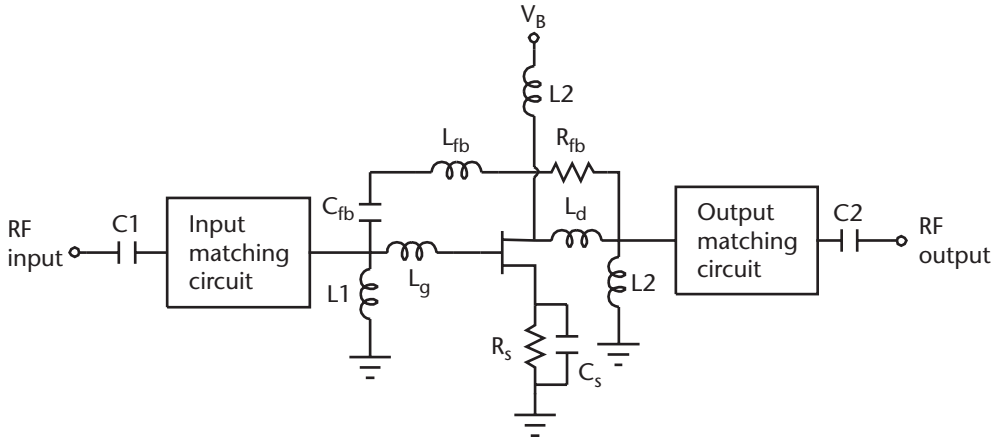


Figure 6.19 Single-stage feedback amplifier circuit.

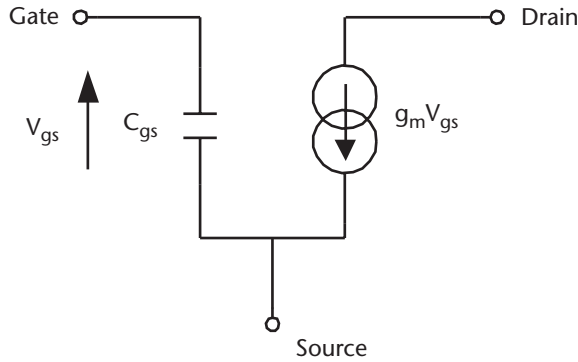


Figure 6.20 FET equivalent circuit.

elements are neglected. The resulting negative feedback equivalent circuit is shown in Figure 6.21.

The admittance matrix for the circuit shown in Figure 6.21 is given by

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{R_{fb}} & -\frac{1}{R_{fb}} \\ \frac{g_m}{1 + g_m R_s} - \frac{1}{R_{fb}} & \frac{1}{R_{fb}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (6.4)$$

The S -parameters corresponding to the y -parameters in (6.4) are

$$S_{11} = S_{22} = \frac{R_{fb}(1 + g_m R_s) - g_m Z_0^2}{g_m Z_0^2 + 2Z_0^2(1 + g_m R_s) + R_{fb}(1 + g_m R_s)} \quad (6.5)$$

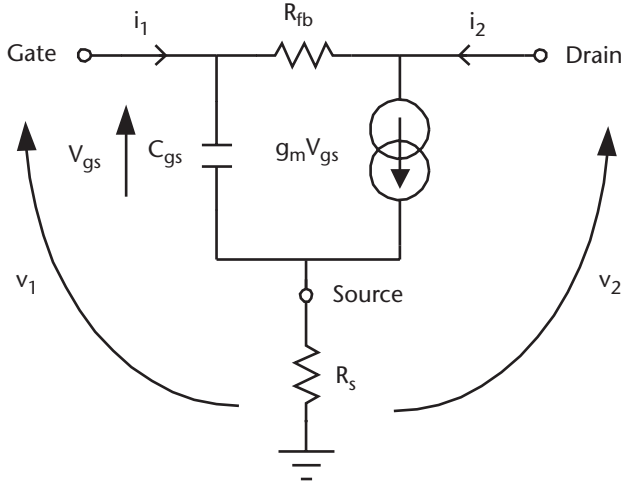


Figure 6.21 FET negative feedback circuit model.

$$S_{21} = G = \frac{2Z_o(1 + g_m R_s) - g_m Z_o R_{fb}}{g_m Z_o^2 + 2Z_o(1 + g_m R_s) + R_{fb}(1 + g_m R_s)} \quad (6.6)$$

and

$$S_{12} = \frac{2Z_o(1 + g_m R_s)}{g_m Z_o^2 + 2Z_o(1 + g_m R_s) + R_{fb}(1 + g_m R_s)} \quad (6.7)$$

where

Z_o = characteristic impedance;
 R_{fb} = shunt feedback resistance;
 R_s = series feedback resistance of the device.

Under matched input and output conditions $S_{11} = S_{22} = 0$ (i.e., input and output VSWR = 1). Hence, from (6.5)

$$R_{fb} = g_m Z_o^2 / (1 + g_m R_s) \quad (6.8)$$

and

$$R_s = (Z_o^2 / R_{fb}) - 1/g_m \quad (6.9)$$

Substituting (6.9) into (6.6) gives

$$G = 1 - (R_{fb} / Z_o) \quad (6.10)$$

Equation (6.10) shows that the gain of the shunt feedback amplifier depends only on R_{fb} and not on the FET's parameters. Therefore gain flattening can be achieved with negative feedback.

Because $g_m R_s \ll 1$, (6.8) and (6.10) become

$$R_{fb} = g_m Z_o^2 \quad (6.11)$$

and

$$G = 1 - g_m Z_o \quad (6.12)$$

Thus, if the value for the device's transconductance is known, then the preliminary values of both the shunt feedback resistance and gain under perfect matched conditions can be obtained using these two expressions.

The low cut-off frequency performance of the amplifier is determined by the components $L1$, $L2$, and C_s , which can be determined from the following equations

$$L1 \ \& \ L2 = 25/f_{\min} \text{ (GHz)} \quad (nH) \quad (6.13)$$

and

$$C_s = 150/f_{\min} \text{ (GHz)} \quad (pF) \quad (6.14)$$

The drain inductance L_d and the feedback inductance L_{fb} control the bandwidth of the feedback amplifier for a given device. In fact, L_d can be used to compensate for the drain-to-source capacitance of the device, and hence the upper frequency band edge. Because L_{fb} affects the S-parameters of the amplifier, it can be adjusted to maximize the feedback at the lower frequency band edge. In addition, it is necessary to include input and output matching networks in the amplifier design to negate parasitic effects, which render the feedback ineffective at the higher frequency end of the band. The matching networks have the benefit of improving the amplifier's terminal VSWR.

The simulated response of the gain and input/output return loss variation with feedback resistor is shown in Figure 6.22. The response shown excludes any device matching. The optimum value of the feedback resistor R_{fb} is in the range of 200Ω to 250Ω , as this gives a very good input and good output return loss performance. The gain of the amplifier corresponding to these values of R_{fb} is predicted to be 8 to 10 dB. This figure also indicates that the output return loss is negligible for R_{fb} values between 250Ω and 680Ω . The variation of the gain and input/output return loss as function of the frequency is shown in Figure 6.23. From the graphs in this figure, it is clear that the lower the magnitude of the feedback resistor, the flatter the gain response as the low frequency gain is sacrificed for flatness. The graph shows that a feedback resistor of 200Ω provides a reasonably flat gain response and a good output return loss performance from dc to 24 GHz. The input return loss deteriorates

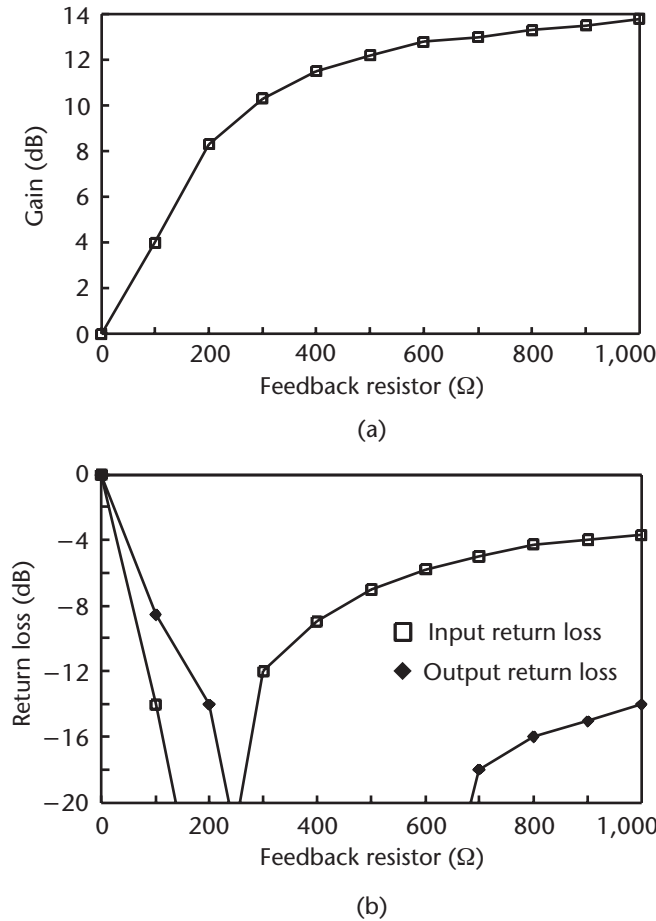


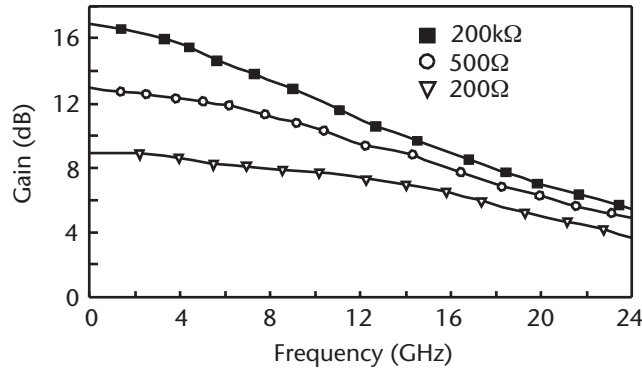
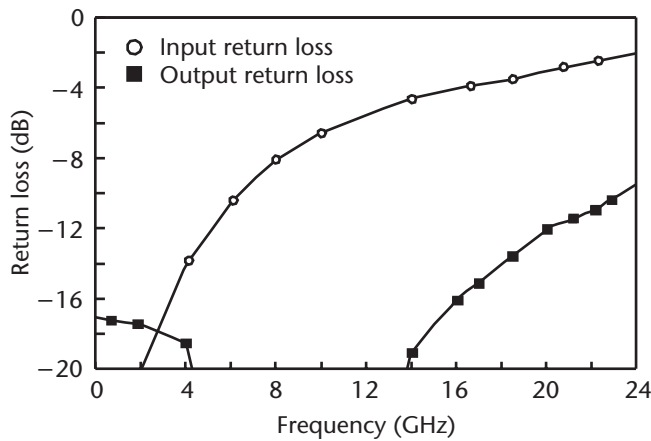
Figure 6.22 Simulated gain, input return loss, and output return loss as a function of the feedback resistor value.

with increasing frequency; however, it can be improved with the inclusion of matching network.

In practice, however, the gain performance of the amplifier is undermined by the device's parasitic elements, bond-wire lengths, biasing parasitic elements, and the input and output matching circuit. Therefore, if these factors are not included in the design process, the resulting amplifiers performance, especially at the high-frequency end, will be nonoptimum.

6.5.2 Design of a Three-Stage Feedback Amplifier

It has been shown that for a given device with transconductance g_m , the magnitude of the feedback resistor can be determined for a perfect input and output match condition using (6.11). Of course, parasitic elements within the device will modify this result. Therefore, (6.11) should be regarded as a general rule that provides a first estimate of the gain of a feedback amplifier. In practical amplifiers, the shunt

(a) For various values of R_{fb} (b) For $R_{fb} = 200\Omega$ **Figure 6.23** Simulated gain, input return loss, and output return loss as a function of frequency.

feedback resistor itself would become a series inductor, resistor, capacitor (LRC) network due to the layout and biasing parasitic elements. Hence, some matching may be necessary to account for the nonideal nature of both the device and the feedback resistor. Moreover, the gain of the amplifier can be made almost constant with frequency with the application of an appropriate shunt feedback resistor across the device.

This procedure was used in the design a high-gain three-stage negative feedback amplifier to operate over the frequency range of 2 to 18 GHz. The value of the feedback resistor for each of the three stages was initially set to 200Ω , assuming perfectly matched conditions. The elements L_{fb} , L_d , L_g , R_{fb} , and input/output matching networks of each of the individual feedback amplifiers were optimized using commercially available simulation tools. The optimized input matching circuits consisted of an open-circuit shunt stub and a series transmission line. The output

return loss was optimized by inserting a series transmission line, which was connected to the output terminal of element L_d . The schematic diagram of this circuit is shown in Figure 6.24. The optimized schematic circuit of the first-stage feedback amplifier comprising of an LPD200 device is shown in Figure 6.25. The second-stage and the third-stage feedback amplifiers were comprised of LP6836 and LP6872 devices, respectively. The optimized simulation result of the small-signal response is shown in Figure 6.26. The predicted gain level of the amplifier is 26 ± 1 dB, with the input and output return loss better than 9.5 dB and 5 dB, respectively.

The output stage of the three-stage feedback amplifier was analyzed under large-signal operation. This amplifier was comprised of an LP6872 device, whose large-signal model in Chapter 4 was used in the simulation. Figure 6.27 shows the variation of the load line on the drain-source current versus drain-source voltage characteristic curves. Because the reactive part of the RF load as seen by the current source of the device contributes to reactive power dissipation, this effect transforms the actual load curve into an ellipse. As the device is matched to 50Ω at the output port, the device load line deviates from the optimum load line trajectory. This causes a nonoptimum large-signal match at the output device and consequently results in low output power and power-added efficiency performance. The value of the resistive RF load for optimum output power performance should be 40Ω ; however, from Figure 6.27, the RF load is 17Ω .

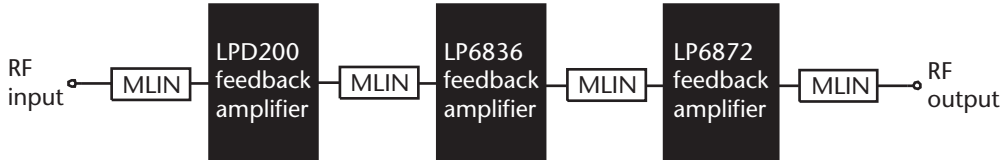


Figure 6.24 Schematic diagram of the three-stage feedback amplifier.

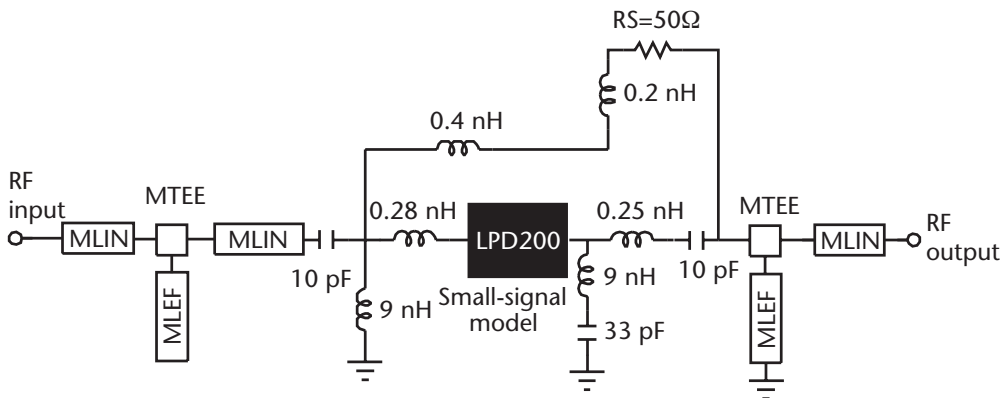


Figure 6.25 Schematic diagram of the first-stage feedback amplifier.

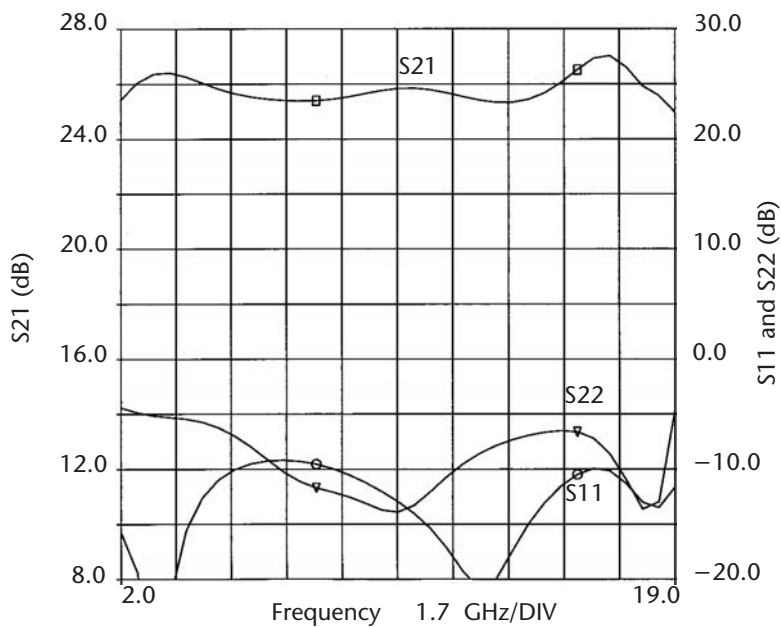


Figure 6.26 Optimized gain, input return loss, and output return loss of the three-stage feedback amplifier.

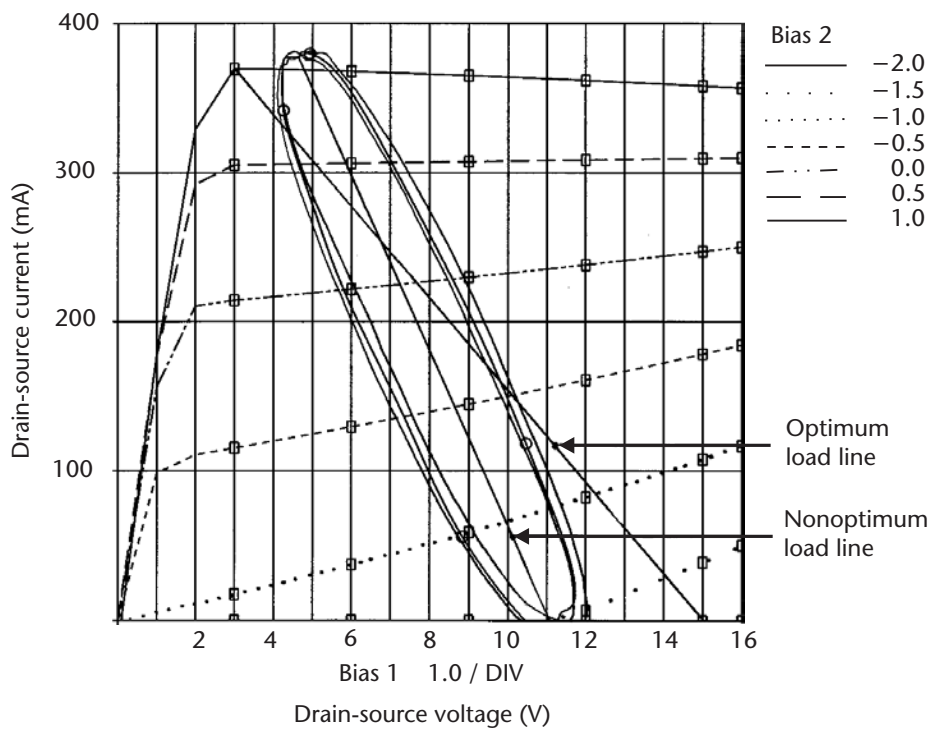


Figure 6.27 Output load line response of three-stage feedback amplifier at 2 GHz, 10 GHz, and 18 GHz.

6.5.3 Fabrication of Three-Stage Feedback Amplifier

Conventional MIC thin-film fabrication technology was used to realize the three-stage feedback amplifier. The detailed practical design considerations and fabrication techniques employed in the realization of the amplifier are outlined in Chapter 7. Figure 6.28 shows the assembly drawing of the three-stage feedback amplifier circuit. The fabricated amplifier is shown in Figure 6.29. All other fabrication details are similar to those provided in Section 6.4.1.

6.5.4 Measured Response of Three-Stage Feedback Amplifier

Figure 6.30 shows the measured small-signal response of the fabricated three-stage feedback amplifier with the devices biased at a drain-source voltage $V_{ds} = 8\text{V}$ at $0.5 I_{dss}$. The small-signal gain level achieved is $26 \pm 1\text{ dB}$, and the input and output return loss is better than 9.5 dB and 5 dB, respectively. The measured small-signal responses are in excellent agreement with the predicted response of Figure 6.26.

The measured output power and power-added efficiency performance of the feedback amplifier is shown in Figure 6.31 at a frequency of 18 GHz. The output power achieved was 21 dBm at the 2 dB compression point, and the power-added efficiency at this point was about 14%. The output power of 21 dBm and a power-added efficiency of 14% were maintained over the 2- to 18-GHz frequency range, as

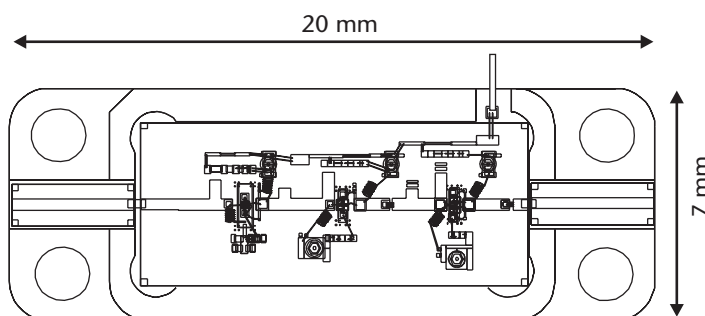


Figure 6.28 Assembly drawing of the three-stage feedback amplifier.



Figure 6.29 Fabricated three-stage feedback amplifier.

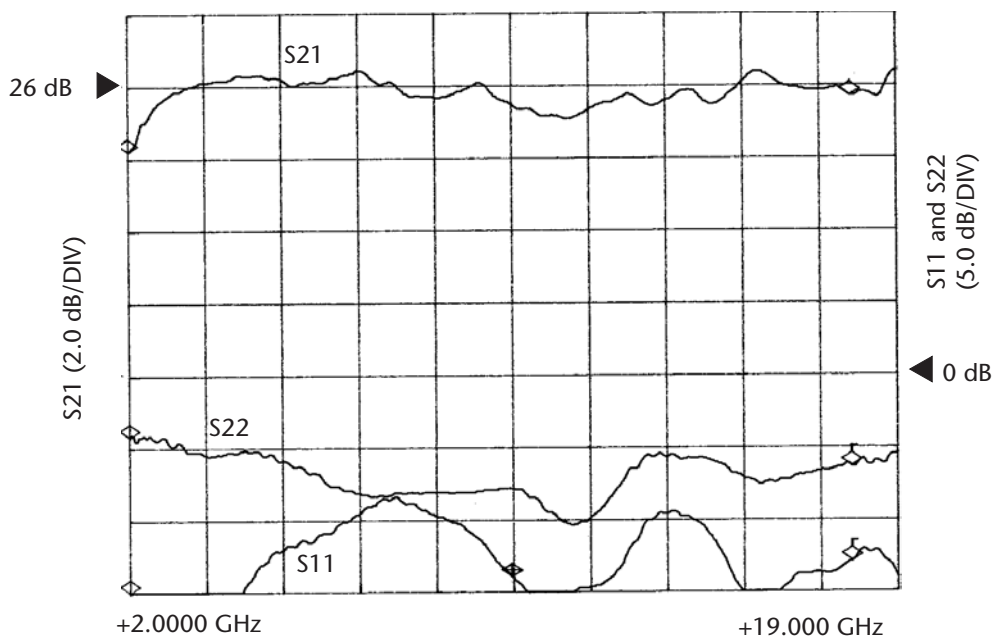


Figure 6.30 Measured small-signal response of the three-stage feedback amplifier.

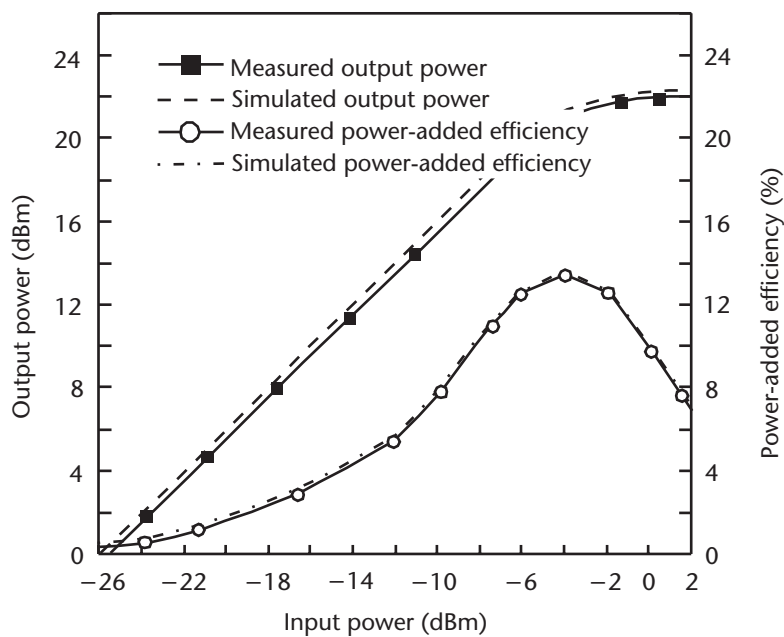


Figure 6.31 Simulated and measured output power and power-added efficiency as a function of input power of the three-stage feedback amplifier at 18 GHz.

shown in Figure 6.32. The agreement between the simulated and measured nonlinear performance shown in these figures is excellent, indicating the accuracy of the characterization and modeling of the devices described in Chapter 4.

6.6 CRTSSDAs

6.6.1 Principles of CRTSSDAs

In this section, the CSSDA presented in Chapters 1 and 2 is improved for large-signal operation and enhanced performance in terms of output power and hence power-added efficiency. As will be shown here, this is achieved by employing reactive terminations, and the arrangement of the resulting amplifier is illustrated in Figure 6.33. This amplifier configuration will be referred to as the CRTSSDA.

In the amplifier, the transistor devices (i.e., $T1, T2 \dots Tn$) are connected in a cascaded arrangement between two artificial transmission lines so that the signal power injected at the matched input port is coupled and amplified by the transconductance of each device before finally terminating at the matched output load.

Like the CSSDA, the CRTSSDA configuration has an advantage over the conventional distributed amplifier in that it does not require any phase equalization. This is because the total output current is not dependent on the phase coherence of the individual current generators. The only requirement is to equalize the characteristic impedance of the input gate and the output drain port of the active devices employed. The gate and drain line inductance present in the circuit, however, limits the amplifier's bandwidth performance.

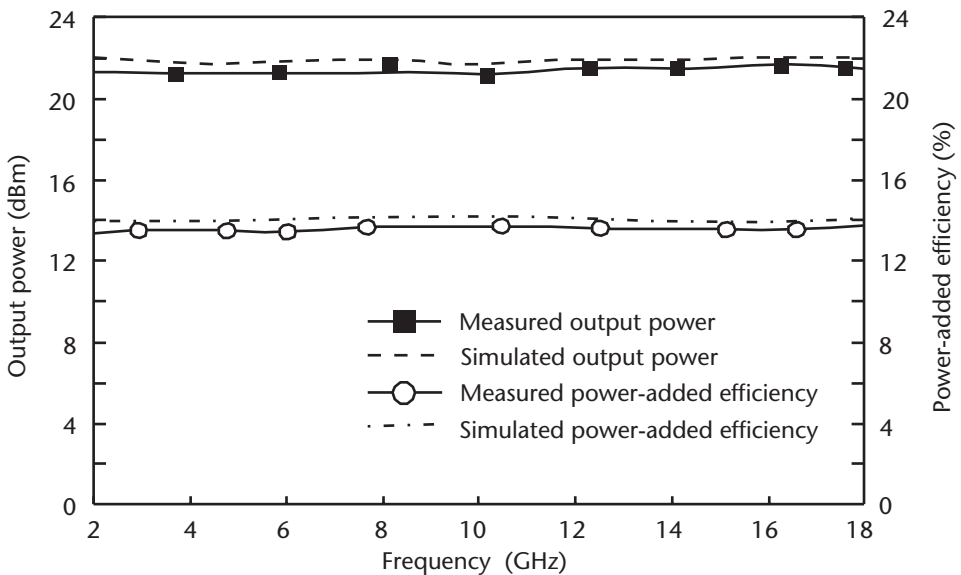


Figure 6.32 Simulated and measured output power and power-added efficiency response of three-stage feedback amplifier over 2 to 18 GHz.

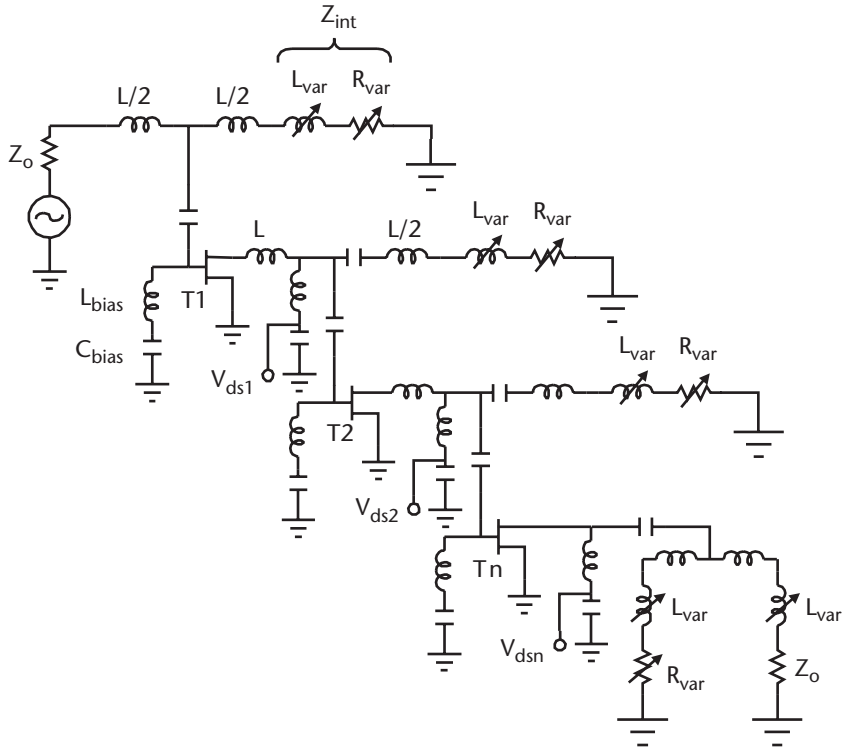


Figure 6.33 The CRTSSDA.

The gain response of the CRTSSDA is increased due to the inclusion of the impedance Z_{int} , represented by the $R_{var}(\omega) + j\omega L_{var}(\omega)$ at the drain terminal of each active device. The effect of the reactive termination is to enhance the voltage swing across each device's input capacitance C_{gs} , which results in an increased output drain current from each device. This consequently improves the amplifier's overall gain performance over the multioctave bandwidth. The input and output characteristic impedance is terminated in the Z_o (i.e., 50Ω). Figure 6.34 shows the equivalent diagram of the n -stage CRTSSDA.

In the CRTSSDA, the active devices are cascaded in series so that the signal propagating forward from the input to the output port is amplified by the successive

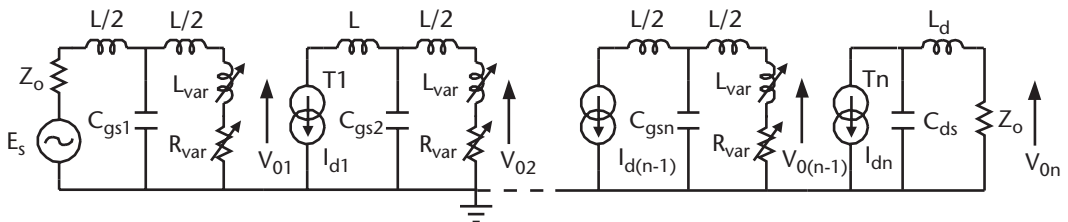


Figure 6.34 Equivalent circuit diagram of the n -stage CRTSSDA.

stages. The resulting gain of this amplifier can be derived, as described in Chapter 2, to be given by

$$G_{\text{crtssda}} = g_m^{2n} Z_{\text{int}}^{2(n-1)} Z_o^2 / 4 \quad (6.15)$$

This is identical to (2.47) and indicates that the gain is an exponential function of the number of device stages n . Therefore, the available power gain of this configuration is substantially higher than that of the conventional traveling wave amplifier (see Section 2.3.1) employing the same number of active devices. This is confirmed in Figure 6.35, which shows the small-signal gain response of a three-stage CRTSSDA and a three-stage conventional traveling wave amplifier, using the same number of identical active devices. The CRTSSDA clearly provides a significantly higher gain than the conventional traveling wave amplifier configuration.

In order for the CRTSSDA module to produce a higher gain than the conventional distributed amplifier, the following relationship must be satisfied

$$G_{\text{crtssda}} \geq G_{\text{twa}} \quad (6.16)$$

$$g_m^{2n} Z_{\text{int}}^{2(n-1)} Z_o^2 / 4 \geq n^2 g_m^2 Z_d Z_g / 4 \quad (6.17)$$

With simplification, this relationship becomes

$$Z_{\text{int}} \geq n^{1/(n-1)} / g_m \quad (6.18)$$

Since $Z_o = Z_g = Z_d$, Equation (6.18) indicates that the impedance Z_{int} decreases as n increases. For example, for n equal to 2 and g_m equal to 101 mS, then Z_{int} is

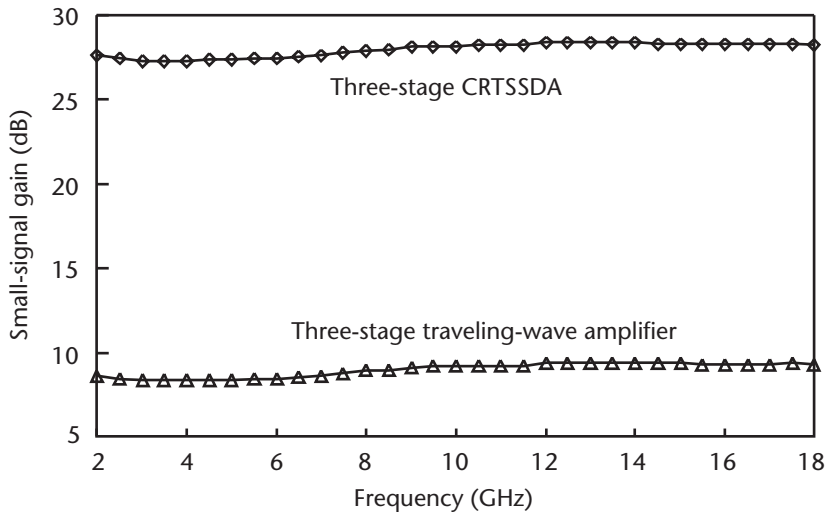


Figure 6.35 Small-signal gain of a three-stage CRTSSDA and a three-stage conventional traveling wave amplifier.

calculated to be 19.8Ω . For n equal to 3, Z_{int} is 17.1Ω . However, (6.15) clearly indicates that for a given number of device stages, the higher the magnitude of impedance Z_{int} , the higher the gain of the amplifier becomes.

Active devices normally have an intrinsic gain roll of -6 dB/octave from dc to an upper operating frequency. Therefore, the design of an n -stage amplifier will have a gain roll off of $-6n$ dB/octave. This means that in order to design a multistage amplifier, it will be necessary to equalize the amplifier's gain for a flat response over the desired bandwidth. In the case of a CRTSSDA, this is simply achieved by adjusting the impedance Z_{int} , because at low frequencies—in the range of 10 kHz to 1 GHz—the effect of $L_{var}(\omega)$ is negligible and R_{var} is virtually independent of frequency. Hence, $Z_{int}(\omega)$ reduces to

$$Z_{int} = R_{var} \quad (6.19)$$

This means that R_{var} can be used to reduce the high gain level of the amplifier at low frequencies. The initial value of the resistance R_{var} can be computed from (6.18), which is dependent on the device transconductance g_m and the number of device stages n constituting the CRTSSDA. Table 6.2 shows the calculated value of R_{var} for various DPHEMT devices.

It should be noted that the calculated value of R_{var} will have to be optimized in order to achieve the required small-signal gain response. The inductive component $L_{var}(\omega)$ will have an effect on the small-signal gain at high frequencies (≥ 2 GHz). The primary effect of this component is to alter the magnitude of the small-signal level at the input port of the respective device in the CRTSSDA chain; that is, the inductive impedance determines the magnitude of the signal voltage that is amplified by the device transconductance. The initial value of $L_{var}(\omega)$ can be calculated from

$$L_{var}(\omega) \geq n^{1/(n-1)} / \omega g_m \quad (6.20)$$

This equation indicates that $L_{var}(\omega)$ is a function of frequency, the device transconductance g_m , and the number of device stages n . Figure 6.36 shows the effect of varying the component $L_{var}(\omega)$ on the small-signal transmission and input/output return loss response of a three-stage CRTSSDA. It can be observed from this figure that $L_{var}(\omega)$ affects the whole response, with the exception of the lower frequency end.

The output power and power-added efficiency of the CRTSSDA module can be improved by incorporating a large-signal impedance matching network in the

Table 6.2 Calculated Value of R_{var}

Device Type	$n = 2$	$n = 3$	$n = 4$	$n = 5$
LPD200	25Ω	21.6Ω	19.8Ω	18.7Ω
LP6836	19.8Ω	17.1Ω	15.7Ω	14.8Ω
LP6872	10.1Ω	8.7Ω	8.0Ω	7.55Ω

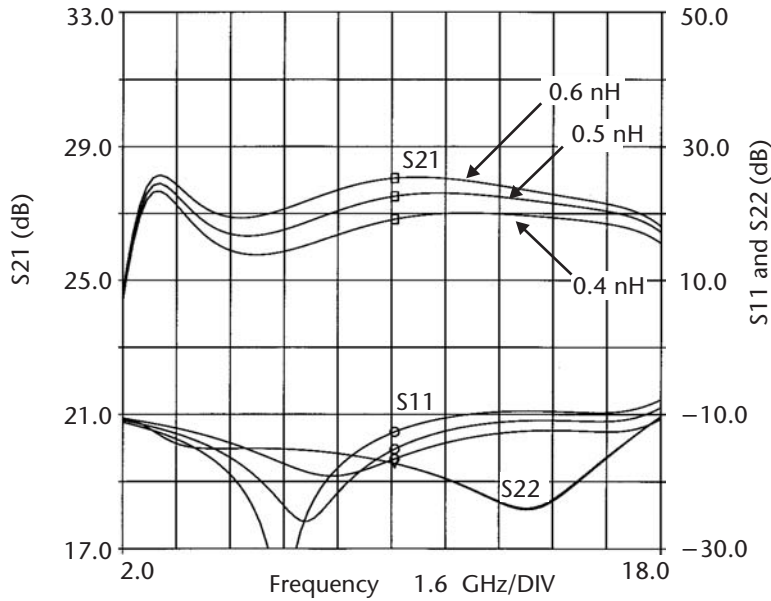


Figure 6.36 Effect of $L_{var}(\omega)$ on the small-signal transmission and input/output return loss response of a three-stage CRTSSDA.

design [17], represented by the impedance transformer ($n:1$) at the output of device T_n , as illustrated in Figure 6.37.

Because the power-added efficiency and output power of an amplifier are related by the expression in (6.1), in order to maximize the amplifier's efficiency, its

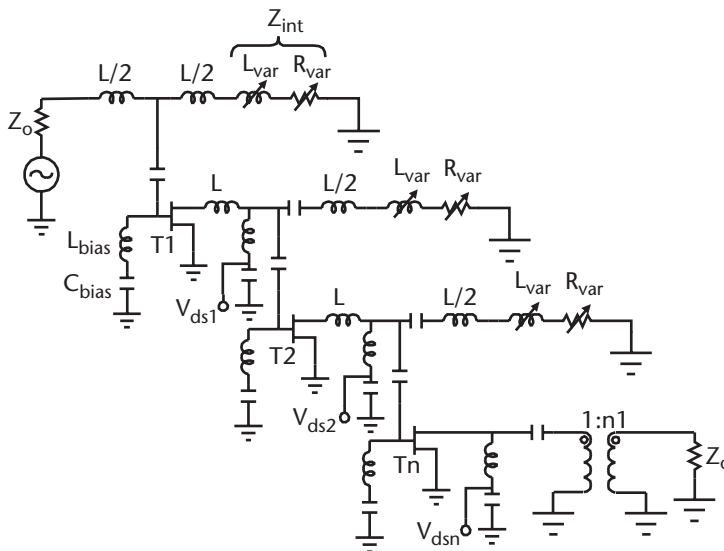


Figure 6.37 CRTSSDA matched for optimum output power and efficiency.

dc power consumption must be minimized and its gain and output power must be maximized. Fortunately, the CRTSSDA configuration has the inherent advantage of offering high gain and output power. However, its power consumption can be minimized by employing devices that have been tailored for minimum dc power consumption at the input and intermediate stages. This is feasible as the large-signal load impedance is determined by the characteristics of the output device in the amplifier configuration. The load impedance is important as it determines the output power. The optimum output power can be determined from

$$R_{Lopt} = (V_{gdb} - V_p - V_k) / I_{max} \quad (6.21)$$

where

- V_{gdb} = gate-to-drain breakdown voltage;
- V_p = pinch-off voltage;
- V_k = knee voltage at which I_{max} is reached;
- I_{max} = maximum drain current.

Load impedance greater than R_{Lopt} results in reduced current swing, while load impedance less than R_{Lopt} results in reduced voltage. In order to provide optimally matched load impedance over the desired bandwidth of operation, it is necessary to analyze the amplifier using the large-signal device model. The trajectory of load impedance at the upper and lower frequency band edges in the device's I_{ds} - V_{ds} characteristic can then be used to determine the optimum load.

6.6.2 Design of High Gain CRTSSDA

The design procedure for a high-gain CRTSSDA begins with calculation of the impedance Z_{int} using (6.18), which depends on the transconductance g_m of the device used and the number of devices n comprising the amplifier. The value of the impedance defined by this equation is the minimum required in the CRTSSDA design to produce a gain level that is higher than that achievable by a conventional distributed amplifier using the same number of identical devices. For a three-stage CRTSSDA employing DPHEMT device LP6836, which has a transconductance value of 101 mS, the calculated value of Z_{int} is 17.15Ω. The gain of the amplifier can then be calculated using (6.15), where the impedance Z_o is 50Ω. The gain level achievable with these values is 17.6 dB. However, as the amplifier was required to have a gain of 27 dB across 2 to 18 GHz, the value of impedance Z_{int} was made to be 29.52Ω.

The gate and drain bond-wire inductance of the devices used were calculated using (2.26) for the required upper cut-off frequency—in this case 18 GHz. As the bias elements determine the amplifier's low frequency cut-off point, in this case 2 GHz, they were calculated using (6.13) and (6.14).

The schematic diagram of the optimized three-stage CRTSSDA comprised of LP6836 devices is shown in Figure 6.38. The broadband stability of the amplifier,

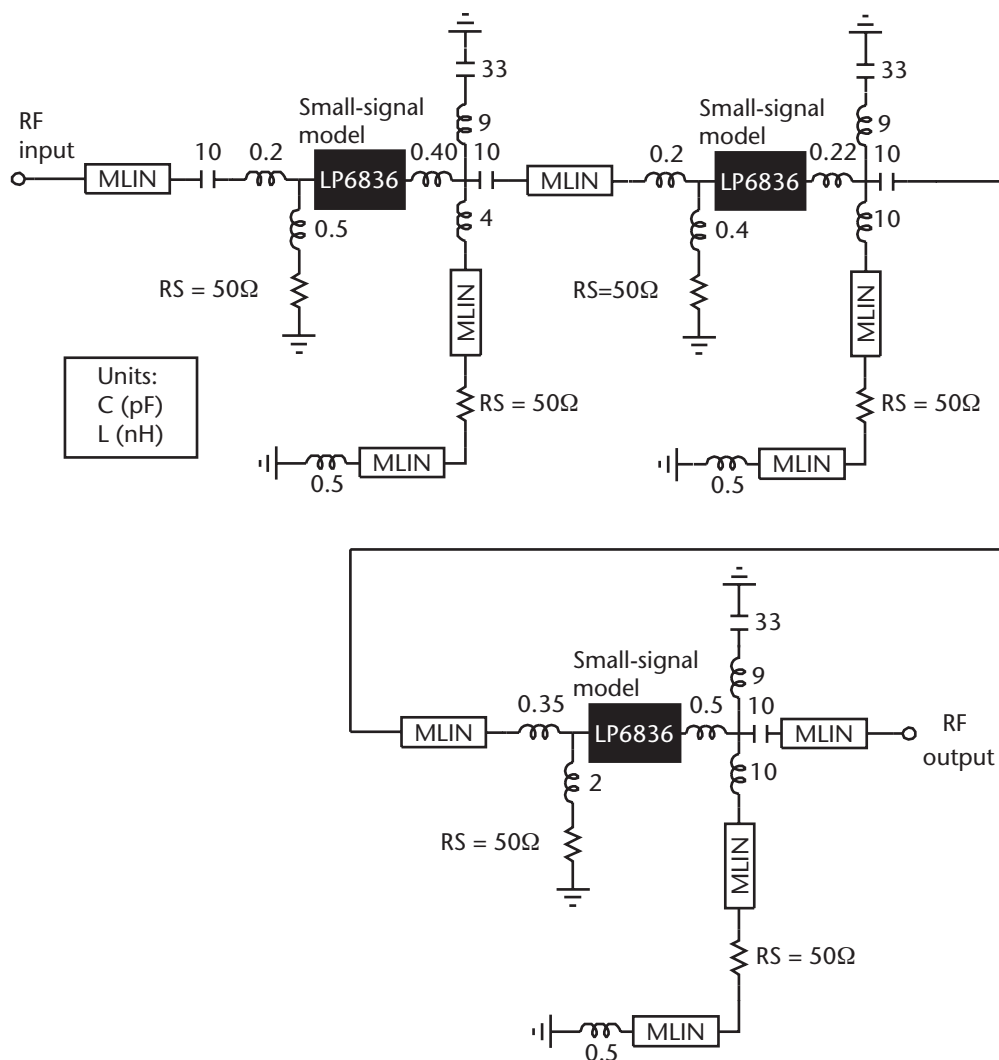


Figure 6.38 Schematic diagram of the optimized three-stage CRTSSDA using LP6836.

shown in Figure 6.39, is greater than unity, which indicates unconditional stability from dc to 50 GHz. The optimized small-signal response of the amplifier, shown in Figure 6.40, predicts a gain level of 27 ± 1 dB with input and output VSWRs better than 9.5 dB.

The output stage of the CRTSSDA was analyzed under large-signal operation by using the large-signal device model for LP6836 obtained in Chapter 4. Figure 6.41 shows how the load line varies on the characteristic I-V curves. The actual load line appears to be an ellipse, as the current source of the device dissipates power in the reactive part of the RF load. As the device is matched to 50Ω at the output port, the device load line will deviate from the optimum load line trajectory. This will

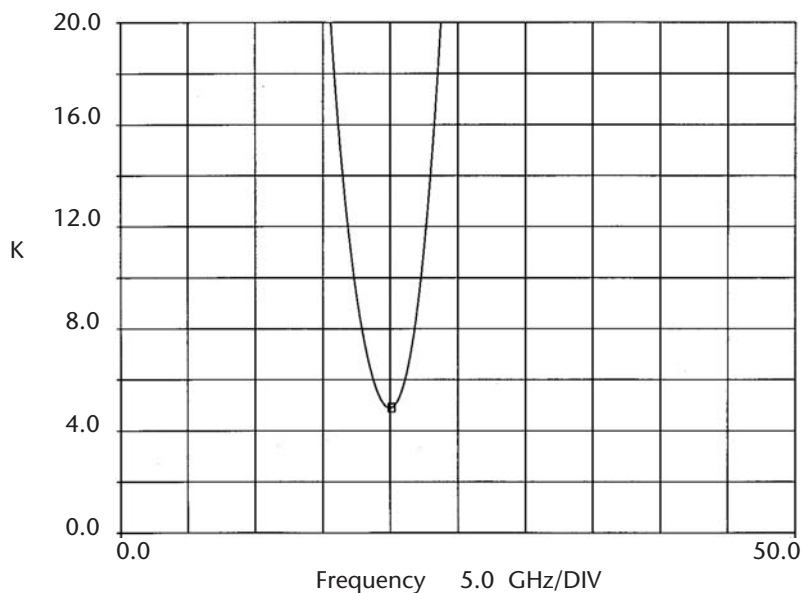


Figure 6.39 Stability factor 'K' of the three-stage CRTSSDA.

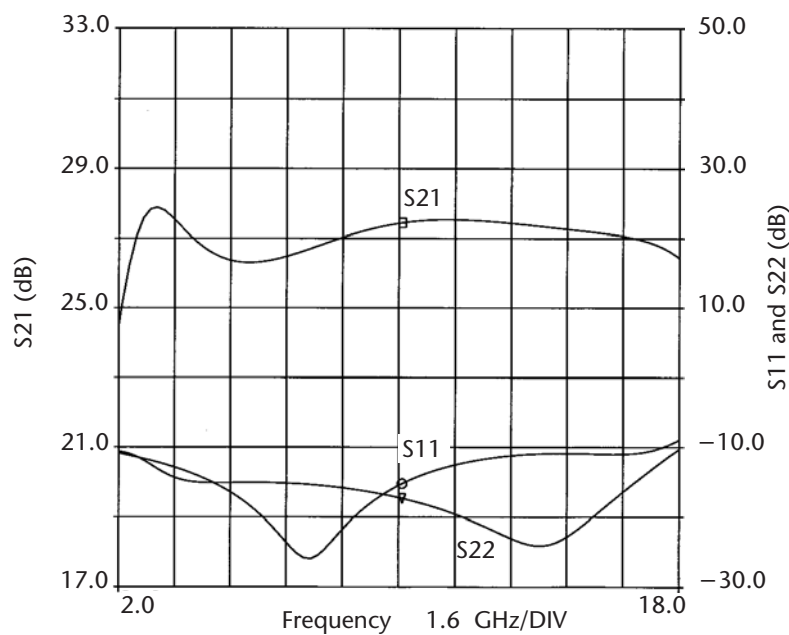


Figure 6.40 Optimized transmission and input/output return loss response of the three-stage CRTSSDA.

cause a nonoptimum large-signal match at the output device, and consequently this will erode the amplifier's output power performance. For this device the optimum

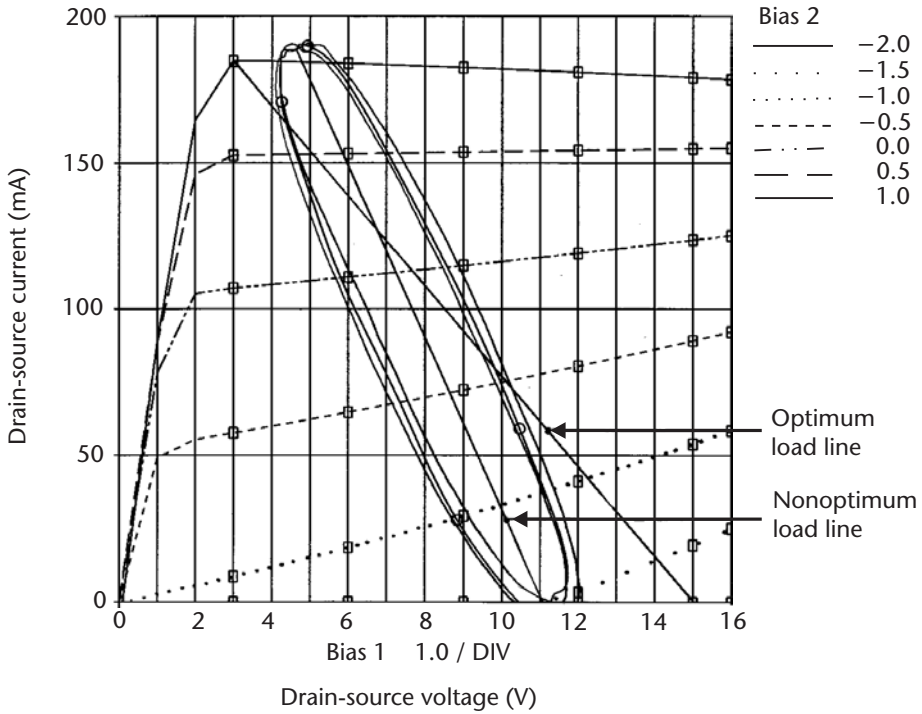


Figure 6.41 Output load line response of the three-stage CRTSSDA at 2 GHz, 10 GHz, and 18 GHz.

value of the large-signal RF load should be 70Ω for optimum output power performance according to Figure 3.9 in Chapter 3. However, from Figure 6.41, the actual large-signal RF load the device in this amplifier configuration sees is 33.5Ω .

The amplifier's small-signal performance was analyzed to determine which of the circuit elements defined in Figure 6.42 affected it most significantly. This was done to establish the critical elements that would need tight control in the amplifier's fabrication stage. The amplifier is comprised of 18 circuit elements, which are defined as:

- L_{d1} : Drain inductance of first device;
- L_{d2} : Drain inductance of second device;

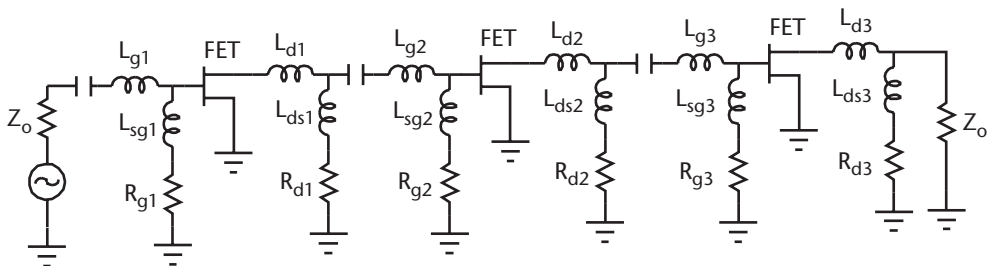


Figure 6.42 Circuit elements of the three-stage CRTSSDA.

- L_{d3} : Drain inductance of third device;
- L_{g1} : Gate inductance of first device;
- L_{g2} : Gate inductance of second device;
- L_{g3} : Gate inductance of third device;
- L_{sg1} : Shunt gate inductance of first device;
- L_{sg2} : Shunt gate inductance of second device;
- L_{sg3} : Shunt gate inductance of third device;
- L_{ds1} : Shunt drain inductance of first device;
- L_{ds2} : Shunt drain inductance of second device;
- L_{ds3} : Shunt drain inductance of third device;
- R_{g1} : Shunt gate resistance of first device;
- R_{g2} : Shunt gate resistance of second device;
- R_{g3} : Shunt gate resistance of third device;
- R_{d1} : Shunt drain resistance of first device;
- R_{d2} : Shunt drain resistance of second device;
- R_{d3} : Shunt drain resistance of third device.

The elements that affect the amplifier's small-signal response appreciably by applying small variations to their optimized values are L_{d2} , L_{g3} , L_{sg1} , L_{sg2} , and R_{g2} , as shown by the simulation in Figures 6.43–6.47. These results clearly show that element L_{d2} and L_{g3} mainly effect the response over the mid- and high-frequency band,

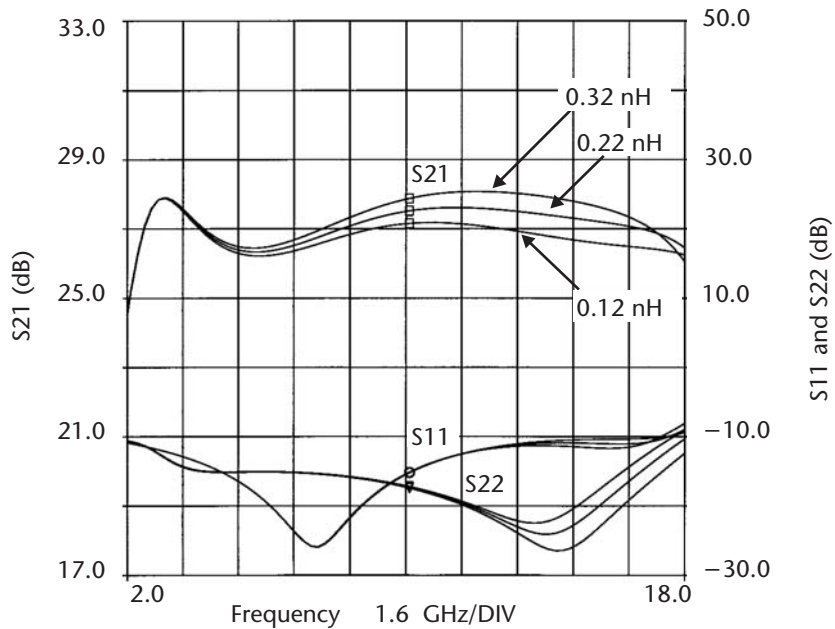


Figure 6.43 Effect of L_{d2} on the small-signal response of a three-stage CRTSSDA.

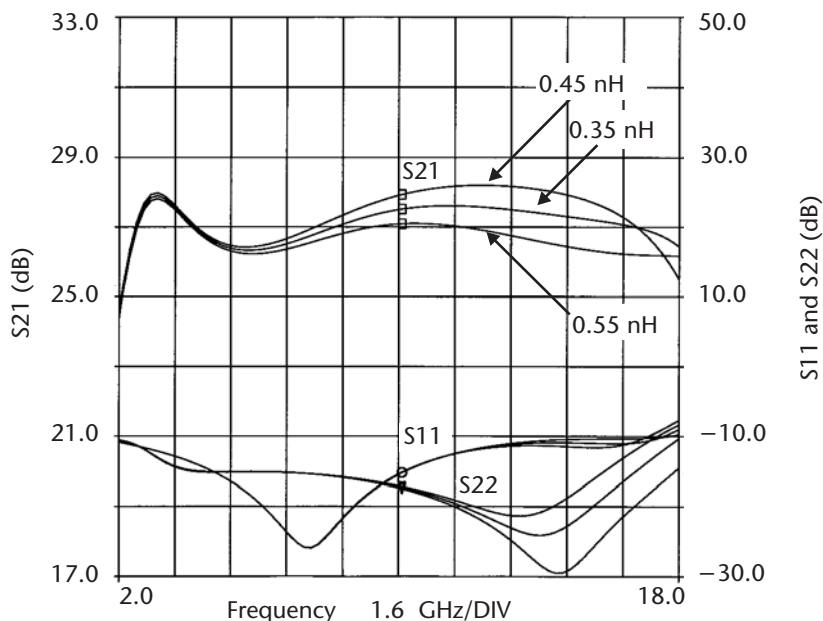


Figure 6.44 Effect of L_{g3} on the small-signal response of a three-stage CRTSSDA.

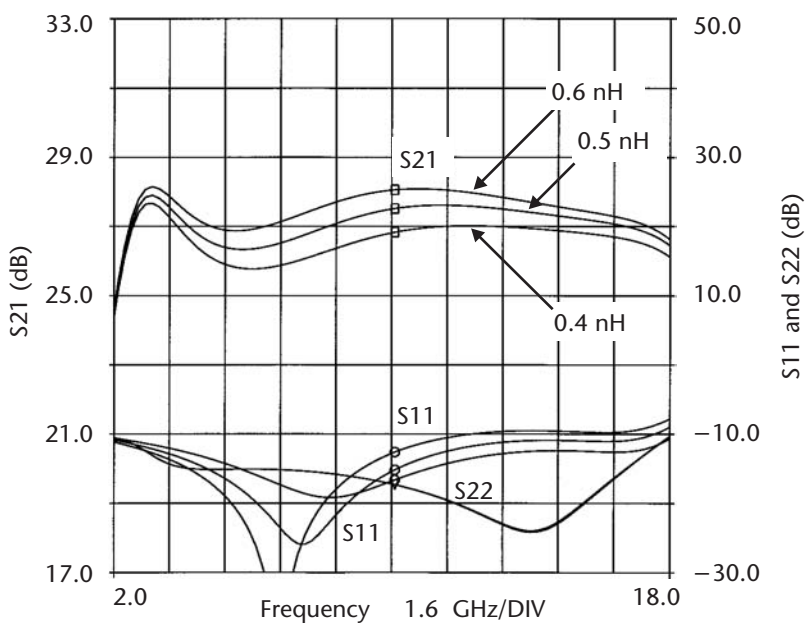


Figure 6.45 Effect of L_{sg1} on the small-signal response of a three-stage CRTSSDA.

whereas the effect of L_{sg1} and L_{sg2} is across the whole response. However, the effect of L_{sg2} is particularly severe between 5 to 13 GHz. The element R_{g2} appears to have a

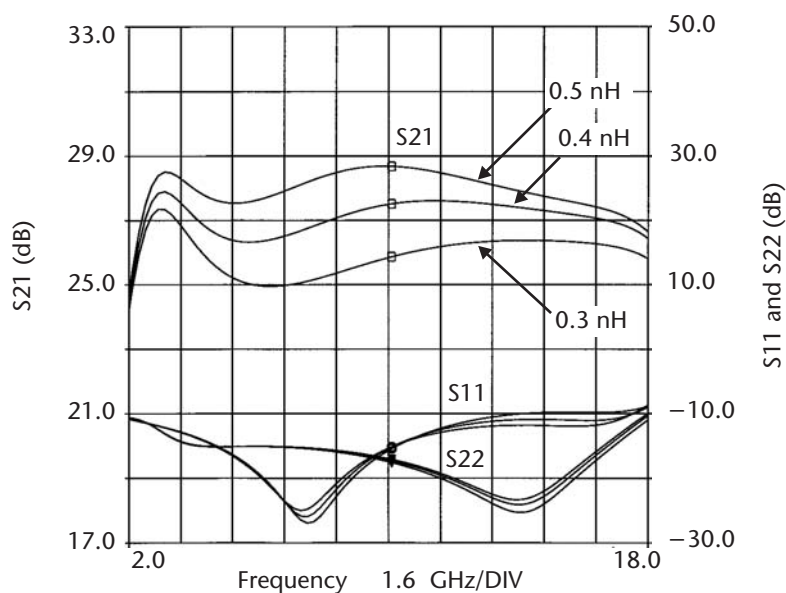


Figure 6.46 Effect of L_{sg2} on the small-signal response of a three-stage CRTSSDA.

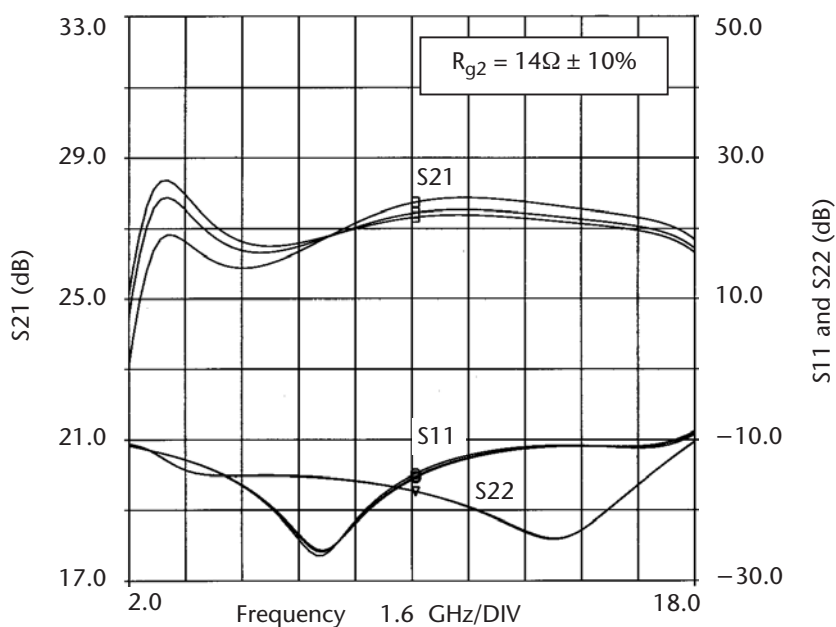


Figure 6.47 Effect of R_{g2} on the small-signal response of a three-stage CRTSSDA.

large effect only at the lower end of the frequency response. The tolerance values of these elements will therefore need to be more tightly controlled in the amplifier's fabrication. The other elements had small or negligible effect.

6.6.3 Design of Power CRTSSDA

This section goes through the design of a three-stage power CRTSSDA that was optimized for output power and hence power-added efficiency performance. The design procedure is identical to the high-gain CRTSSDA described earlier and begins with the calculation of the impedance Z_{int} using (6.18). The amplifier's gain can then be calculated using (6.15). It was necessary to increase the value of Z_{int} so that the required gain of 27 dB was achieved over the operating range of 2 to 18 GHz. The power amplifier is comprised of the following three DPHEMT devices: LPD200, LP6836, and LP6872. The gate and drain bond-wire inductances of the devices were calculated using (2.26) for an upper cut-off frequency of 18 GHz. The bias elements of the amplifier determine the low frequency cut-off frequency (2 GHz) and were calculated using (6.13) and (6.14). The schematic diagram of the optimized power amplifier is shown in Figure 6.48. The amplifier is unconditionally stable over a

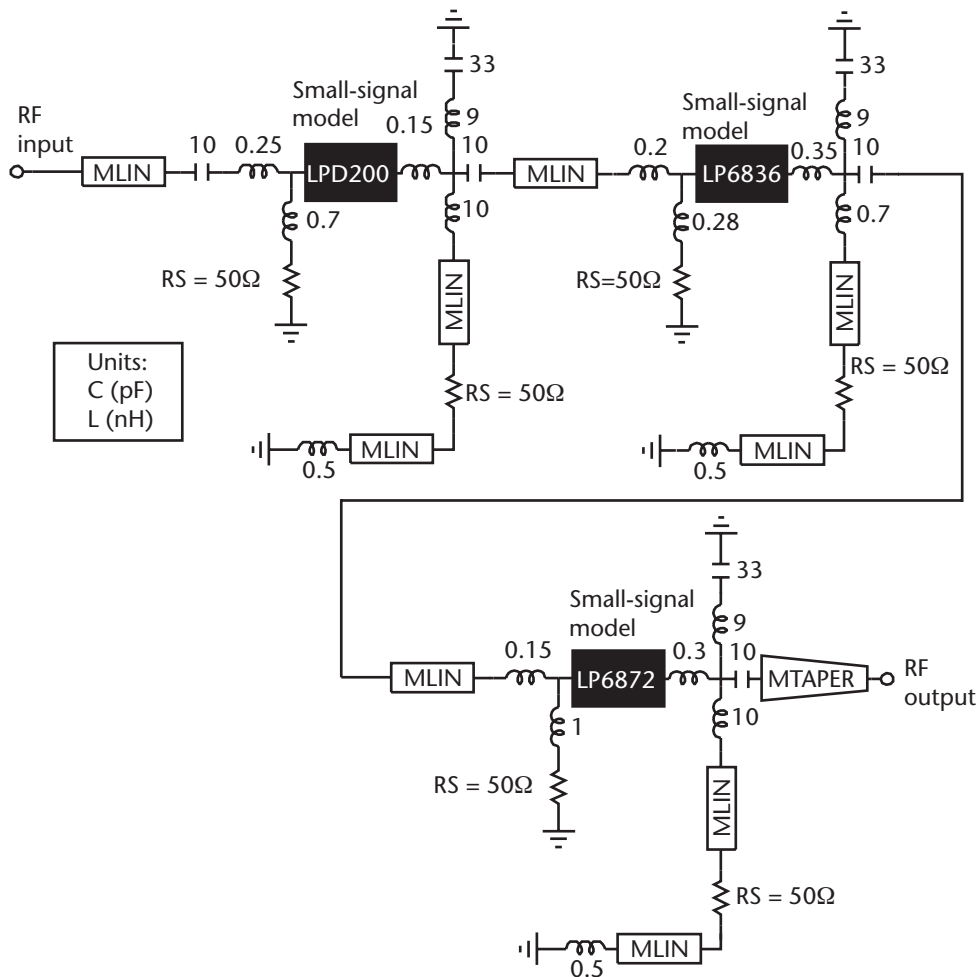


Figure 6.48 Schematic diagram of the optimized three-stage power CRTSSDA.

broad bandwidth from dc to 40 GHz, as shown in Figure 6.49, as its stability factor is greater than unity. The amplifier’s optimized small-signal response shown in Figure 6.50 predicts a gain level of 27 ± 1 dB and input VSWR better than 9.5 dB.

The amplifier’s output stage was analyzed under large-signal operation. This involved using the large-signal model of LP6872, determined in Chapter 4. The reactive part of the RF load as seen by the current source of the device contributes to

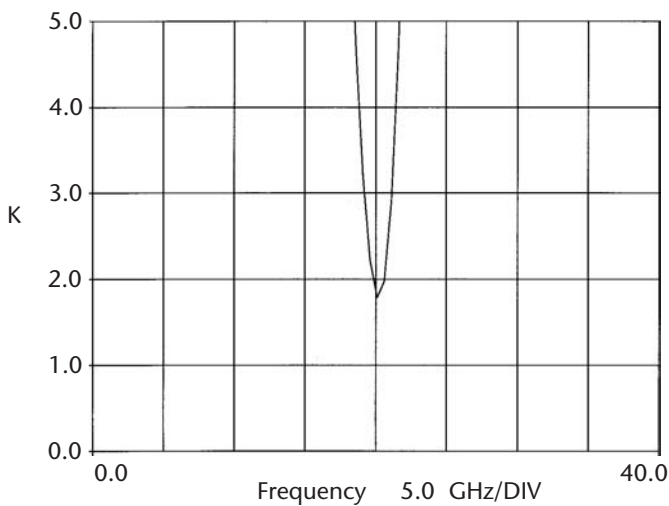


Figure 6.49 Stability factor ‘ K ’ of three-stage power CRTSSDA.

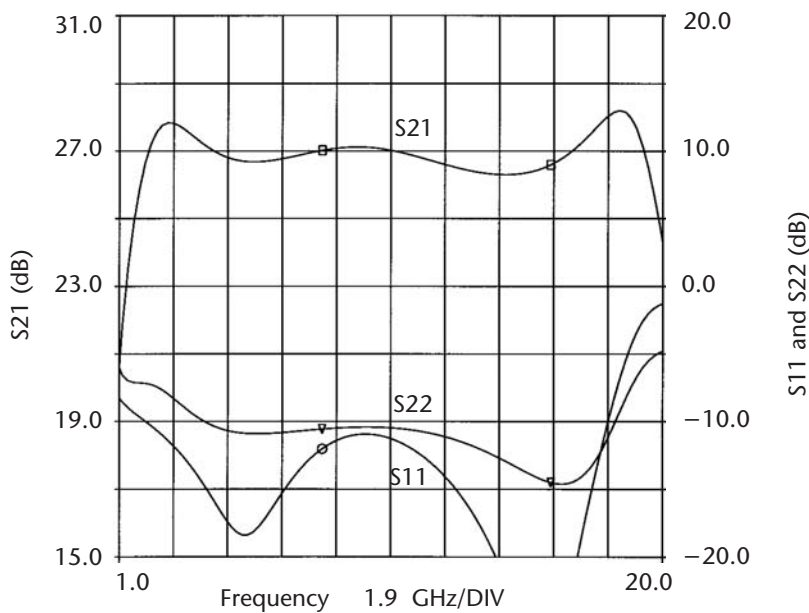


Figure 6.50 Optimized transmission and input/output return loss response of the three-stage power CRTSSDA.

reactive power dissipation, which transforms the actual load curve into an ellipse, as shown in Figure 6.51. The output device was matched to the optimum load impedance by employing a broadband microstrip taper. The value of the resistive RF load for this device should be 40Ω for optimum output power performance from Figure 3.9 in Chapter 3. However, the value of the resistive RF load of this device in the power amplifier configuration is 25Ω from Figure 6.51.

The circuit elements defined in Figure 6.42 were analyzed to determine which of these elements affected the power amplifier's small-signal performance. This was done to establish the elements whose tolerances would have to be tightly controlled in the amplifier's fabrication. This investigation showed that the elements that particularly influenced the amplifier's performance were essentially the same as for the high-gain three-stage CRTSSDA in Section 6.6.2, with the addition of L_{d1} and L_{g2} . The affect of these elements on the amplifiers gain response is shown in Figures 6.52 and 6.53. These figures show that the effect of these two elements is predominant in the mid to high end of the amplifier's frequency response. As the components L_{ds3} and R_{ds3} have negligible effect on the small-signal response of the amplifier, they can effectively be replaced with the large-signal matching network to optimize the amplifier's output power.

6.6.4 Fabrication of High Gain and Power CRTSSDA Modules

The CRTSSDA modules were realized using the conventional thin-film MIC fabrication technology. The detailed practical design considerations and fabrication

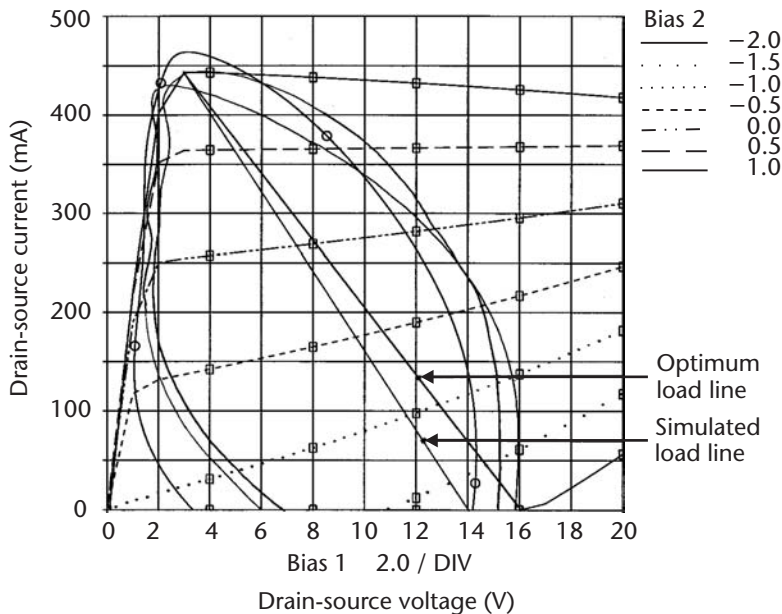


Figure 6.51 Output load line response of the three-stage power CRTSSDA at 2 GHz, 10 GHz, and 18 GHz.

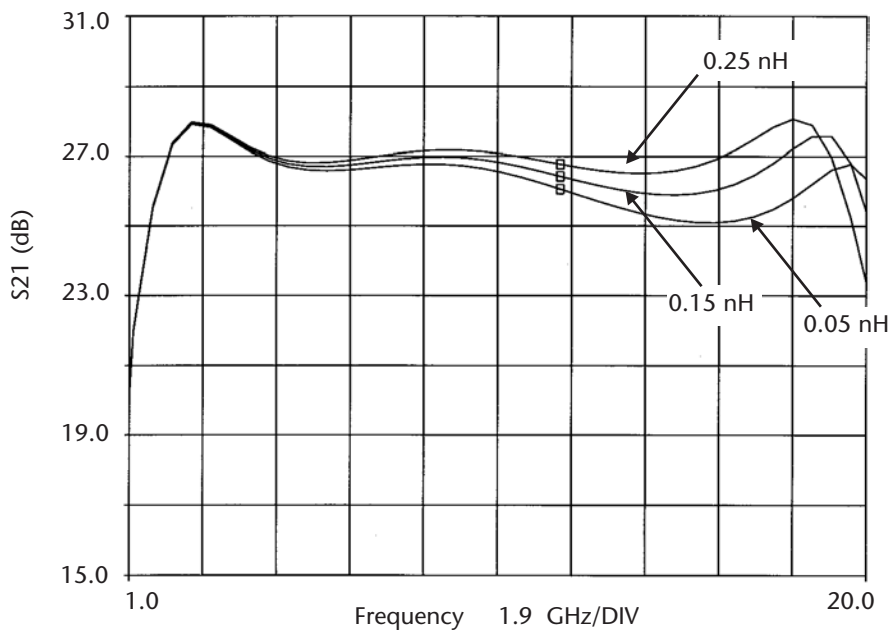


Figure 6.52 Effect of L_{dt} on the small-signal response of a three-stage power CRTSSDA.

techniques employed in the realization of the amplifiers is given in Chapter 7. Figure 6.54 shows the assembly drawing of the three-stage high-gain CRTSSDA

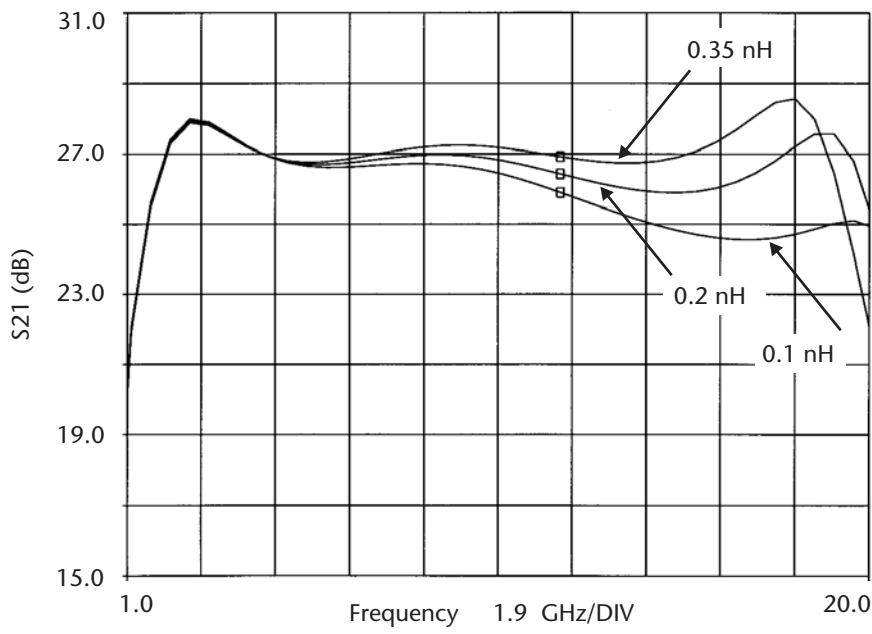


Figure 6.53 Effect of L_{g2} on the small-signal response of a three-stage power CRTSSDA.

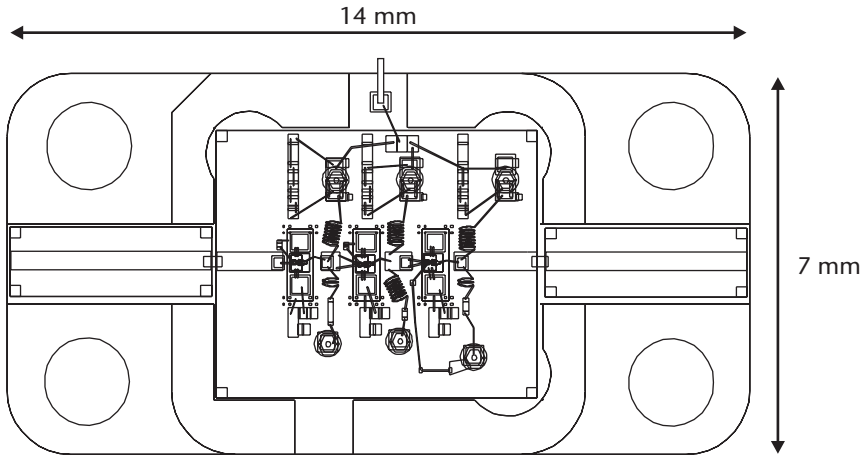


Figure 6.54 Assembly drawing of the three-stage high-gain CRTSSDA module.

module comprising of the LP6836 DPHEMT device. The assembly drawing of the three-stage power CRTSSDA module employing DPHEMT devices LPD200, LP6836, and LP6872 is shown in Figure 6.55. The photographs of the fabricated amplifier modules are shown in Figures 6.56 and 6.57. All other fabrication details are similar to those given in Section 6.4.1.

6.6.5 Measured Results of CRTSSDA Modules

The measured small-signal gain, input return loss, and output return loss over 2 to 18 GHz of the three-stage high-gain CRTSSDA module is shown in Figure 6.58. The amplifier was biased in the *self-bias* mode of operation with a V_{ds} of 8V at $0.5I_{dss}$. The measured gain level obtained is 26 ± 1.5 dB, and the input and output return loss is better than 9.5 dB (i.e., VSWR of better than 2:1). A comparison with the simulated

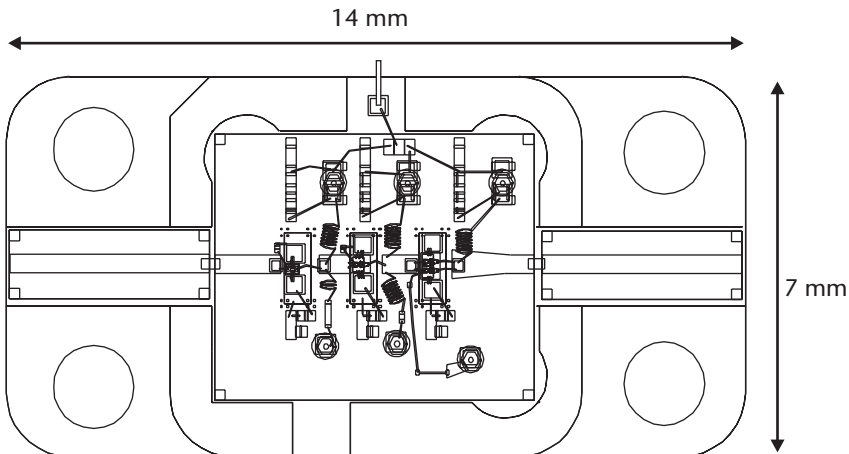


Figure 6.55 Assembly drawing of the three-stage power CRTSSDA module.

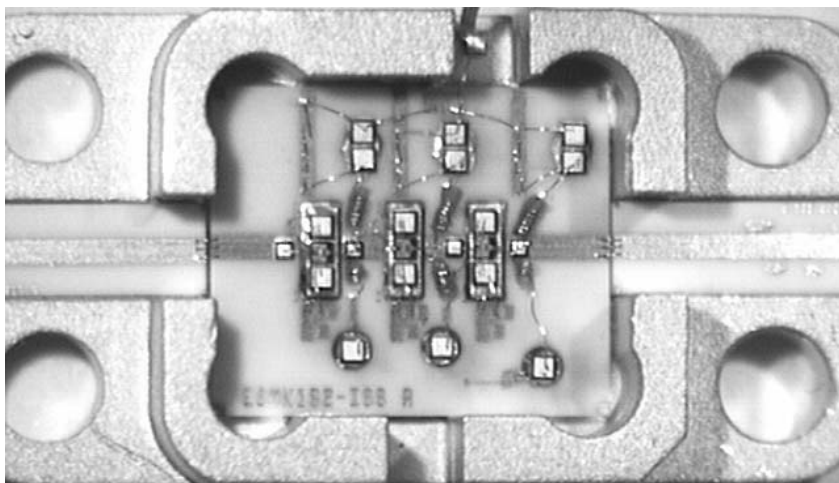


Figure 6.56 Photograph of the fabricated three-stage high gain CRTSSDA module.

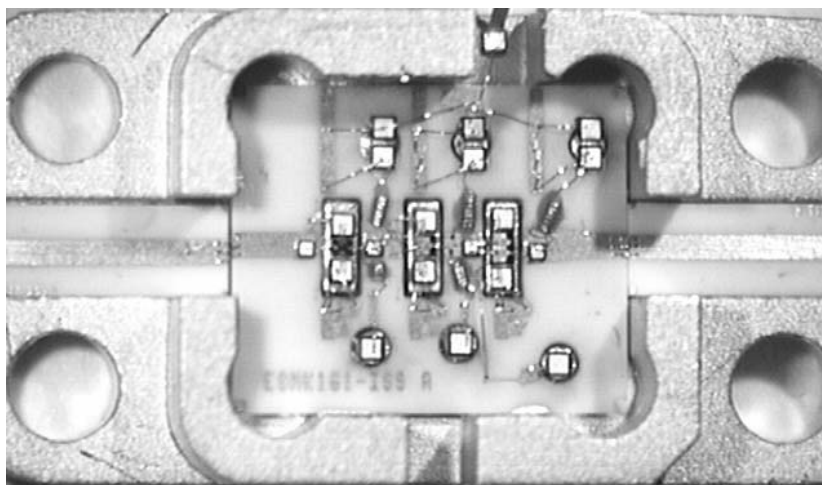


Figure 6.57 Photograph of the fabricated three-stage power CRTSSDA module.

response in Figure 6.40 shows excellent agreement between the two results. The measured and predicted output power and power-added efficiency performance of the amplifier at 18 GHz is shown in Figure 6.59. An output power of 21 dBm at the 2-dB compression point has been achieved with a power-added efficiency of 14%. Figure 6.60 shows that the amplifier's output power of 22 dBm and a power-added efficiency of 14% are maintained across the required 2- to 18-GHz bandwidth. These results clearly show the excellent agreement that is achieved between the simulated and measured nonlinear performance, which can be attributed to the accuracy of the characterization and modeling of the devices described in Chapter 4.

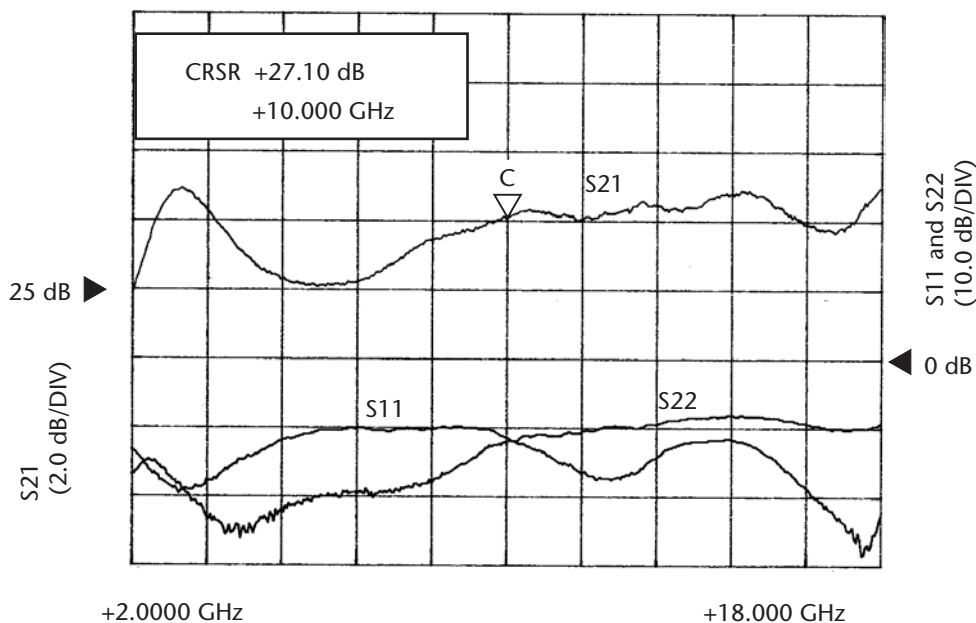


Figure 6.58 Measured small-signal response of the three-stage high-gain CRTSSDA module.

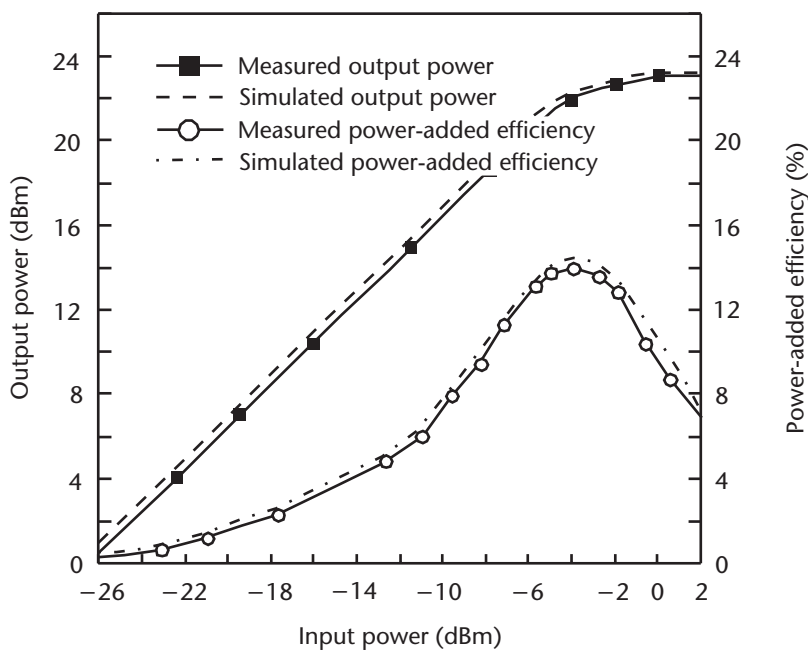


Figure 6.59 Simulated and measured output power and power-added efficiency as a function of the input power of the three-stage high-gain CRTSSDA module at 18 GHz.

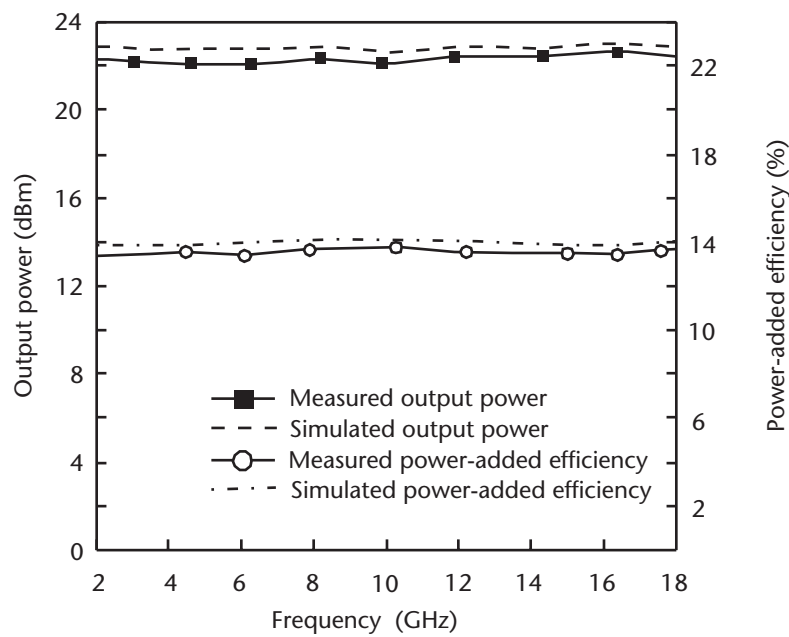


Figure 6.60 Simulated and measured output power and power-added efficiency response of the three-stage high-gain CRTSSDA module over 2 to 18 GHz.

The three-stage power amplifier’s measured small-signal gain and input/output return loss performance over 2 to 18 GHz is shown in Figure 6.61. The amplifier was biased for optimum output power, which is determined by the bias settings of

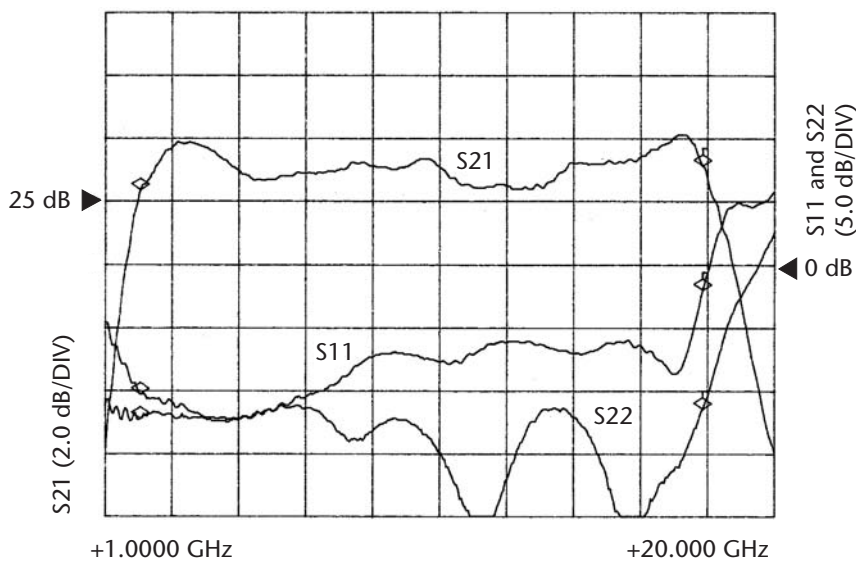


Figure 6.61 Measured small-signal response of the three-stage power CRTSSDA module.

the individual devices. All of the devices were biased in the self-bias mode of operation. The optimized bias setting for the device LPD200 was $V_{ds} = 4\text{V}$ at $0.25I_{dss}$, for LP6836 was $V_{ds} = 6.5\text{V}$ at $0.3I_{dss}$, and for LP6872 was $V_{ds} = 7\text{V}$ at $0.4I_{dss}$. The measured gain obtained is $26 \pm 1.0\text{ dB}$ and the input return loss is better than 9.5 dB . A comparison of the measured performance with the simulated response in Figure 6.50 shows the excellent agreement between the two results. The amplifier's predicted and measured output power and power-added efficiency performance at 18 GHz is shown in Figure 6.62. The measured output power at the 2-dB compression point is 24.5 dBm with a power-added efficiency of 27% . The measured output power and power-added efficiency performance is maintained over the 2- to 18-GHz bandwidth, as shown in Figures 6.63 and 6.64.

6.7 High-Dynamic-Range Broadband Amplifier

6.7.1 Design of High-Dynamic-Range Broadband Amplifier

Broadband communication, radar, and EW receivers require high-dynamic-range broadband amplifiers. These amplifiers have to satisfy the requirements of low NF and high third-order output intercept point. To achieve the lowest possible NF, the reflection noise-matched input network is employed. This approach, however, tends to restrict the amplifier's bandwidth. This problem can be circumvented by employing the conventional distributed amplifier in the design of the dynamic-range

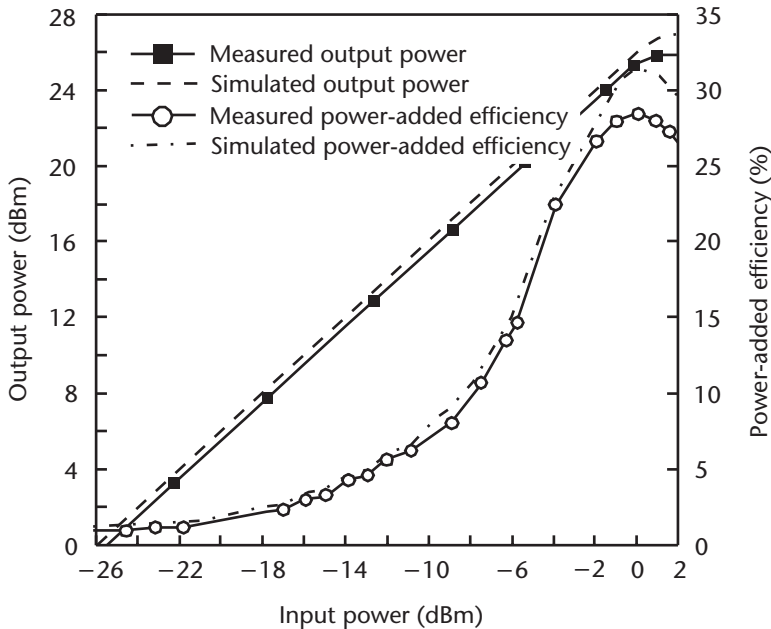


Figure 6.62 Simulated and measured output power and power-added efficiency as a function of input power of the three-stage power CRTSSDA module at 18 GHz .

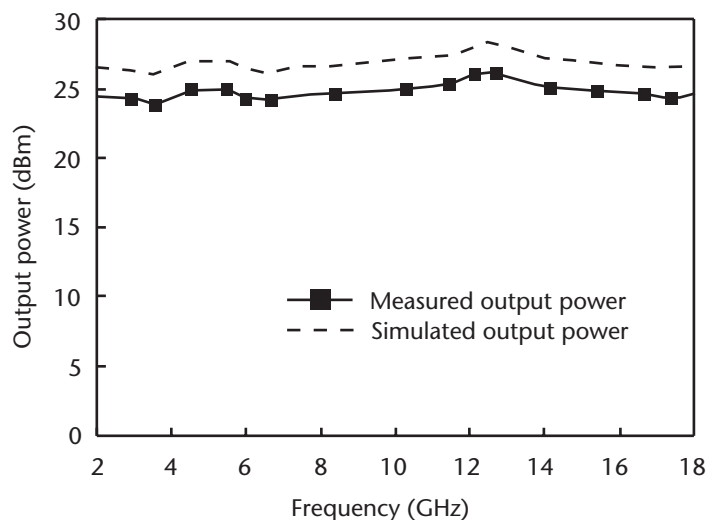


Figure 6.63 Simulated and measured output power response of the three-stage power CRTSSDA module over 2 to 18 GHz.

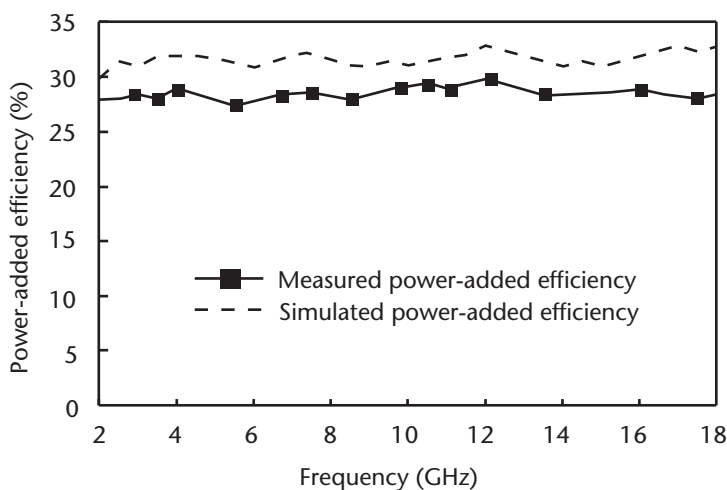


Figure 6.64 Simulated and measured power-added efficiency response of the three-stage power CRTSSDA module over 2 to 18 GHz.

broadband amplifier, as distributed amplifiers provide very broadband amplification with excellent input and output matching. However, the major drawback of the distributed amplifier is that of high NF ($\sim 4.5\text{--}8$ dB), low gain ($\sim 8\text{--}9$ dB), and poor output power at 1-dB compression point ($\sim 18\text{--}20$ dBm). The concept of CRTSSDA, in particular the power CRTSSDA described in Section 6.6.3, provides an alternative solution to the conventional distributed amplifier. This is made possible because the power CRTSSDA possesses characteristics of high gain, high output power, and good input and output match over a wide bandwidth. Because the shunt

feedback amplifier, described in Section 6.5, yields a good terminal match and low NF over a wide bandwidth, in this section it is therefore shown that the shunt feedback amplifier and the CRTSSDA can be integrated together to realize a high-dynamic-range broadband amplifier.

The high-dynamic-range broadband amplifier design is comprised of a low noise resistive feedback amplifier integrated with a power CRTSSDA, as shown in Figure 6.65. The circuit design was analyzed and optimized using simulation tools. The low noise small-signal model of the SPHEMT device LPS200, derived in Chapter 4, was used in the design of the low-noise feedback amplifier. The optimized performance of the low-noise single-stage resistive feedback amplifier is shown in Figure 6.66. The predicted gain level of this amplifier is 9 ± 1.0 dB, the input return loss is better than 9.5 dB, and NF is better than 2.5 dB.

The design of the three-stage power CRTSSDA is given in Section 6.6.3. This amplifier was integrated with the low-noise single-stage resistive feedback amplifier to form the dynamic-range broadband amplifier. The optimized performance of the

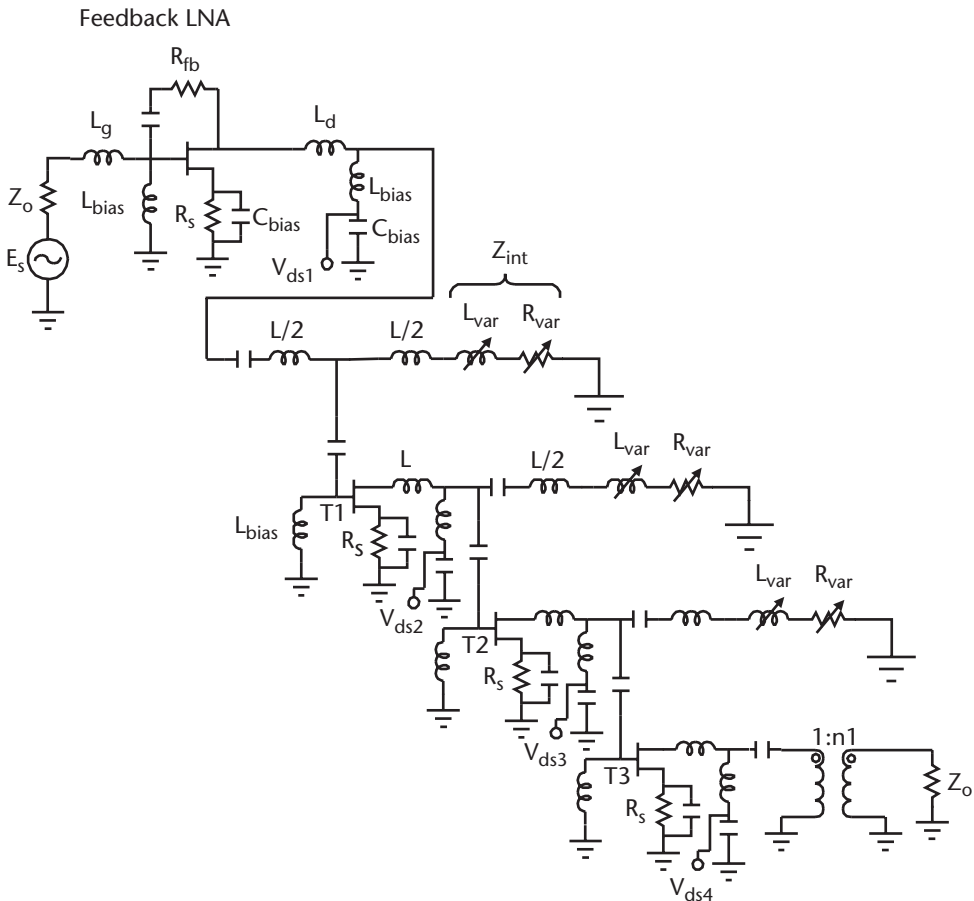


Figure 6.65 Circuit diagram of the high-dynamic-range broadband amplifier.

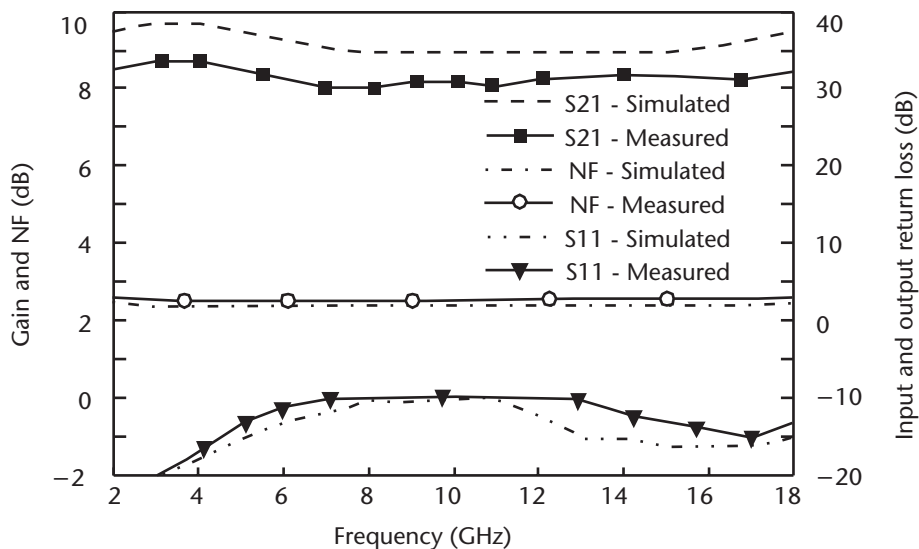


Figure 6.66 Simulated and measured small-signal response of the low-noise single-stage resistive feedback amplifier.

dynamic-range broadband amplifier over 2 to 18 GHz is shown in Figure 6.67. The predicted gain level of this amplifier is 35 ± 1.5 dB, the input return loss is better than 2:1, and the NF is better than 3.0 dB. Large-signal simulation was also performed on this amplifier, and the results of this simulation in terms of the output power at a 1-dB gain compression point and the third-order output intercept point performance over the 2- to 18-GHz range is shown in Figure 6.68. The predicted

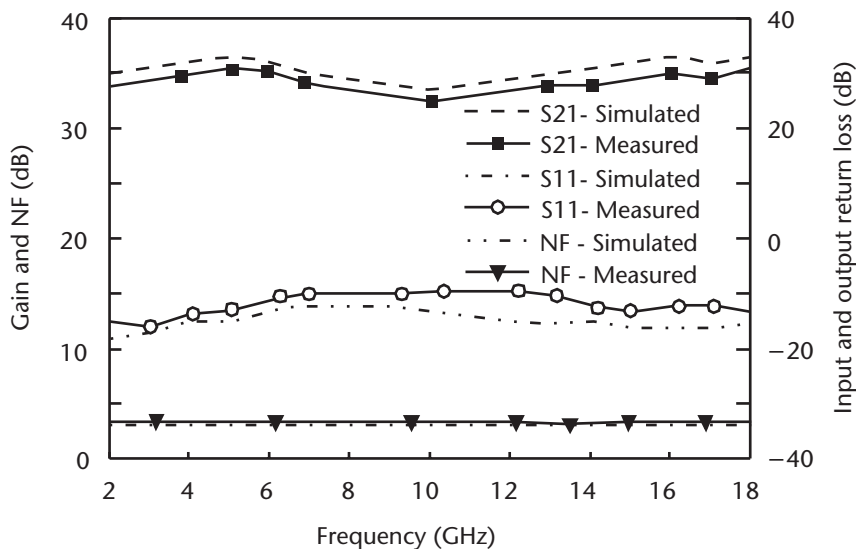


Figure 6.67 Simulated and measured small-signal response of the high-dynamic-range amplifier.

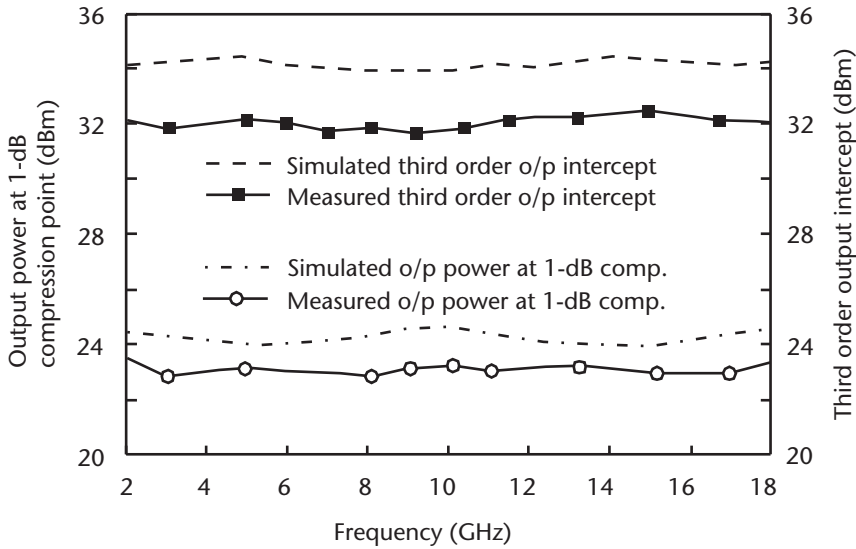


Figure 6.68 Simulated and measured output power at a 1-dB gain compression point and third-order output intercept performance of a high-dynamic-range broadband amplifier.

average output power at a 1-dB compression point is 25 dBm with an associated average third-order output intercept of 34 dBm.

6.7.2 Fabrication of the High-Dynamic-Range Broadband Amplifier

The high-dynamic-range broadband amplifier was realized using MIC fabrication technology. The amplifier was realized on Alumina substrate with a dielectric constant of $\epsilon_r = 9.8$ and substrate thickness of $h = 0.381$ mm. All other fabrication details are the same as in Section 6.4.1; however, the detailed practical design considerations and fabrication techniques employed in the realization of the amplifier is given in Chapter 7. Figure 6.69 shows the assembly drawing of the high-dynamic-range broadband amplifier. The photograph of the fabricated amplifier is shown in Figure 6.70.

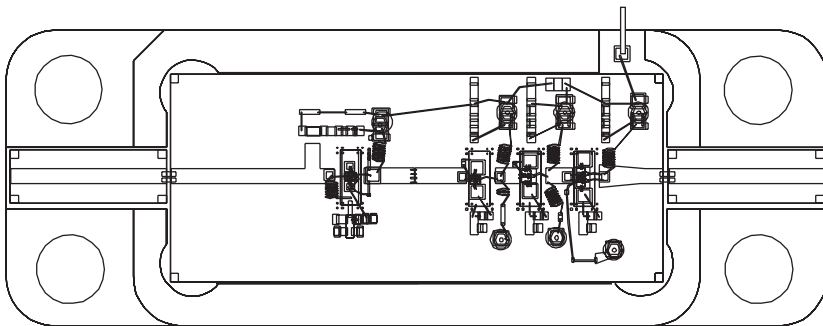


Figure 6.69 Assembly drawing of the high-dynamic-range broadband amplifier.

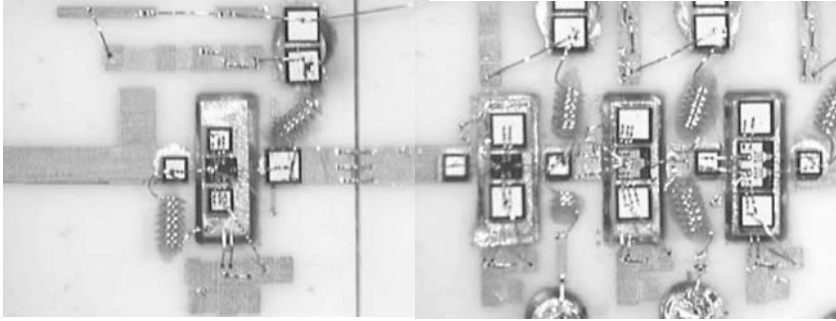


Figure 6.70 Photograph of the fabricated high-dynamic-range broadband amplifier.

6.7.3 Measured Response of High-Dynamic-Range Broadband Amplifier

The high-dynamic-range broadband amplifier was biased for optimum output power and low-noise performance. This is determined by the bias settings of the individual devices. All of the devices were biased in the self-bias mode of operation. The optimized bias for the three-stage power CRTSSDA was as follows: for the device LPD200, $V_{ds} = 4\text{V}$ at $0.25I_{dss}$; the device LP6836, $V_{ds} = 6.5\text{V}$ at $0.3I_{dss}$; and the device LP6872, $V_{ds} = 7\text{V}$ at $0.4I_{dss}$. The device LPS200 used in the low-noise single-stage resistive feedback amplifier was optimized at $V_{ds} = 3\text{V}$ at $0.25I_{dss}$.

The measured small-signal performance of the single-stage low-noise feedback amplifier is shown in Figure 6.66. The measured gain achieved by the amplifier was $8.5 \pm 1.0\text{ dB}$, the input/output return loss was better than 9.5 dB , and the NF was a maximum of 2.6 dB . The measured small-signal performance of the high-dynamic-range broadband amplifier is shown in Figure 6.67. The amplifier provided a gain level of $34 \pm 1.0\text{ dB}$, input return of better than 9.5 dB , and an NF of 3.2 dB . The output power at a 1-dB gain compression point and the associated third-order output intercept performance over 2 to 18 GHz is shown in Figure 6.68. The average output power at a 1-dB compression point was 23 dBm , and the average third-order output intercept was of 32 dBm . In all cases, there was an excellent agreement between the measured and predicted results, which can be attributed to the accuracy of the device characterization and modeling described in Chapter 4.

6.8 Broadband Feedback Amplifiers Employing Current Sharing

6.8.1 Design of Broadband Feedback Amplifiers Employing Current Sharing

The inexorable drive to increase the packaging density of microwave subsystems and reduce package size inevitably puts great demand on miniaturization of components and devices that are employed in their realization. This demand also puts severe constraints on the current consumption requirements of these subsystems so as to minimize the power dissipation from the components and devices that constitute them.

The concept of current sharing, shown in Figure 6.72, is a modified version of the circuit shown in Figure 6.71. The supply voltage V_B is used to bias T_2 , and the overall current drawn by the two-stage feedback amplifier is set by the source resistor R_s of the first device T_1 that is biased in the self-bias mode. Biasing of the second device T_2 is set by the potential divider connected at the gate terminal of device T_2 (V_1). The drain voltage of T_2 (V_d) is connected to the source decoupling capacitors C_2 (assuming negligible drain-source potential drop), which establishes the correct gate-source voltage ($V_{gs} = V_1 - V_d$) to forward bias the device T_2 . The current flows from supply V_B through T_2 , T_1 , and R_s to ground. Inductor LX provides the necessary RF isolation between the source terminal of device T_2 and the drain terminal of device T_1 . Figure 6.73 shows the current sharing implemented in a balanced amplifier arrangement.

6.8.2 Fabrication of Amplifiers Using Self-Bias and Current-Sharing Modes

The broadband amplifiers using self-bias and current-sharing modes were realized using MIC fabrication technology. The amplifiers were realized on Alumina substrate with a dielectric constant of $\epsilon_r = 9.8$ and substrate thickness of $h = 0.381$ mm. All other fabrication details are the same as in Section 6.4.1; however, the detailed practical design considerations and fabrication techniques employed in the realization of the amplifier is given in Chapter 7. The assembly drawing of these amplifiers is shown in Figures 6.74 and 6.75. The photograph of the fabricated amplifier using the current sharing mode is shown in Figure 6.76.

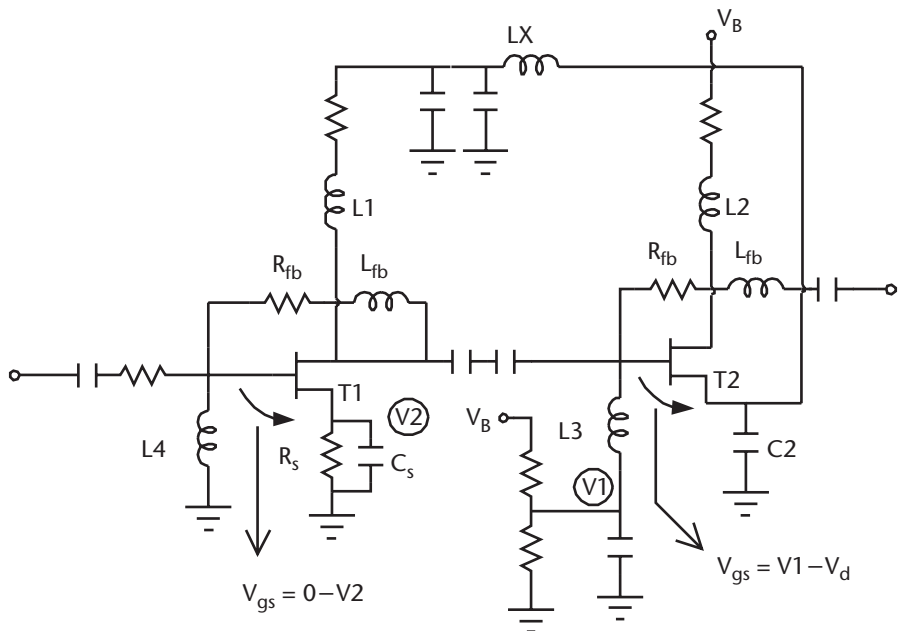


Figure 6.72 Two-stage feedback amplifier circuit in the current-sharing mode.

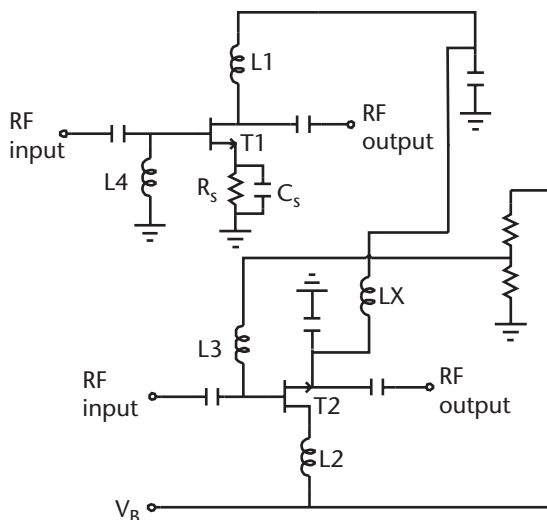


Figure 6.73 Balanced amplifier circuit in the current-sharing mode.

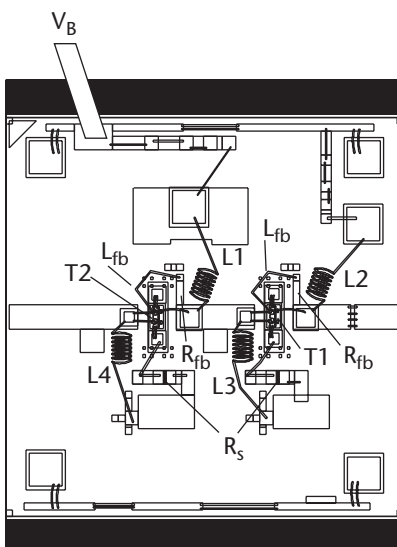


Figure 6.74 Layout of the two-stage feedback amplifier circuit using the self-bias mode (dimensions 6 mm \times 7 mm).

6.8.3 Measured Results of Broadband Feedback Amplifiers Using Self-Bias and Current-Sharing Modes

The measured small-signal response of the two-stage feedback amplifier is shown in Figure 6.77. The devices in the amplifier were connected to operate in the self-bias mode at $V_{ds} = 3\text{V}$ and $I_{ds} = 40\text{mA}$. The measured gain obtained was about 15 dB, the input/output return loss was better than 10 dB, and the NF was about 3 dB. The

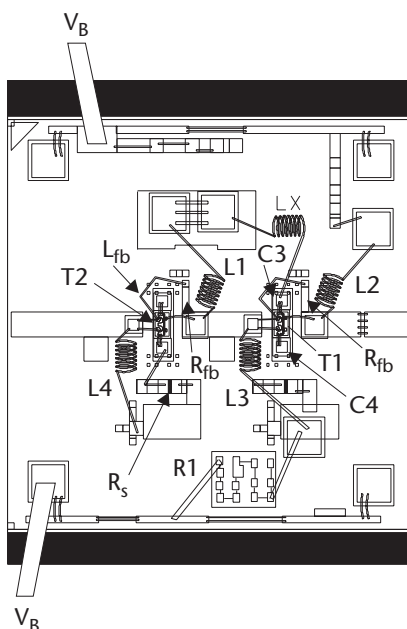


Figure 6.75 Layout of the two-stage feedback amplifier using the current-sharing mode (dimensions 6 mm \times 7 mm).

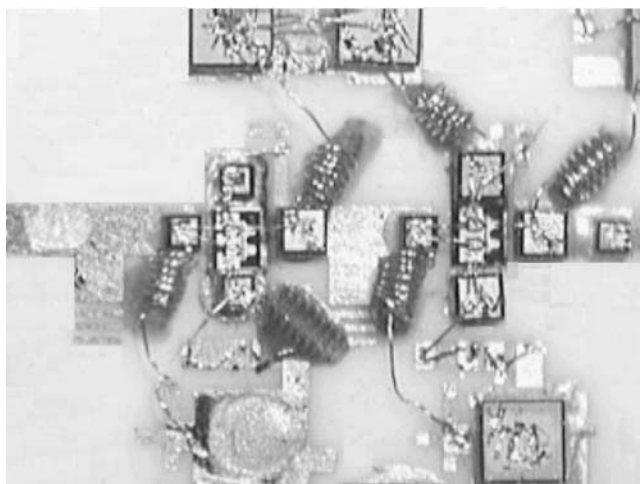


Figure 6.76 Photograph of the fabricated two-stage feedback amplifier using the current-sharing mode (dimensions 6mm \times 7mm).

measured output power performance of the amplifier at 2, 10, and 18 GHz is shown in Figure 6.78. The output power at a 1-dB compression point achieved by the amplifier is 13 dBm.

The two-stage feedback amplifier incorporating the current-sharing mode of operation was found to exhibit low-frequency oscillations as the dc bias was applied,

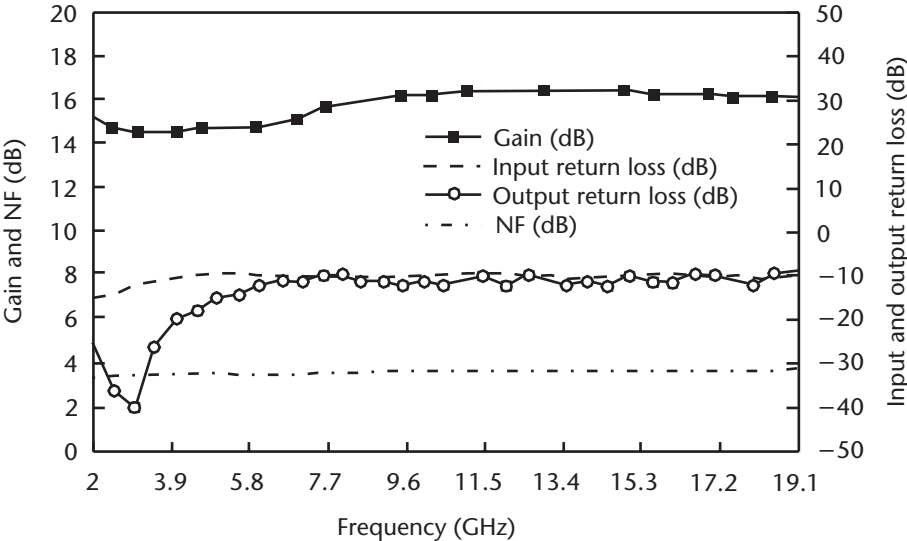


Figure 6.77 Measured small-signal response of the two-stage feedback amplifier in the self-bias mode.

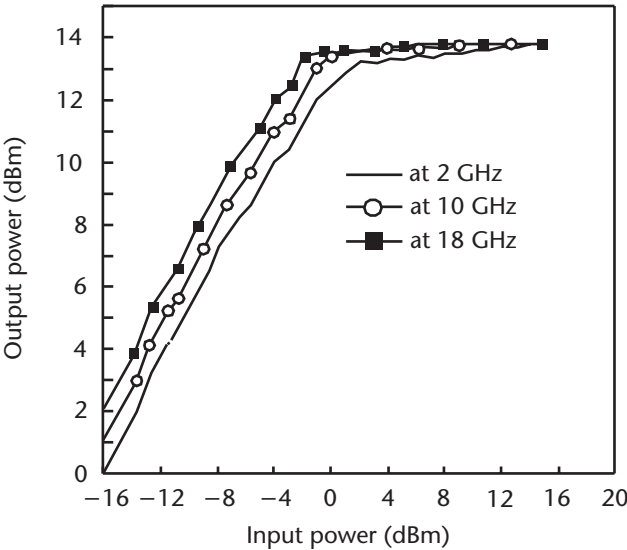


Figure 6.78 Measured output power versus input power response of the two-stage feedback amplifier in the self-bias mode.

and this caused the gain level to fluctuate. It was found that the source-decoupling capacitor $C2$ and the isolating inductor LX connecting the source terminal of device $T2$ to the drain terminal of device $T1$ required some optimization in order to stabilize the amplifier performance and eliminate the low-frequency oscillations. Figure 6.79 shows the measured small-signal response of the amplifier operating in the current-sharing mode. This performance is found to match the self-bias mode performance

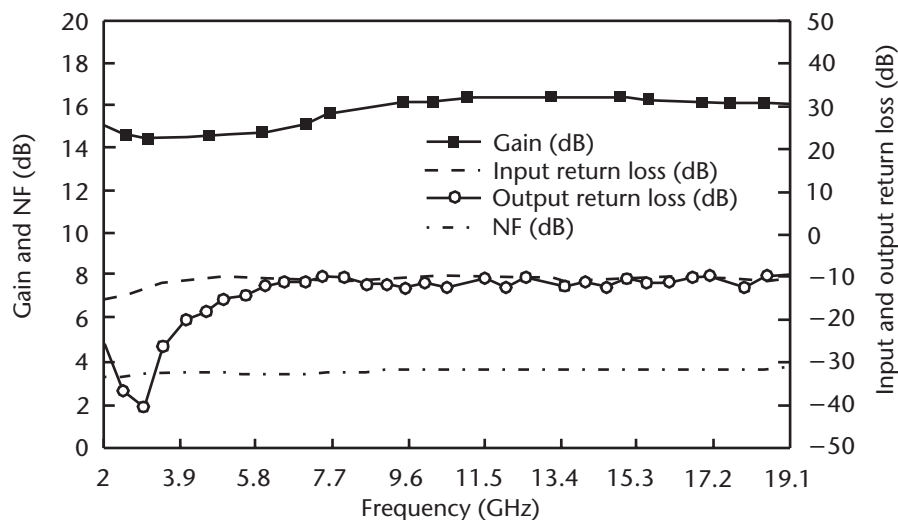


Figure 6.79 Measured small-signal response of the two-stage feedback amplifier in the current-sharing mode.

shown in Figure 6.77, with the advantage that the current consumed was only 20 mA (i.e., a 50% reduction compared to the self-bias mode). The measured output power performance at 2, 10, and 18 GHz of the amplifier is shown in Figure 6.80. The output power at a 1-dB gain compression point is 12 dBm. The power-added efficiency performance of the amplifiers in the self-bias and current-sharing modes is shown in Figure 6.81. This figure clearly demonstrates an almost two-fold improvement in the

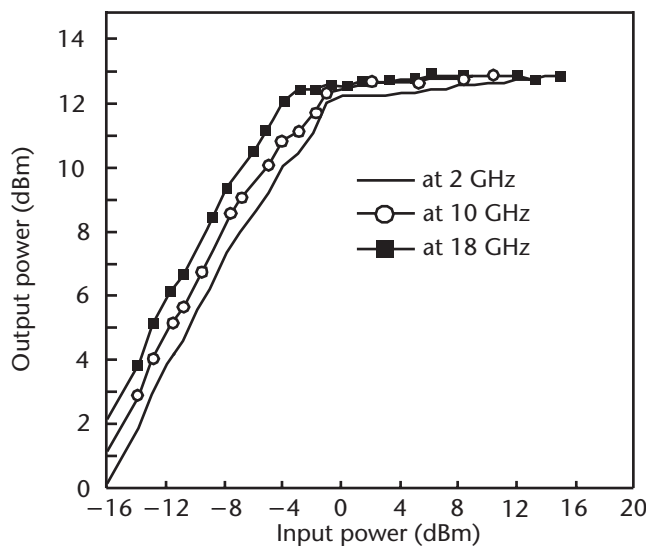


Figure 6.80 Measured output power versus input power response of the two-stage feedback amplifier in the current-sharing mode.

efficiency performance using the current sharing mode at an input signal power of around 0 dBm.

The current-sharing technique verified on the two-stage feedback amplifier was implemented onto a 2- to 4-GHz balanced amplifier. Figure 6.82 shows the

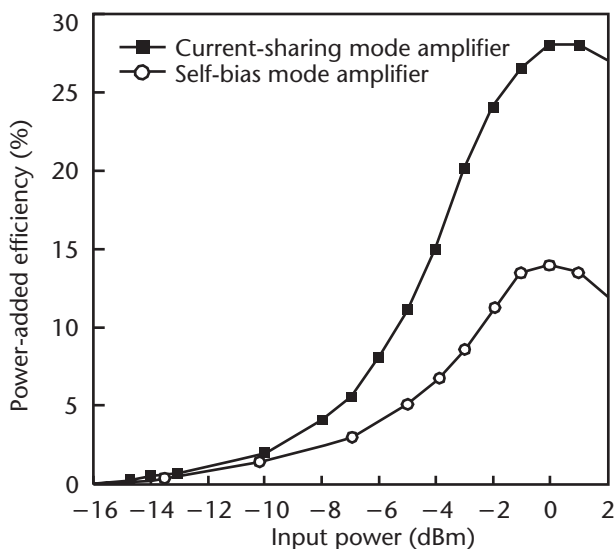


Figure 6.81 Measured power-added efficiency performance.

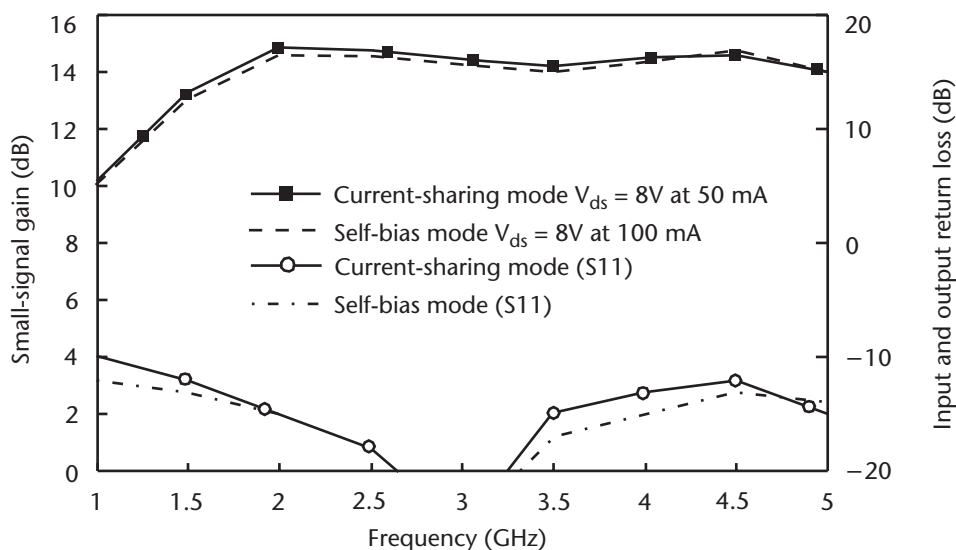


Figure 6.82 Measured small-signal response of the balanced amplifier in current-sharing and self-bias modes.

measured small-signal response of the amplifier using self-bias mode and an identical amplifier using the current-sharing mode. These results clearly show that the performance achieved by the amplifier in either bias modes is virtually the same, with the exception of the current consumption. The amplifier biased in the current-sharing mode only consumed half the amount of current as the amplifier biased in the self-biased mode.

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Fabrication of Broadband Amplifiers

7.1 Introduction

This chapter describes the practical design considerations and the fabrication technique employed in the realization of the broadband amplifiers described in Chapter 6. The chapter starts with an explanation of how the readily available microwave passive components were characterized for broadband performance. Accurate equivalent circuit models of these components were developed using the measured results and used in the simulation analysis of the amplifiers. The broadband amplifiers were fabricated using the hybrid MIC technology on thin-film Alumina substrates.

7.2 Practical Design Considerations and Fabrication Procedure

In the realm of broadband microwave circuit design, the behavior of ideal and real components is quite different. The ideal components are characterized as having negligible parasitic elements associated with them, whereas the real components exhibit the parasitic elements that tend to degrade the broadband performance of the amplifier circuit. For example, at frequencies greater than 5 GHz, a chip capacitor behaves like an equivalent resistor-, inductor-, capacitor (RLC) circuit due to the capacitor's associated parasitic elements. These parasitic elements will tend to degrade the performance of the broadband amplifier by introducing either a gain roll-off or inband resonances. This effect also applies to inductor and resistor components. Usually, the manufacturers of these components do not normally supply S-parameter data characterizing these passive components at various frequencies; therefore, it may be necessary to measure their performance over the frequency range of interest. The equivalent circuit model of these components can then be derived and used in the amplifier design to enable an accurate prediction of an amplifier's performance.

The amplifier's circuit will include distributed microstrip transmission lines; however, the major problem associated with using microstrip lines, especially for broadbandwidth designs, is that of length variation with frequency. That is, as the frequency of the input signal gets higher, the physical length of the line will appear longer, and its width will become comparable to the signal's wavelength. Moreover,

the discontinuities associated with the microstrip line due to the width step change, tee connection, and line bend junctions will further affect the amplifier's performance. Hence, as these effects may adversely affect the amplifier's performance, it is therefore necessary to take them into account in the amplifier's model, including the actual physical layout of the amplifier.

Figure 7.1 shows the general procedure that is adopted in the fabrication of broadband amplifiers. It begins with the generation of the equivalent electrical

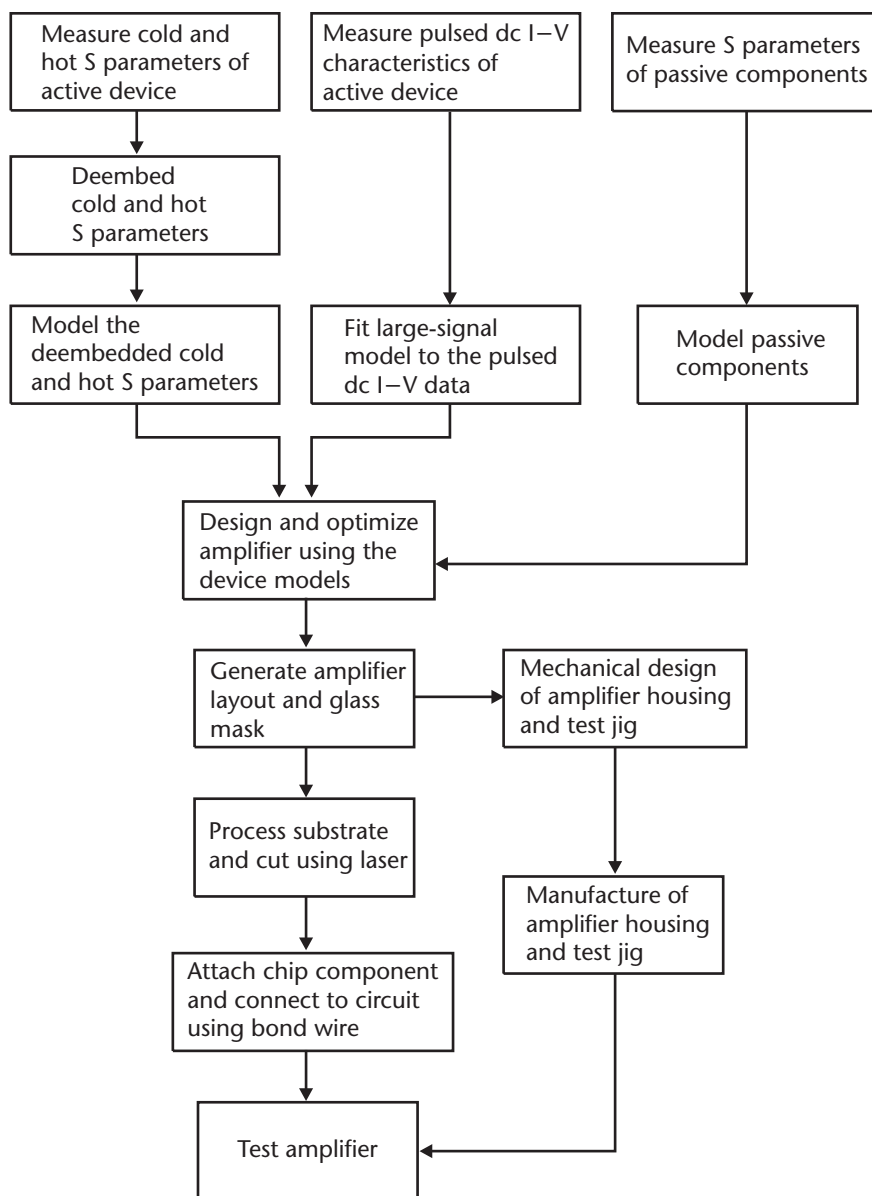


Figure 7.1 Fabrication procedure of broadband amplifiers.

circuit model of both the active and passive microwave components. The circuit models of these components are then employed to model the broadband amplifier design. When the amplifier's performance is optimized, a physical layout of the design is generated using a high-precision chrome glass mask. The mask is used in the processing of the Alumina substrate to produce high-definition gold tracks and high-tolerance thin-film nichrome resistors. The *pattern up plating* process [1] is used in the realization of the high-definition gold tracks. The Alumina substrate is then drilled to provide circular and rectangular cut outs for mounting gold posts after the processing stage and finally saw cut into individual circuits.

7.2.1 Skin-Depth Effect

The skin-effect phenomenon is observed at microwave frequencies, where the current tends to flow mostly near the surface of the conductive material. The conductive material used for MIC designs should have the following properties: high conductivity, a low temperature coefficient of resistance, low RF resistance, good adhesion to the substrate, good etchability and soldering, and be easy to deposit or electroplate. The resistance is determined by the RF surface resistivity and skin depth. The skin depth determines the thickness the conductive material required.

In the design examples described in Chapter 6, the conductor material used is gold, as it meets the aforementioned requirements. The minimum gold conductor thickness that is required in order to avoid attenuation due to the *skin-depth effect* is calculated using [2]

$$\delta = \sqrt{2/\sigma\omega\mu_o} \quad (7.1)$$

where

- δ is the skin depth;
- σ is the conductivity of gold;
- ω is the frequency;
- μ_o is the permeability of air.

Therefore, by using (7.1), the skin depth for gold conductor at a 1-GHz frequency is calculated to be $2.47 \mu\text{m}$. In the fabrication process of the MICs, the conductor thickness should be at least three times skin depth, to include 98% of the current density and to minimize resistive losses.

7.2.2 Thin-Film Resistors

The realization of resistors on MICs is achieved by depositing thin-film resistive materials on the substrate. The properties required for a resistive material are good stability, low temperature coefficient of resistance, and sheet resistivities in the range of 10 to $2,000 \Omega/\text{square}$. The commonly used resistive materials are

nichrome and tantalum nitride, which can be deposited on the Alumina substrate using one of the following techniques: vacuum evaporation, electron-beam evaporation, or sputtering. The resistance of the nichrome layer is 50Ω per square, with a tolerance of $\pm 2\%$. The length of a nichrome resistor can be calculated using [3]

$$l = (RW)/R_s \quad (7.2)$$

where

- l is the length of the nichrome resistor (mm);
- R is the resistance value (Ω);
- W is the width of the resistor (mm);
- R_s is the sheet resistivity ($50\Omega/\text{square}$).

7.2.3 Mounting Posts

The RF and dc grounding of the circuit components were provided by using gold-plated mounting posts for their low-inductance ground connections and good thermal dissipation paths. Figure 7.2 shows the circular and rectangular mounting post and their respective dimensions. The rectangular mounting posts were specifically employed in the mounting of the DPHEMT devices.

The size of the mounting post is calculated to ensure that the relevant chip component can be mounted onto it easily. However, the magnitude of the inductance associated with the rectangular mounting post is critical, as it adds onto the source inductance of the active device that is mounted onto the post. Too high a value of the mounting post inductance can cause the amplifier to become unstable. Therefore, it may be necessary to characterize the mounting post by shunt mounting the post with a high-tolerance chip capacitor. Figure 7.3 shows the test carrier used, which is similar to the test carrier used for the characterization of DPHEMT devices, described in Chapter 4. The schematic diagram of the shunt-mounted capacitor with a value 2.5 pF ($\pm 0.5 \text{ pF}$) and its simulated response are shown in Figures 7.4 and 7.5 respectively. The inductance associated with the gold bond wires connecting the shunt-mounted 2.5 pF capacitor to the $50\text{-}\Omega$ lines is calculated to be 0.2 nH , as described in Section 7.2.6. From the transmission response in Figure 7.5, it can be observed the resonant dip of the circuit occurs at a frequency of 16.39 GHz . This

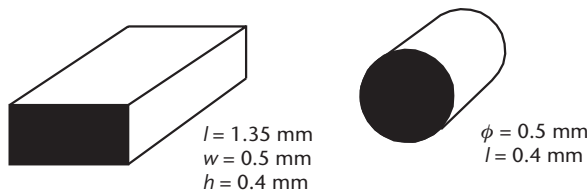


Figure 7.2 Gold-plated copper circular and rectangular mounting posts.

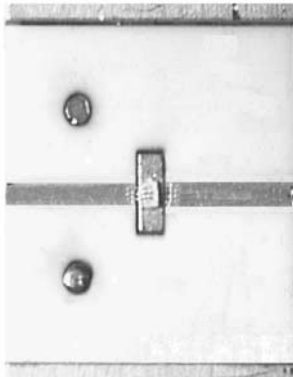


Figure 7.3 Test carrier with 2.5-pF shunt-mounted capacitor (board size 7 mm × 6 mm).

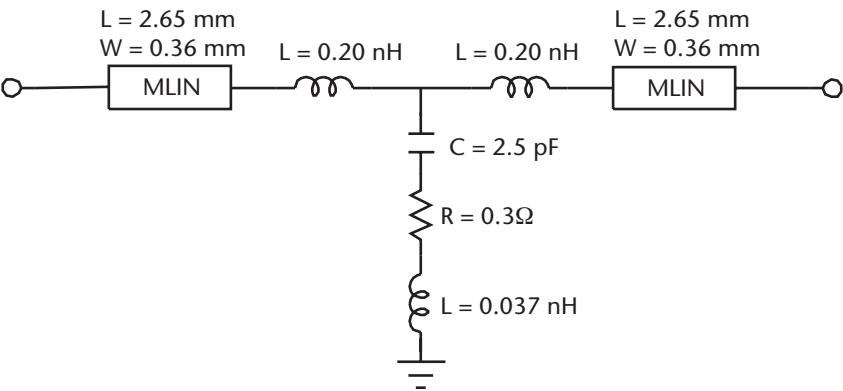


Figure 7.4 Schematic diagram of the shunt-mounted capacitor.

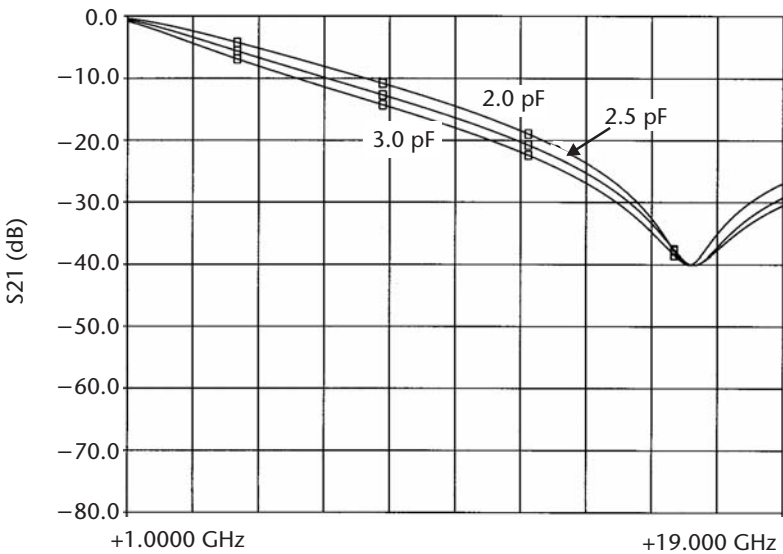


Figure 7.5 Simulated S_{21} response of the shunt-mounted capacitor.

result correlates very well with the measured results shown in Figure 7.6. The value of the mounting post inductance can then be calculated using [4]

$$L = 1/(2\pi f)^2 C \quad (7.3)$$

where

- L is the mounting post inductance (H);
- C is the value of the shunt-mounted capacitor (F);
- f is the resonance frequency (Hz).

Using (7.3), the calculated value of the inductance is 0.038 nH. This value was used in the device modeling and amplifier designs described in Chapter 6.

7.2.4 Broadband Chip Capacitors

In the fabrication of the broadband amplifier circuits, there is a need to provide dc block and RF bypass capacitors. The blocking chip capacitor is placed in series with a transmission line to prevent dc voltage of one stage from affecting another, whereas the purpose of the bypass chip capacitor is to provide an ac short circuit to the RF signal. The microwave chip capacitors, however, have associated parasitic elements, which can undermine the broadband amplifier's optimum performance. Hence, it is therefore necessary to take them into account in the amplifier's model. The equivalent electrical circuit model of a chip capacitor consists of series RLC, as shown in Figure 7.7 [5].

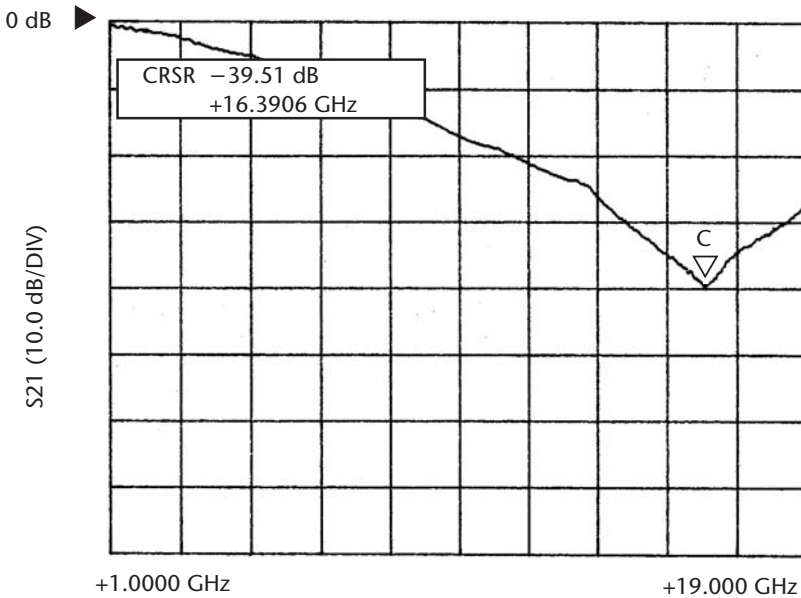


Figure 7.6 Measured S_{21} response of the shunt-mounted capacitor.

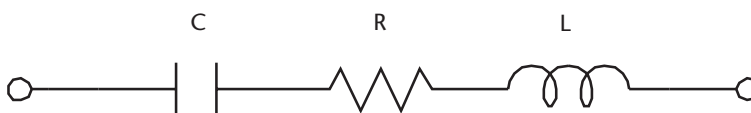


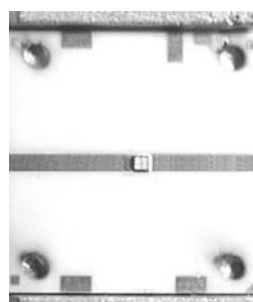
Figure 7.7 Equivalent circuit model of a chip capacitor.

In the model, C represents the desired capacitance, L is the parasitic series inductance, and R is a parasite series resistance. Over the frequency range of interest, the capacitor's parasitic elements should be negligible. In practice, however, resistor R will be the dominant parasitic element that contributes to the forward loss in the capacitor when used as a dc block. The blocking capacitor must have a low forward loss and good input and output return loss (<10 dB) across the desired frequency range in order to maintain a good RF power transmission.

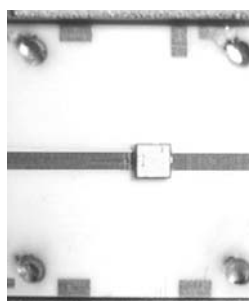
The capacitors used in the fabrication of the amplifiers were characterized with reference to a $50\text{-}\Omega$ microstrip transmission line. Figure 7.8 shows three test carriers consisting of a $50\text{-}\Omega$ transmission line; the first is a straight through line, and the other two carriers have 33-pF and 150-pF chip capacitors connected between the $50\text{-}\Omega$ input/output feed lines, respectively.



(a) $50\text{-}\Omega$ transmission line
(board size $7\text{ mm} \times 6\text{ mm}$)



(b) 33-pF chip capacitor
(board size $7\text{ mm} \times 6\text{ mm}$)



(c) 150-pF chip capacitor
(board size $7\text{ mm} \times 6\text{ mm}$)

Figure 7.8 Test carriers.

The measured forward transmission loss S_{21} and input return loss S_{11} performance of the 33-pF chip capacitor with reference to the 50- Ω transmission line is shown in Figure 7.9. The graph shows that the worst-case forward transmission loss between the 33-pF chip capacitor line and the 50- Ω line is 0.13 dB, and the input return loss for both is better than 10 dB at 18 GHz.

The measured performance of the 150-pF chip capacitor with reference to the 50- Ω transmission line is shown in Figure 7.10. This graph indicates the worst-case

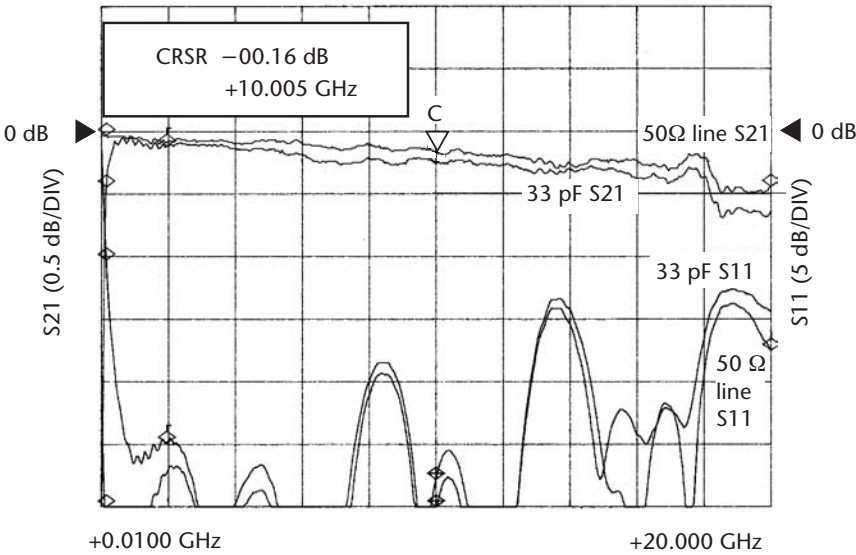


Figure 7.9 Measured S_{21} and S_{11} response of the 33-pF chip capacitor.

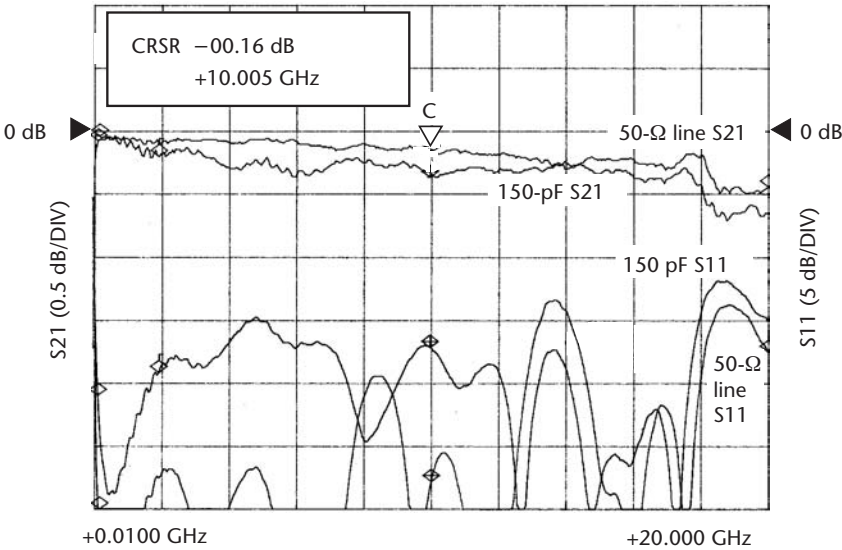


Figure 7.10 Measured S_{21} and S_{11} response of the 150-pF chip capacitor.

forward transmission loss between the 150-pF chip capacitor line and the 50- Ω line is 0.25 dB, and the input return loss for both is better than 10 dB at 18 GHz.

7.2.5 Broadband RF Chokes

The dc biasing of the amplifiers is accomplished by using RF chokes that exhibited low loss and no inband resonances f_r . The broadband amplifier designs in Chapter 6 used 7-turn and 33-turn RF chokes to provide broadband biasing over 2 to 18 GHz and 10 MHz to 20 GHz, respectively. The size and number of turns of the chokes for a given inductance can be calculated using [5]

$$L = 10(nd)^2 / (4.5d + 10l_c) + 0.8l_f \quad (7.4)$$

where

- L is the inductance value (nH);
- n is number of coil turns;
- d is the coil diameter (mm);
- l_c is the coil length (mm);
- l_f is the total length of the feed coil wire (mm).

To avoid the coil reflecting a short circuit at its input, the total wire length is made less than one-half guide wavelength at the highest frequency of operation. The total length l_t is given by

$$l_t = \pi dn + l_f \quad (7.5)$$

The resonance frequency associated with the coil is given by

$$f_r = 150/l_t \quad (7.6)$$

The coils can be fabricated using a 1-mil gold wire. Table 7.1 gives the number of turns and the calculated inductance and resonance frequencies using 1-mil (25.4- μ m) diameter gold wire. The fabricated 7-turn gold coil and its measured response are shown in Figures 7.11 and 7.12, respectfully. The coil offers excellent performance from 2 to 19 GHz with 0.4 dB worst-case insertion loss and an input return loss of better than 10 dB. Figure 7.13 shows the fabricated 33-turn gold coil. The measured response of this coil from 10 MHz to 1 GHz and from 10 MHz to 20 GHz is shown in Figures 7.14 and 7.15. The coil offers excellent ultrabroadband performance with 0.4-dB insertion loss at 18 GHz and input return loss of better than 10 dB.

Table 7.1 Coil Inductance Values for Various Coil Turns

<i>Coil Turns (n)</i>	<i>Calculated Inductance (nH)</i>	<i>Resonance Frequency (GHz)</i>
2.5	2	44
7	9.44	19.74
33	180	2.5

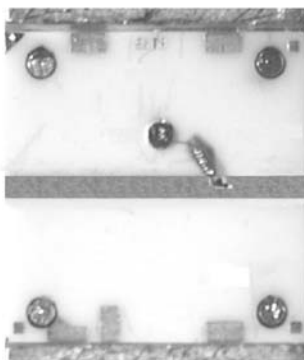


Figure 7.11 Fabricated 7-turn gold coil (board size 7 mm × 6 mm).

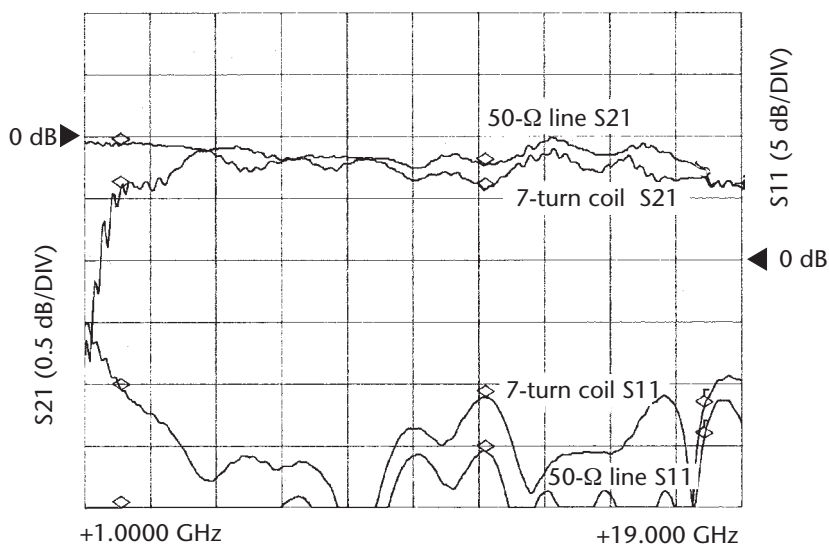


Figure 7.12 Measured S_{21} and S_{11} response of the 7-turn gold coil.

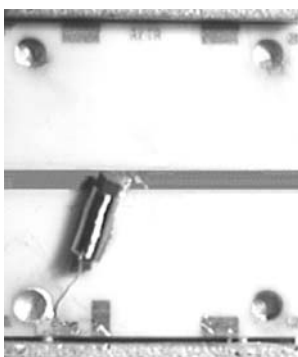


Figure 7.13 Fabricated 33-turn gold coil (board size 7 mm × 6 mm).

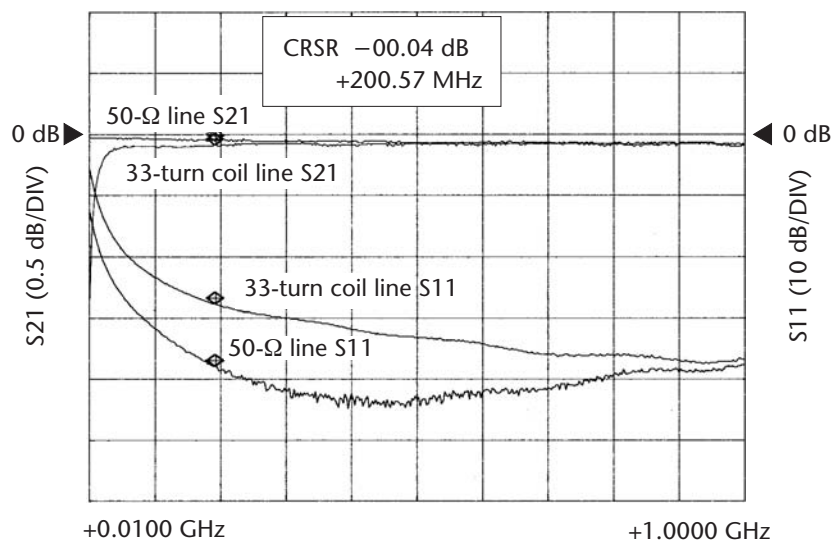


Figure 7.14 Measured S_{21} and S_{11} response of the 33-turn gold coil over 10 MHz to 1 GHz.

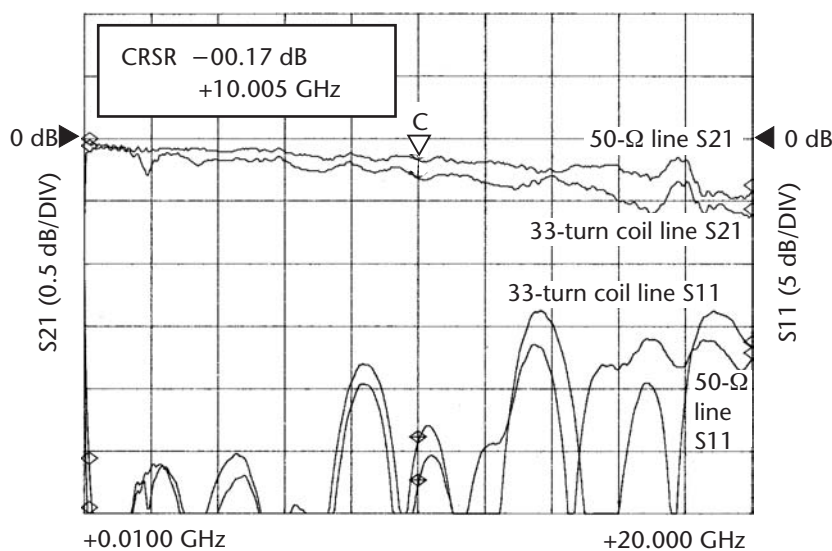


Figure 7.15 Measured S_{21} and S_{11} response of the 33-turn gold coil over 1 to 20 GHz.

7.2.6 Bond-Wire Inductance

The cross-section of a DPHEMT device placed on a rectangular mounting post with gate and drain bond wires connected to its terminals is shown in Figure 7.16. The device can have single or double bond-wire connections. This is dependent on the value of the inductance required, as a double bond wire has lower inductance compared with a single bond wire of the same physical length. The lumped inductors

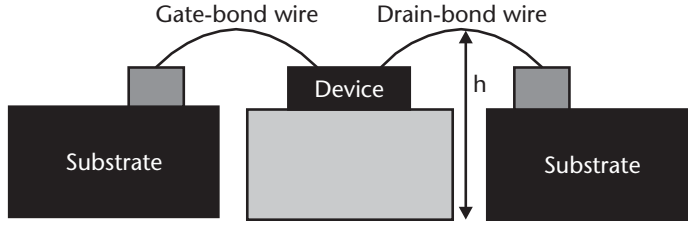


Figure 7.16 Mounted DPHEMT device with gate and drain bond-wire connections.

used at the gate and drain terminals of the active device in the amplifier designs in Chapter 6 were made of 0.7-mil ($17.78\text{-}\mu\text{m}$) diameter gold wire.

The characteristic impedance of a single gold wire above a ground plane is given by

$$Z_1 = (60/\sqrt{\epsilon_e})a \cosh(2000h/d) \quad (7.7)$$

where

Z_1 is the characteristic impedance of the single gold wire (Ω);

d is the diameter of gold wire (μm);

h is the height of gold wire above the ground plane (mm);

ϵ_e is the effective relative dielectric constant.

Therefore, the inductance L_1 in nH/mm of the single gold wire can be obtained from

$$L_1 = Z_1 \sqrt{\epsilon_e} / 300 \quad (7.8)$$

The characteristic impedance of a double gold wire above a ground plane is given by

$$Z_2 = (30/\sqrt{\epsilon_e}) \ln \left[(4000h/d) \sqrt{1 + (2h/s)^2} \right] \quad (7.9)$$

where s is the separation of wires (mm). Therefore, the inductance L_2 in nH/mm of the double gold wire is given by

$$L_2 = Z_2 \sqrt{\epsilon_e} / 300 \quad (7.10)$$

The inductance of the single and double gold-wire varies with height of the wire above the ground plane as shown in Figure 7.17. The figure enables the inductance in nH/mm to be calculated for a given physical height of the wire above the ground plane in the case of a single or double gold wire (for a wire separation of 0.15 mm).

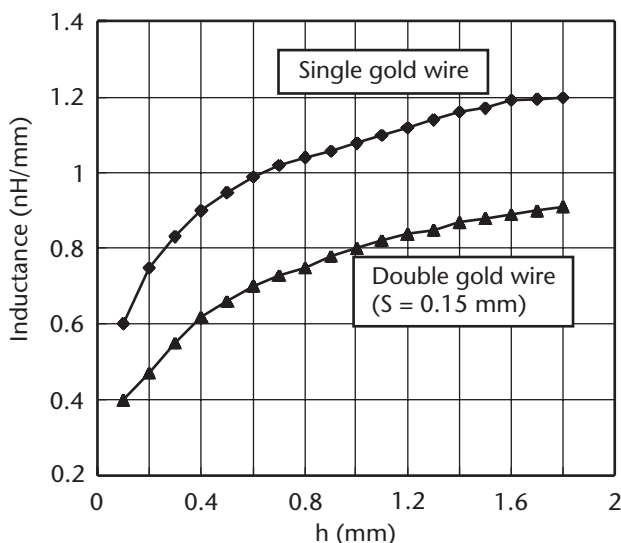


Figure 7.17 Inductance variation of 0.7-mil diameter gold-wire above the ground plane.

7.2.7 dc Biasing

The broadband amplifiers were dc biased by using the technique of self-bias mode [6], which is provided through source resistor R_s and source decoupling capacitor C_s , as illustrated in Figure 7.18. The value of the source resistor R_s determines the current drawn by the device. As the gate of the device is connected to ground via an inductor, the current drawn by the device causes a potential drop across the source resistors R_s given by $V_{gs} = -V_s$. Because the device's source terminal is connected to the capacitor C_s , the potential at this terminal will rise up with respect to the gate's potential until it eventually settles, thus providing the correct gate-source bias voltage to forward bias the device. The advantage of this bias method is that the device can be operated from a single positive supply without the need to have separate gate and drain bias.

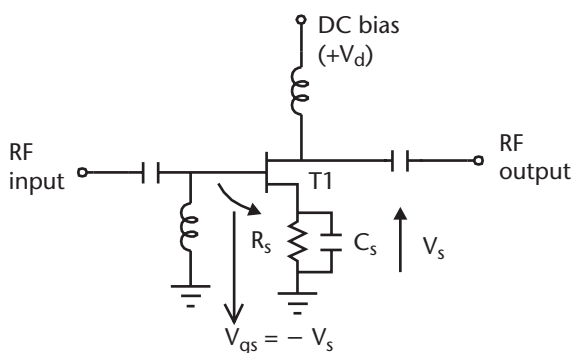


Figure 7.18 Self-bias circuit.

7.2.8 Substrate Material

The selection of the substrate depends upon the specific application required and on the frequency of operation. High dielectric constant substrates result in small-size circuits; however, a trade-off with size versus performance has to be made. The choice of the thickness of the substrate depends on the frequency of operation. Thinner substrates are required as the frequency becomes higher. For power amplifiers, good heat dissipation is required through the substrate.

The choice of substrate material in the realization of microstrip circuits is made broadly between the two classes known as *softboard*, which are low-loss plastic-type materials, and the *ceramic* or *crystalline materials*, such as Alumina, sapphire, and quartz [7]. The latter materials have the properties of mechanical rigidity at high temperatures, enabling the conducting metal layer to be deposited onto them by evaporation or sputtering techniques. The resultant coated substrate can be then be masked and chemically etched to provide conductive patterns with very high resolution (typically 10 μm). On the other hand, softboard material is usually clad with copper foil, and circuit patterns realized on it are limited to resolution of about 100 μm . This type of substrate can offer low dielectric constant ($\epsilon_r \approx 2$) and can be used to fabricate circuits using printed circuit board (PCB) etch techniques. In addition, the softboard material offers low cost and relaxed circuit tolerances.

MICs requiring higher resolution can be fabrication using *thin-film* techniques. Alumina is the most common material used for thin-film MICs. This material allows other materials to be deposited onto it, such as resistive material like commonly used nichrome or tantalum nitride. The nichrome layer is used to realize resistors, as described in Section 7.2.2. Onto the nichrome layer, a conductive material such as gold is sputtered. The Alumina substrate is available in various sheet sizes of different thickness, which can be polished to a high-surface finish with very accurate dimensions. Its high dielectric constant ($\epsilon_r = 9.8$) is useful at lower microwave-frequency MIC designs, as it enables the realization of reduced size circuits.

Crystalline materials such as sapphire have similar electrical properties to Alumina; however, it can be polished to a much higher quality of surface finish than Alumina. This can significantly reduce the loss at higher frequencies above the X band. The downside of sapphire is that it's more brittle than Alumina due to its crystalline structure. From an electrical point of view, quartz (fused silica) represents an excellent compromise as a microwave thin-film material, due to its fairly low dielectric constant ($\epsilon_r = 4$) coupled with very low losses in suitably processed material. Unfortunately, quartz is a very fragile material and requires great care in its handling.

Alumina substrate coated with nichrome and gold layers, having sheet dimensions of $2'' \times 2'' \times 0.015''$ thickness were utilized in the fabrication of the broadband amplifier circuits in Chapter 6. The physical properties of the Alumina substrate that was used are given in Table 7.2.

Table 7.2 Physical Properties of Alumina Substrate

Dielectric constant at 1 MHz	9.8 ± 0.1
Dissipation factor at 1 MHz	0.0001
Loss factor at 1 MHz	0.001
Thermal conductivity	34.7 W/m K

7.3 Circuit Layout and Mask Generation

The optimized MIC designs of the broadband feedback amplifier, traveling wave amplifier, and the CRTSSDA, described in Chapter 6, were transferred from their schematic circuit representation to the physical circuit layout using commercially available simulation tools. The physical circuit layout is used to generate a high-resolution chrome glass mask set, comprised of a *dark field* mask and a *light field* mask. The tolerances achievable on the glass masks are to within $\pm 1 \mu\text{m}$. The dark field mask is employed in the generation of the gold tracks and the light field mask enables the generation of the printed nichrome resistors.

7.3.1 Fabrication of MICs

The high-resolution chrome glass masks were employed in the processing of Alumina substrates using photolithography techniques. Photolithography or photo-etch, as it is often referred to, makes use of photographic techniques and photosensitive polymers. The photosensitive polymer is referred to as a photoresist that was applied as a thin layer to the thin-film circuit to be etched. The photoresist is then exposed with ultraviolet (UV) light through the chrome glass masks, and an image of the circuit pattern is formed through it. After developing the exposed photoresist, the desired pattern is created on the Alumina substrate. Because the photoresist is resistant to most chemical etchants, areas of the thin-film, which were unprotected, are removed by the etchant, leaving the remainder of the film delineated by the photoresist pattern. Figure 7.19 shows the stages involved in the processing of thin-film Alumina circuits.

The procedure normally used in the processing of the thin-film Alumina substrates is as follows:

- Metalized substrate comprised of nichrome and gold seed layers is baked at 125°C for 30 min.
- Substrate is prepared (clean substrate using trichloroethylene, acetone, or isopropanol)
- Photoresist coating is applied by spinning the substrate at 4,000 revolutions per min (RPM) to achieve a thickness of $1.5 \mu\text{m}$.
- Coated substrate is allowed to air dry for 15 min and then baked at 90°C for 2 min in a forced-air oven.
- Substrate is exposed to UV light ($\text{UV} \approx 300\text{-nm}$ wavelength) for 10 to 20 sec depending on lamp intensity using *dark field mask M51*.

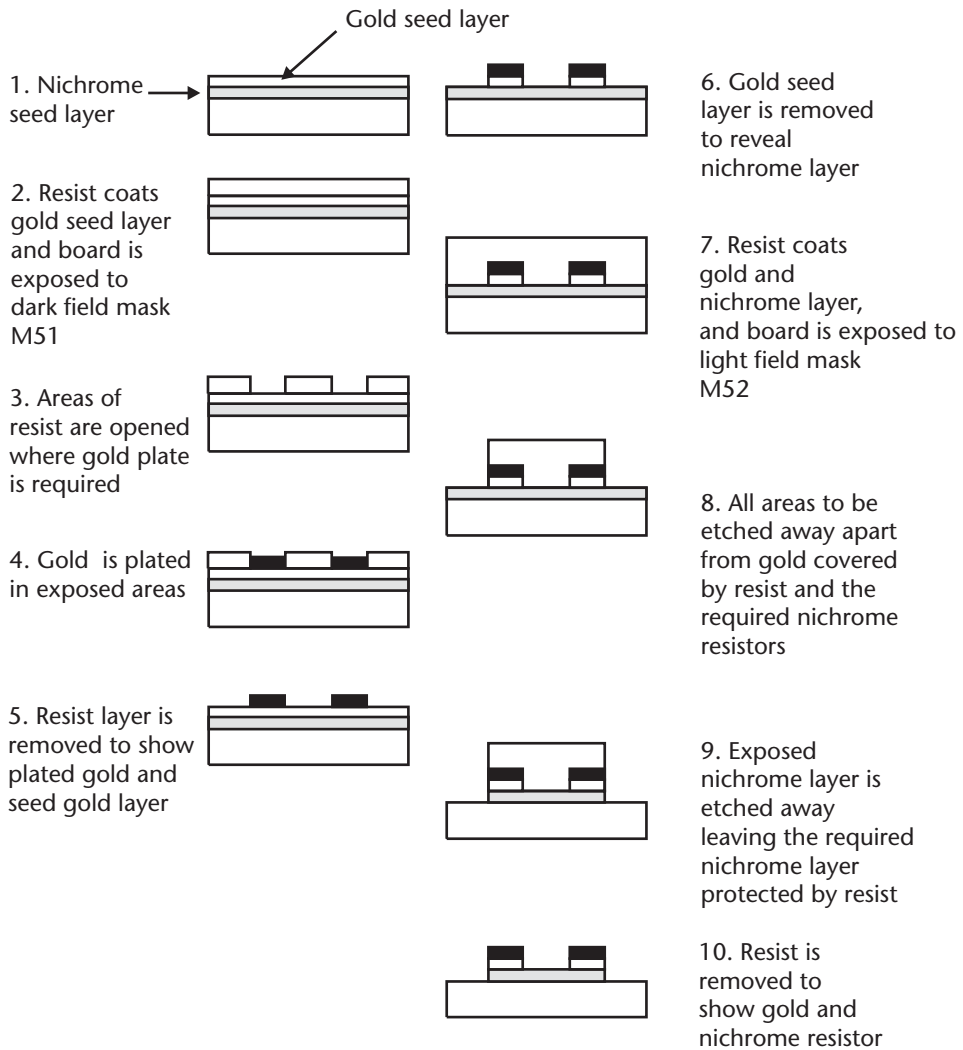


Figure 7.19 MIC processing of thin-film Alumina circuits.

- Circuit tracks exposing seed gold layer is gold plated to a thickness of 5 to $6\mu\text{m}$.
- Gold is etched.
- Substrate is immersed in developer and gently agitated for 1 min followed by a wash in deionized water and rinsed.
- This is spun dry at 2,000 RPM.
- Photoresist coating is applied by spinning the substrate at 4,000 RPM to achieve a thickness of $1.5\mu\text{m}$.
- Coated substrate is allowed to air dry for 15 min and then baked at 90°C for 2 minutes in a forced-air oven.

- Substrate is exposed to UV light for 10 to 20 sec depending on lamp intensity using *light field mask M52*.
- Nichrome is etched.
- Substrate is immersed in developer and gently agitated for 1 min followed by a wash in deionized water and rinsed.
- This is spun dry at 2,000 RPM.
- Then, this is post baked at 150°C to improve resist adhesion.

If the exposure time is correct and the developer is reacting properly, the photomask pattern should replicate the pattern on the substrate. The circuit pattern was realized using the *pattern-plate* process method. This method is an additive technique and offers the following advantages over subtractive methods:

- Precious gold metal is deposited only where it is required (i.e., contact pad areas and conductor lines).
- Close dimensional tolerances are easily achieved.
- Thick, narrow lines are possible, which would otherwise be unattainable using chemical etchants, and the cross-section of the line pattern is more nearly rectangular than trapezoidal, as illustrated in Figure 7.20, and more desirable for MIC.

The processed substrates are lasered to provide circular and rectangular cut outs for the gold-plated mounting posts onto which chip components were mounted. Figures 7.21 to 7.24 show drawings of the individual amplifier Alumina substrates. The 2" × 2" × 0.015"—Alumina tiles were cut into individual substrates using a diamond

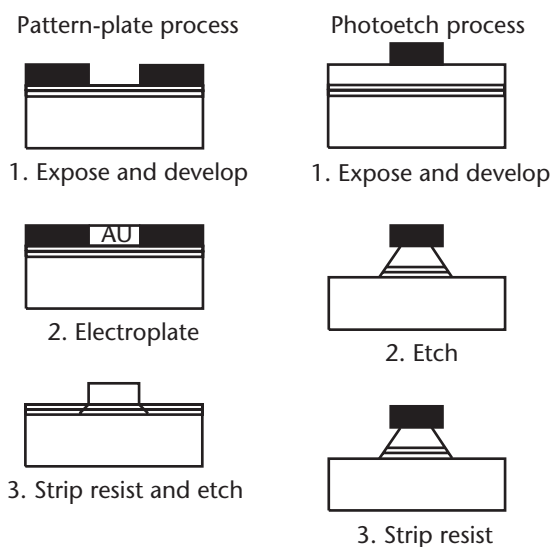


Figure 7.20 Schematic compares pattern plating and photoetch processes.

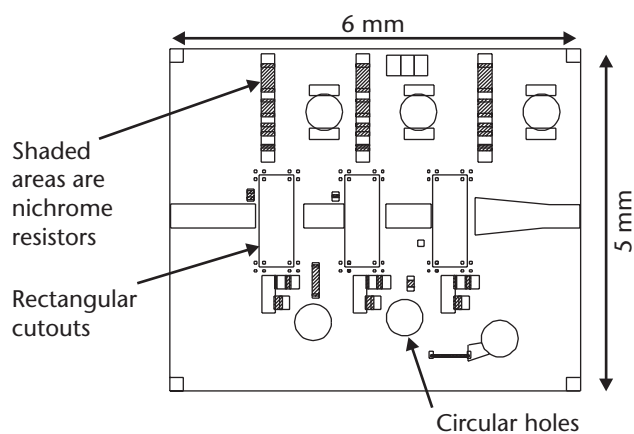


Figure 7.21 Alumina substrate of the CRTSSDA circuit with a tapered output-match.

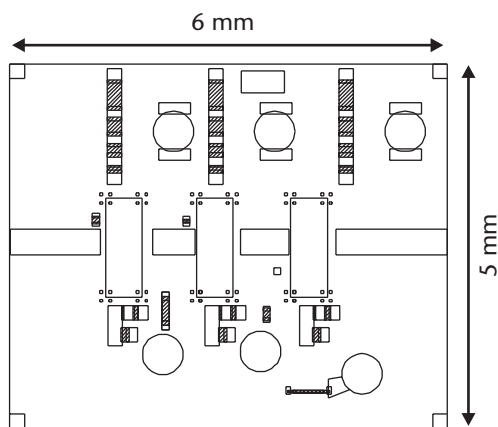


Figure 7.22 Alumina substrate of the CRTSSDA circuit with 50-Ω output.

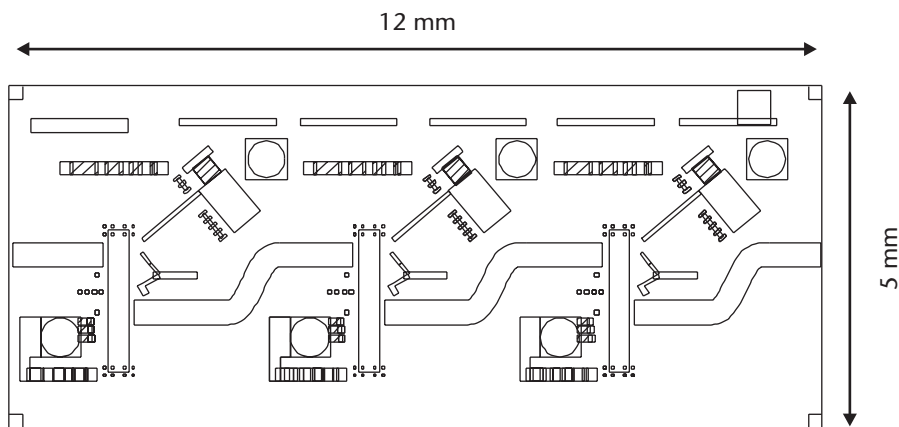


Figure 7.23 Alumina substrate of the traveling wave amplifier circuit.

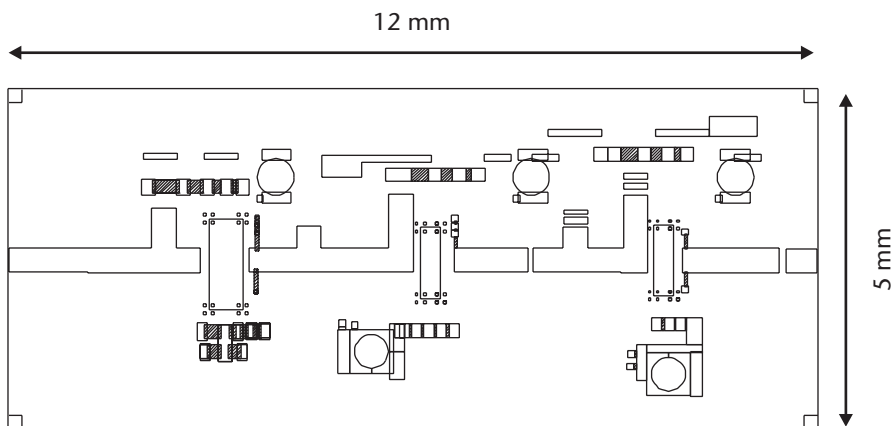


Figure 7.24 Alumina substrate of the feedback amplifier circuit.

saw. The completed circuits are comprised of high-definition thin-film gold tracks and high-tolerance printed nichrome resistors. The individual Alumina substrates and the mounting post were soldered using gold/tin solder in a belt furnace onto the gold-plated tungsten/copper amplifier housing. The chip components were manually placed onto the mounting posts and attached using silver-loaded conductive epoxy that is cured at 150°C for 1 hr. The attached components are then wire bonded using 0.7-mil gold wire. Gold coils were also attached where necessary using nonconductive epoxy.

7.4 Fabrication of Test Carriers and Amplifier Housings

The test carriers, amplifier housings, and test jigs were all designed using the AutoCad® package. The material selected for the fabrication of the test carriers and amplifier housings was copper-tungsten, because its coefficient of thermal expansion is closely matched to the GaAs and the Alumina ceramic materials. Table 7.3 shows the material characteristics for copper-tungsten, GaAs, and Alumina [7].

The machined test carriers and amplifier housings are first nickel plated to a thickness of 3 to 5 μm and then gold plated to a thickness of 5 μm. The test carrier and test jig used is shown in Figures 7.25 and 7.26. The amplifier housings and the

Table 7.3 Material Characteristics

Material	Thermal Conductivity (W/m°C)	Coefficient of Thermal Expansion (PPM/°C)
Alumina	17	6.7
GaAs	54	6.5
Copper-tungsten	180	6.5 to 8.3

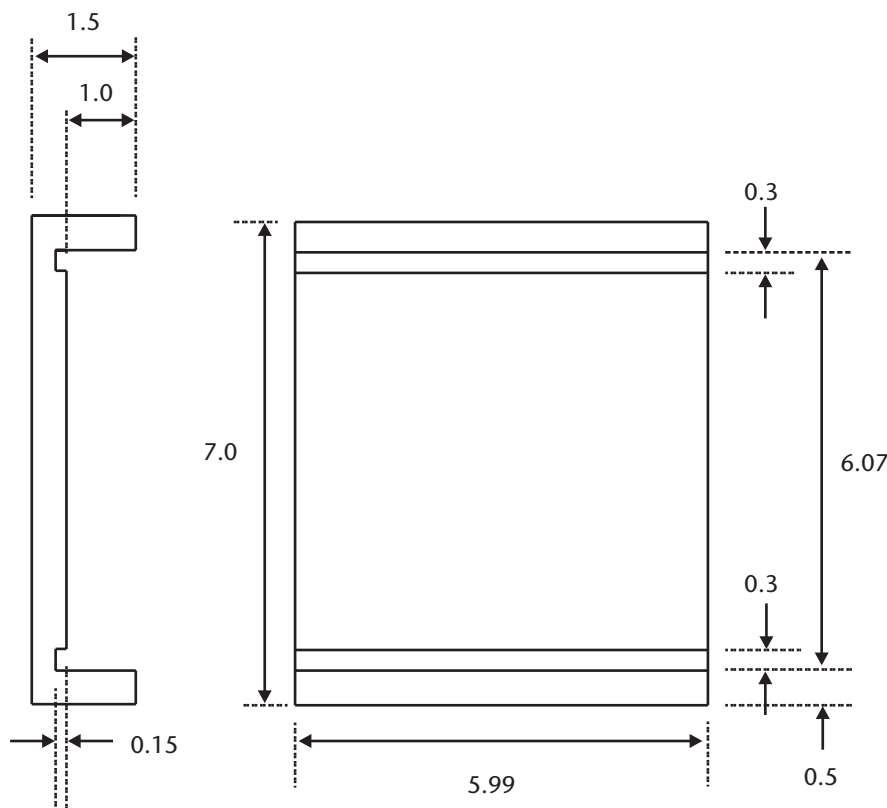


Figure 7.25 Test carrier (dimensions in mm).

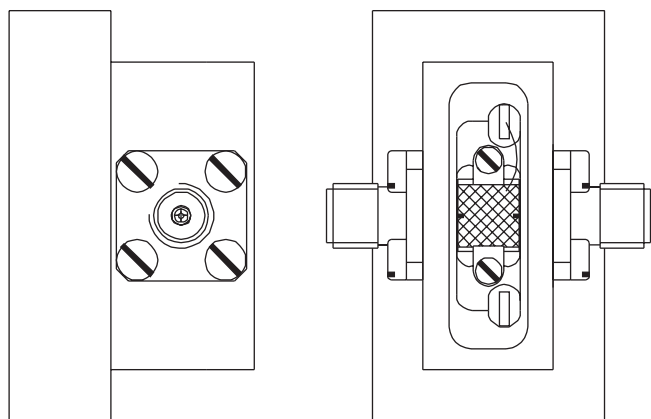


Figure 7.26 Test jig for carrier.

test jigs that were used to test the amplifiers are shown in Figures 7.27 to 7.30. The test jigs were all fabricated from brass.

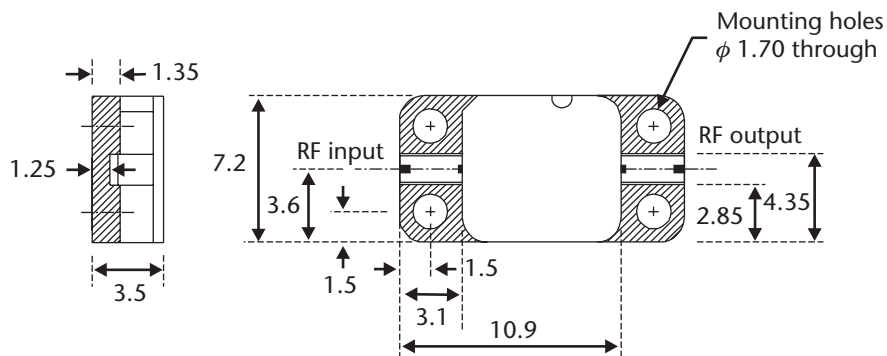


Figure 7.27 14-mm amplifier housing.

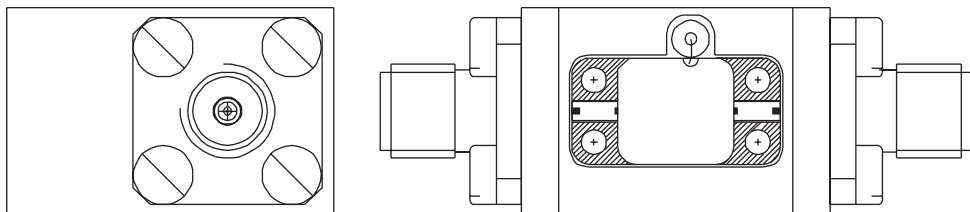


Figure 7.28 14-mm amplifier housing test jig.

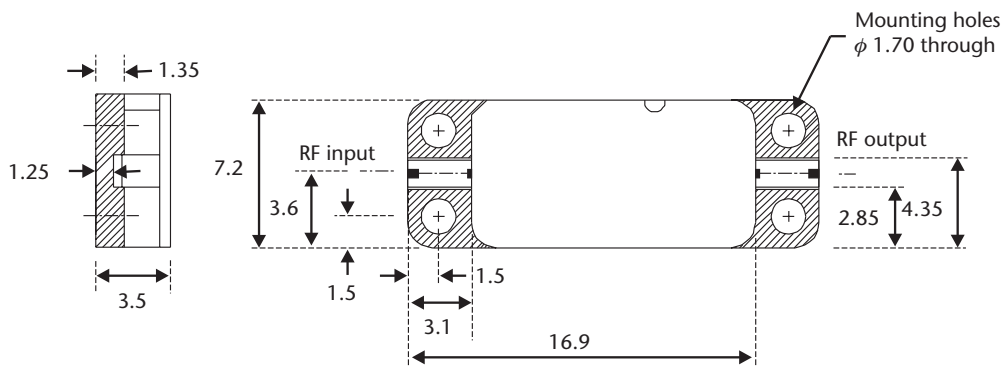


Figure 7.29 20-mm amplifier housing.

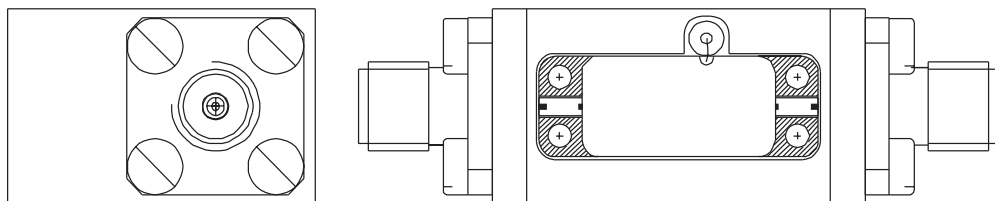


Figure 7.30 20-mm amplifier housing test jig.

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Ultrabroadband Hybrid and Broadband Monolithic Amplifiers

8.1 Introduction

Broadband amplifiers find application in EW, instrumentation, and fiber-optic communication systems. In the case of EW systems, the amplifiers are typically required to operate over a frequency range of 2 to 20 GHz. However, amplifiers for instrumentation and fiber-optic communication applications have to meet a more stringent requirement of operating over an ultrabroadband range extending from 30 kHz to 40 GHz. In addition, they have to exhibit a flat gain and low input and output VSWR over the entire operating frequency range.

The distributed amplifier provides a viable technique for realizing ultrawideband amplifiers [1]. They consist of artificial input and output lines that are constructed with a series of transmission lines and the parasitic capacitances of the transistor, as described in Chapter 2. These lines have very high cut-off frequencies and cancel out the effects of parasitic capacitances associated with the active devices. Hence, these amplifiers inherently possess wideband characteristics. This technique, when used in conjunction with novel device technologies, can produce impressive wideband amplifiers for millimeter-wave applications up to 180 GHz [2, 3].

This chapter gives practical design examples and the measured performance of ultrabroadband and broadband amplifiers realized using the TWDA and CSSDA.

8.2 Ultrabroadband Hybrid MIC Amplifier

In this section, multioctave (30 kHz to 40 GHz) amplifier designs are presented using the concept of CRTSSDA and TWDA for optical application.

A CRTSSDA and a traveling wave amplifier, each comprising of three active devices, were designed and implemented for multioctave performance using the methodology described in Chapter 6. The schematic circuit diagram of the CRTSSDA is shown in Figure 8.1. Figures 8.2 and 8.3 show the respective amplifier performance simulated across 30 kHz to 40 GHz. These results clearly show that the CRTSSDA offers considerably higher gain compared to the traveling wave amplifier using the same number of identical active devices. In fact, the TWDA

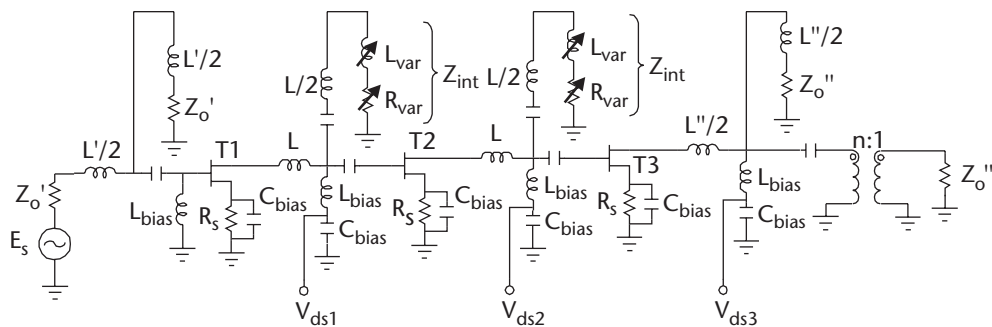


Figure 8.1 Three-stage CRTSSDA.

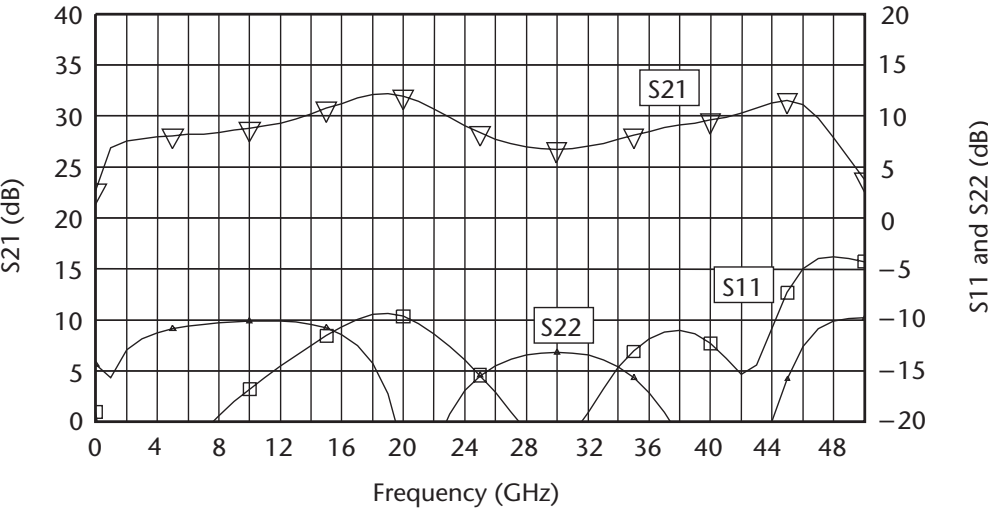


Figure 8.2 Transmission and return loss response of the CRTSSDA.

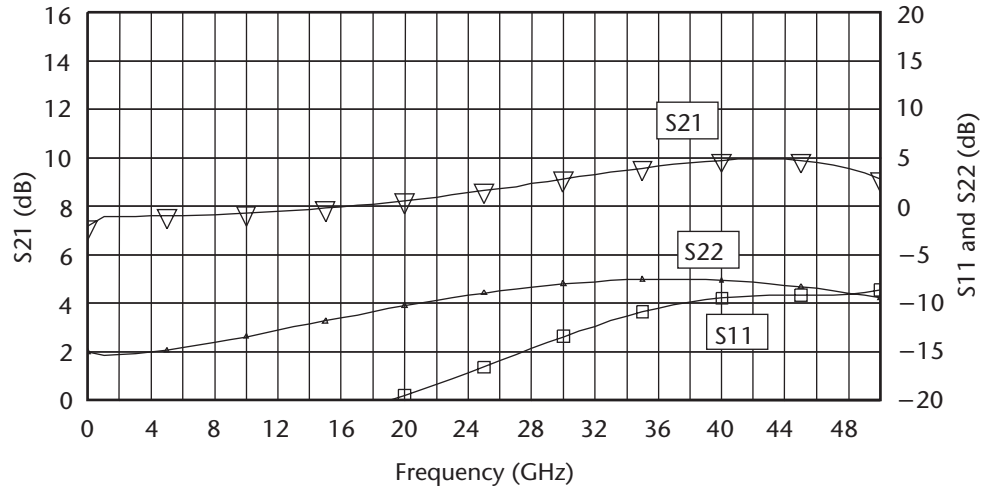


Figure 8.3 Transmission and return loss response of the TWDA.

would require a cascade of three stages to achieve a comparable gain to the CRTSSDA. Moreover, the current consumption by the CRTSSDA is 40 mA, whereas the comparable three-stage TWDA would require 120 mA, as thrice the number of active devices is used. Consequently, the three-stage TWDA would dissipate proportionately more power than the CRTSSDA.

8.3 Ultrabroadband Hybrid Amplifier as Data Modulator Driver

The transmission of digital data by fiber-optic link has found important applications in high-capacity and long-distance communication systems. At present, the commercial high-speed fiber-optic communication systems operate at data rates of 2.5 Gbps, 10 Gbps, 12.5 Gbps and 20 Gbps. This is made possible by the use of ultrawideband amplifiers as data modulator drivers in fiber-optic transmission systems. Such digital optical systems require high-performance amplifiers that are power efficient, exhibit extremely flat group delay variations over the entire frequency band of operation extending from kilohertz to gigahertz to avoid data distortion, and are relatively small. This section describes the design and development of a 30-kHz to 20-GHz data modulator driver amplifier that supports transmission of data rates from 2.5 Gbps to 20 Gbps.

8.3.1 Driver Amplifier for Optical Transmitter

The block diagram of a simple fiber-optic transmission system is shown in Figure 8.4. Here, the ultrawideband amplifier is used as a data driver in the transmitter chain. In particular, the data driver amplifier is used to modulate the base-band data onto the optical signal using the Lithium Niobate Mach-Zehnder phase modulator. To drive the phase modulator, the amplifier must be capable of producing a pair of differential electrical voltages with a peak-to-peak amplitude in the range of $\pm 3\text{V}$ to $\pm 4\text{V}$, which corresponds to a saturated output power of 19.5 dBm to 22 dBm, respectfully.

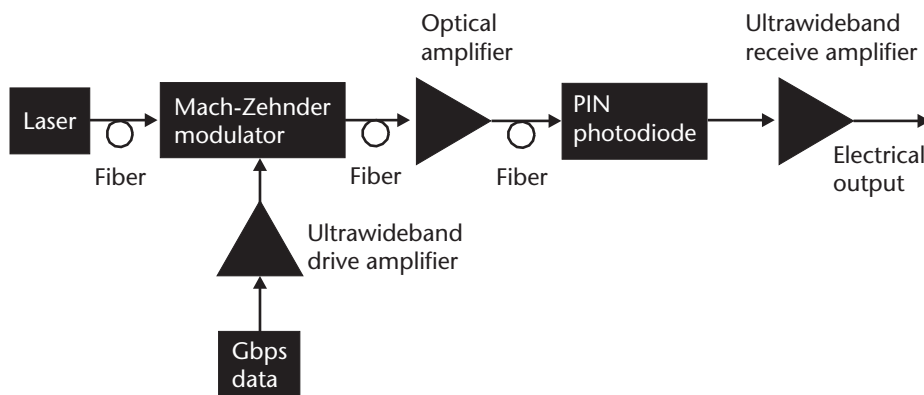


Figure 8.4 Fiber-optic digital transmission system.

8.3.2 Amplifier Requirements

The main requirements for high-speed driver amplifiers are very broad instantaneous bandwidth, constant gain response, very good phase linearity, constant output power response, detector outputs, and variable gain control. Table 8.1 gives the typical performance requirements.

8.3.3 Amplifier Design

The amplifier design implemented comprised of a cascade of three broadband TWDAs, as shown in Figure 8.5. The amplifier line up is selected to meet the required small-signal gain level and to ensure that the amplifier is maintained into saturation at the minimum input signal level.

The MMIC amplifiers were used, as they offer the low-frequency extension (LFE) down to 30 kHz and gain control to allow the eye amplitude to be changed. Two detector circuits were employed to provide temperature-compensated dc output. The *RF detector* circuit was used to monitor the output voltage of the amplifier, and the *reference detector* circuit was used to minimize the temperature variation of the detector output.

Figure 8.6 shows the simulation response of the three-stage amplifier without the inclusion of the low-frequency compensation (LFC) circuit. This figure shows that the gain rises sharply at low frequencies from about 2 GHz to 10 MHz. Fortunately, the TWDAs incorporate auxiliary gate and drain bonding pads that can be exploited to provide the LFE down to 30 kHz. The rising gain response at the low frequency end was reduced to make it flat by using additional LFC circuit on the drain connection of the first and last TWDA. Also, although the bias feed presented the necessary high impedance at the upper end of the amplifiers bandwidth, it was very crucial to provide high impedance at the lower frequencies, too. Otherwise, the amplifier’s performance may be compromised at the lower frequencies. This was circumvented on the first and second TWDAs by biasing the drain through resistors and on the third TWDA by providing dc bias through a combination of low- and high-value inductors. The latter awkward biasing technique is necessary to minimize any voltage drop at the drain and therefore achieve the maximum peak-to-peak voltage swing. Broadband dc block in the amplifier circuit was provided by using OPITICAPS®. Figure 8.7 shows simulation of the LFC compensated amplifier, and Figure 8.8 shows the completed RF and the integrated amplifier assembly.

Table 8.1 Typical Performance Requirements for High-Speed Driver Amplifiers

Frequency response	30 kHz–20 GHz
Small-signal gain	23 to 18 dB
Gain ripple	5 dB
Peak-to-peak output voltage	8V (min)
Eye crossing	45 % to 50 %
Eye opening	80 % at 10 Gbps

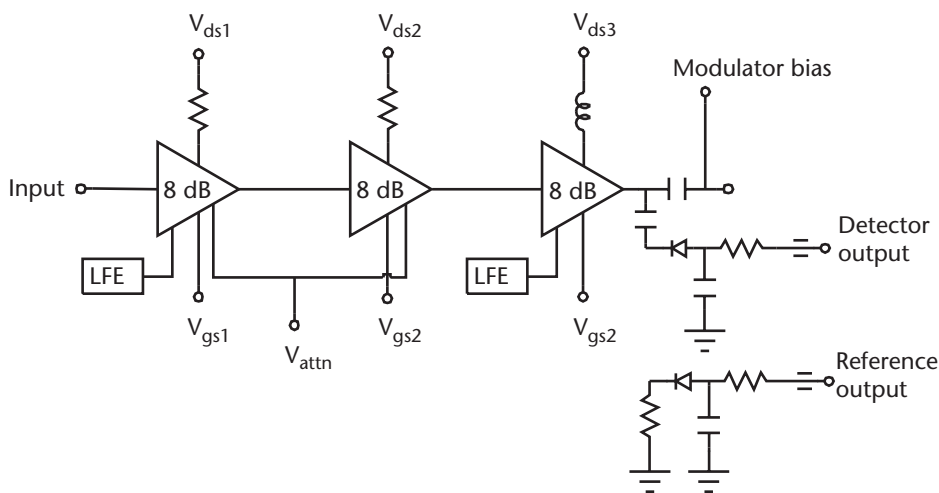


Figure 8.5 Three-stage TWDA amplifier line up.

8.3.4 Amplifier Performance

Figure 8.9 shows the measured small-signal performance of the amplifier. The measured performance correlates excellently with the simulated response in Figure 8.7. The optimized amplifier eye performance for maximum output voltage and 50% eye crossing at data rates of 2.5 Gbps, 10 Gbps, 12 Gbps, and 20 Gbps with an input signal level of 600 mV are shown in Figures 8.10–8.13. The typical current drawn by the amplifier was 500 mA at +11-V supply and 5 mA at the –5-V supply.

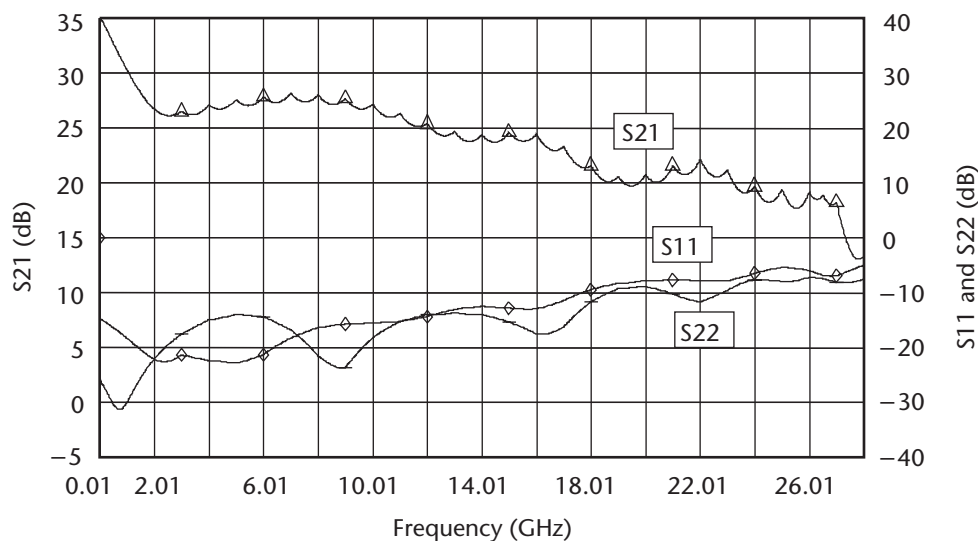


Figure 8.6 Transmission and return loss response of the uncompensated amplifier.

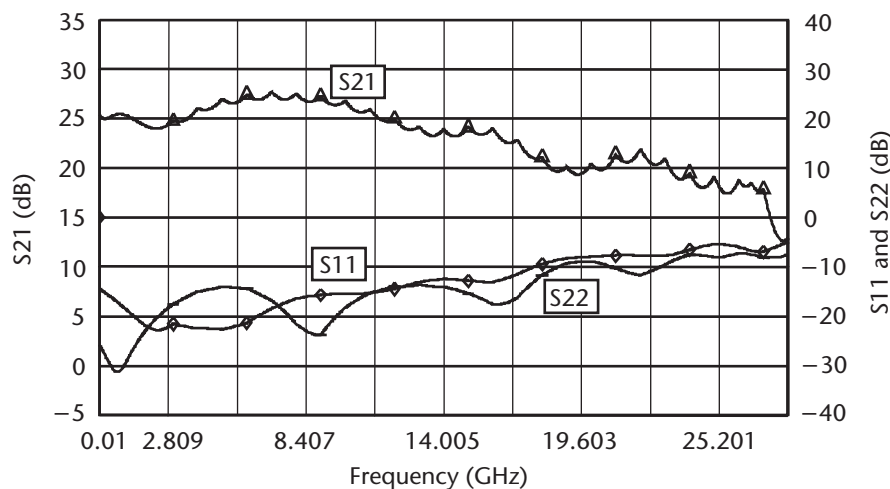


Figure 8.7 Transmission and return loss response of the LFE compensated amplifier.

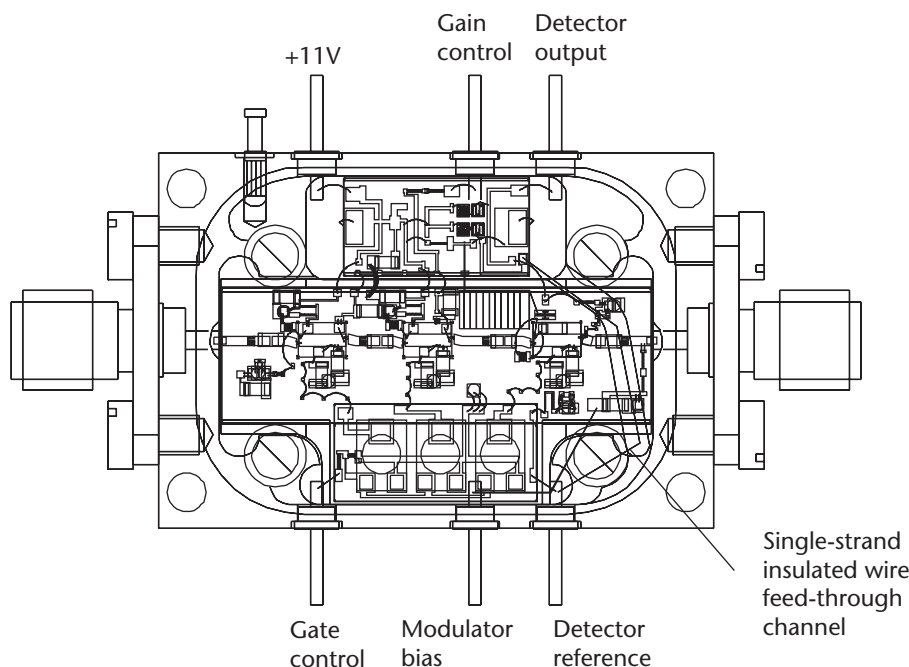


Figure 8.8 Amplifier assembly.

These results demonstrate that the design and fabrication of a Lithium Niobate Mach-Zehnder modulator driver is capable of operating at data rates from 2.5 Gbps to 20 Gbps.

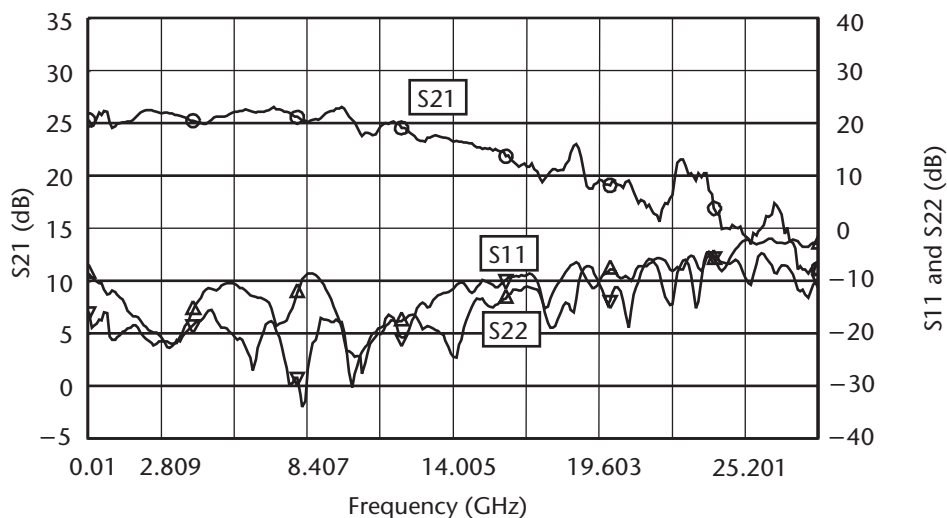


Figure 8.9 Amplifier's small-signal gain response.

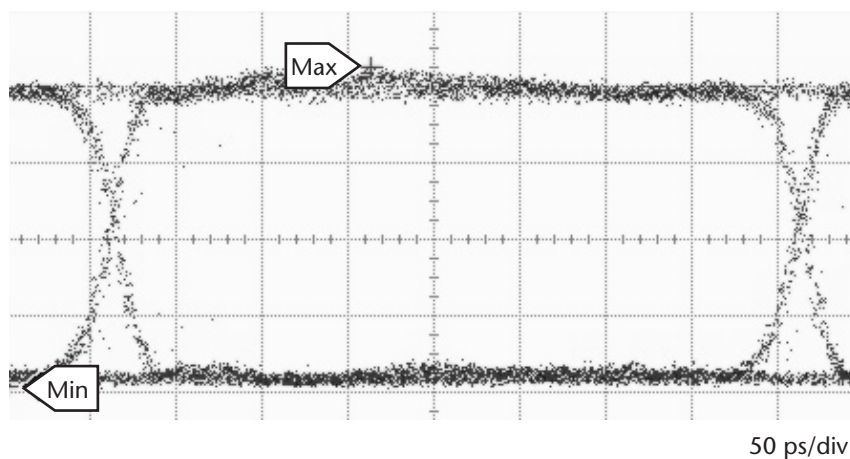


Figure 8.10 Output eye diagram at 2.5 Gbps.

8.4 Broadband MMIC Distributed Amplifier

In this section, it is shown that the CSSDA design, described in Chapter 2, is amenable to MMIC technology. A two-stage CSSDA has been fabricated using MMIC technology [4]. The distributed amplifier occupies a chip size of $1.5 \times 1 \text{ mm}^2$ and exhibited wide bandwidth, high gain, and flat group delay performance.

The MMIC distributed amplifier was manufactured using GaAs-based PHEMT MMIC foundry process. The active device is a $0.2\text{-}\mu\text{m}$ gate-length PHEMT with a unit current gain frequency (f_T) and a maximum oscillation frequency (f_{max}) of 53 GHz and 80 GHz, respectively. The peak of transconductance and maximum

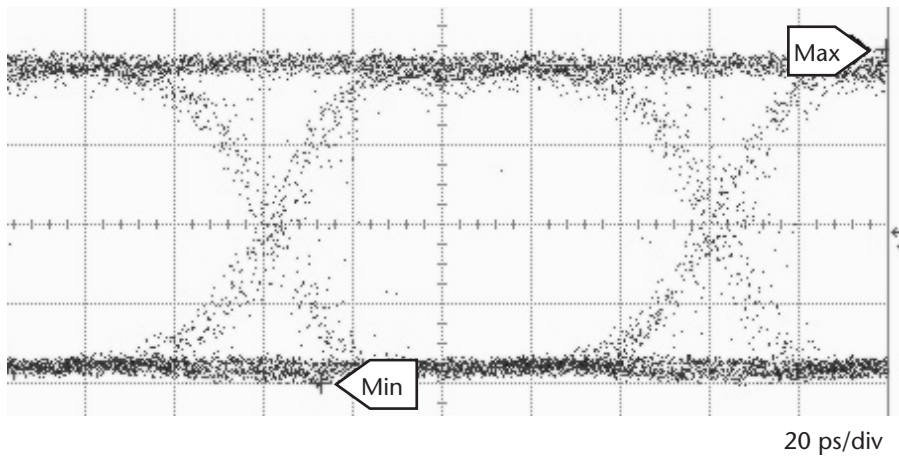


Figure 8.11 Output eye diagram at 10 Gbps.

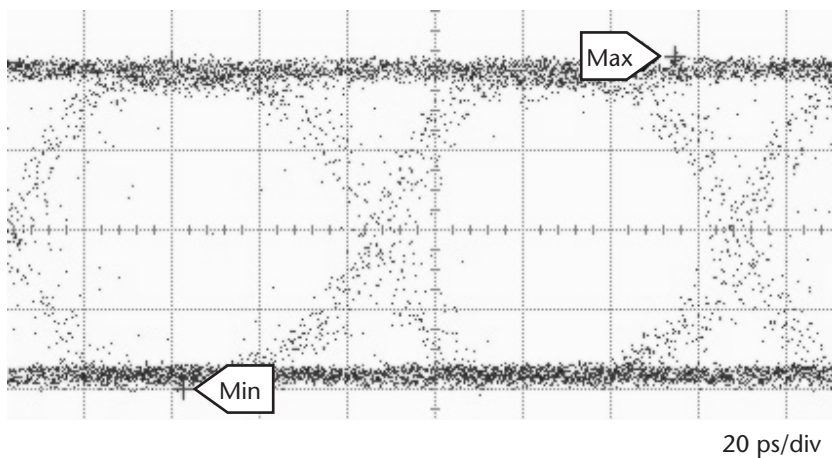


Figure 8.12 Output eye diagram at 12 Gbps.

current at peak transconductance are 220 mS/mm and 180 mA/mm, respectively. The passive components in the design include GaAs thin-film resistor, metal-insulator-metal (MIM) capacitor, inductor, and via hole through 100- μ m GaAs substrate. The entire chip is protected by silicon-nitride passivation for reliability. Figure 8.14 shows the photograph of the fabricated MMIC chip.

Figure 8.15 shows the measured gain and input/output return losses of the MMIC distributed amplifier. The amplifier provides a small-signal gain of 15 dB with flatness of 1 dB and input/output return loss better than 8 dB with total dc power consumption 100 mW in the frequency range of 0.5 to 27 GHz. The gain roll-off of this amplifier is very gradual, which is important for digital optical

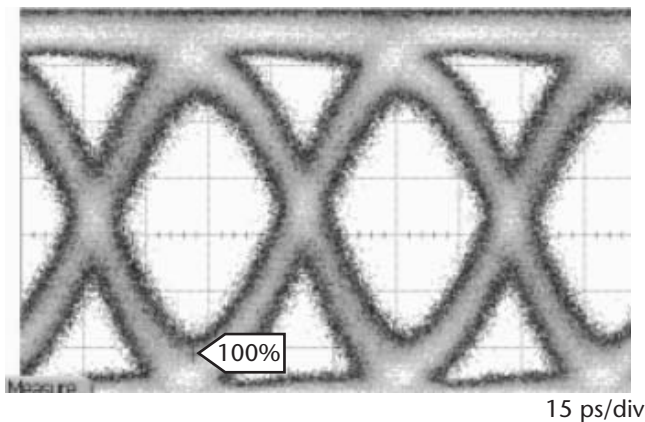


Figure 8.13 Output eye diagram at 20 Gbps.

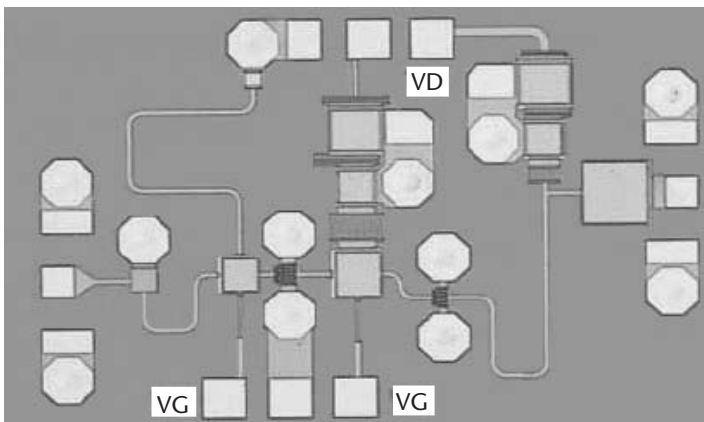


Figure 8.14 Photograph of the MMIC distributed amplifier. (From: [4], © 2003 European Microwave Conference)

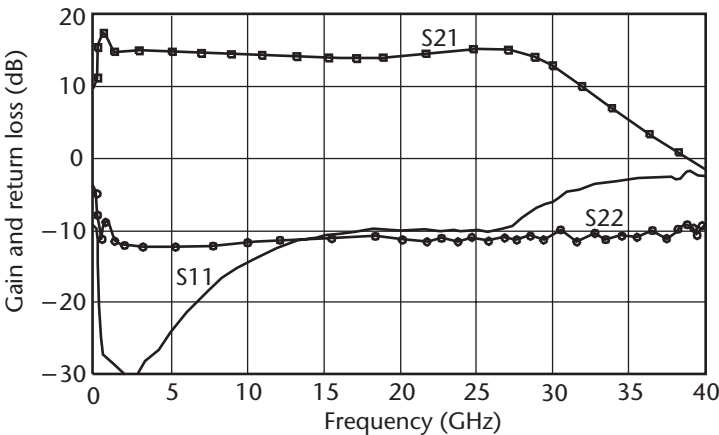


Figure 8.15 Measured small-signal gain and return loss of the MMIC amplifier. (From: [4], © 2003 European Microwave Conference.)

communication applications, as the sharp gain roll-off often seen in distributed amplifiers leads to excessive group delay peaking and a deteriorated eye diagram.

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- [4] Kuo-Liang, D., et al., "A Miniature High Gain and Broadband MMIC Distributed Amplifier," *33rd European Microwave Conference*, Munich, 2003, pp. 615–618.

Artificial Transmission Line Theory Related to Distributed Amplifiers

A.1 Artificial Transmission Line

The ideal artificial transmission line is associated with negligible attenuation and therefore is purely resistive. In practice, it may be realized for a specified frequency range using lumped element capacitors and inductors, as illustrated by the network in Figure A.1. Assuming that these components are lossless, this structure exhibits a lowpass filter characteristic with cut-off frequency f_c . When the structure is correctly terminated in its characteristic impedance Z_o , the line presents no attenuation at frequencies below f_c . The characteristic impedance, however, in reality is frequency dependent, and for frequencies below f_c it is resistive yet at other frequencies it becomes reactive. Furthermore, any signal traveling through such an artificial transmission line suffers a phase delay and distortion.

A.2 Ladder Network

Ladder network is an artificial transmission line composed of complex lumped series and shunt impedances Z_1 and Z_2 , respectively. The ladder network is illustrated in Figure A.2

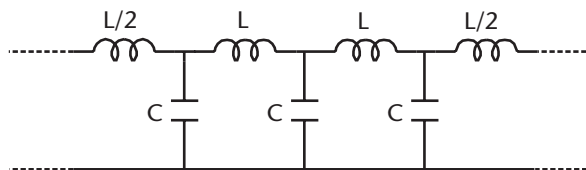


Figure A.1 Artificial transmission line.

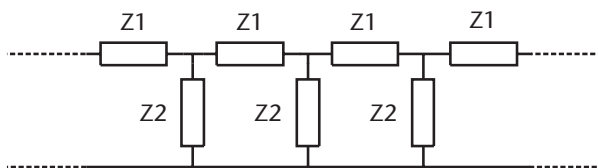


Figure A.2 The ladder network.

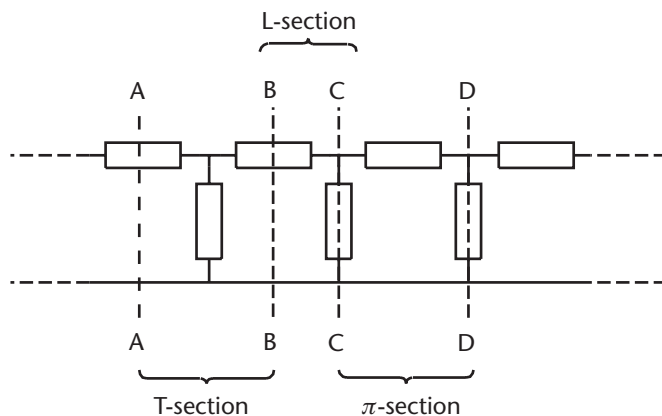


Figure A.3 Ladder network sections.

Ladder network can be considered to be constructed from cascading a combination of T-sections, π -sections, and L-sections, as illustrated in Figure A.3. The behavior of the ladder network can be determined by analyzing these types of sections.

Imagine a section to be taken from this network by cutting along lines AA and BB in Figure A.3. The result is the T-section shown in Figure A.4, and the ladder network could be built up simply by cascading a large number of such T-sections.

Now image a section to be taken by cutting along lines CC and DD. The result is the π -section shown in Figure A.5, and again the ladder network could be built up by cascading a series of π -sections.

Similarly, cutting a section at BB and CC will result in an L-section, as shown in Figure A.6. The ladder network can be considered constructed from a series of L-sections.

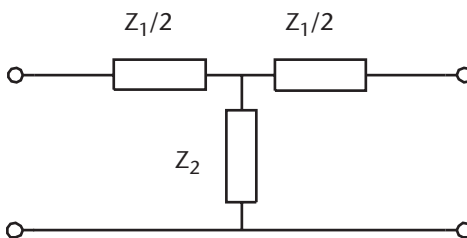


Figure A.4 T-section network.

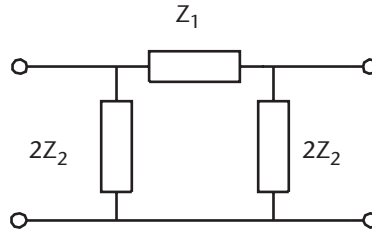
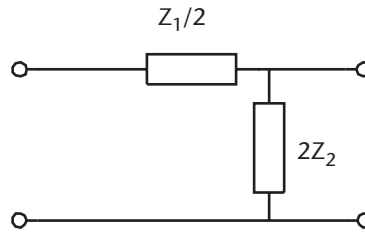
Figure A.5 π -section network.

Figure A.6 The L-section network.

A.3 Characteristic Impedance Z_o

The characteristic impedance is a particular load impedance that, when connected across the output terminal of a two-port network, makes the input impedance exactly equal to the load impedance. The characteristic impedance given by [1]

$$Z_o = \sqrt{Z_{oc} Z_{sc}} \quad (\text{A.1})$$

where Z_{sc} and Z_{oc} are the short- and open-circuit impedance, respectively. Z_{sc} is the impedance at the input terminal when the output terminal is short circuited, and Z_{oc} is the input impedance when the output is open circuited.

It can be shown that when a chain of cascaded identical sections in a network are terminated at both ends in its characteristic impedance, every individual section in the chain is also terminated at both ends in their characteristic impedances, as illustrated in Figure A.7.

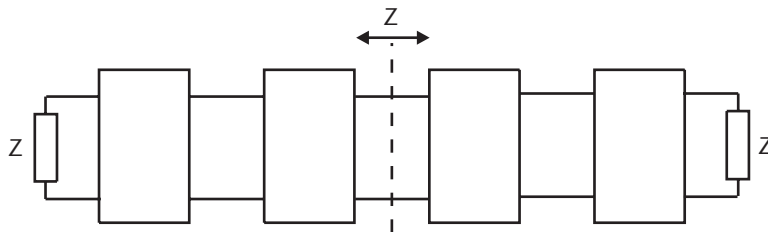


Figure A.7 Chain of cascaded networks terminated by their characteristic impedances.

A.4 T-Section

The input impedance of the open-circuit T-section Z_{OCT} , shown in Figure A.8, is given by

$$Z_{OCT} = Z_1/2 + Z_2 \quad (\text{A.2})$$

Under short-circuit condition, the input impedance of the T-section Z_{SCT} is given by

$$Z_{SCT} = Z_1/2 + (Z_1 Z_2 / 2) / [(Z_1/2) + Z_2] \quad (\text{A.3})$$

Hence, the characteristic impedance Z_o of the T-section is then obtained by substituting (A.2) and (A.3) into (A.1). That is,

$$Z_{OT} = \sqrt{[Z_1 Z_2 (1 + Z_1/4Z_2)]} \quad (\text{A.4})$$

A.5 π -Section

The input impedance of an open-circuit and short-circuit π -section, shown in Figure A.9, are given by

$$Z_{OC\pi} = [2Z_2 (Z_1 + 2Z_2)] / (Z_1 + 4Z_2) \quad (\text{A.5})$$

$$Z_{SC\pi} = 2Z_1 Z_2 / (Z_1 + 2Z_2) \quad (\text{A.6})$$

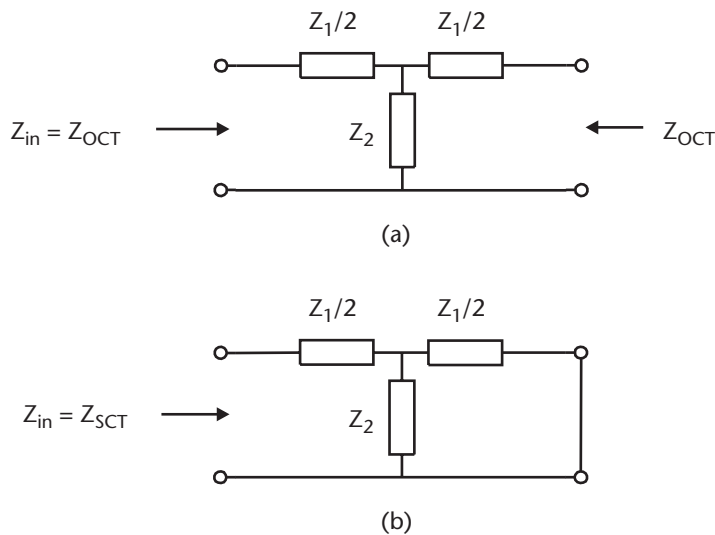


Figure A.8 T-section: (a) open circuit, and (b) short circuit.

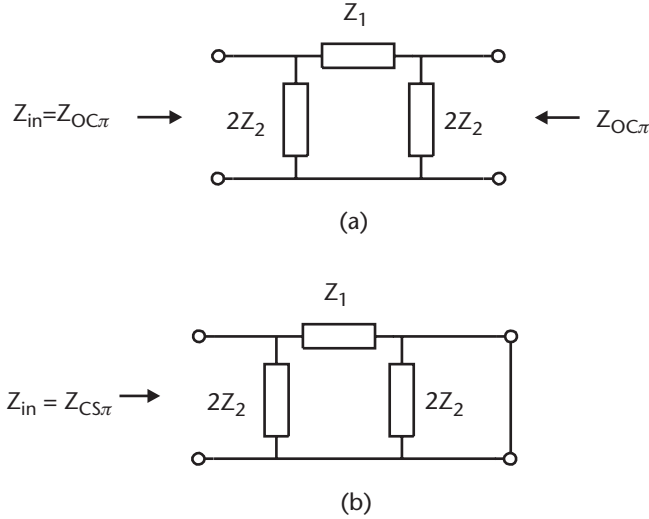


Figure A.9 π -section: (a) open circuit, and (b) short circuit.

The corresponding characteristic impedance Z_o of the π -section is then obtained by substituting (A.5) and (A.6) into (A.1). That is,

$$Z_{O\pi} = \sqrt{Z_1 Z_2 / [1 + (Z_1 / 4Z_2)]} \quad (\text{A.7})$$

A.6 L-Section

Figure A.10 shows two L-sections out from a ladder network whose series and shunt impedances are $Z_1/2$ and $2Z_2$, respectively. If end AA in Figure A.10(a) is terminated with an impedance equal to the characteristic impedance of the T-section, then the input impedance is given by

$$Z_{in} = 2Z_2 (Z_{OT} + Z_1/2) / (2Z_2 + Z_{OT} + Z_1/2) \quad (\text{A.8})$$

Multiplying the numerator and denominator of (A.8) by $Z_1/2$, gives

$$Z_{in} = Z_1 Z_2 (Z_{OT} + Z_1/2) / [Z_1 Z_2 (1 + Z_1/4Z_2) + Z_1 Z_{OT}/2] \quad (\text{A.9})$$

The term $Z_1 Z_2 (1 + Z_1/4Z_2)$ in the denominator can be substituted by Z_{OT}^2 from (A.4). Thus,

$$Z_{in} = Z_1 Z_2 (Z_{OT} + Z_1/2) / Z_{OT} (Z_{OT} + Z_1/2) = \sqrt{Z_1 Z_2 / (1 + Z_1/4Z_2)} \quad (\text{A.10})$$

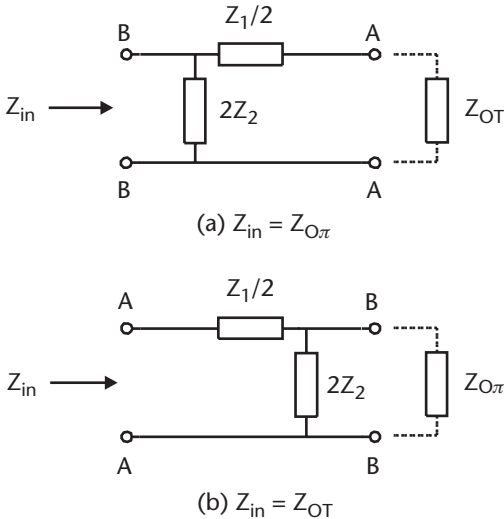


Figure A.10 L-section network.

This equation corresponds to the characteristic impedance of the π -section given by (A.7). Similarly, it can be shown that if end BB is terminated by $Z_{O\pi}$, as in Figure A.10(b), then the input impedance is equal to Z_{OT} . These two impedances, $Z_{O\pi}$ and Z_{OT} , are the image impedances of the L-section.

Reference

[1] Williams, E., *Electrical Filter Circuits—An Introduction Course*, London: Sir Isaac Pitman and Sons Ltd, 1963.

List of Acronyms

2-DEG	Two-dimensional electron gas
ac	Alternating current
AM	Amplitude modulation
CAD	Computer-aided design
C/I	Carrier-to-third order intermodulation product ratio
CSSDA	Cascaded single-stage distributed amplifier
CRTSSDA	Cascaded reactively terminated single-stage amplifier
dc	Direct current
DPHEMT	Double-heterojunction pseudomorphic high-electron-mobility transistor
EW	Electronic warfare
FET	Field effect transistor
InGaAs	Indium gallium arsenide
InALAs	Indium aluminum arsenide
HEMT	High-electron mobility transistor
HJ-FET	Heterojunction field effect transistor
IF	Intermediate frequency
IMD	Intermodulation distortion
JFET	Junction field-effect transistor
LFC	Low-frequency compensation
LO	Local oscillator
LFE	Low-frequency extension
MBE	Molecular-beam-epitaxy
MESFET	Metal-semiconductor field effect transistor
MIC	Microwave integrated circuit

MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MOS	Metal-oxide-semiconductor
NF	Noise figure
PCB	Printed circuit board
PHEMT	Pseudomorphic high-electron-mobility transistor
PM	Phase modulation
RF	Radio frequency
RPM	Revolutions per minute
SPHEMT	Single-heterojunction pseudomorphic high-electron-mobility transistor
SSTWA	Single-stage traveling wave amplifier
TEM	Transverse electromagnetic
TRL	Thru reflect line
TWDA	Traveling wave distributed amplifier
UV	Ultraviolet
VSWR	Voltage standing wave ratio

List of Symbols

A_d	Drain-line attenuation
A_g	Gate-line attenuation
C	Capacitor
c	Velocity of light in free space, which is 2.998×10^8 m/s
C_a, C_b, C_c	Fringing capacitance
C_{ds}	Drain-source capacitance
C_{dsp}	Drain-source package capacitance
C_{fb}	Feedback capacitor
C_{gd}	Gate-drain capacitance
C_{gdp}	Gate-drain package capacitance
C_{gs}	Gate-source capacitance
C_{gsp}	Gate-source package capacitance
dB	Decibel
f_{max}	Maximum frequency of oscillation
f_t	Maximum cut-off frequency
f_T	Unity current gain frequency
G	Gain
GaAs	Gallium arsenide
$G_{crtssda}$	Available power gain of the CRTSSDA
GHz	Gigahertz
g_m	Transconductance
h_d	Depletion-layer depth
I_{ds}	Drain-source current
I_{dss}	Drain-source saturated current
I_{dssm}	Maximum drain-source saturated current

K	Stability factor
KHz	Kilohertz
L	Inductor
L_d	Drain inductance
L_{fb}	Feedback inductor
L_g	Gate inductance
l_g	Gate length
L_s	Source inductance
MHz	Megahertz
P_{dc}	dc power consumption
P_o	Output power
R	Resistor
R_d	Drain resistance
R_{ds}	Drain-source resistance
R_{fb}	Feedback resistor
R_g	Gate resistance
R_i	Gate-source resistance
R_s	Source resistance
S_{11} (dB)	Input return loss
S_{12} (dB)	Reverse transmission (isolation)
S_{21} (dB)	Forward transmission (gain or insertion loss)
S_{22} (dB)	Output return loss
V_{gdb}	Gate-drain breakdown voltage
V_{ds}	Drain-source voltage
V_{gs}	Gate-source voltage
V_k	Knee voltage
V_p	Pinch-off voltage
V_ϕ	Forward gate-source voltage
Z	Impedance
Z_o	Characteristic impedance
Z_{od}	Drain characteristic impedance
Z_{og}	Gate characteristic impedance

Z_{opt}	Optimum load impedance
β	Phase constant
δ	Skin depth
ϵ_{eff}	Effective dielectric constant
ϵ_r	Dielectric constant
ϵ_s	Semiconductor dielectric constant
λ	Wavelength in free space
λ_g	Guide wavelength
μ	Permeability of air
σ	Conductivity
τ	Electrical delay
v_{sat}	Saturated carrier velocity
ω_c	Cut-off angular frequency

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