"Heaven's Light is Our Guide"

Rajshahi University of Engineering & Technology, Rajshahi

Lab Report

Department of Electrical & Computer Engineering (ECE-22)

Course Code: ECE - 2112
Course Title(Sessional): Digital Techniques

Experiment Name: Design and implement a Programmable Logic Array (PLA) using basic logic gates in the Deeds Digital Circuit Simulator (Deeds-DcS).

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Experiment no. : 06
Experiment name: Design a mod-12 synchronous counter using T flip-flop.

Theory : A synchronous counter is a type of sequential circuit where all flip-flops are triggered simultaneously by a common clock signal. This simultaneous activation eliminates the ripple effect seen in asynchronous counters, leading to faster and more reliable operation with minimal propagation delay. Because all flip-flops transition at the same time, synchronous counters provide better timing accuracy and can operate at higher frequencies than their asynchronous counterparts.

A MOD-12 counter is a digital counter that counts from 0 to 11 (a total of 12 unique states in decimal), and then resets to 0, repeating the cycle. Such counters are commonly used in digital clocks, timers, and frequency dividers, where specific counting ranges are required.

Since a MOD-12 counter requires 12 unique states, and 2^4 = 16, we use 4 flip-flops to represent the states in binary form. This results in 4 unused (invalid) states — from decimal 12 to 15 — which must be handled appropriately (either by self-correction logic or by resetting the counter) to maintain reliable operation within the desired range.

State diagram:

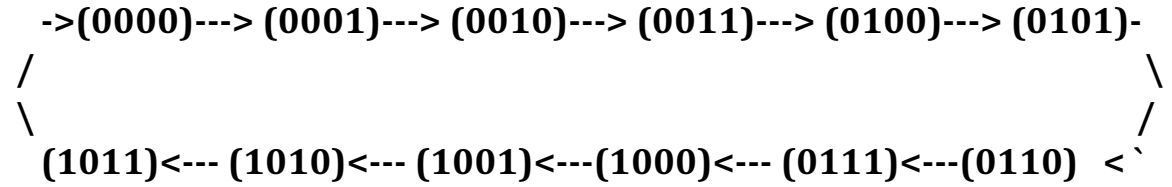

Fig. MOD-12

Truth table(T):

Q	**Qn**	**T**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Truth table:

[Present state] [Next state] ---> [T Flip-Flop]

Q8	Q4	Q2	Q1	Q8n	Q4n	Q2n	Q1n	--->	T8	T4	T2	T1
0	0	0	0	0	0	0	1	--->	0	0	0	1
0	0	0	1	0	0	1	0	--->	0	0	1	1
0	0	1	0	0	0	1	1	--->	0	0	0	1
0	0	1	1	0	1	0	0	--->	0	1	1	1
0	1	0	0	0	1	0	1	--->	0	0	0	1
0	1	0	1	0	1	1	0	--->	0	0	1	1
0	1	1	0	0	1	1	1	--->	0	0	0	1
0	1	1	1	1	0	0	0	--->	1	1	1	1
1	0	0	0	1	0	0	1	--->	0	0	0	1
1	0	0	1	1	0	1	0	--->	0	0	1	1
1	0	1	0	1	0	1	1	--->	0	0	1	1
1	0	1	1	0	0	0	0	--->	1	0	1	1

T1 =1

T2 =Q1

T4 =Q1.Q2.Q8’

T8 =Q1.Q2(Q4+Q8)

Circuit diagram:

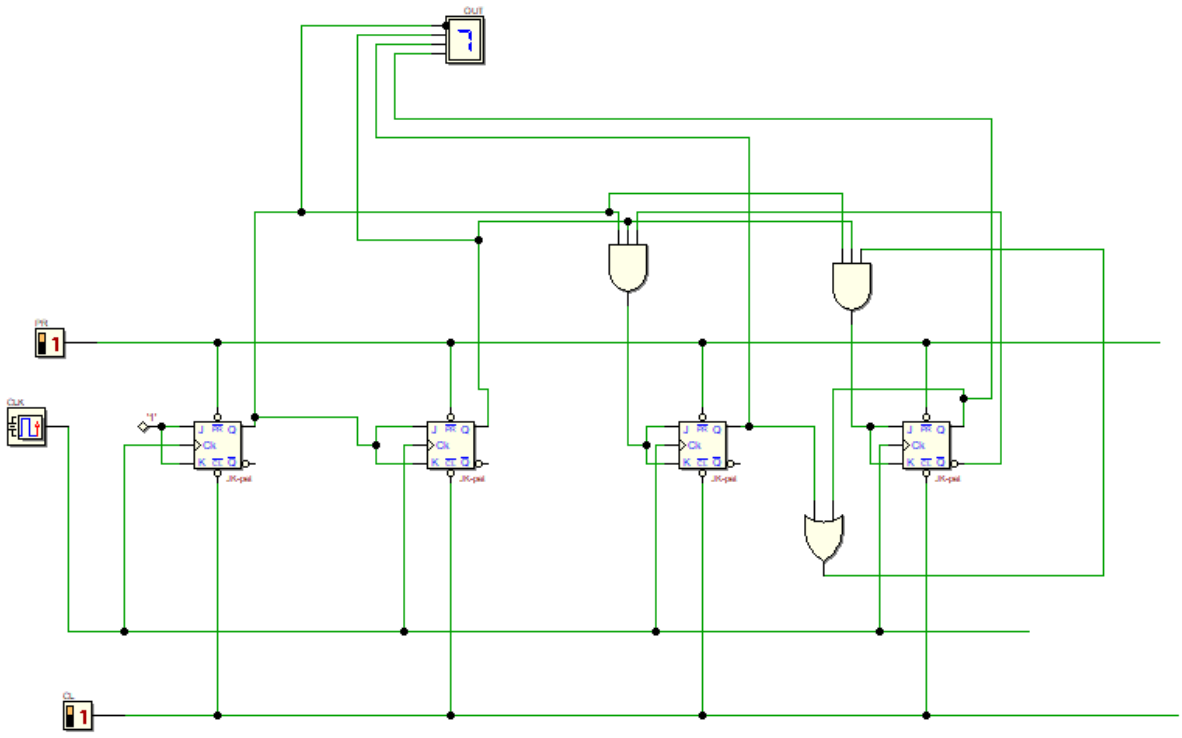

Fig. MOD-12 synchronous up counter

Discussion: In this design, we implement a MOD-12 synchronous counter using T (Toggle) flip-flops. The T flip-flop changes (toggles) its output state when the T input is high (1) on the triggering edge of the clock, and holds its state when T is low (0). By determining appropriate logic expressions for each T input based on the current state and desired next state, the counter is configured to progress through the 12-state sequence accurately.