"Heaven's Light is Our Guide"

Rajshahi University of Engineering & Technology, Rajshahi

Lab Report

Department of Electrical & Computer Engineering (ECE-22)

Course Code: ECE - 2112
Course Title(Sessional): Digital Techniques

Experiment Name: Design and implement a Programmable Logic Array (PLA) using basic logic gates in the Deeds Digital Circuit Simulator (Deeds-DcS).

Date of Submission: 01-05-2025

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Experiment no. : 06
Experiment name: Design a synchronous counter that has given counting sequence 1,3,5,7.....(Repeat).

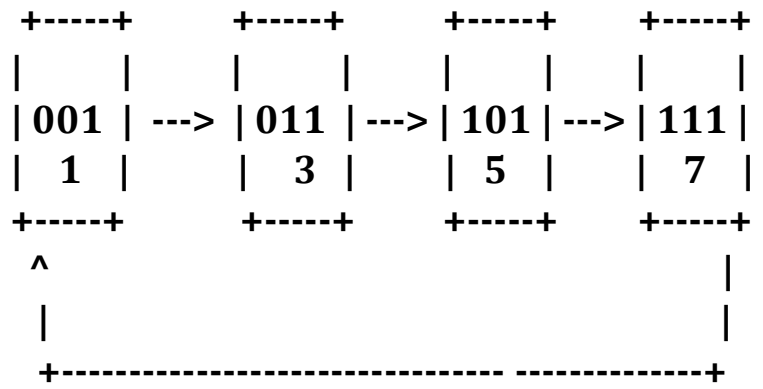
Theory : A synchronous counter is a type of digital counter in which all flip-flops are triggered simultaneously by a common clock signal. Unlike asynchronous counters (or ripple counters), synchronous counters eliminate the delay caused by the propagation of the clock signal through multiple stages.In this lab, we aim to design a 3-bit synchronous binary counter that follows an odd-counting sequence:

1 (001), 3 (011), 5 (101), 7 (111) and repeats back to 1.

This sequence involves only the odd numbers within a 3-bit binary range. The sequence is cyclic and skips even numbers (000, 010, 100, 110).

The number of flip-flop required is 3 .

State diagram:



Truth table(D):

Q	Qn	D
0	0	0
0	1	1
1	0	0
1	1	1

Truth table:

[Present state] [Next state] ------>[D Flip-Flop]

Q4	Q2	Q1	Q4n	Q2n	Q1n	---->	D4	D2	D1
0	0	1	0	1	1	---->	0	1	1
0	1	1	1	0	1	---->	1	0	1
1	0	1	1	1	1	---->	1	1	1
1	1	1	0	0	1	---->	0	0	1

D1 = 1
D2 = Q2’
D4 = Q2’.Q4 + Q2.Q4’

Circuit diagram:

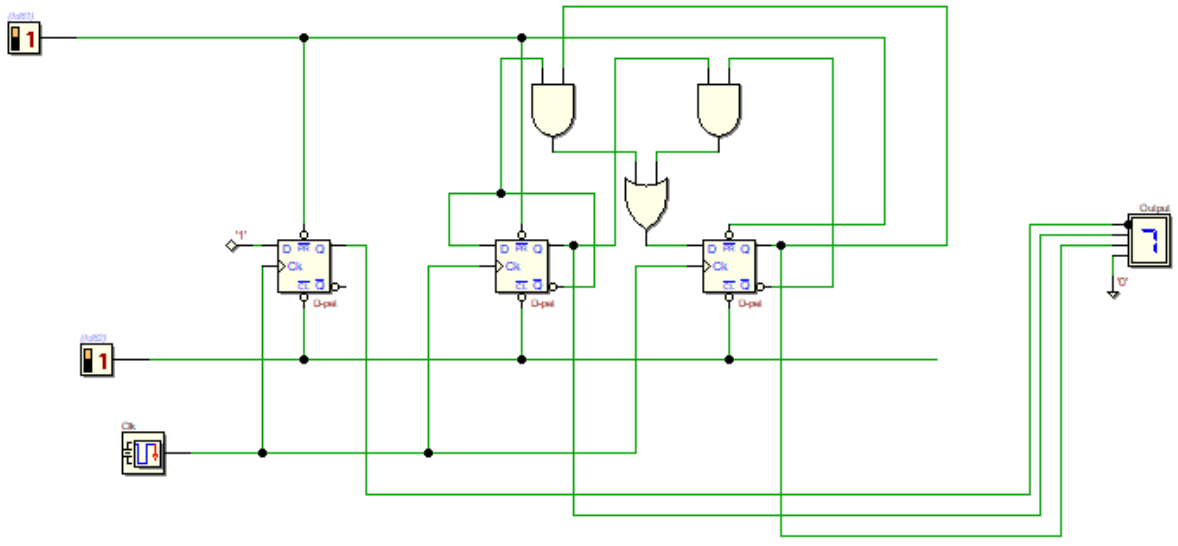


Fig. Synchronous up counter (Using D flip-flop)

Discussion: This synchronous counter design demonstrates the practical application of sequential circuit theory using D flip-flops . It effectively cycles through a custom-defined sequence of odd numbers (1, 3, 5, 7) and resets correctly, making it suitable for use in digital systems requiring such specific behaviour.