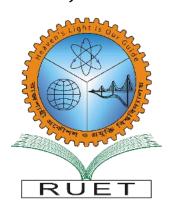
## "Heaven's Light is Our Guide"

## Rajshahi University of Engineering & Technology, Rajshahi



Lab Report

# Department of Electrical & Computer Engineering (ECE-22)

Course Code: ECE - 2112

Course Title(Sessional): Digital Techniques

Experiment Name: Design and implement a Programmable Logic Array (PLA) using basic logic gates in the Deeds Digital Circuit Simulator (Deeds-DcS).

Date of Experiment: 17-02-2025 Date of Submission: 21-04-2025

Submitted To Submitted By

Md. Omaer Faruq Goni Name: Sanumong Marma

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Dept. Of Electrical & Computer Reg. No: 1115

Engineering Session:2022-23

#### **Experiment no.:** 05

**Experiment name:** Design and implement a Programmable Logic Array (PLA) using basic logic gates in the Deeds Digital Circuit Simulator (Deeds-DcS).

**Theory:** A Programmable Logic Array (PLA) is a type of programmable logic device used to implement combinational logic circuits. It consists of a programmable array of AND gates followed by a programmable array of OR gates, allowing users to define custom logic functions. Unlike fixed-function circuits, PLAs are not configured during manufacturing; instead, they are programmed by the user before deployment.

PLAs are capable of performing a wide range of logical operations and often include memory features that support flexible configurations. This makes them suitable for reconfigurable digital circuit design, enabling the creation of application-specific hardware solutions. Their versatility lies in their ability to implement multiple logic functions, making PLAs valuable in areas that require customizable and efficient logic design.

#### **Block diagram:**

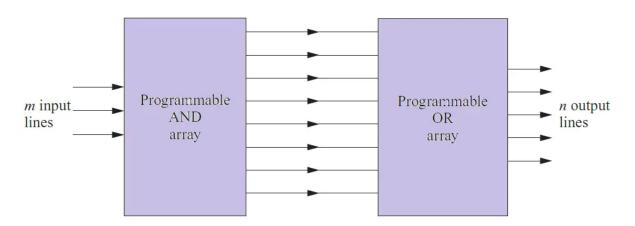


Fig. PLA

### Truth table:

A	В	С	F1	F2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

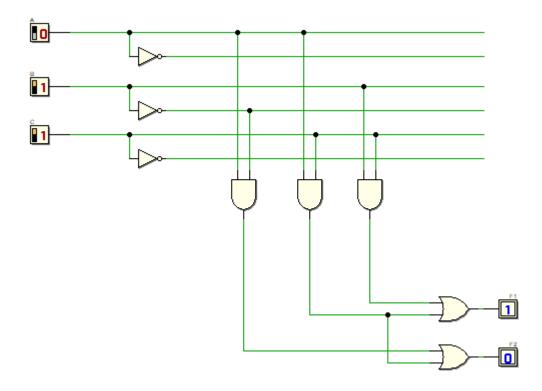
F1 = AB'C' + ABC' + ABC

By simplifying, F1 = AB + AC'

F2 = A'BC + AB'C + ABC

By simplifying, F2 = BC + AC

## Circuit diagram:



**Discussion:** PLA is used for the implementation of various combinational circuits using a buffer, AND gate, and OR gate. In PLA, all the minterms are not realized but only required minterms are implemented. As PLA has a programmable AND gate array and a programmable OR gate array, it provides more flexibility but the disadvantage is, it is not easy to use.