

Lab final project report

ELCE 202

Team members:

Sanzhar Yergaliyev, Id: 201894694

Abzal Aidakhmetov, Id: 201726640

Rauan Toilybayev, Id: 201740372

Date: 05.12.20

Contribution

Sanzhar

Module names: Key expansion, (inverse) Mix columns, Encryption, Decryption.

Abzal

Module names: (inverse) Shift rows, Test bench.

Rauan

Module names: (inverse) Byte substitution.

Peripherral work: Report

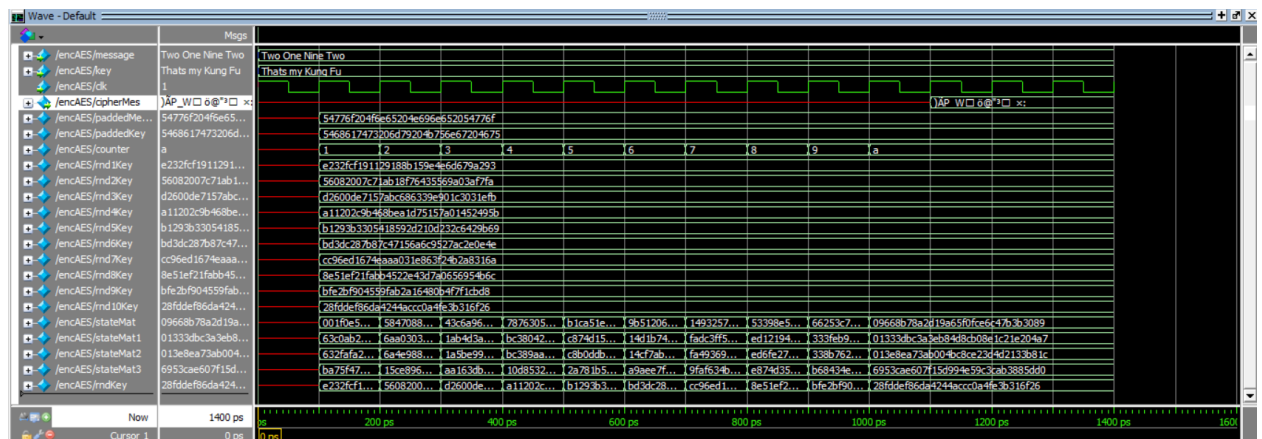
Implemented protion of project

Every part of 128 bit encryption and decryption is implemented.

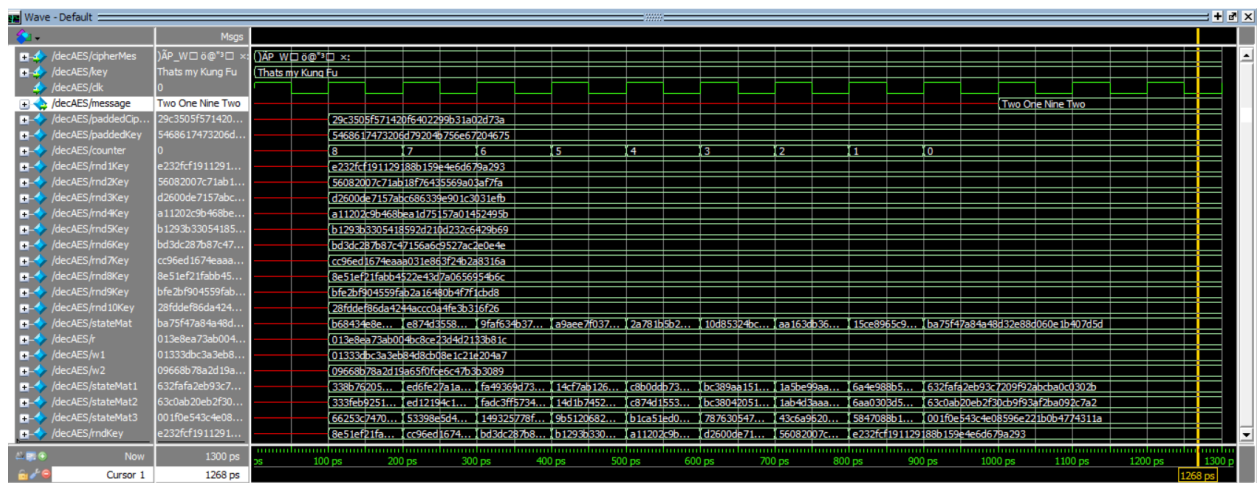
But we lack a block wise divider logic that allows to input larger than 128 bit messages and cipher texts. So the input is bounded by 128 bits.

Screen shots of simulation

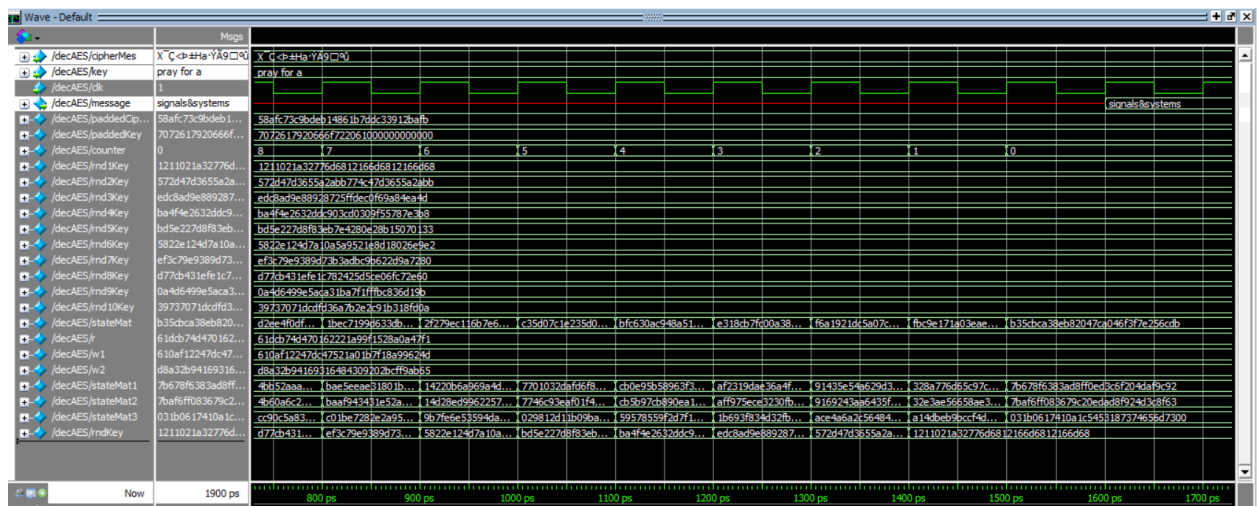
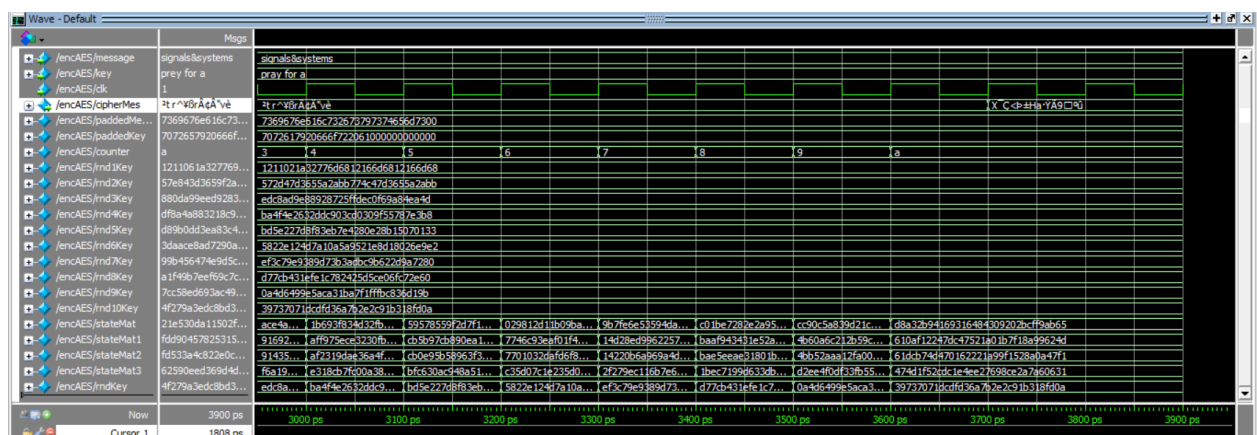
Simulation of encryption of the provided example:



Simulation of decryption of the provided example:



Simulation of encryption and decryption of a generic input:



Features

- Sub modules are all **combinational**.
- Encryption, decryption modules are **sequential**.
- Inputs could be processed only if there are **even** number of hexadecimal characters.
- It takes 12 clock cycles for encryption and 11 clock cycles for decryption to output the result. Assuming inputs are exactly 128 bit long.
- Zero padding may take at max 15 additional clock cycles.