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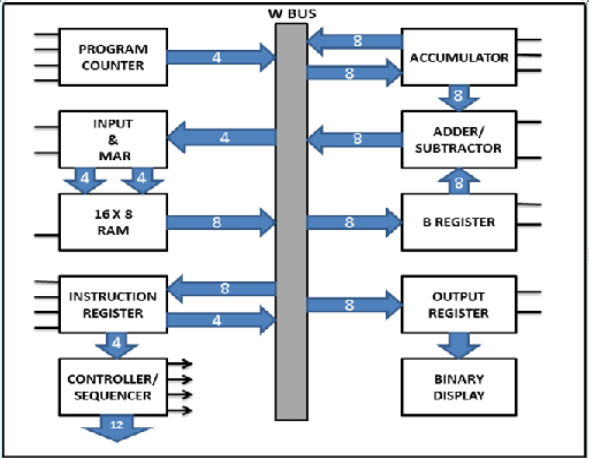
Section : ”A”

Assignment: 1

***Introduction SAP(Simple As Possible) :***

The SAP (Simple-As-Possible) computer has been designed for beginners. The main purpose of SAP is to introduce all the crucial ideas behind computer operation without burying you in unnecessary detail. SAP-1 is the first stage in the evolution toward modern computers. SAP-1 is a big step for beginners.

# *SAP-1 architecture :*



1. ***Program Counter :***

The program is stored at the beginning of the memory with the first instruction at binary address 0000, the second instruction at 0001 and so on. The program counter which is part of the control unit, counts from 0000 to 1111. Its job is to send to the memory the address of the next instruction to be fetched and executed

      The program counter is reset to 0000 before each computer run. When the computer run begins, the program counter sends the address 0000 to the memory. The program counter is then incremented to get 0001. After the first instruction is fetched and executed, the program counter sends address 0001 to the memory. Again the program counter is incremented. After the second instruction is fetched and executed, the program counter sends address 0010 to the memory. So this way, the program counter keeps track of the next instruction to be fetched and executed.

***2. Input & MAR :***

The Input and MAR includes the address and data switch registers. Switch registers are part of input unit, allows us to send 4 address bits and 8 data bits to the RAM.

The memory address register (MAR) is the part of SAP-1 memory. During a computer run, the address in the program counter is latched in to the MAR. A bit later, the MAR applies this 4-bit address to the RAM where a read operation is performed.

***3.The RAM :***

The RAM is a 16 X 8 static TTL RAM. We can program the RAM by means of the address and data switch registers. This allows you to store a program and data in the memory before a computer run.

During a computer run, the RAM receives 4-bit addresses from the MAR and a read operation is performed. In this way, the instruction or data word stored in the RAM is placed on the W bus for use in some other part of the computer.

***4.******Instruction Register :***

The instruction register is the part of the control unit. To fetch an instruction from the memory the computer does a memory read operation. This places the contents of the addressed memory location on the W bus. At the same time, the instruction register is set up for loading on the next positive clock edge. The content of the instruction register are split into two nibbles. The upper nibble goes directly to the block “Controller – Sequencer”. The lower nibble is read onto the W bus when needed.

***5.Controller – Sequencer :***

Before each computer runs, a CLR signal is sent to the program counter and CLK signal to the instruction register. This resets the program counter to 0000 and wipes out the last instruction in the instruction register.

      A clock signal CLK is sent to all buffer registers; this synchronizes the operation of the computer ensuring that things happen when they are supposed to happen.

      The 12 bits that come out of the controller sequencer form a word controlling the rest of the computer (like a supervisor telling others what to do). The 12 wires carrying the control word are called the control bus. The control word has the format of: CON = CPEPLMCE   L1E1LA EA   SUEULBLO

      This word determines how the registers will wait to the next positive CLK edge. For example, a high EPand a low LM means that the program counter are latched into the MAR on the next positive clock edge. As another example, a low CE and a low LA means that the addressed RAM word will be transferred to the accumulator.

***6.Accumulator :***

The accumulator (A) is a buffer register that stores intermediate answers during a computer run. Accumulator has two outputs, one directly goes to the adder-subtractor and the other goes to the W bus.

***7.The Adder – Subtractor :***

SAP-1 uses a 2’s complement adder-subtractor. When SU is low, the sum out of the adder-subtractor is S = A + B. When SU is high, the difference appears as A = A + B ’.

***8. B Register :***

The B register is another buffer register. It is used in arithmetic operations. A low LB and positive clock edge load the word on the W bus into the B register. The two state output of the B register drives the adder-subtractor, supplying the number to be added or subtracted from the content of the accumulator.

***9.******Output Register :***

At the end of the computer run, the accumulator contains the answer to the problem being solved. At this point, we need to transfer the answer to the outside world. This is where the output register is used.

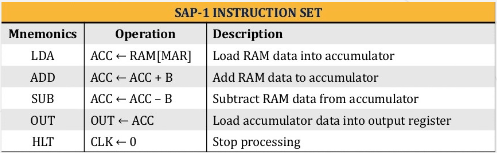
      When EA is high and LO is low, the next positive clock edge loads the accumulator content to the output register. The output register is often called an output port because the processed data can leave the computer through this register.

***10.******Binary Display :***

The binary display is a row of eight light emitting diodes (LED’s). Because each LED connects to one flip-flop of the output port, the binary display shows us the content of the output port. Therefore, after we transferred an answer from the accumulator to the output port, we can see the answer in binary form.

***SAP-1 INSTRUCTION SET:***

This means loading step-by-step instruction into the memory before the start of computer run. Before you can program a computer, however, you must learn its instruction set, the basic operations it can perform.it is shown in fig.



***LDA Instruction:***

LDA stands for ”load the Accumulator”. A complete LDA instruction includes the hexadecimal address of the data to be loaded.

For example, LDA 8H means ”Load the accumulator with the contents of memory location 8H”.

Therefore given, RAM[8]= 1111 0000.The execution of LDA 8H results in ACC = 1111 0000

***ADD Instruction:***

ADD 9H means “add the data of memory location 9H with data of accumulator and save the result in accumulator”.

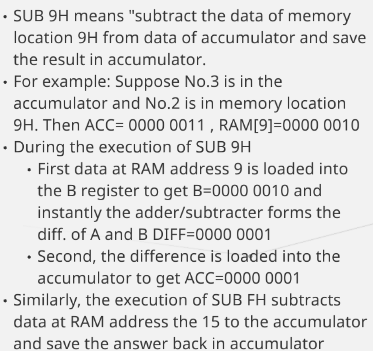
For example : Suppose No.2 is in the accumulator and No.3 is in memory location 9H. Then ACC = 0000 0010 , RAM[9]=0000 0011

During the execution of add 9H

* First data at RAM address 9 is loaded into the B register to get B= 0000 0011 and instantly the adder/sub forms the sum A and B SUM == 0000 0101.
* Second, this sum is loaded into the accumulator to get ACC= 0000 0011

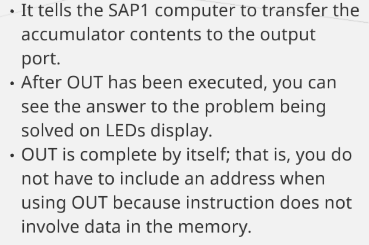
Similarly, the execution of ADD FH adds data at RAM address the 15 to the accumulator and save the answer back in accumulator overwriting the previous value.

***SUB Instruction:***

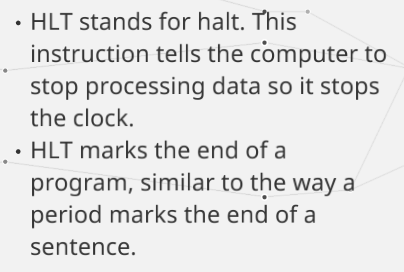




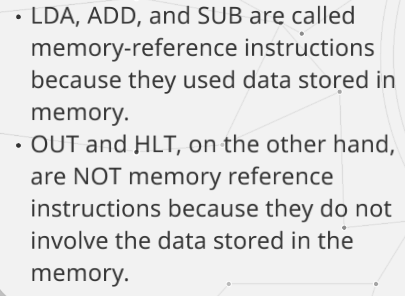
***OUT Instruction:***



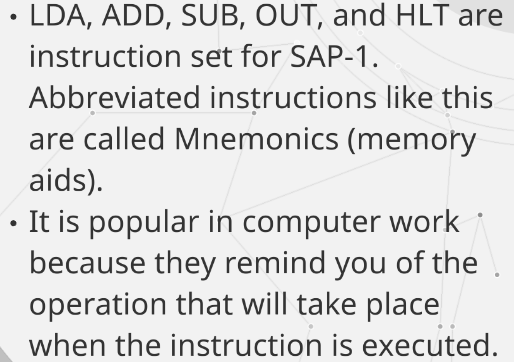
***HLT Instruction :***



***Memory Reference Instructions:***



***Mnemonics :***



***RAM :***

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