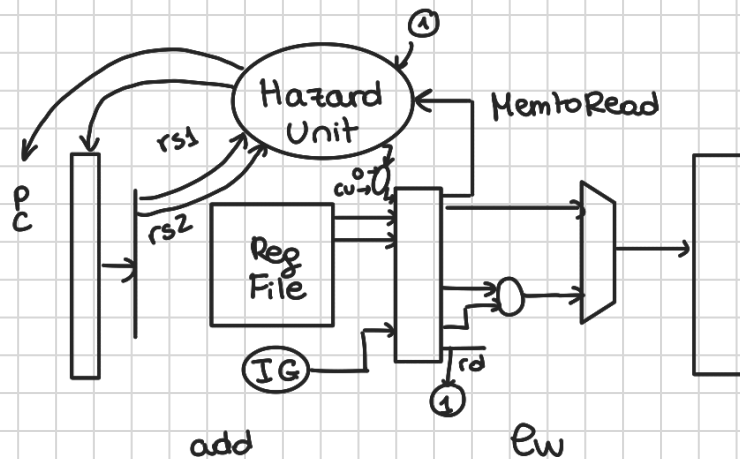


CONTROL HAZARDS

lw x6, 0(x7)
add x8, x8, x6



Hazard Unit → to detect the hazard

So, for this case, we need to know:

- rs1
- rs2
- MemtoRead
- rd from lw stage

LOGIC BEHIND

if $ID/EX. MemRead$ and $(ID/EX.rd = IF/ID.rs1$
or $ID/EX.rd = IF/ID.rs2)$
stall the pipeline.

A **false positive** will introduce a bubble even if it's not needed

- if x6 = 0
- this **hazard unit** can detect if an instruction is a lw but it won't understand what's the next instruction which may cause it to introduce unnecessary bubble.

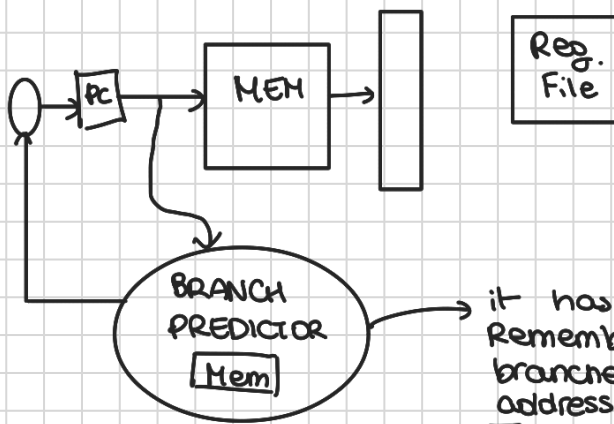
Ex. lw x6, 0(x7)
add x8, x8, imm

BRANCH PREDICTION

- this is done by the hardware



for $i = 1$ to 100000

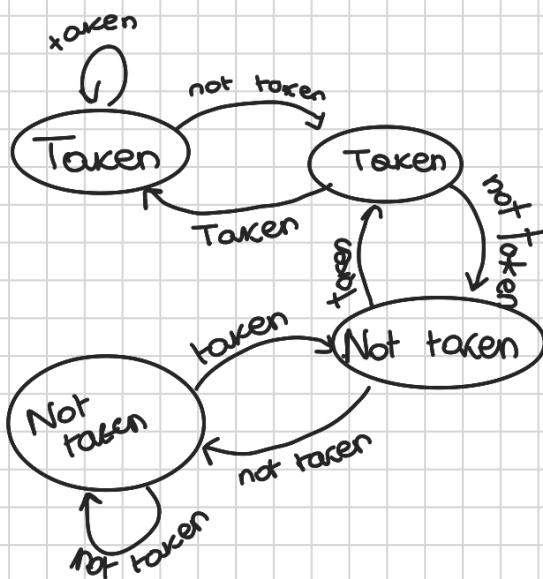
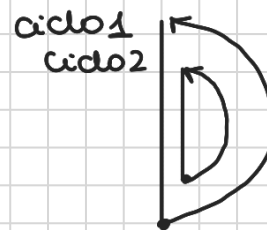


it has a small memory.
Remembers the previous
branches by storing their
address.
The result is also stored.

Usually you get the first
and last prediction wrong.

We lose one clock cycle by doing a wrong
prediction

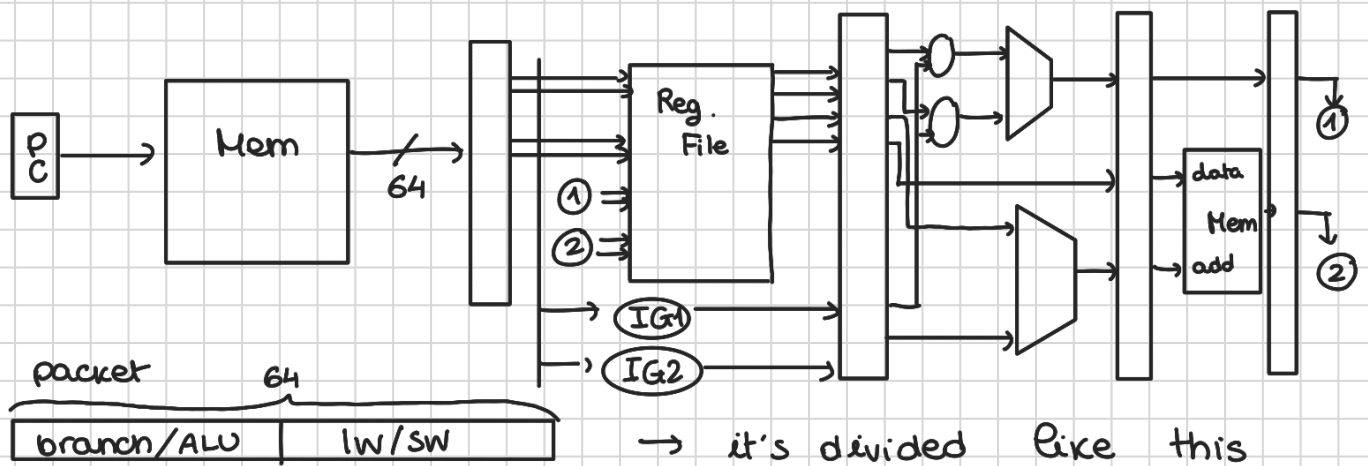
for $i = 1$ to 100000
for $j = 1$ to 4



MULTIPLE ISSUE

- static multiple issue

↳ you can't put any pair of instr.



load two instr. instead of one
(they are connected, packets)

PERFORMANCE

. data

x: .word
y: .word
z: .word
n: .word 100000

. text

```

lw t0, n
la t1, x
la t2, y
la t3, z
ciclo: 1 lw t4, 0(t1)
       2 lw t5, 0(t2)
       3 → 4 add t6, t5, t4
       5 sw t6, 0(t3)
       6 addi t1, t1, 4
       7 addi t2, t2, 4
       8 addi t3, t3, 4
       9 addi t0, t0, -1
      10 bne t0, zero, ciclo
      11 ↻
  
```

(3) instructions

① Single Clock Cycle 200MHz

9 clock cycles · 10⁶ = cycles

$$\frac{9 \cdot 10^6}{200 \cdot 10^6} = 0,045 \text{ s}$$

200 MHz
 1 MHz = 1Hz · 10⁶
 1 GHz = 1Hz · 10⁹

$$0,045 \text{ s} \cdot 10^3 = 45 \text{ ms}$$

1ms = 10⁶ ns → 45 · 10⁶ ns *

② Pipeline arch. 1GHz

(no branch pred.)

$$11 \cdot 10^6 \text{ ns} = 11 \text{ ms}$$

↑ since there's no branch prediction it will load the next instruction

③ Pipeline arch 1GHz (branch predic.) (code re-ordering)

no bubble

$$\hookrightarrow 9 \cdot 10^6 \text{ ns} = 9 \text{ ms}$$

(we don't have hazard unit ↓)

ALU/BRANCH	LW/SW
ciclo: addi t1, t1, 4	lw t4, 0(t1)
addi t2, t2, 4	lw t5, 4(t2)
addi t0, t0, -1	
add t6, t5, t4	
addi t3, t3, 4	sw t6, 0(t3)
bne t0, zero, ciclo	

④ Multiple issue arch 1GHz

(branch prediction)

6 loops

$$\downarrow 6 \cdot 10^6 \text{ ns} = 6 \text{ ms}$$

```

add, t0, t0, -2      lw t4, 0(t1)
add, t3, t3, 8        lw t5, 0(t2)
add, t1, t1, 8        lw t8, 4(t1)
add, t6, t4, t5        lw t9, 4(t2)
add, t2, t2, 8        sw t6, -8(t3)
add, t10, t8, t9
bne t0, zero, ciclo sw t10, -4(t3)

```

⑤

MULTIPLE ISSUE ARCH 1GHz

(Loop unrolling +
branch prediction)

reduces penalty branches

$$T_{ns} = 500 \cdot 10^3 = 3,5 \text{ ms}$$

*

Let's say it was 4GHz and not 200MHz.

$$1 \text{ GHz} = 1 \text{ Hz} \cdot 10^9 \text{ so}$$

$$\frac{9 \times 10^6}{4 \times 10^9}$$

$$= 0,00225$$

$$0,00225 \leftarrow s$$

$$\text{Ans} \times 10^3$$

$$2,25 \leftarrow ms$$