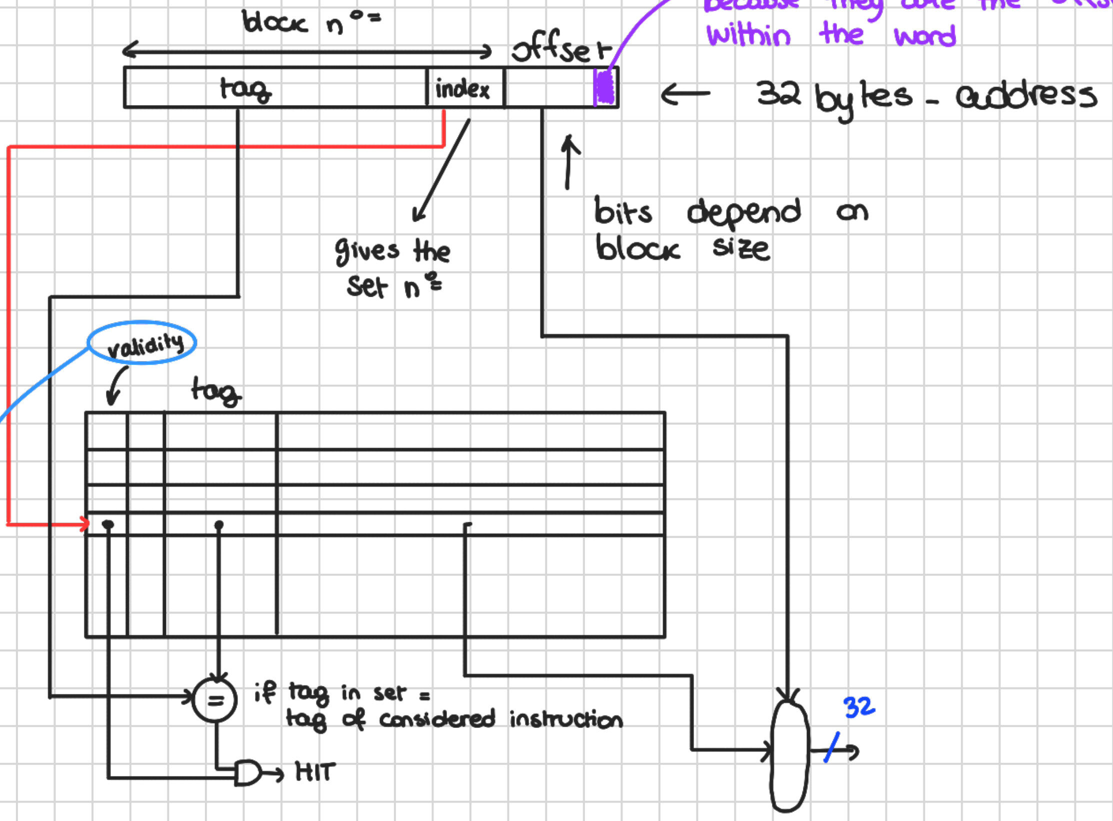
Comp. Arch DATE: 29/4/2022

CACHE

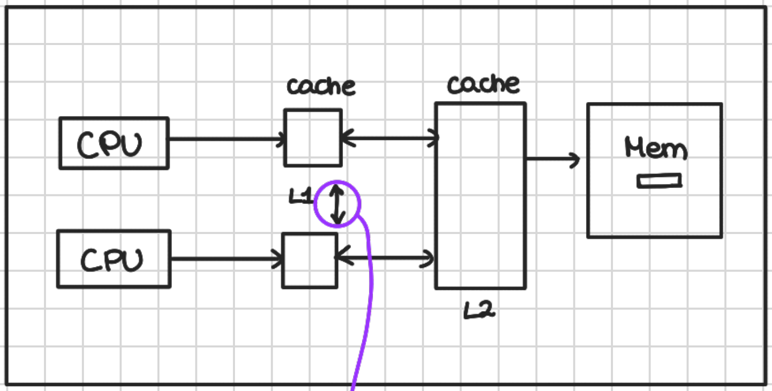
we don't need the last 2 bits because they are the offset within the word



We need one bit to determine if the block content is meaningful or if its empty. This is the "validity" part of the cache.

There is a hierarchy

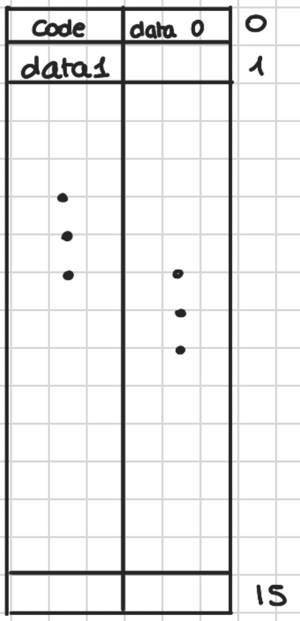
In your PC, you wiee have more than one cache and in modern types more than one CPU as well. (4 CPU - quad core). All of this is usually contained in one chip.



To solve conflicts, one solution is making the caches communicate with each other. If they share the same word, it propagates the updates
It is used in many IBM systems, specially NUMA control.
The other solution involves no talk between cache but more instructions to intercept on a software level.

EXERCISE (2- WAYS ASSOCIATIVE)

block size 64
2-way associative cache
n° sets = 16



. data

x: .word ________
n: .word 1024

. text

```
ciclo:  lw   t2, 0(t0)      1 + 1
        add  t3, t3, t2     3
        addi t0, t0, 4      4
        addi t1, t1, -1     5
        bne  t1, zero, ciclo  6
```

REMARK: when you have to replace a block, you discard the least recently used (LRU) block.
We need bits to do this.

To know how many instructions a block contains: $\longrightarrow$ $\frac{\text{block size}}{4} = \frac{64}{4} = 16$

one instr 4 words

Iteration 0 : 1 miss
6 memory accesses

" 1 : 0 miss
6 memory access

: // same

" 16 : 1 miss
6 memory access

" 17 : 0 miss
6 memory access

MISS RATE (of 1st block) $= \frac{1}{16 \cdot 6} = 1\%$ (1.01)

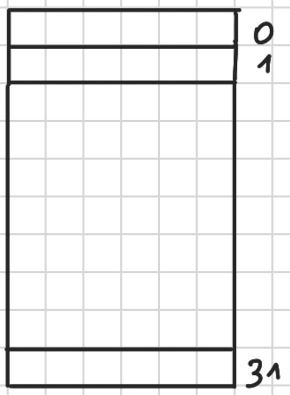
n° misses

iterations

memory access

EXERCISE (ONE-WAY ASSOCIATIVE)

block size 64
1-way associative cache
with 32 sets



. text

```
ciclo :   lw   t2 , 0(t0)
          add  t3 , t3,  t2
          addi t0 , t0,  4
          addi t1 , t1 , -1
          bne  t1, zero , ciclo
```

it 0	:	6	2	block 0
" 1	:	6	2	
it 2	:			
⋮				
it 15	:	6	2	
it 16	:	6	1	data 1
" 17	:	6	0	
⋮				
it 31	:	6	0	

n° block % n° sets

$1 \% 32 = 1$

$$\text{MISS RATE} = \frac{32 + 31(1)}{16 \cdot 6 + 31(16 \cdot 6)}$$

(or $32(16 \cdot 6)$)

n° of misses from iteration 16 to iteration 1023

n° of misses from iteration 0 to iteration 15

n° of sets

$$\frac{32 + 31}{32(16 \cdot 6)}$$