PWB, Artemis Plus

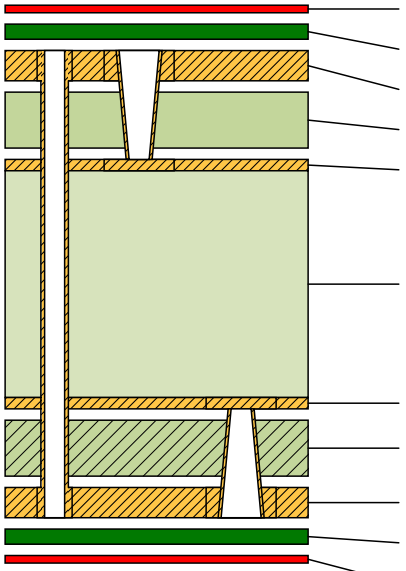
Rev: C

11/5/2023

Project: Artemis Plus		
Title: Cover Page		
Size: A	Number: 1011	Revision: C
Date: 11/5/2023 Time: 10:15 PM		Sheet: 1 of 17
File: Artemis_Plus-PWB .PCBDwf		

Stack up dimmensions can be adjusted as needed Desired thickness is to be a ~0.8mm.

Rigid Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.02mm(0.8mil)	Solder Resist	Solder Mask	GTS
Copper	**L1(Top)**	**0.04mm(1.6mil)**		**Signal**	**GTL**
Prepreg		*0.07mm(2.9mil)*	*FR-4*	*Dielectric*	
Copper	**L2**	**0.02mm(0.6mil)**		**Signal**	**G1**
Core		*0.57mm(22.4mil)*	*FR-4*	*Dielectric*	
Copper	**L3**	**0.02mm(0.6mil)**		**Signal**	**G2**
		0.07mm(2.9mil)	*FR-4*	*Dielectric*	
Copper	**L4(Bot)**	**0.04mm(1.6mil)**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.02mm(0.8mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.87mm(34.2mil)

1) IPC 6012 Class 2
2) ENIG Surface Finish
3) Green Soldermask / White Silkscreen
4) All through hole vias are to be filled with non-conductive epoxy, and copper capped (Type 7).
5) All microvias are to be copper filled.

Project: Artemis Plus		
Title: Layer Stack-up		
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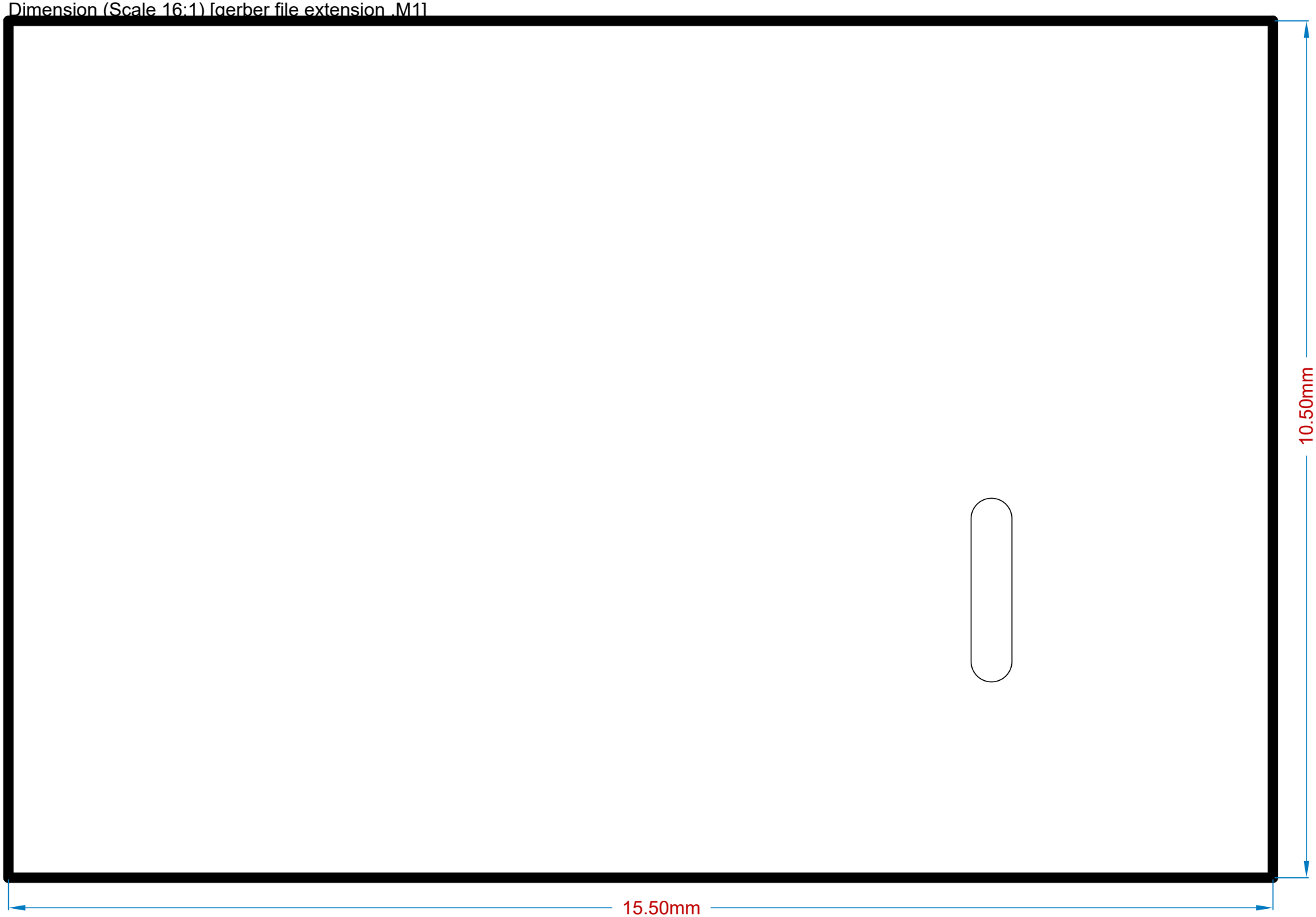
Dimension (Scale 16:1) [gerber file extension .M1]



Project: Artemis Plus		
Title: Board Outline		
Size: A	Number: 1011	Revision: C
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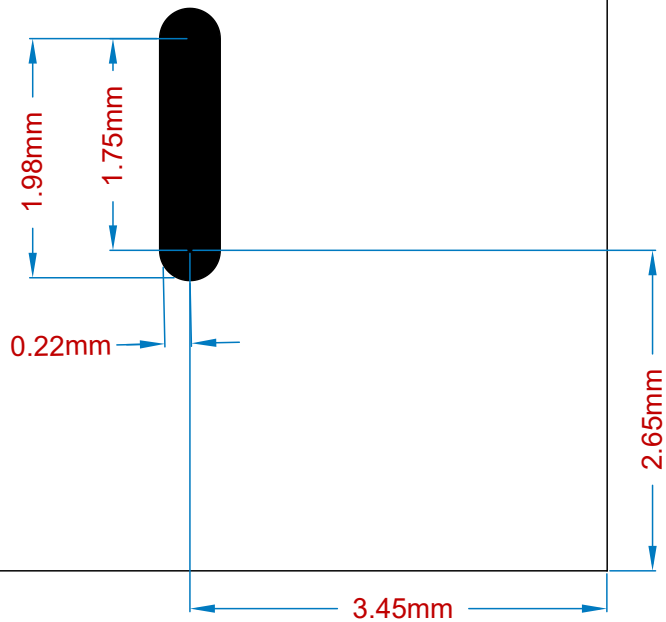
Route Tool Path (Scale 16:1) [gerber file extension .M2]



Project: Artemis Plus		
Title: Board Slot		
Size: A	Number: 1011	Revision: C
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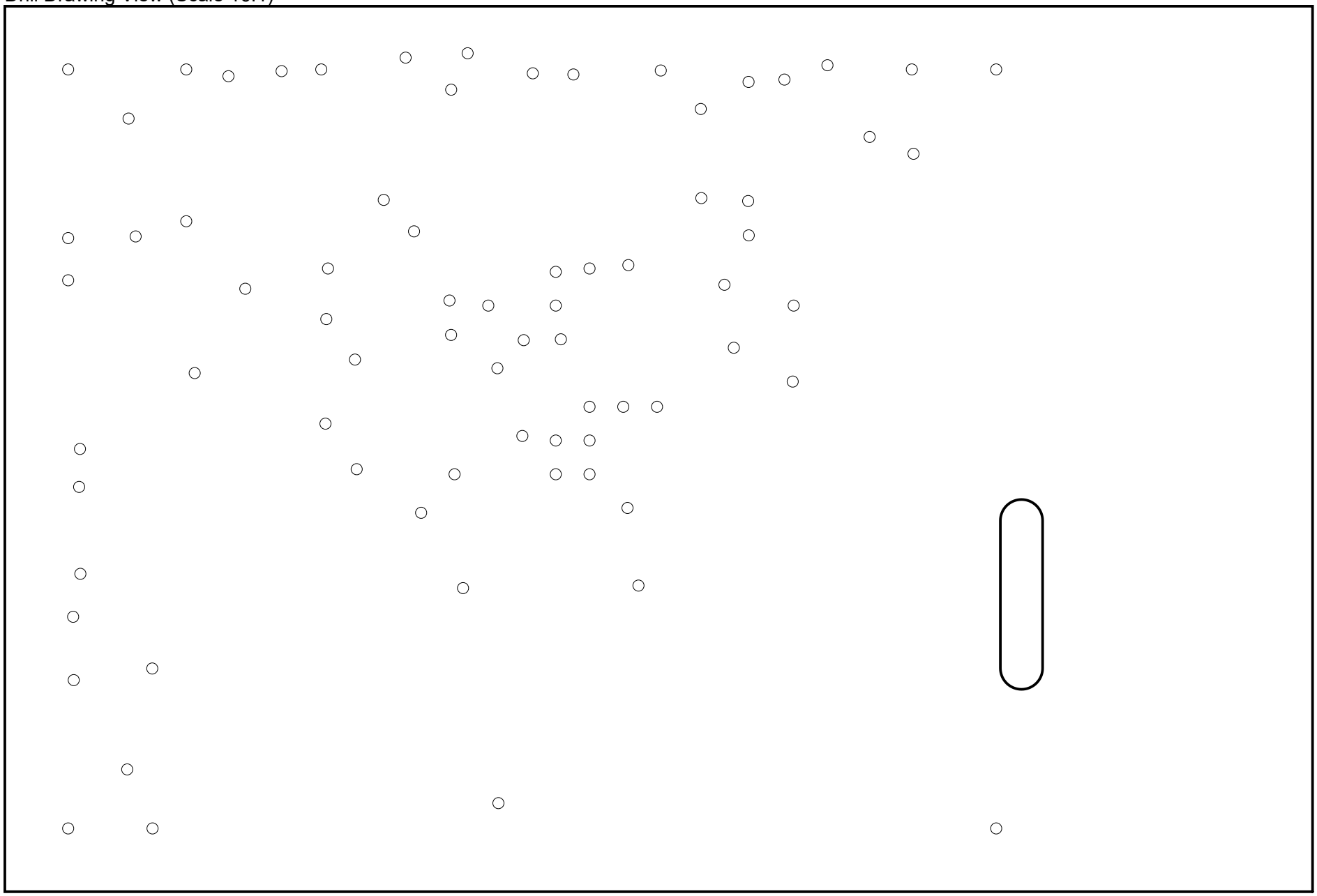
Drill Drawing View (Scale 16:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad	Via Type	Via Feature
○	74	0.15mm	Plated	Round	L1(Top) - L4(Bot)	Via	Type 7	Filling, Capping Both
	74 Total							

Project: Artemis Plus		
Title: Through Hole Drills		
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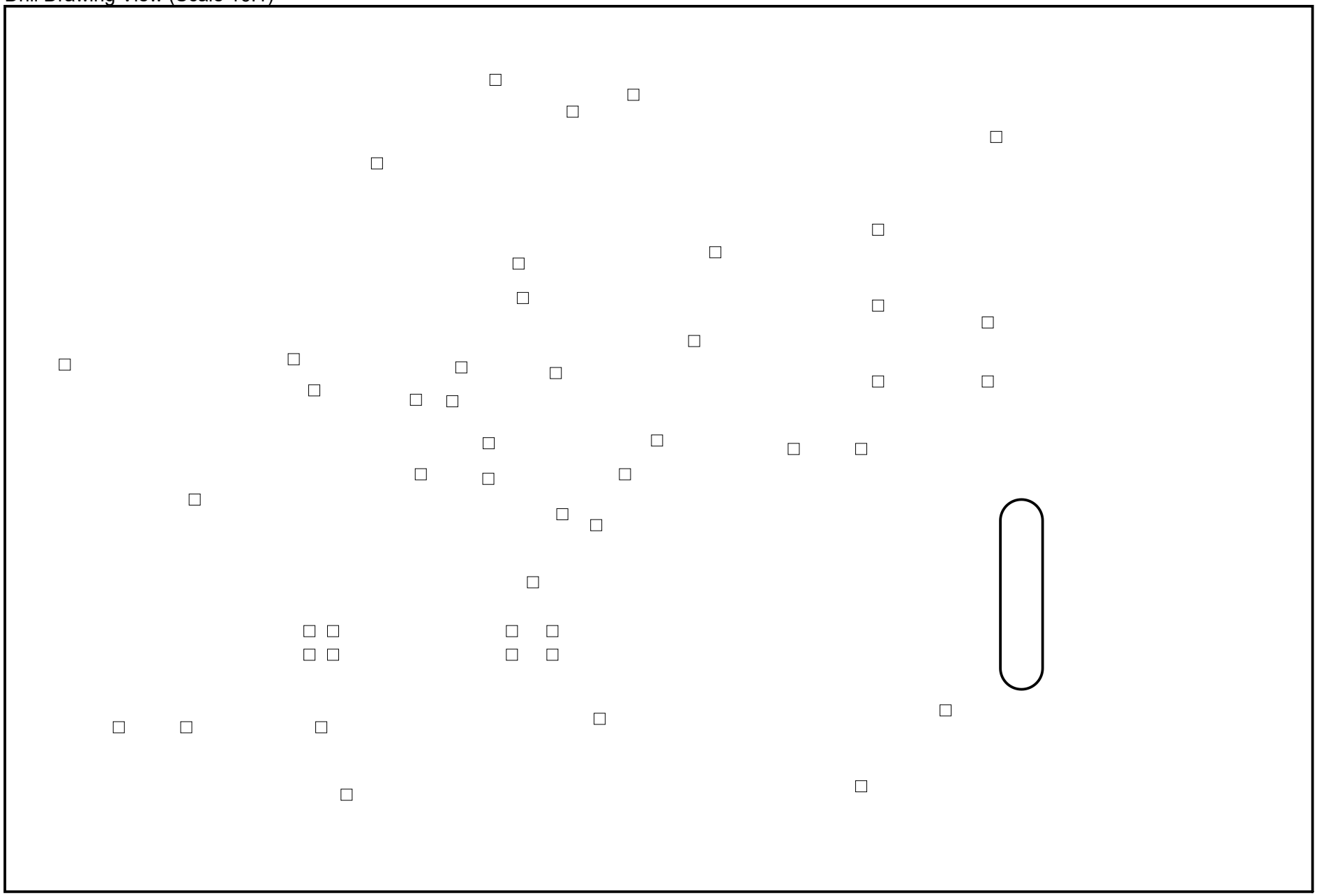
File: Artemis_Plus-PWB .PCBDwf		

Drill Drawing View (Scale 16:1)



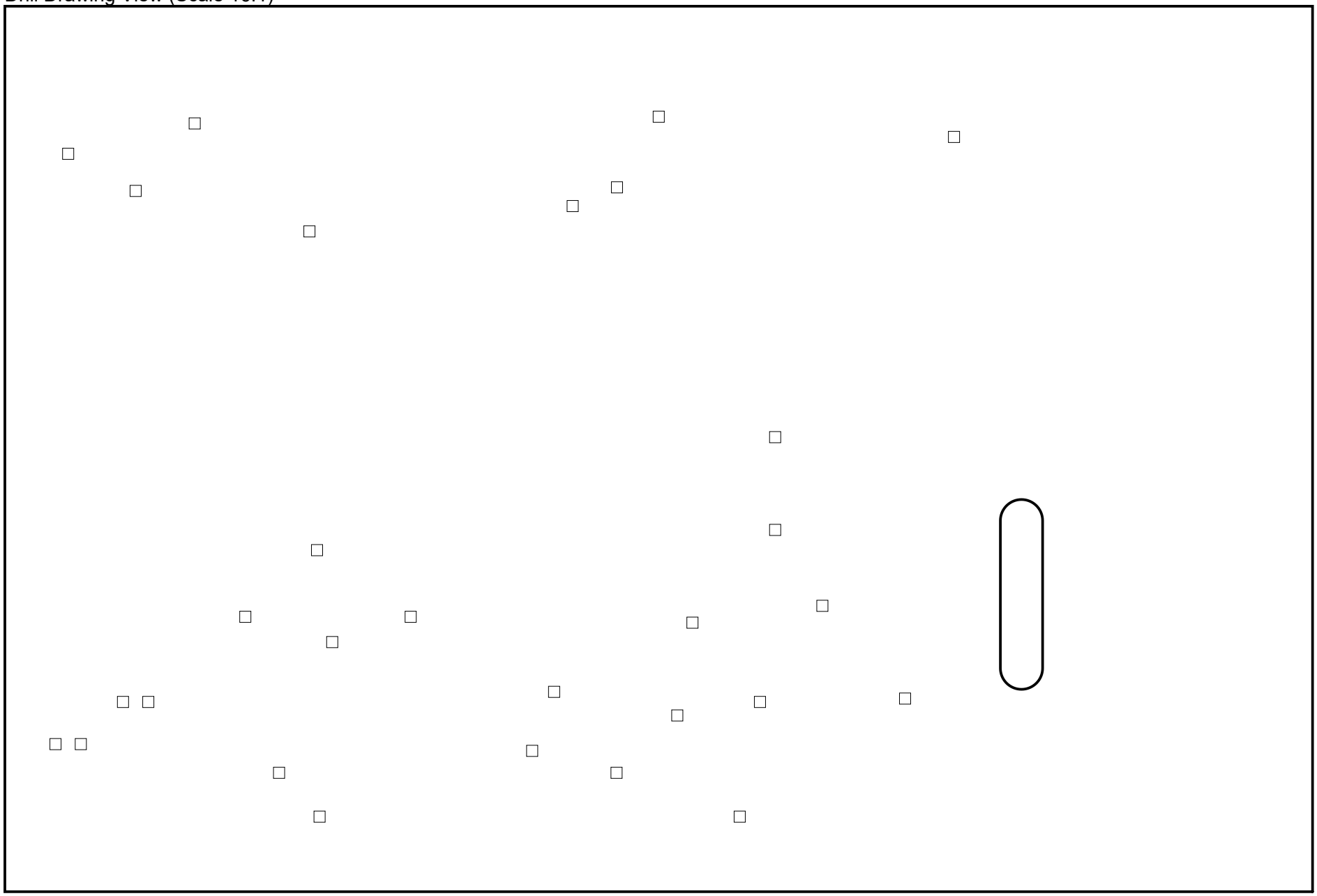
Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad
□	47	0.12mm	Plated	Round	[UVIA] L1(Top) - L2	Via
	47 Total					

All microvias are to be copper filled.

Project: Artemis Plus		
Title: L1(Top) to L2 Microvias		
Size: A	Number: 1011	Revision: C
Date: 11/5/2023 Time: 10:15 PM		Sheet: 6 of 17
File: Artemis_Plus-PWB .PCBDwf		

Drill Drawing View (Scale 16:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via / Pad
□	29	0.12mm	Plated	Round	[UVIA] L3 - L4(Bot)	Via
	29 Total					

All microvias are to be copper filled.

Project: Artemis Plus		
Title: L4(Bot) to L3 Microvias		
Size: A	Number: 1011	Revision: C
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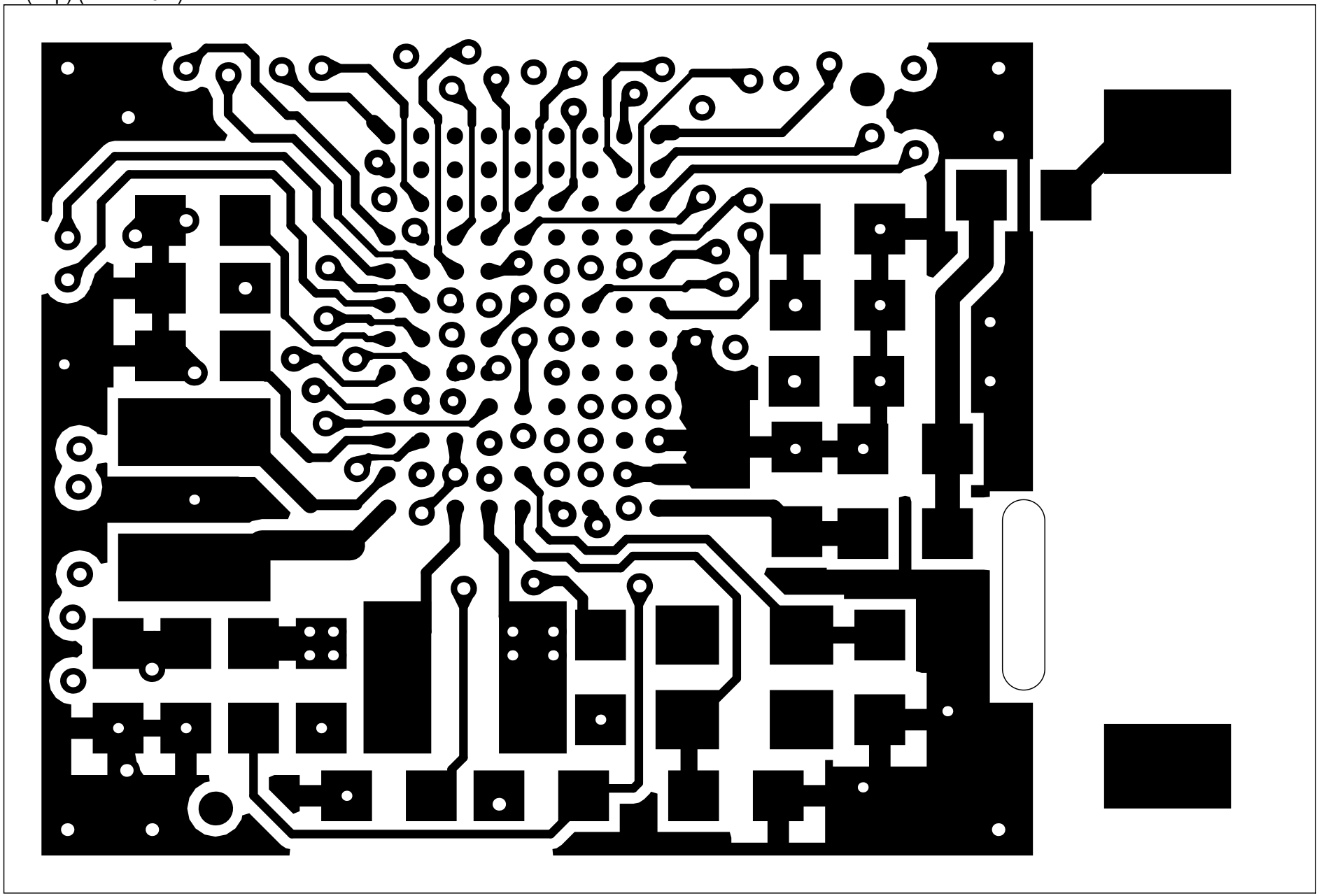
L1(Top) (Scale 16:1)



Project: Artemis Plus		
Title: L1 (Top) Copper		
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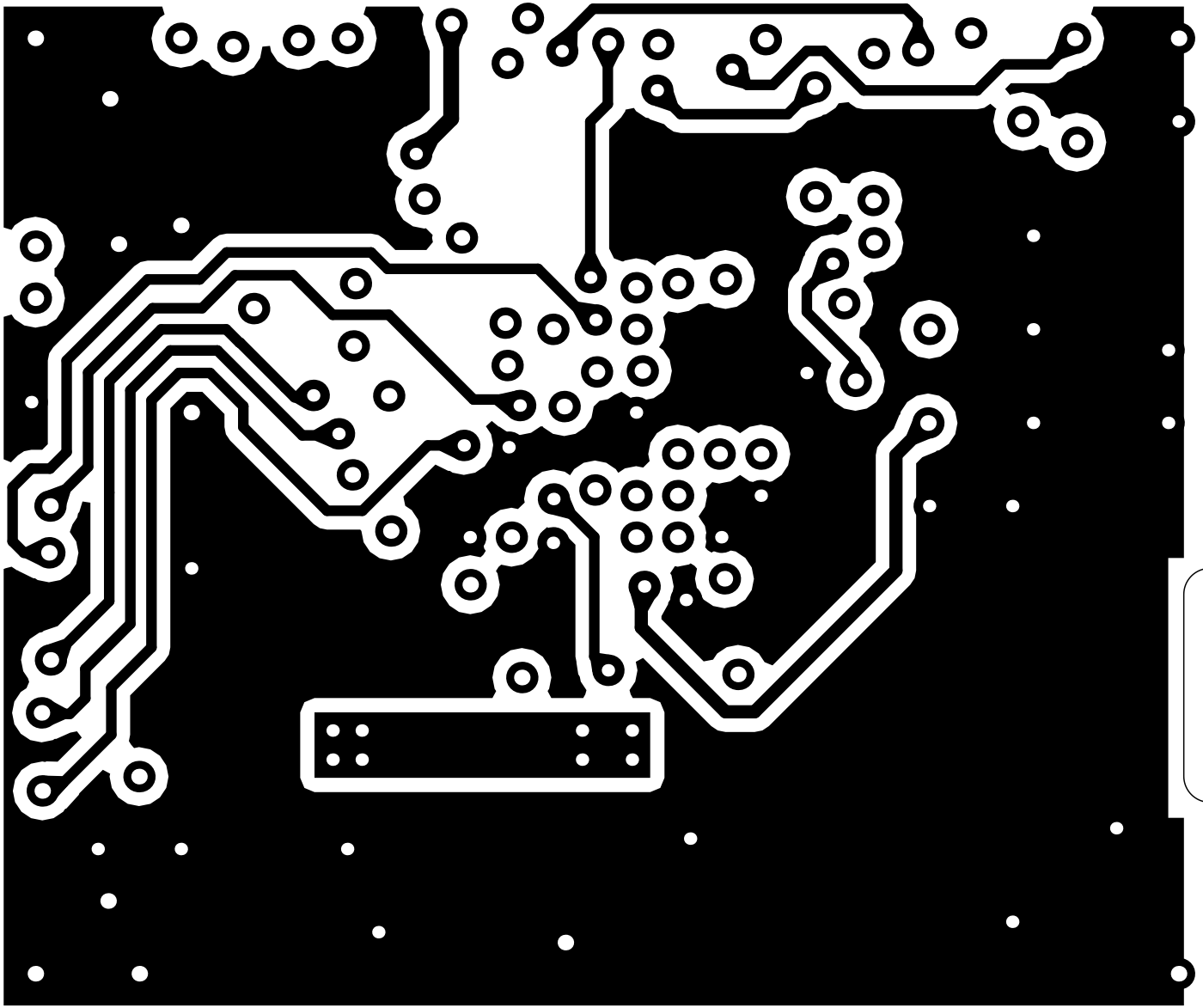
L2 (Scale 16:1)



Project: Artemis Plus		
Title: L2 Copper		
Size: A	Number: 1011	Revision: C
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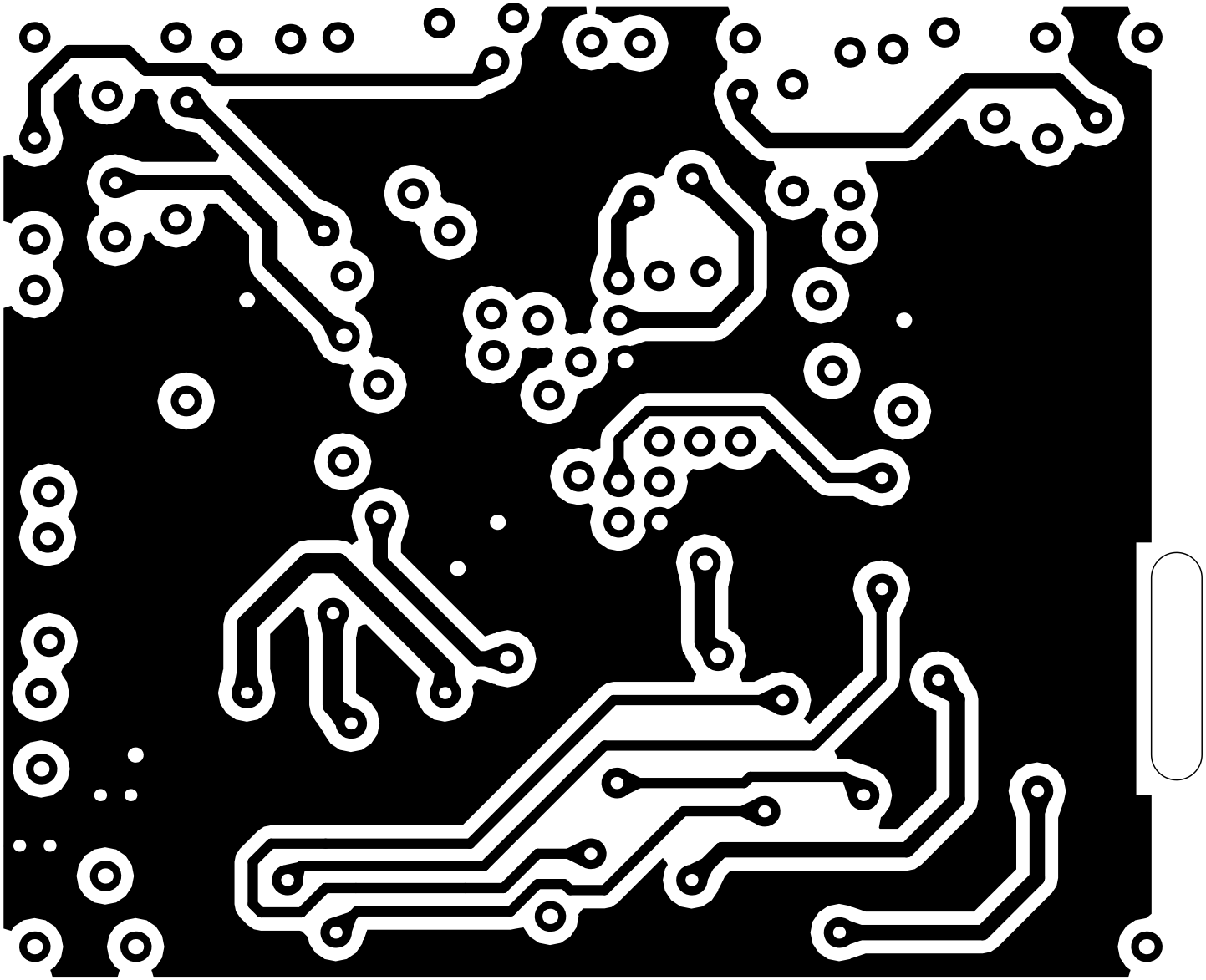
L3 (Scale 16:1)



Project: Artemis Plus		
Title: L3 Copper		
Size: A	Number: 1011	Revision: C
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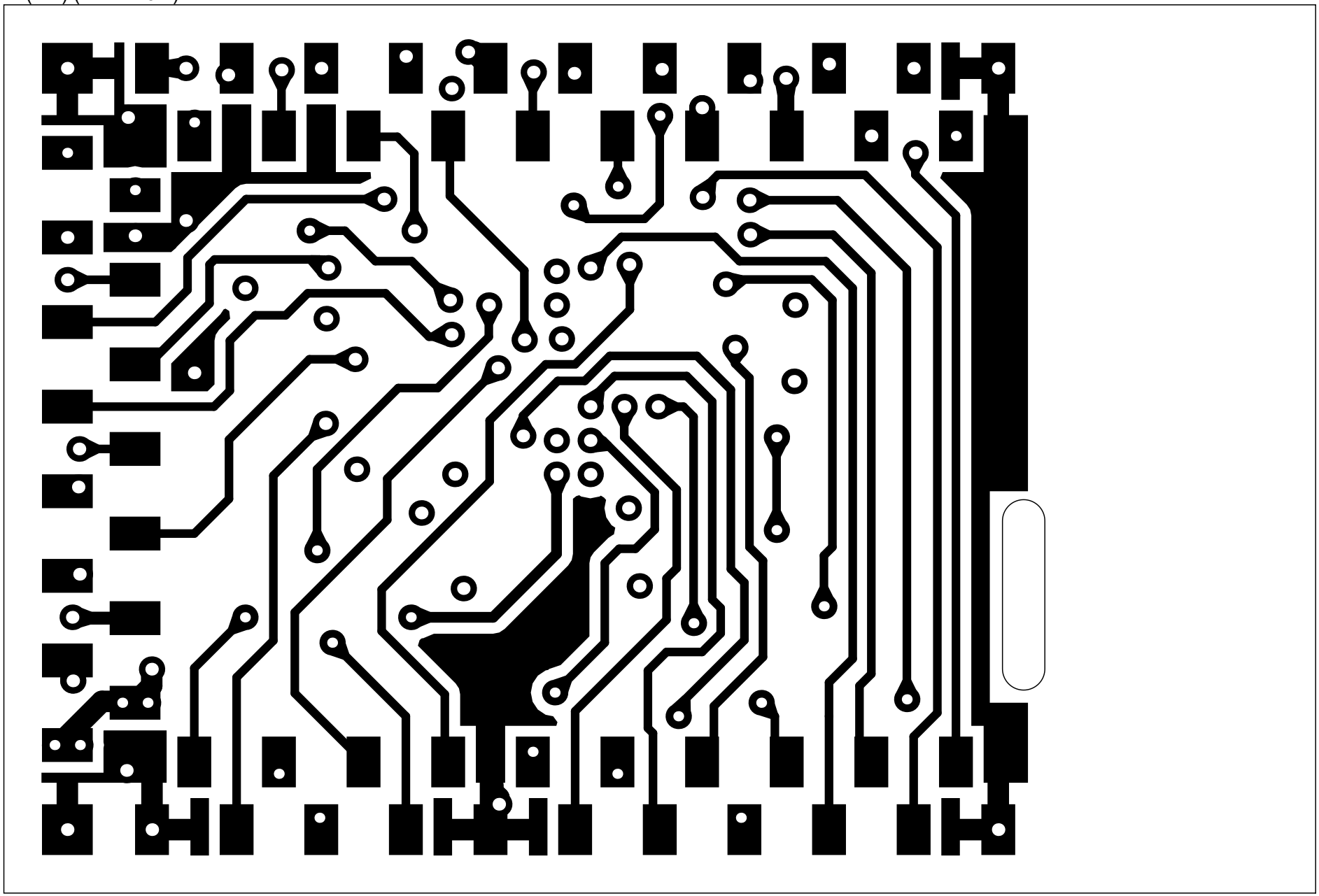
L4(Bot) (Scale 16:1)



Project: Artemis Plus		
Title: L4 Copper		
Size: A	Number: 1011	Revision: C
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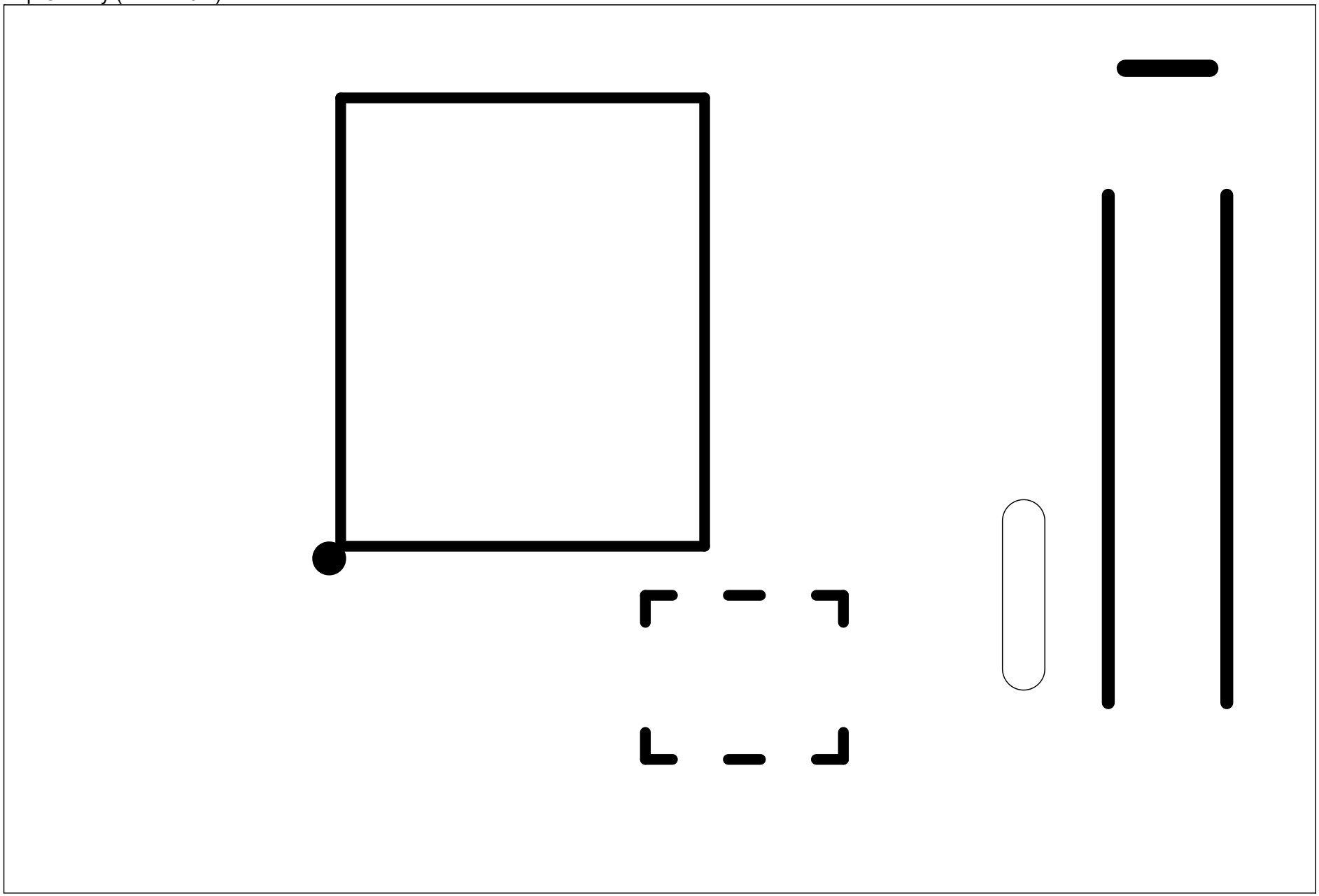
Top Overlay (Scale 16:1)



Project: Artemis Plus		
Title: Top Silkscreen		
Size: A	Number: 1011	Revision: C
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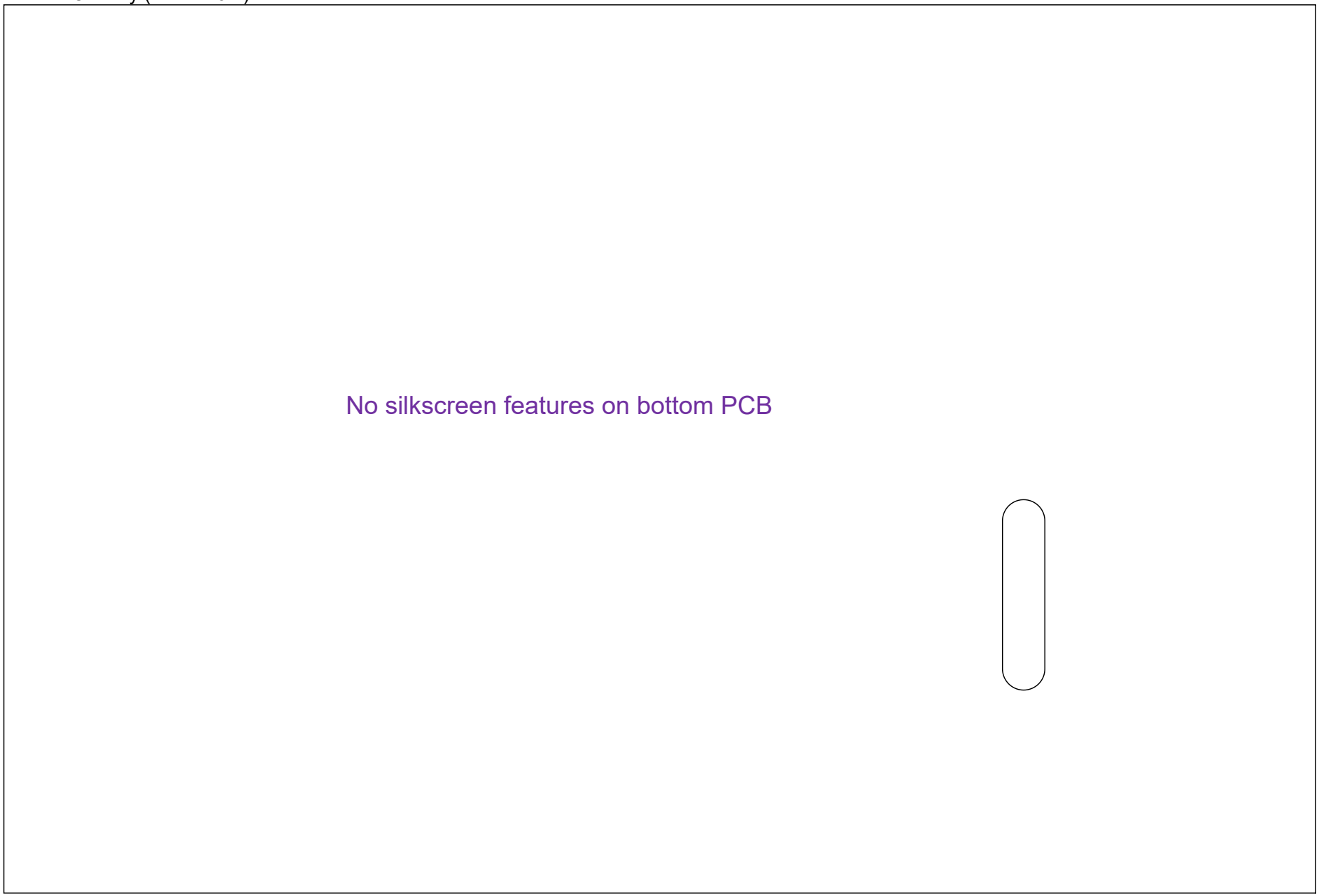
Bottom Overlay (Scale 16:1)



Project: Artemis Plus		
Title: Bottom Silkscreen		
Size: A	Number: 1011	Revision: C
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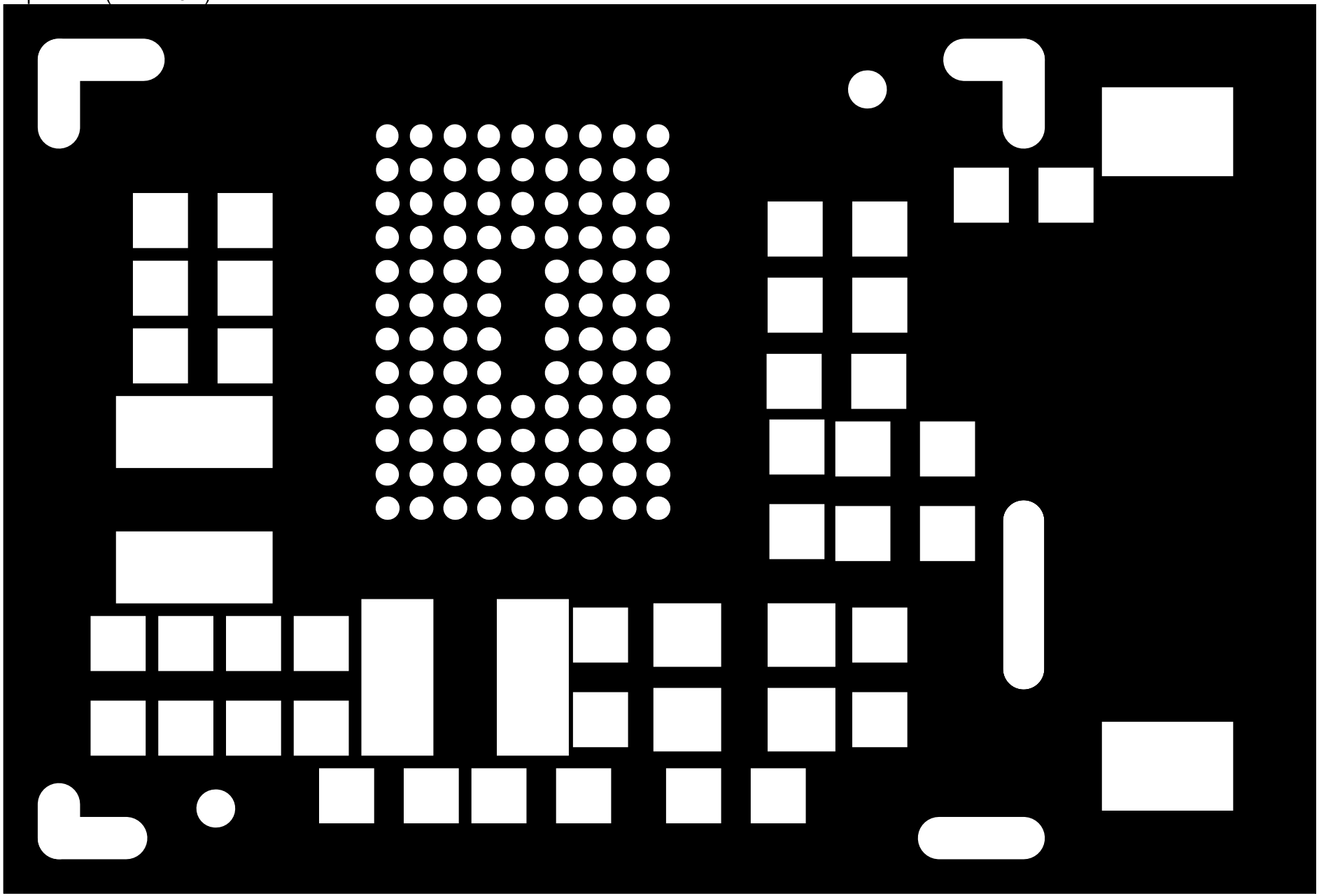
Top Solder (Scale 16:1)



Project: Artemis Plus		
Title: Top Soldermask		
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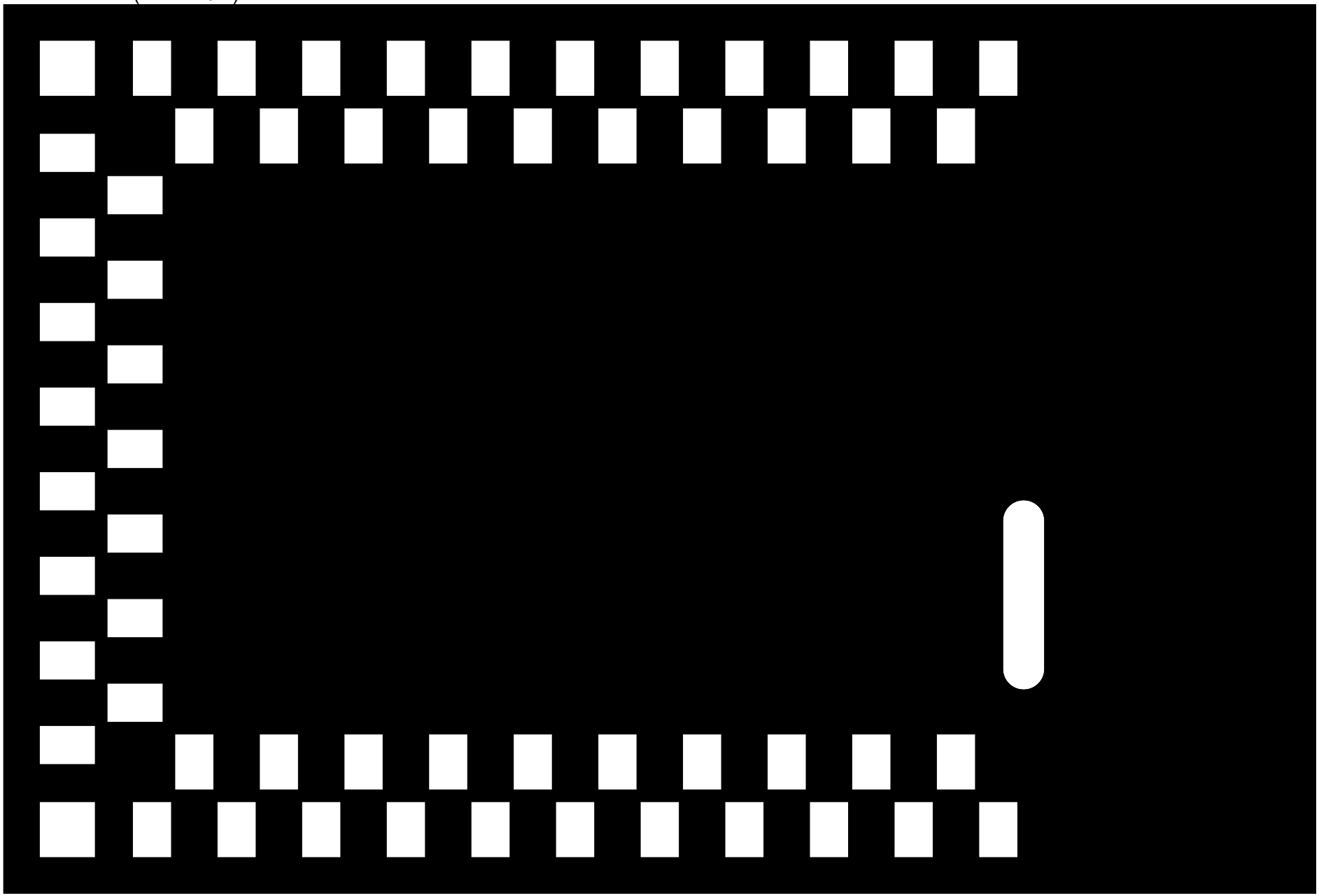
Bottom Solder (Scale 16:1)



Project: Artemis Plus		
Title: Bottom Soldermask		
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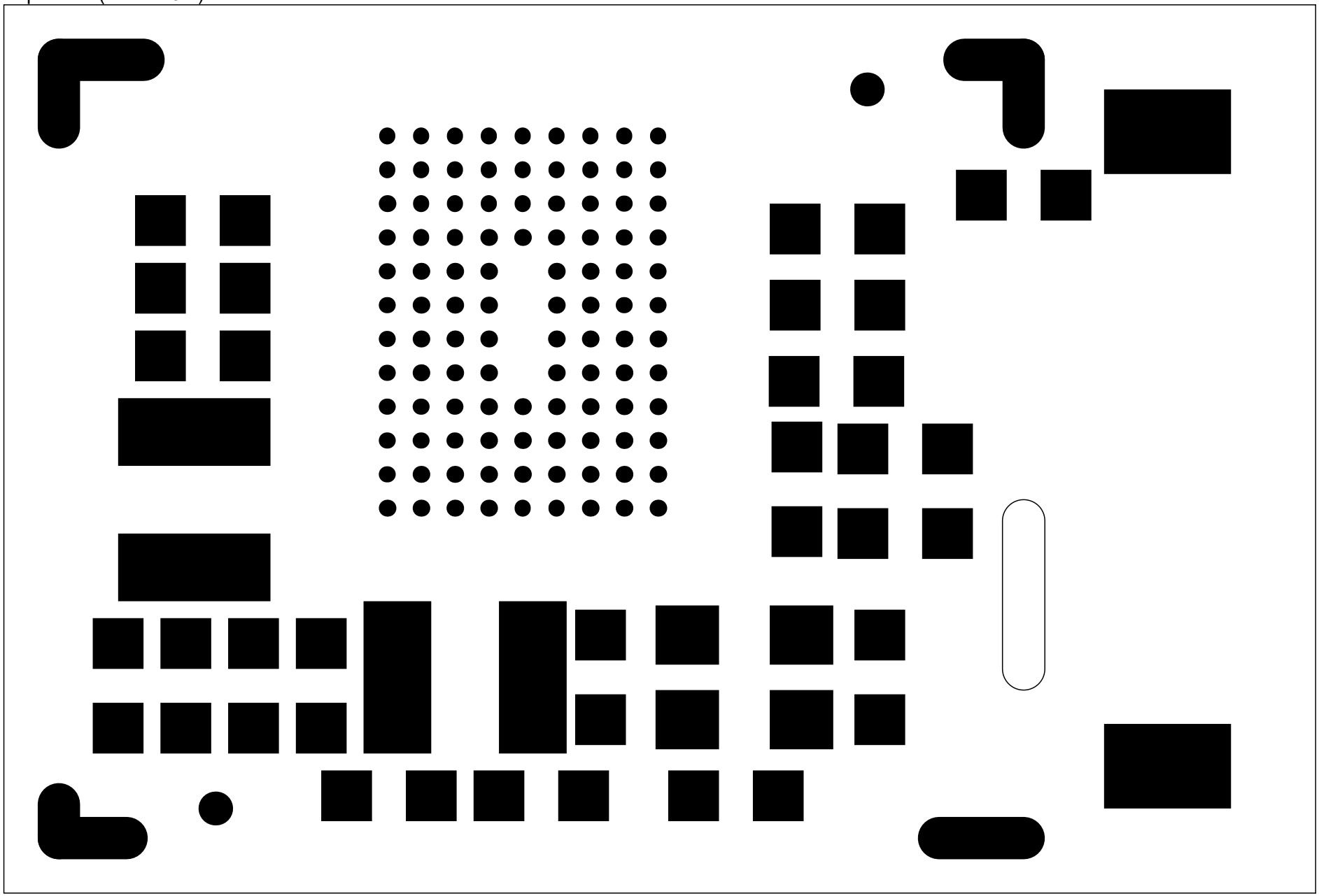
Top Paste (Scale 16:1)



Project: Artemis Plus		
Title: Top Paste		
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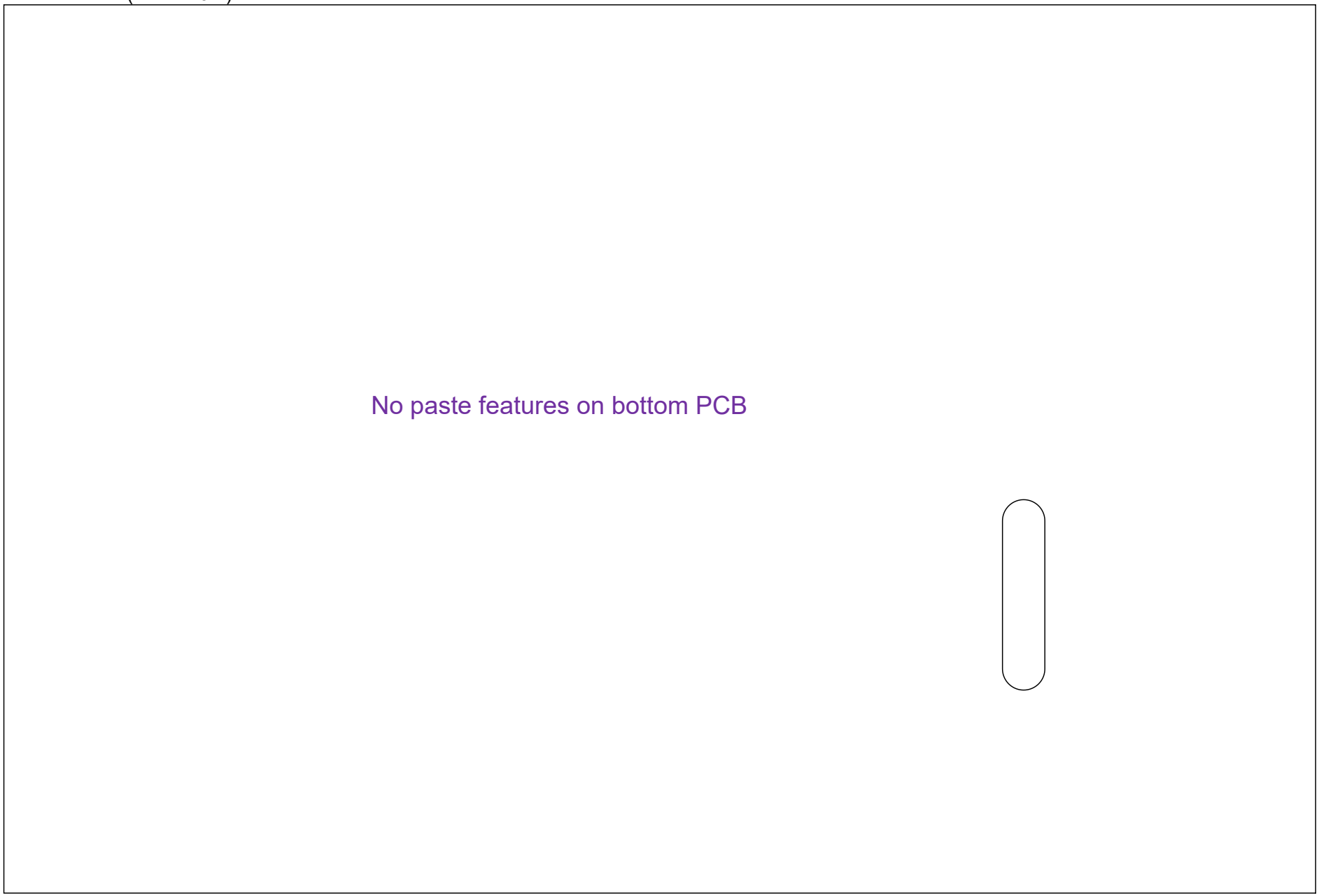
Bottom Paste (Scale 16:1)



Project: Artemis Plus		
Title: Bottom Paste		
Size: A	Number: 1011	Revision: C
Date: 11/5/2023 Time: 10:15 PM		Sheet: 17 of 17
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