



Ahsanullah University of Science & Technology
Department of Computer Science & Engineering

Course No : CSE3110
Course Title : Digital System Design Lab.
Assignment No : 02
Experiment Name : 4x4 Booth Implementation

Date of Experiment : 29th December 2022
Date of Submission : 14th January 2023

Submitted To : MD. Ragibul Hasan & Anika Rahman

Submitted By-
Section : C
Lab Group: C1
Group : 02
Group Members :
1. Shuvashis Sarkar (20200104116)
2. Shamim Rahim Refat (20200104125)
3. Ahnaf Tajwar Basunia (20200104104)
4. Sheikh Fardeen Ishaque (19 0104 011)

Problem Statement: Design a 4×4 Booth multiplier.

Introduction:

Booth's algorithm is a multiplication algorithm that can multiply both positive and negative numbers. For this experiment, we will make a 4×4 booth multiplier using "booth's Algorithm". Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. It does not need a large number of additions or subtractions. It operates on that fact that strings of 0's in the multiplier require just shifting a string of the 1's in the multiplier from bit weight 2^k to weight 2^m can be treated as 2^{k+1} to 2^m .

Booth's Algorithm (Flowchart)


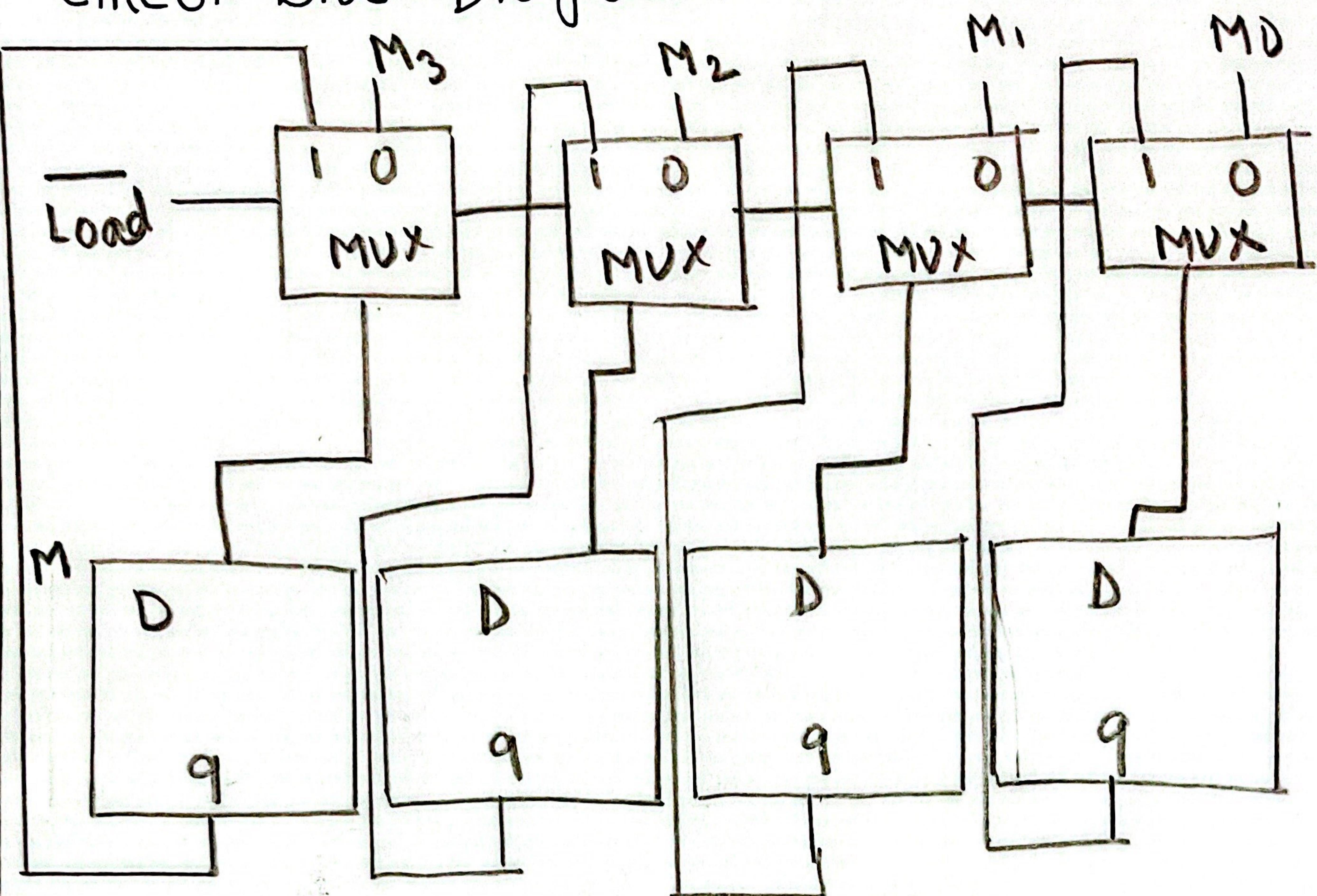


Fig: Flowchart of signed Multiplication (Booth's Algorithm)


Circuit Block Diagram:



Q_0	Q_{-1}	Operation	X	Y	C_{in}
0	0	$A+0$	A	0	0
0	1	$A+M$	A	M	0
1	0	$A-M$	A	\bar{M}	0
1	1	$A+0$	A	0	0

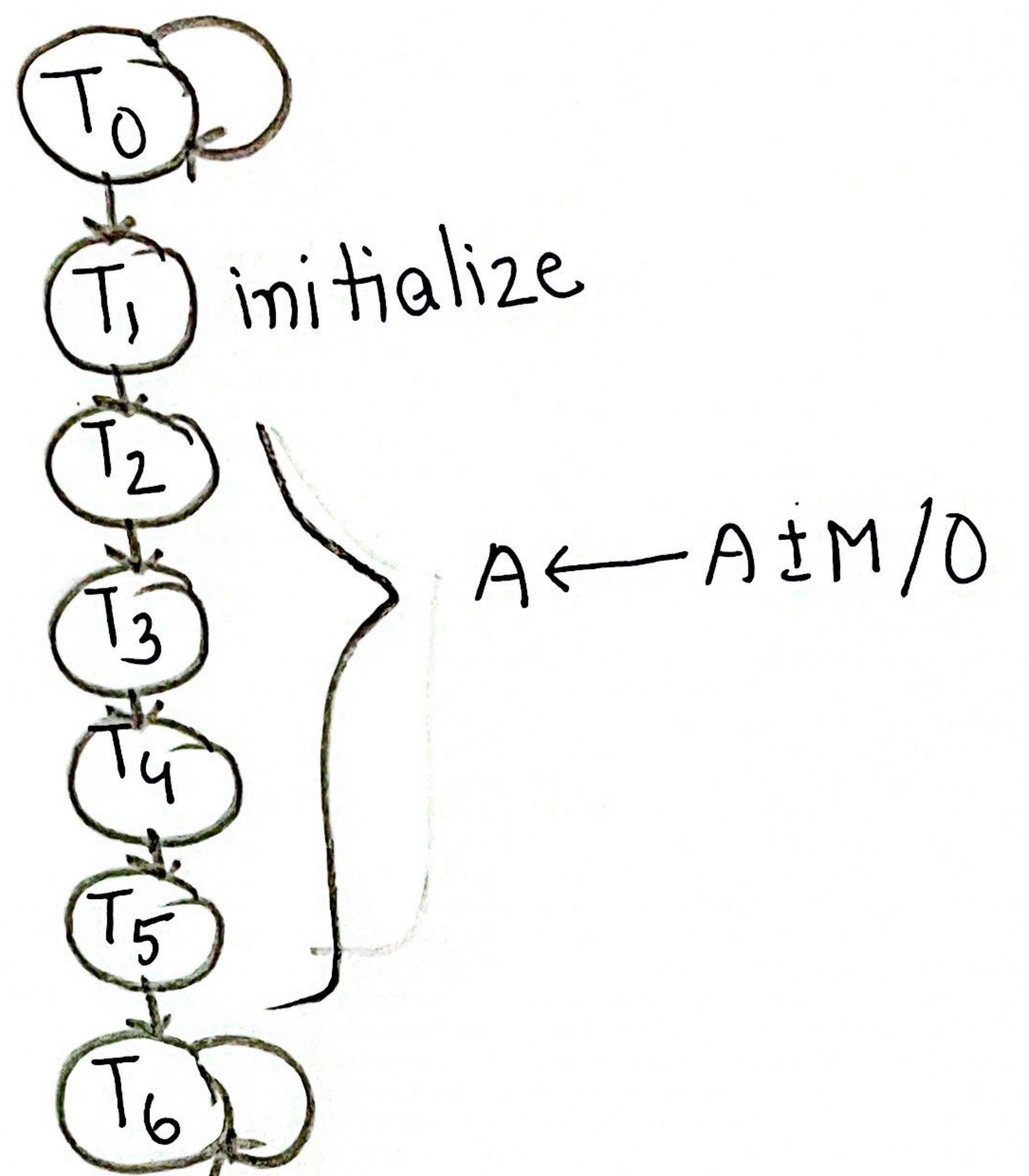
$$Y = \bar{Q}_0 \bar{Q}_{-1} M + Q_0 \bar{Q}_{-1} \bar{M}$$

$$C_{in} = \bar{Q}_0 \bar{Q}_{-1}$$



Control Unit Design:

State Diagram:



Control Signal:

State	$\overline{\text{clear}}$	$\overline{\text{Load/Shift}}$	Clk-enable
T_0	0	0	1
T_1	1	0	1
T_2	1	1	1
T_3	1	1	1
T_4	1	1	1
T_5	1	1	1
T_6	1	1	0

Boolean Expression:

$$DT_0 = T_0 \overline{Start}$$

$$DT_1 = T_0 Start$$

$$DT_2 = T_1$$

$$DT_3 = T_2$$

$$DT_4 = T_3$$

$$DT_5 = T_4$$


$$DT_6 = T_5 + T_6$$

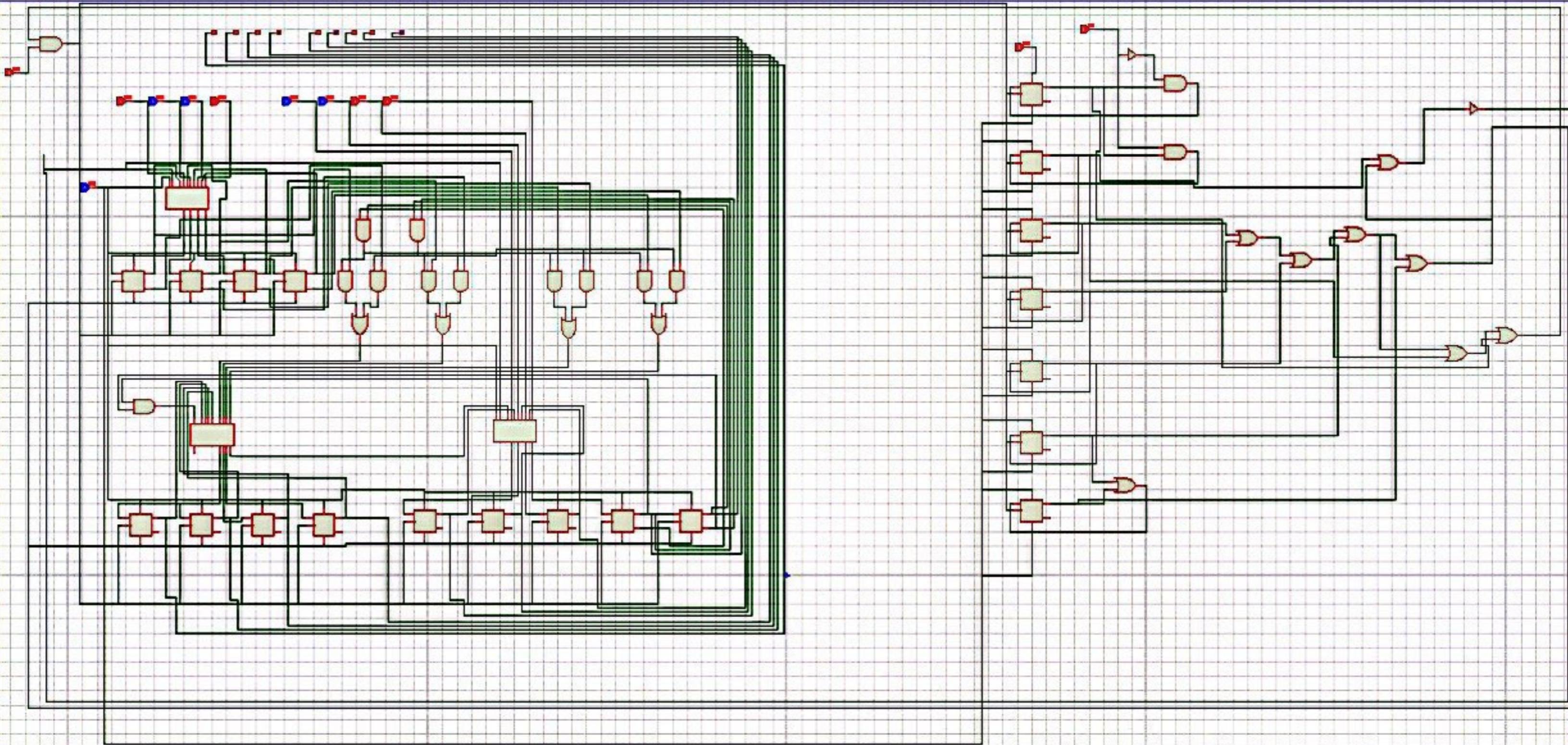
$$\overline{Clear} = T_1 + T_2 + T_3 + T_4 + T_5 + T_6$$

$$\overline{Load/Shift} = T_2 + T_3 + T_4 + T_5 + T_6$$

$$Clk\text{-enable} = T_0 + T_1 + T_2 + T_3 + T_4 + T_5$$

Control Unit Circuits





Conclusion:

To design this circuit, we have used proteus and implemented our multiplier with various values and got the expected output. Through this process we can say that our simulation is working properly. We faced no error and the total cost of this simulation was quite reasonable.