

## Ahsanullah University of Science & Technology

### Department of Computer Science & Engineering

**Course No** : CSE3110

**Course Title** : Digital System Design Lab.

**Assignment No** : 03

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**Submitted To** : MD. Raqibul Hasan & Anika Rahman

**Submitted By-**

**Section** : C

**Lab Group:** C1

**Group** : 2

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Name of the Experiment: Implementation of SAP-1

Introduction: SAP-1 is the first stage in the evolution towards modern computers. The main purpose of SAP is to introduce all the crucial ideas behind computer operation being a simple computer, SAP-1 also covers many advanced concepts. SAP-1 is a bus organised computer. All registers are connected to W bus with the help of tri state buffers. The full form of SAP is simple as possible.

## Block Diagram: (SAP-1)

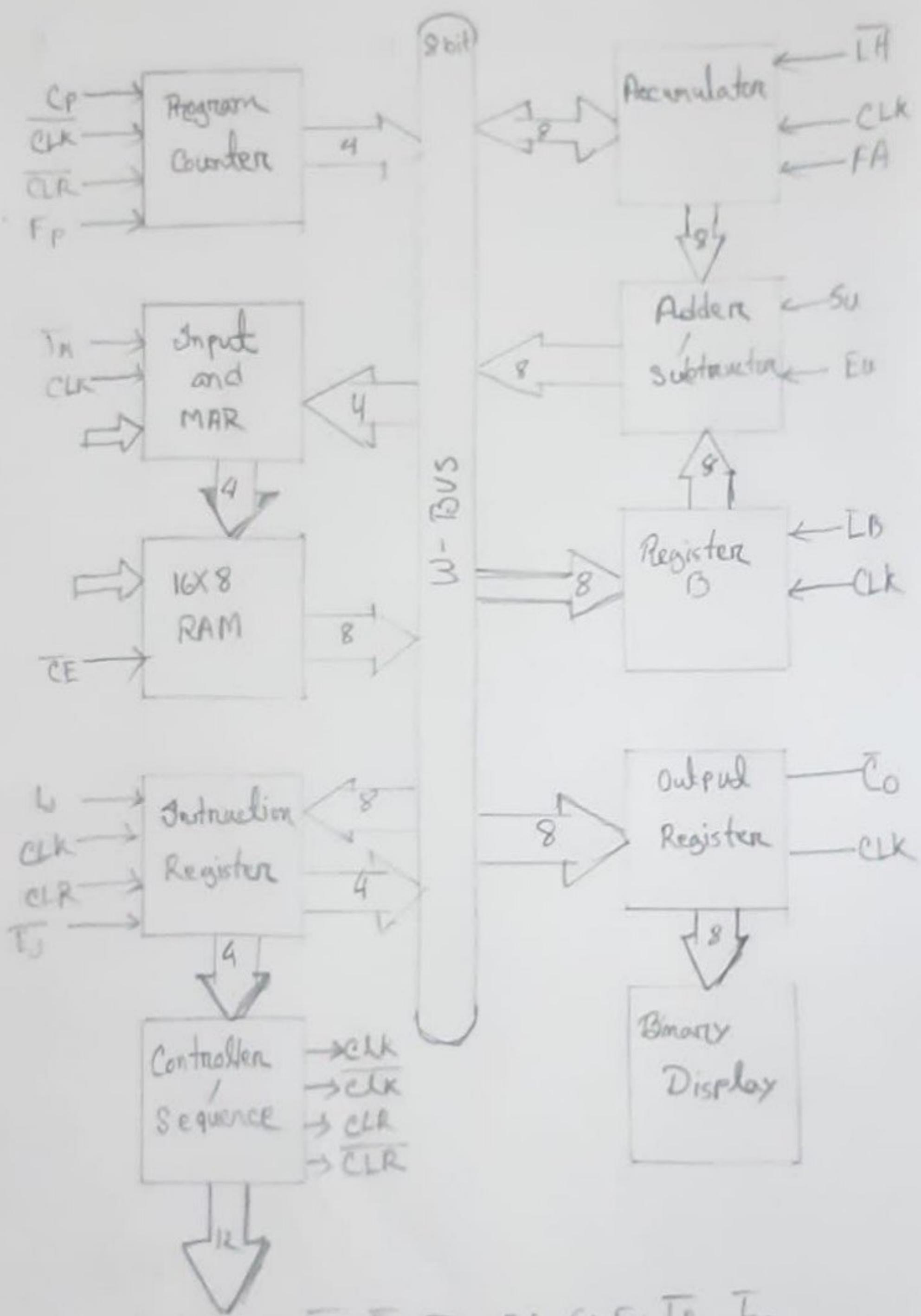
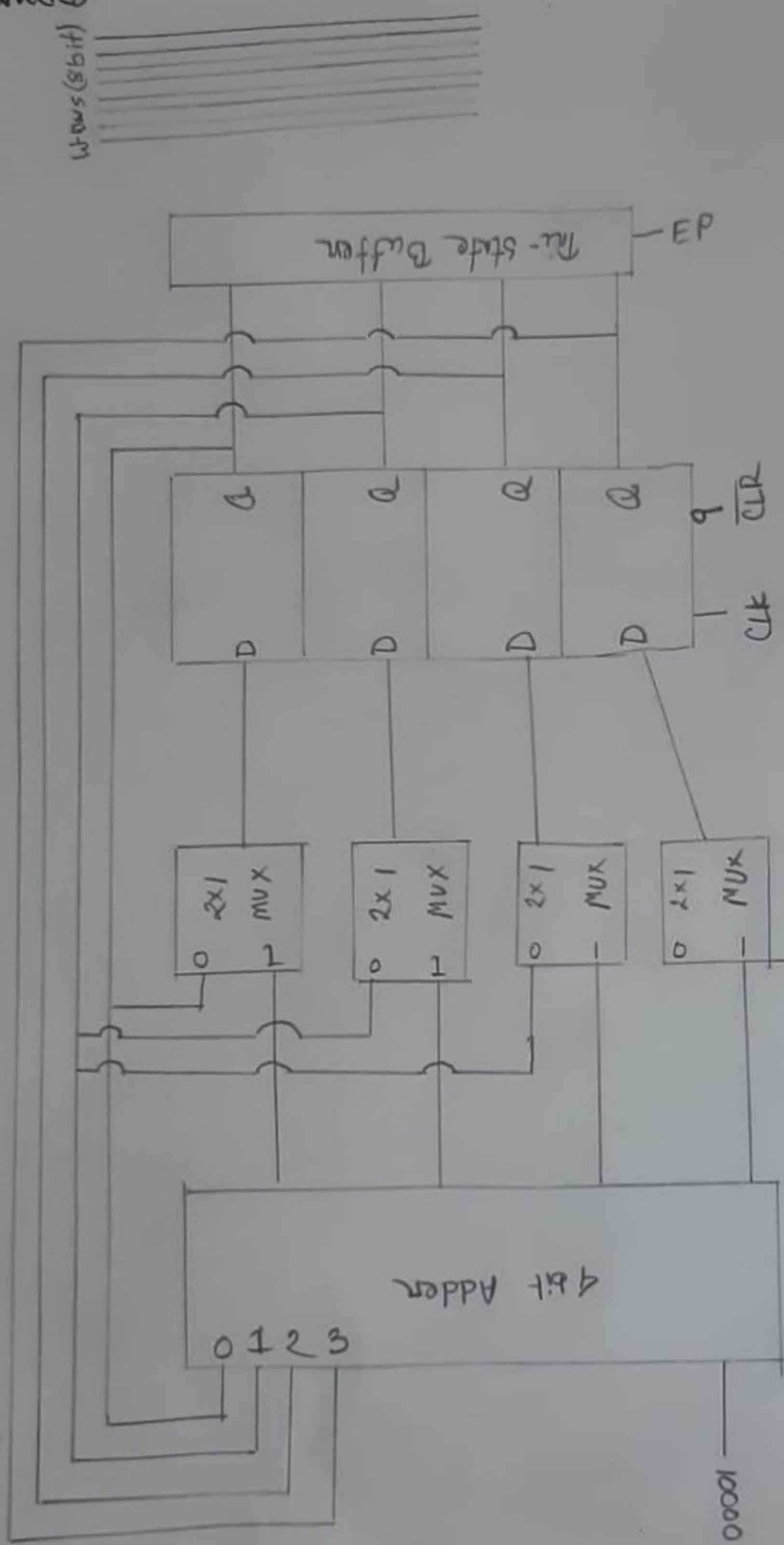


Fig: SAP-1

## Program Counter



# Memory Address Register (MAR)

IM	Function
0	Load
1	Hold

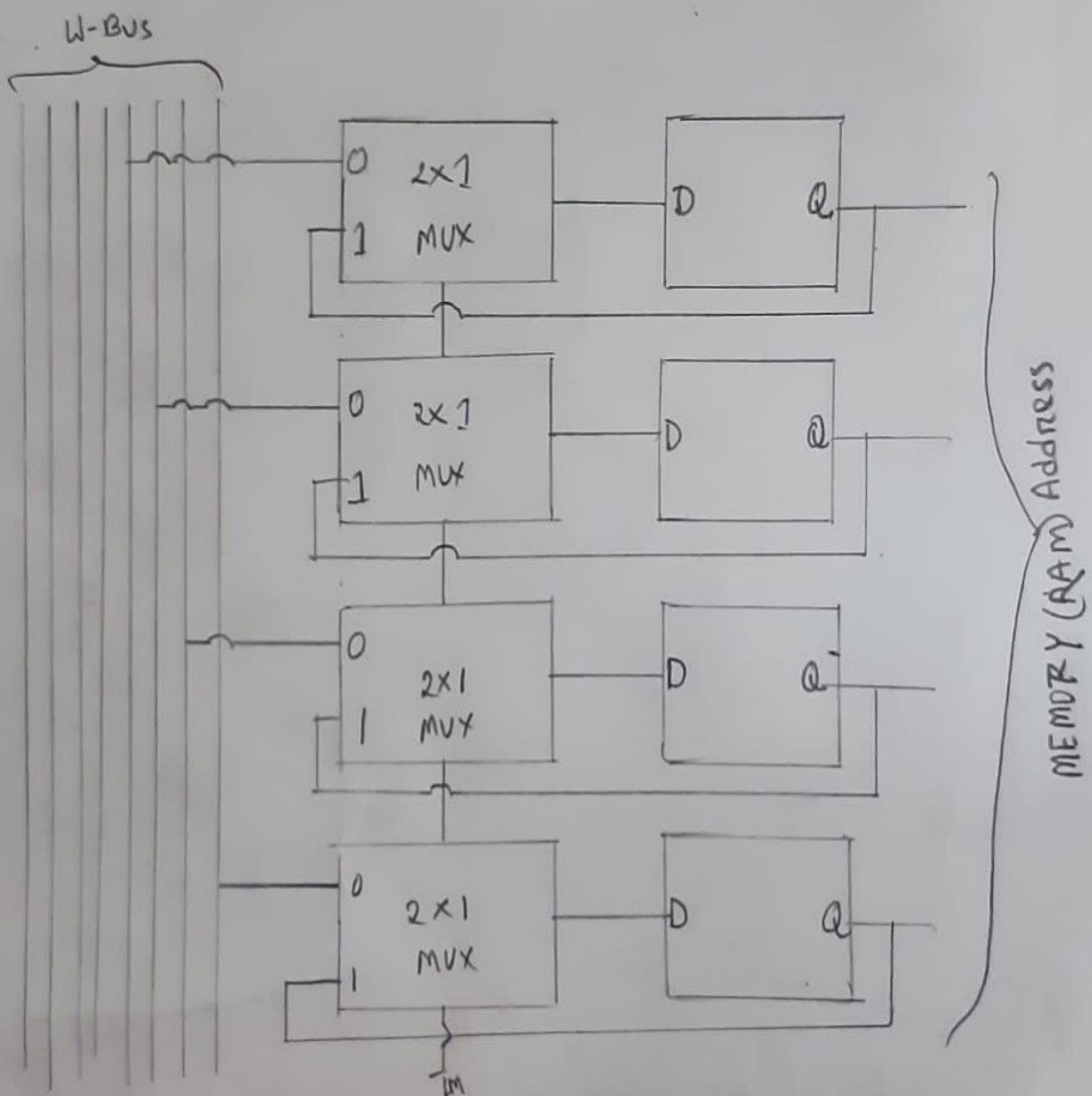
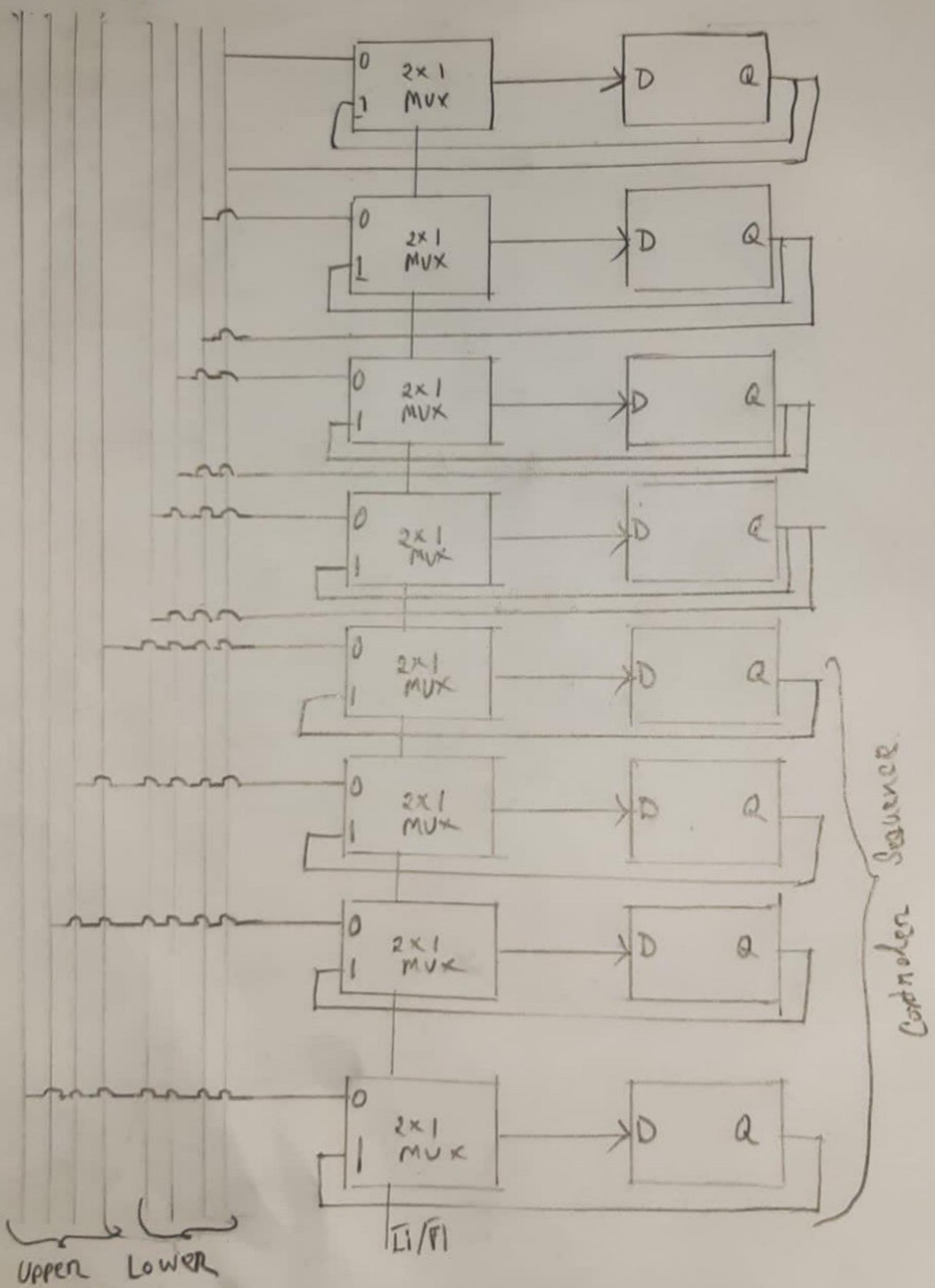
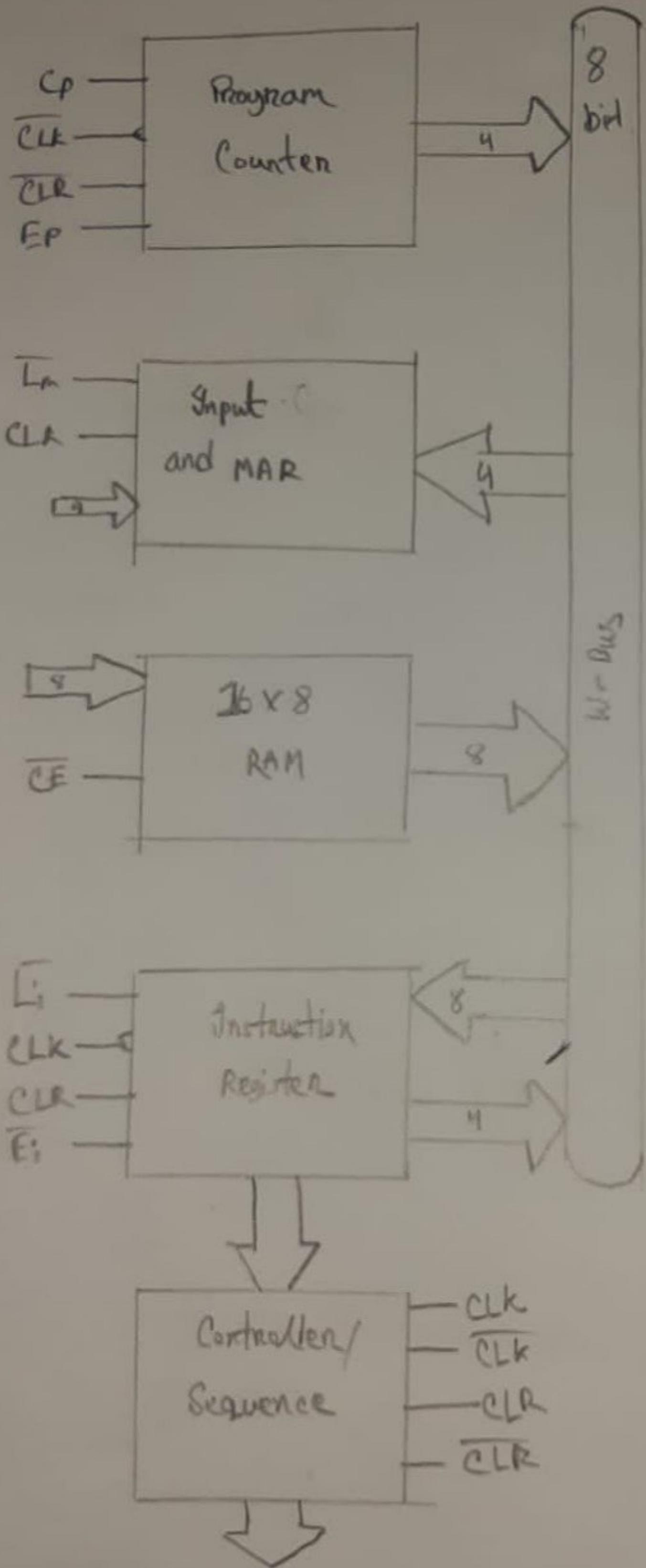


Fig: MAR

# Circuit Diagram of Instruction Register (IR):

w-bus (8 bit)





$C_P, E_P, \overline{I_m}, \overline{CE}, I_i, E_i, \overline{E_A}, E_A, S_U, E_U, \overline{I_B}, \overline{L}$

## Control Unit:

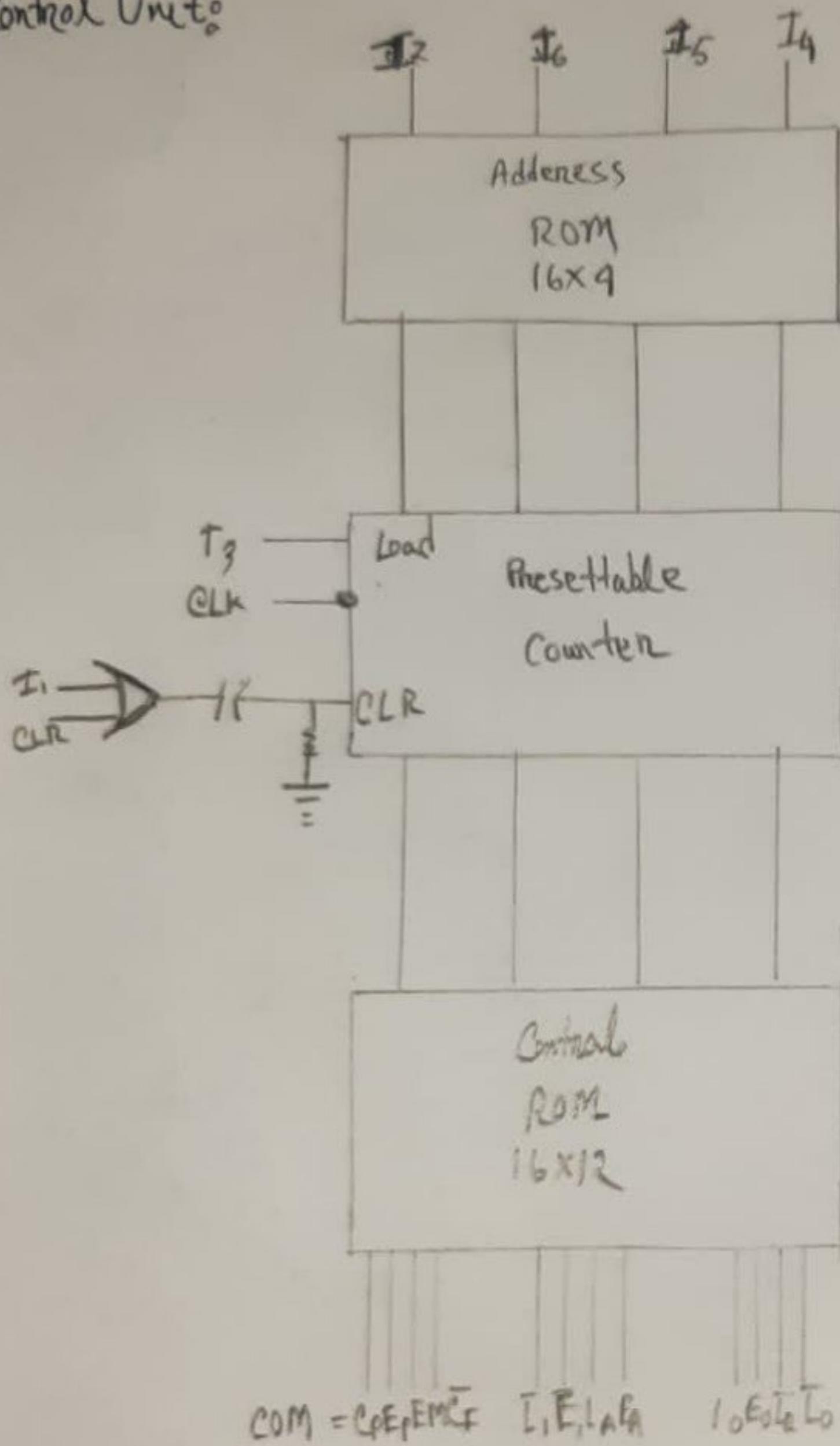
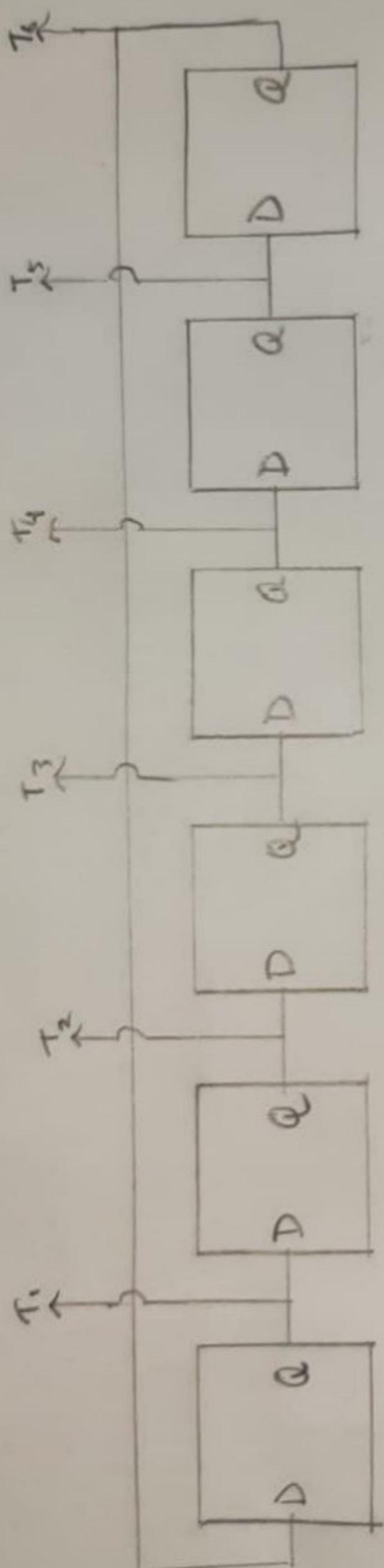
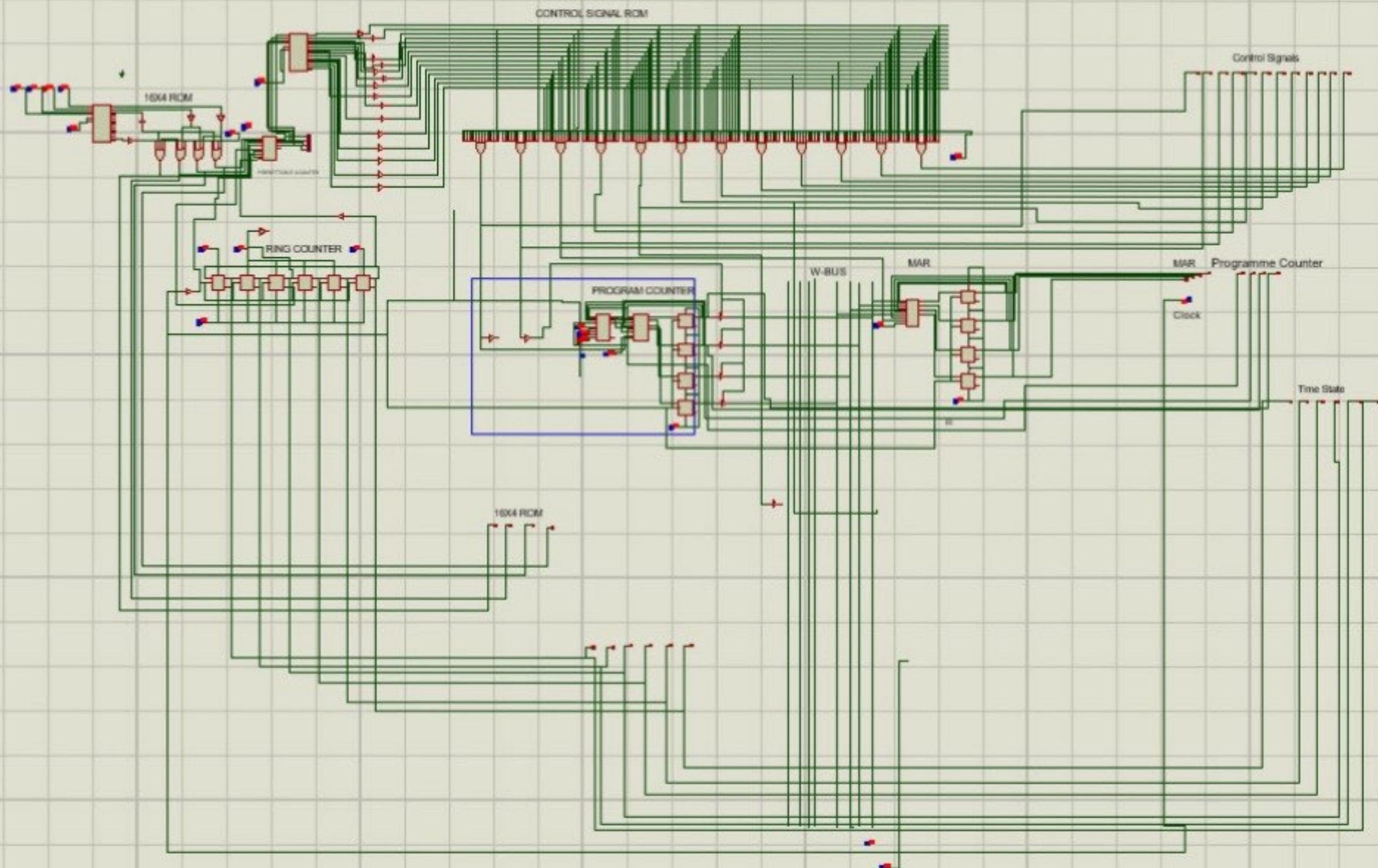


Fig: Microprogrammed Control of SAPI

# Ring Counter





NOT

CLK

U49



NOT

0

SET

0

# RING COUNTER

0

U64

NOT

U43:A

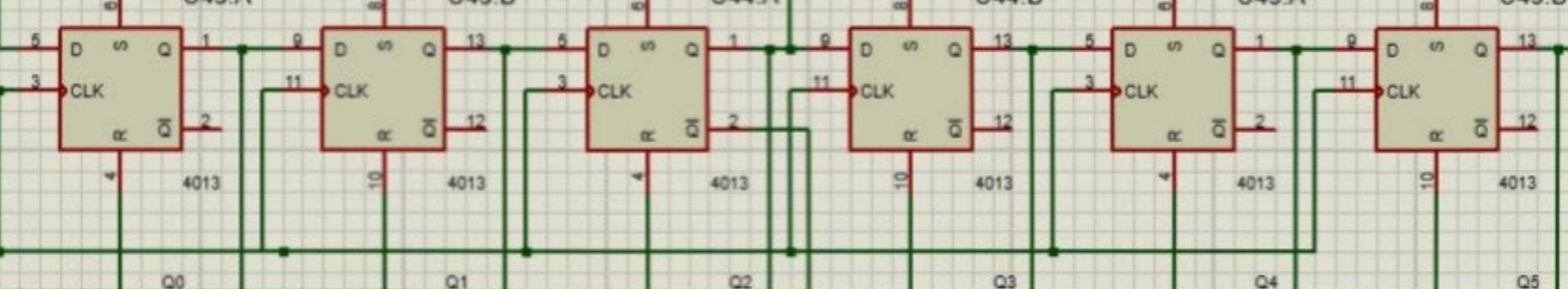
U43:B

U44:A

U44:B

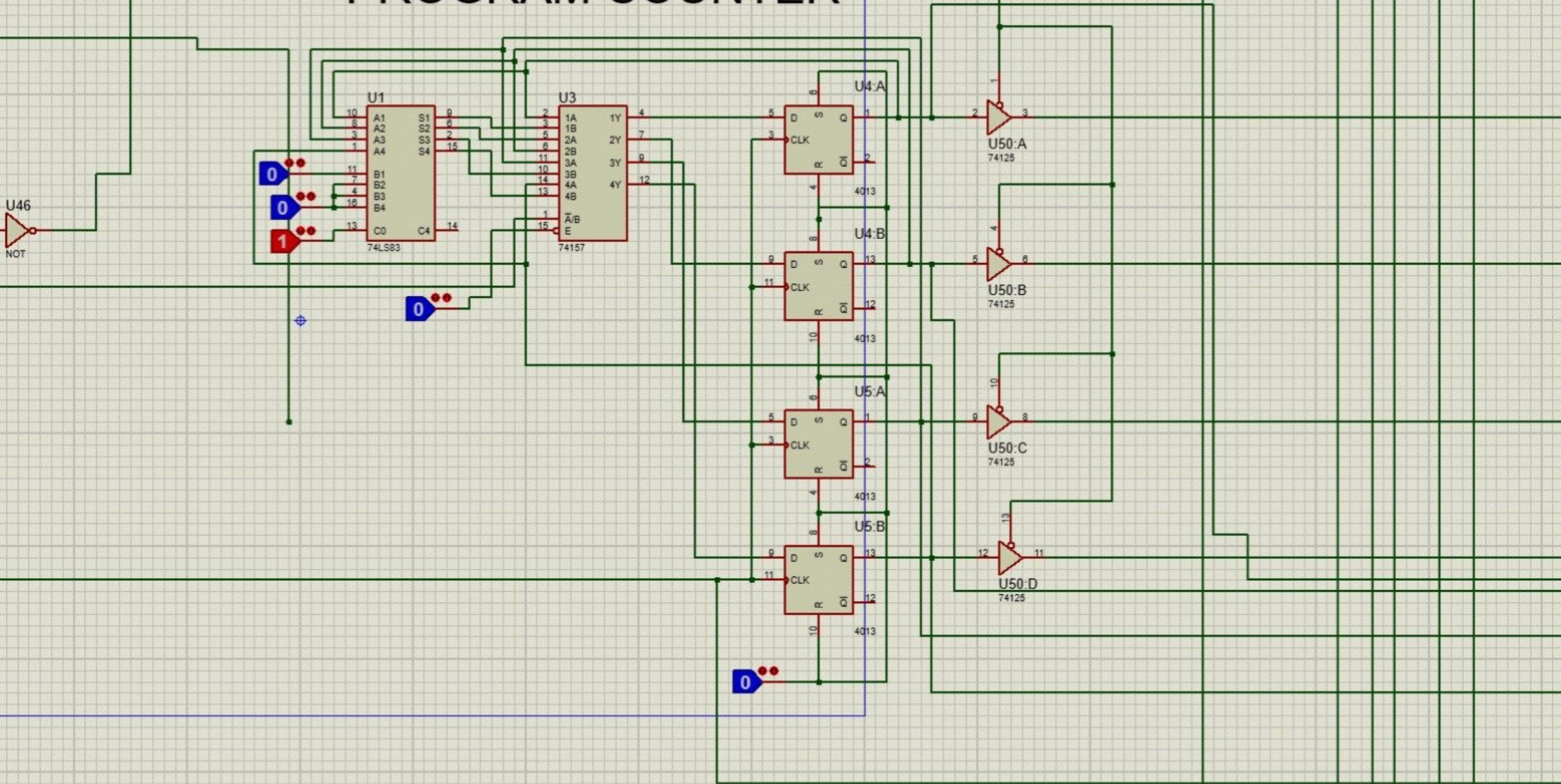
U45:A

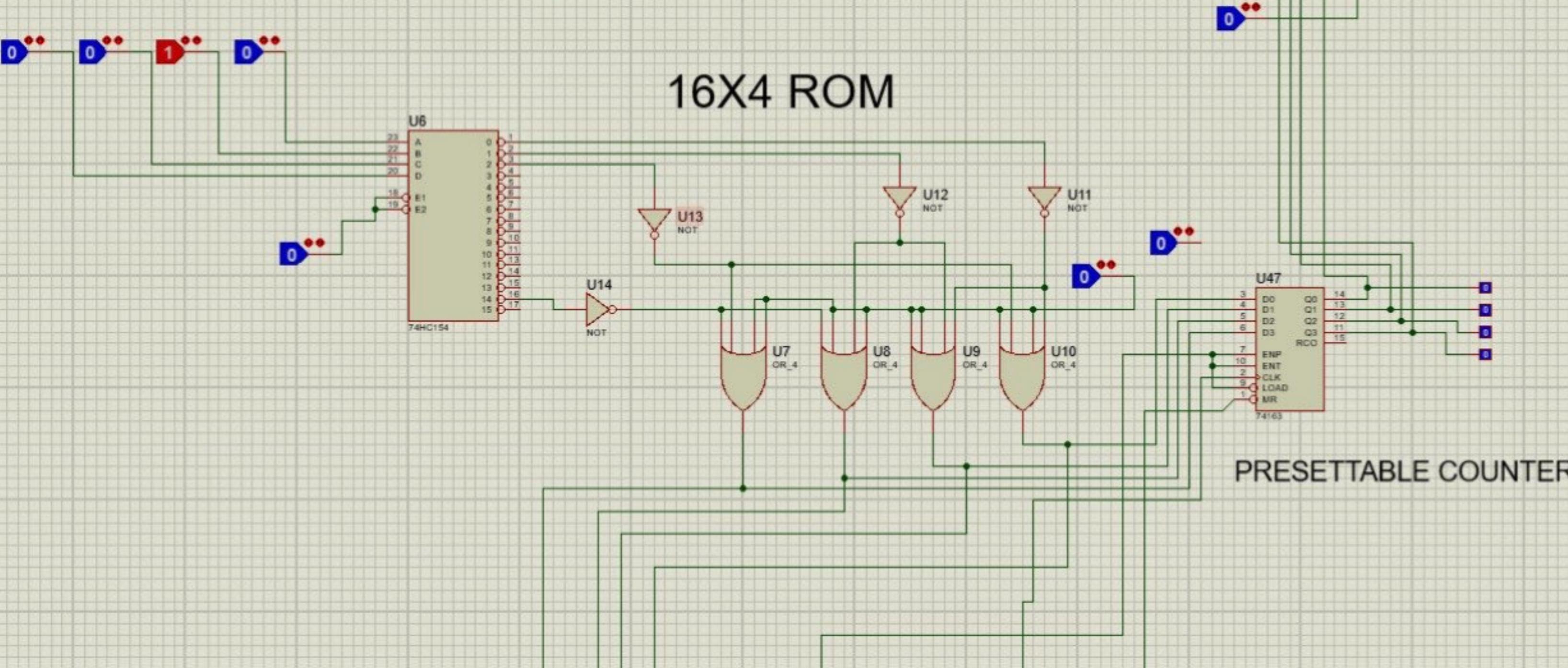
U45:B



0

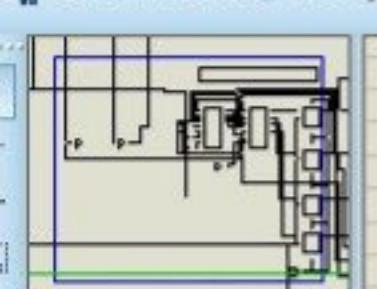
# PROGRAM COUNTER





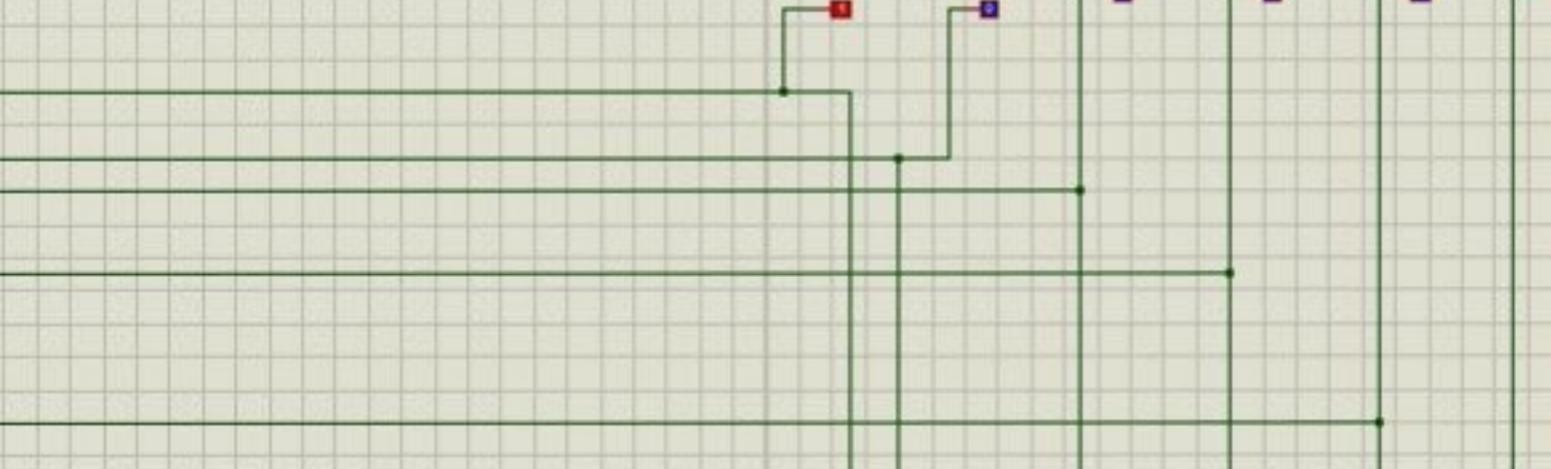
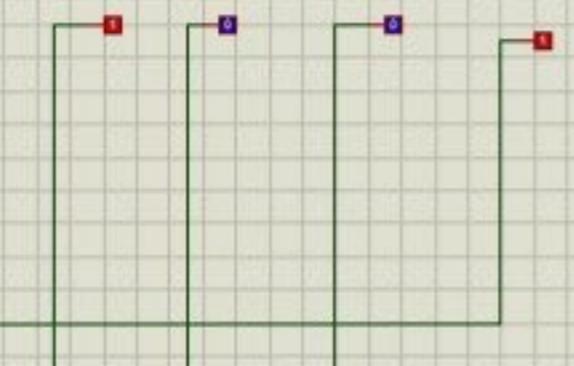


Schematic Capture X



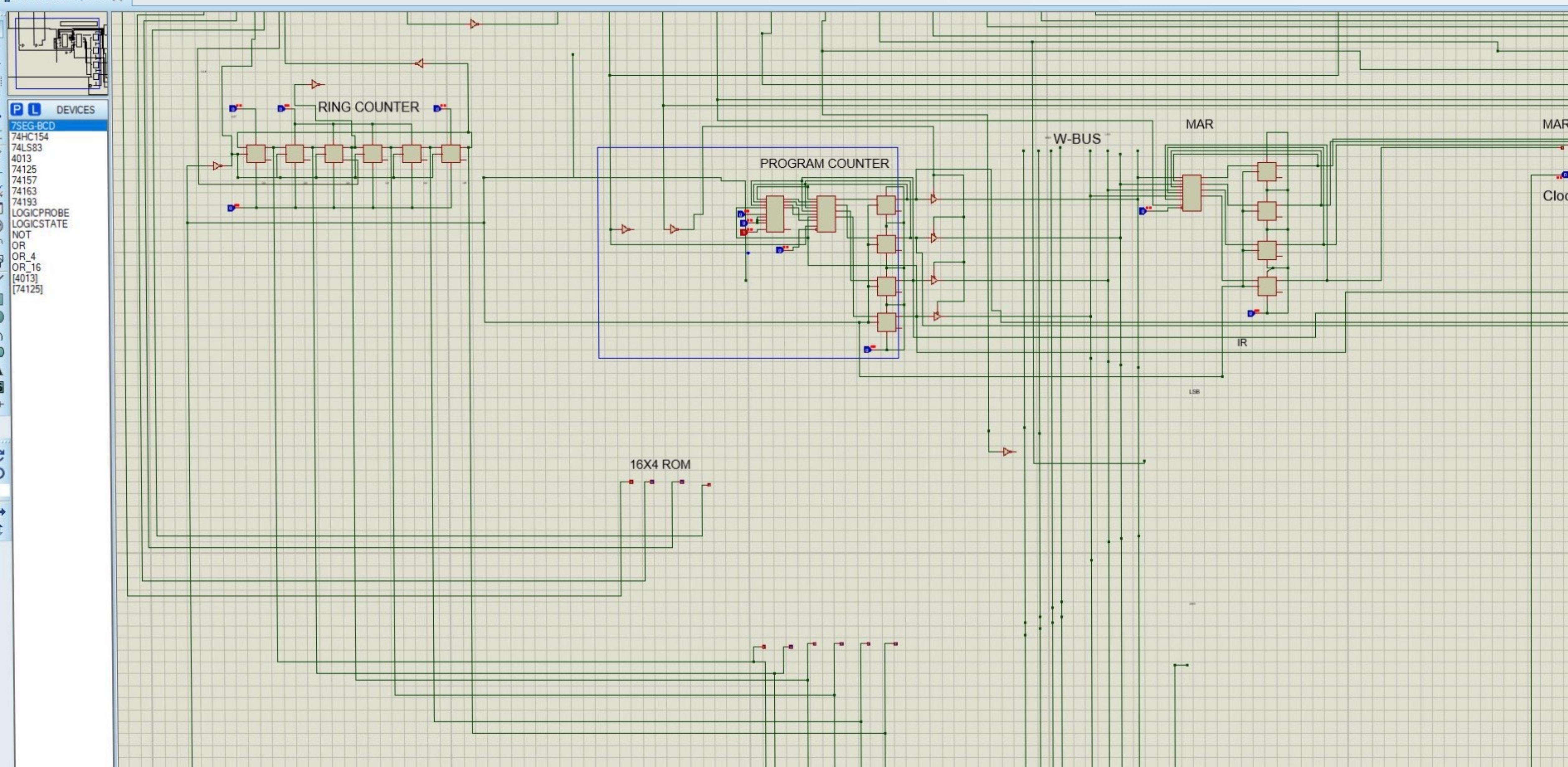
P	L	DEVICES
7SEG-BCD		
74HC154		
74LS83		
4013		
74125		
74157		
74163		
74193		
LOGICPROBE		
LOGICSTATE		
NOT		
OR		
OR_4		
OR_16		
[4013]		
[74125]		

16X4 ROM

U48  
NOT

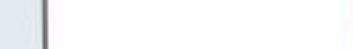
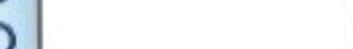
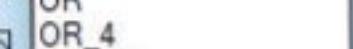
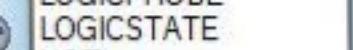
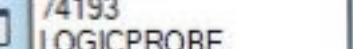
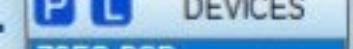
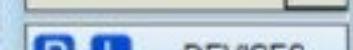
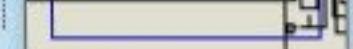
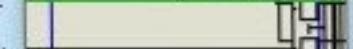
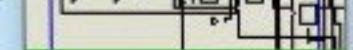
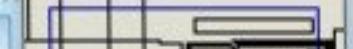


Schematic Capture X



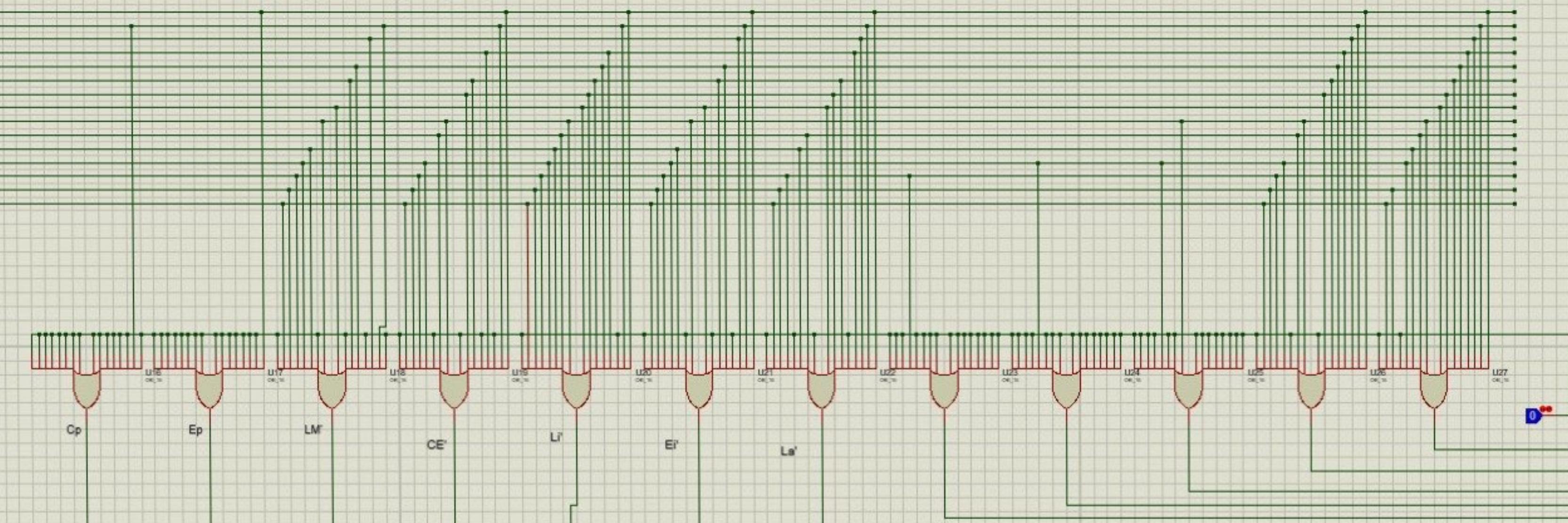


Schematic Capture X



## CONTROL SIGNAL ROM

U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U27



U63

R 0

U45A U45B

U46

U2

U46

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U27

U50A U50B

U51 U52A U52B U53A U53B

U54A U54B

U55A U55B

U56A U56B

U57A U57B

U58A U58B

U59A U59B

U60A U60B

## PROGRAM COUNTER

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U27

U50A U50B

U51 U52A U52B U53A U53B

U54A U54B

U55A U55B

U56A U56B

U57A U57B

U58A U58B

U59A U59B

U60A U60B

## W-BUS

U51 U52A U52B U53A U53B

U54A U54B

U55A U55B

U56A U56B

U57A U57B

U58A U58B

U59A U59B

U60A U60B

## MAR

U51 U52A U52B U53A U53B

U54A U54B

U55A U55B

U56A U56B

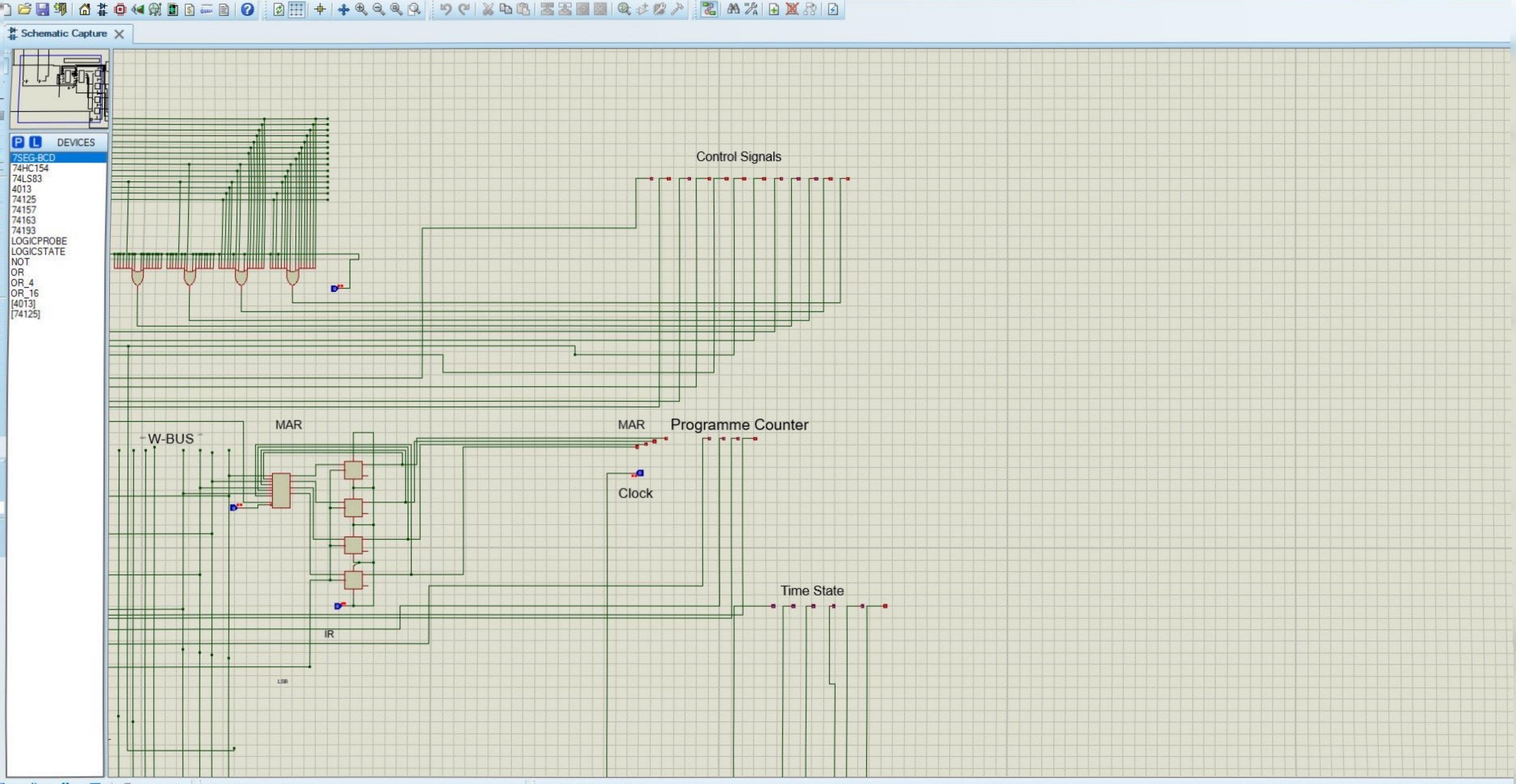
U57A U57B

U58A U58B

U59A U59B

U60A U60B





Conclusion:

There are some advantages of SAP-1 like flexibility. The architecture of SAP-1 is 8 bits of data bus and compromised of  $16 \times 8$  memory. Therefore 16 memory location. It needs 4 address lines which either comes from PC during computers run phase or may come from 4 address switches during the program phase.

These features of SAP-1 allows to make complex operation done.