

Ahsanullah University of Science & Technology

Department of Computer Science & Engineering

Course No	: CSE3110
Course Title	: Digital System Design Lab.
Assignment No	: 01
Date of Experiment	: 16 th November 2022
Date of Submission	: 10th December 2022
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Introduction:

An arithmetic logic unit (ALU) is used to perform arithmetic such as addition, subtraction, multiplication, division and logic operations such as AND, OR etc. It represents the fundamental building block of the central processing unit (cpu) of a computer. The main purpose of this experiment is to design a 4 bit arithmetic and

logical unit from the given function table.
we derived an equation of three input functions and simplified it. Then we implemented this function in proteus. We used a combination of basic gate and a 4 bit full adder to create ALU.
Depending on the selector (S_2) bit our ALU will perform the arithmetic ($S_2=1$) and the logical ($S_2=0$) operations accordingly and will show output of the given functions.

Problem Statement:

S_2	S_1	S_0	Output	Function
1	1	0	$A_i - 1$	Decrement A
1	0	1	$A_i + B_i + 1$	Add with carry
1	1	1	$A_i - B_i$	Subtract
1	0	0	A_i	Transfer A
0	0	x	$A_i \cdot B_i$	AND
0	1	x	$A_i \oplus B_i$	XOR

Function Generation

S_2	S_1	S_0	C_{in} (Z ₀)	ALU Function	X_i	Y_i	Z_i
1	1	0	0	$A_i - 1$	A	1	C_i
1	0	1	1	$A_i + B_i + 1$	A	B	C_i
1	1	1	1	$A_i - B_i$	A	\bar{B}	C_i
1	0	0	0	A_i	A	0	c_i
0	0	0	0	$A_i \cdot B_i$	$A_i + \bar{B}_i$	\bar{B}_i	0
0	0	1	0	$A_i \cdot B_i$	$A_i + \bar{B}_i$	\bar{B}_i	0
0	1	0	0	$A_i \oplus B_i$	A_i	B_i	0
0	1	1	0	$A_i \oplus B_i$	A_i	B_i	0

K Map :

For X_i :

$S_2 S_0$	$\bar{S}_2 \bar{S}_0$	$\bar{S}_2 S_0$	$S_2 S_0$	$S_2 \bar{S}_0$
\bar{S}_2	$A_i + \bar{B}_i$	$A_i + \bar{B}_i$	A_i	A_i
S_2	A_i	A_i	A_i	A_i

The Simplified expression is

$$\begin{aligned}
 & S_2 A_i + S_1 A_i + \bar{S}_2 \bar{S}_1 (A_i + \bar{B}_i) \\
 = & S_2 A_i + S_1 A_i + \bar{S}_2 \bar{S}_1 A + \bar{S}_2 \bar{S}_1 \bar{B}_i \\
 = & S_1 A_i + A_i (S_2 + \bar{S}_2 \bar{S}_1) + \bar{S}_2 \bar{S}_1 \bar{B}_i \\
 = & S_1 A_i + A_i (S_2 + \bar{S}_1) + \bar{S}_2 \bar{S}_1 \bar{B}_i \\
 = & S_1 A_i + A_i S_2 + A_i \bar{S}_1 + \bar{S}_2 \bar{S}_1 \bar{B}_i \\
 = & A_i (S_1 + \bar{S}_1) + A_i S_2 + S_2 \bar{S}_1 \bar{B}_i \\
 = & A_i + A_i S_2 + \bar{S}_2 \bar{S}_1 \bar{B}_i \\
 = & A_i + \bar{S}_2 \bar{S}_1 \bar{B}_i
 \end{aligned}$$

For y_i

$S_2 \quad S_1 S_0$	$\bar{S}_1 \bar{S}_0$	$\bar{S}_1 S_0$	$S_1 S_0$	$S_1 \bar{S}_0$
\bar{S}_2	$\boxed{\bar{B}_i}$	$\boxed{\bar{B}_i}$	$\boxed{B_i}$	$\boxed{B_i}$
S_2	0	$\boxed{B_i}$	$\boxed{\bar{B}_i}$	\boxed{I}

The simplified expression

$$\begin{aligned}
 & \bar{S}_2 \bar{S}_1 \bar{B}_i + \bar{S}_2 S_1 B_i + S_2 \bar{S}_1 S_0 B_i + S_2 S_1 S_0 \bar{B}_i + \\
 & S_2 S_1 \bar{S}_0 \\
 = & \bar{S}_2 (\bar{S}_1 \bar{B}_i + S_1 B_i) + S_2 S_0 (\bar{S}_1 B_i + S_1 + \bar{B}_i) + \\
 & S_2 S_1 \bar{S}_0 \\
 = & \bar{S}_2 (\overline{S_1 \oplus B_i}) + S_2 S_0 (S_1 \oplus B_i) + S_2 S_1 \bar{S}_0 \\
 = & \bar{S}_2 (\overline{S_1 \oplus B_i}) + S_2 (S_0 (S_1 \oplus B_i) + S_1 \bar{S}_0)
 \end{aligned}$$

For z_i

$S_2 \quad S_1 S_0$	$S_1 S_0$	$S_1 S_0$	$S_1 S_0$	$S_1 \bar{S}_0$
\bar{S}_2	0	0	0	0
S_2	C_i	C_i	C_i	C_i

$$= S_2 C_i$$

For C_i

S_2	$\bar{S}_1 S_0$	$\bar{S}_1 \bar{S}_0$	$\bar{S}_1 S_0$	$S_1 S_0$	$S_1 \bar{S}_0$
\bar{S}_2	0	0	0	0	0
S_2	0	1	1		0

The simplified equation is

$$S_2 S_0$$

Results

For $A_i - 1$

For $A_i + B_i + l$

Input							Output								
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	F_3	F_2	F_1	F_0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	1	1	0	0	1	0	1	0	1	1
			0	0	1	0	1	1	1	0	0	0	1	1	1

For $A_i - B_i$

Input												Output			
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	$Cout$	F_3	F_2	F_1	F_0
1	1	1	1	0	1	1	0	1	0	1	1	0	1	1	0
1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	0
			0	1	0	1	0	1	0	0	1	0	0	0	1

For A_i

Input												Output			
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	$Cout$	F_3	F_2	F_1	F_0
1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1
			0	1	0	0	0	0	0	0	0	0	0	1	0


For $A_i \cdot B_i$

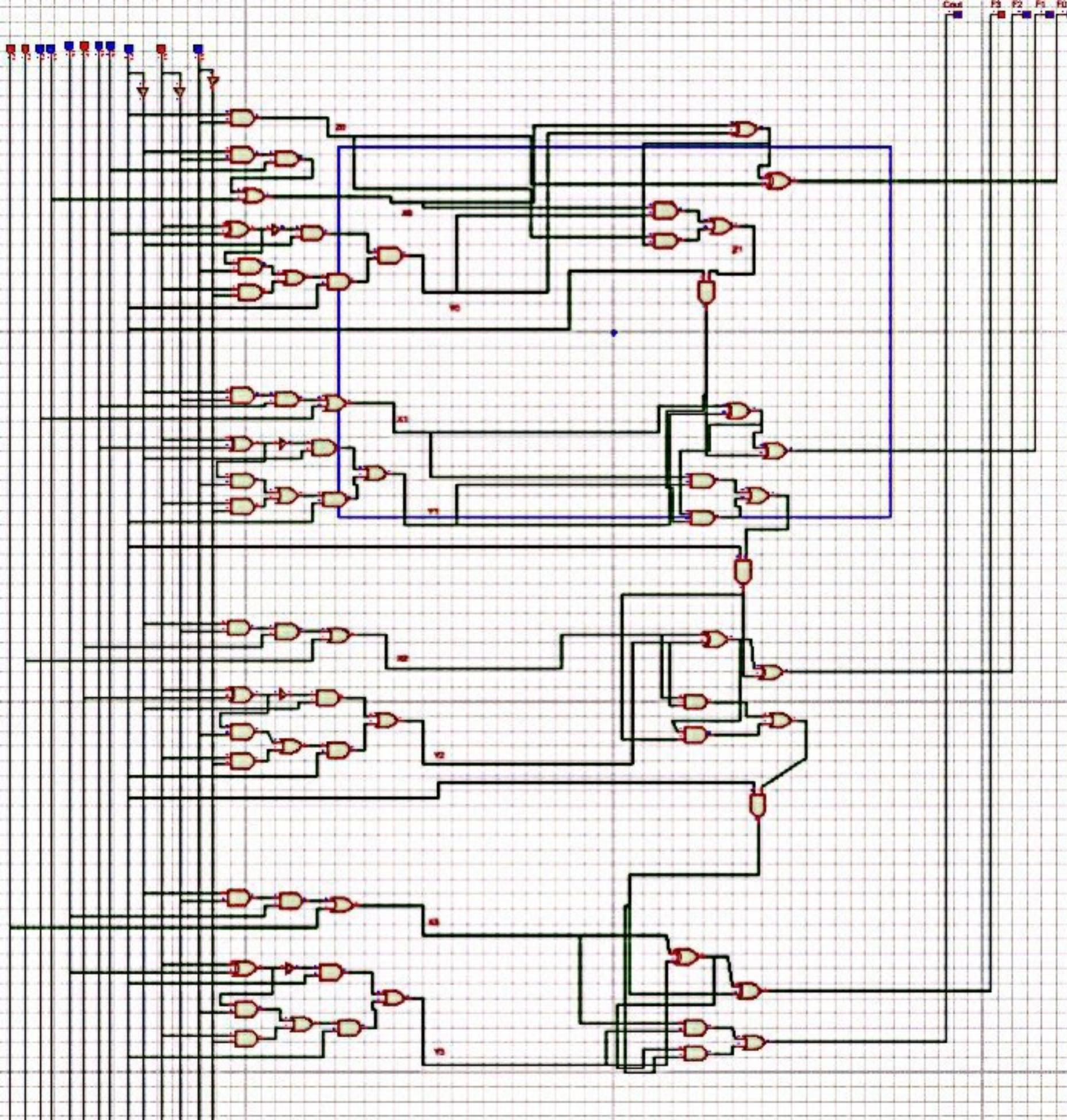
Input												Output			
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	$Cout$	F_3	F_2	F_1	F_0
			0	0	0	0	1	0	1	1	0	0	0	0	0
0	0	X	0	0	1	0	1	1	1	1	0	0	0	1	0
			0	1	1	1	0	0	0	1	1	0	0	0	1

For $A_i \timesor B_i$

Input												Output			
S_2	S_1	S_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	$Cout$	F_3	F_2	F_1	F_0
0	1	X	1	1	0	0	0	0	1	0	0	0	1	0	0
			0	1	1	1	0	0	0	1	0	0	1	0	0

Circuit Diagram:





Conclusion:

In this experiment we created an ALU which can perform both arithmetic and logical operations. There were some issues when we implemented the circuit for the first time. At our first attempt when we derived the equation of the input, we simplified those input equations and minimised the equation. Also minimised the use of ICs making it easier to implement. The circuit worked correctly after implementing 4 one bit full adders. All the operation executed without any problems. There was no error in the circuit while simulation.