Body-Biased Operation for Improved MEM Relay Energy Efficiency

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Introduction: The energy efficiency of complementary metal-oxide semiconductor (CMOS) logic circuits is fundamentally limited by the off-state leakage (I_{off}) of the transistors [1]. Mechanical switches can achieve zero I_{off} and hence can overcome this limit, in principle; therefore, scaled relay technologies recently have been investigated for ultra-low-power digital integrated-circuit (IC) applications [2]. In general, IC design involves a trade-off between operating energy, signal propagation delay, and die area (cost); design optimization aims to minimize one of these metrics given constraints on the other two. The methodology for co-optimizing the operating voltage and threshold voltage to minimize energy for a given delay in a fixed CMOS process (*e.g.* minimally sized transistors) has been well established [3]. In this work, a similar methodology is described for scaled logic relay technology.

Logic Relay Design and Operation: The electrostatically actuated six-terminal relay technology developed in [4] has been demonstrated to be well-suited for digital IC applications [5] and therefore is used to experimentally investigate the energy-delay-area tradeoff in this work. **Fig. 1** illustrates the relay structure and operation: When the magnitude of the gate-to-body voltage (V_{GB}) is larger than that of the pull-in voltage (V_{PI}), the electrostatic force (F_{elec}) is sufficient to actuate the body downward such that the channels (narrow metal strips attached to the underside of the body via an insulating dielectric layer) come into physical contact with their respective source and drain (S/D) electrodes, so that current (I_{DS}) suddenly can flow. When V_{GB} is lowered back down below the release voltage (V_{RL}), the spring restoring force of the folded-flexure suspension beams actuates the body upward, such that contact between the channels and their respective S/D electrodes is broken so that I_{DS} suddenly drops to zero. **Fig. 2** shows measured I_{DS} *vs.* V_G characteristics. The hysteretic switching behavior is due to the pull-in phenomenon (which occurs if the as-fabricated contact air-gap thickness g_d, *i.e.* the vertical displacement of the body in the ON state, is greater than 1/3 of the actuation air-gap thickness g_0) and is exacerbated by contact surface adhesive force.

Effect of Body Biasing on Relay Performance: A body bias voltage (V_B) can be used to pre-actuate the body downward to reduce the contact gap thickness (by g_x), so that a smaller gate voltage V_G and hence less energy (E) is required to switch ON the relay:

$$E = V_{GB}(C_{ON}V_{GB} - C_{OFF}|V_B|) = \frac{\varepsilon A_{ACT}}{g_0 - g_d}{V_{GB}}^2 - \frac{\varepsilon A_{ACT}}{g_0 - g_x}V_{GB}|V_B| \qquad (1)$$

If V_G is reduced with body biasing (to maintain constant V_{GB}), however, the average velocity of the body decreases [6] so that the relay turn-on delay (τ_{ON}) increases with decreasing E, as shown in **Fig. 3**. Alternatively, if V_G is kept constant, body biasing can be used to reduce τ_{ON} − but at a significant cost of increased E − as shown in **Fig. 4**. Note that $|V_B|$ is constrained to be no greater than V_{RL}, to ensure that the relay is in the OFF state at $V_G = 0$. Calibrated simulations (**Fig. 4b**) indicate that optimal energy-delay tradeoff is achieved by co-optimizing V_B and V_G.

NEM Relay Energy-Delay-Area Co-Optimization: An advanced CMOS back-end-of-line process for air-gapped interconnects [7] can be adapted for fabrication of nanometer-scale vertically oriented electro-mechanical (NEM) relays with very small footprint [8]. For sub-5 nm CMOS process technology, the smallest electrode spacing is projected to be 10 nm [9], which would correspond to the minimum value of g_d. A_{ACT} = 1 μm^2 can be achieved within a compact footprint (< 0.1 μm^2) by using multiple layers of interconnect (**Fig. 5**). For minimum switching energy, V_B should be set to $-V_{RL}$ (cf. Fig. 3). The minimum value of τ_{ON} for a given value of E is then obtained by first calculating the corresponding value of V_G (using Eqn. (1)) and then co-optimizing the values of g_0 and k_{eff}, essentially determining V_{PI}. τ_{ON} can be solved numerically and the optimal combination of (g_0, k_{eff}) found using the conjugate gradient method [10]. For an optimally designed relay implemented in sub-5 nm technology, sub-50 mV operation with sub-100 ns switching delay and sub-0.1 μm^2 footprint is projected, for $|V_B| \leq 1$ V.

Conclusion: Body biasing is an effective means for dynamically adjusting the energy-delay tradeoff (*i.e.* for lowering the switching energy or improving the switching speed) of a relay, and is key to minimizing the switching energy across a wide range of switching delay.

Acknowledgments:

This work was supported in part by the National Science Foundation (Award #0939514). A. Peschot gratefully acknowledges post-doctoral fellowship support from the Direction générale de l'armement (DGA).

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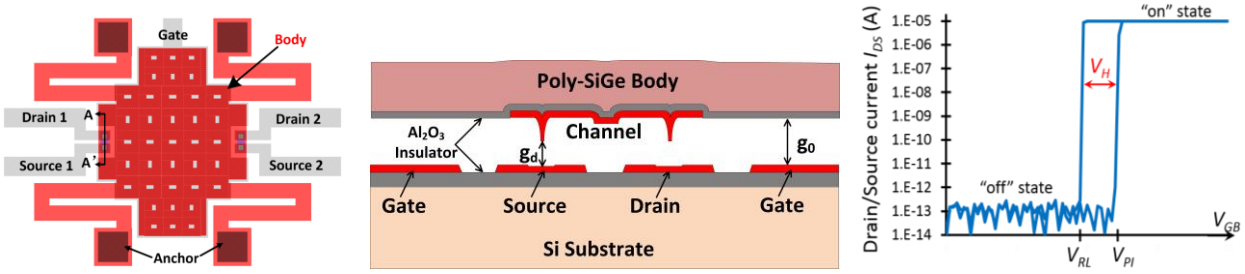


Figure 1. 6-terminal MEM relay developed for digital logic applications: (a) schematic plan view, (b) AA' cross-section, (c) representative *I-V* characteristics.

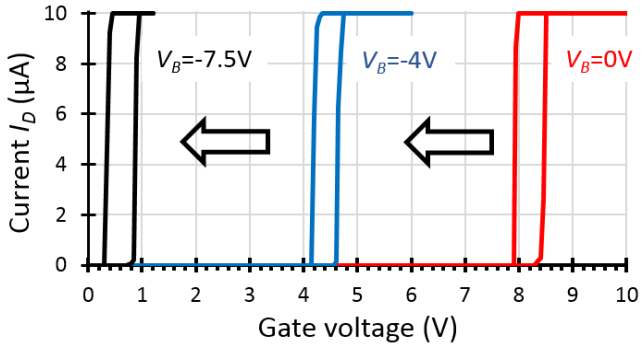
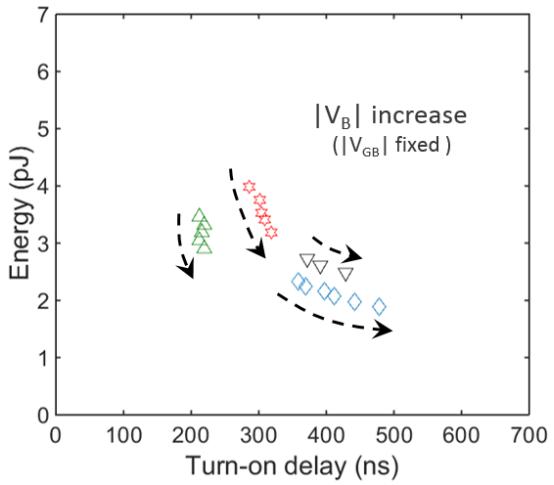


Figure 2. Measured relay *I-V* characteristics demonstrating how an applied body voltage (V_B) reduces the gate voltage (V_G) and hence the energy required to operate the relay.



Relay:	1 ◊	2 ✡	3 Δ	4 ▽
A_{ACT} (μm²)	195	195	340	318
k_{eff} (N/m)	48	96	83	65
V_{PI} (V)	11	17	12	11

Figure 3. Measured effect of body biasing on switching speed, **with V_{GB} fixed**, for 4 different relays. Although body-biasing is effective for lower the switching energy, the turn-ON delay increases with increasing $|V_B|$ due to lower average velocity.

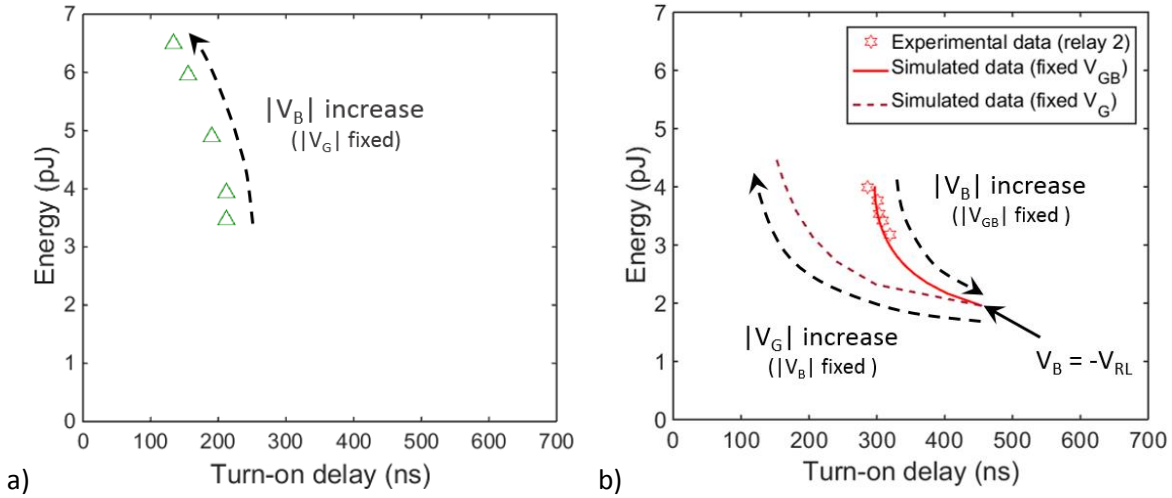


Figure 4. (a) Measured effect of body biasing on switching speed, **with V_G fixed**. The turn-ON delay decreases with increasing body bias voltage, but at the cost of increased switching energy. (b) Numerical simulations of relay switching energy *vs*. delay, calibrated to the experimental data for Relay 2 (cf. Fig. 3). By applying the maximum allowable body bias voltage ($V_B = -V_{RL}$), lower energy is achieved for a given delay.

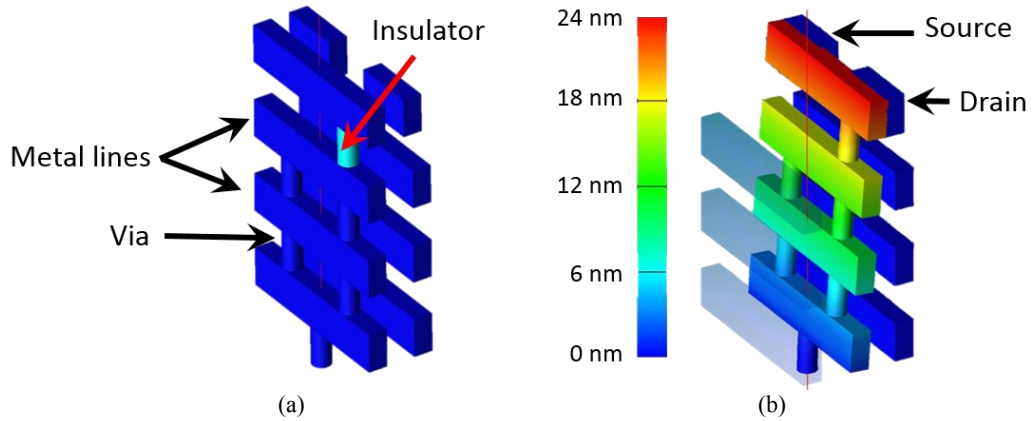


Figure 5. Compact NEM relay design implemented using 4 layers of metal interconnect in a CMOS back-end-of-line process. Note that the source and drain electrodes are co-planar (vertically) with the gate electrode. (a) $V_{GB} = 0$, and (b) $V_{GB} = V_{PI}$.