DESIGN AND FABRICATION OF ELECTROSTATICALLY ACTUATED NANOELECTROMECHANICAL RELAYS AND THEIR INTEGRATION WITH CMOS

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Soogine Chong
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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Philip Wong, Primary Adviser

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Roger Howe

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Subhasish Mitra

Approved for the Stanford University Committee on Graduate Studies.

Patricia J. Gumport, Vice Provost Graduate Education

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Abstract

Over the past few decades, CMOS transistor scaling has resulted in a dramatic increase in computing power. However, continuing the voltage scaling is becoming increasingly difficult because of the increase in subthreshold leakage. This increase is inevitable with threshold voltage scaling, since the subthreshold slope is theoretically limited to be larger than 60 mV/dec at room temperature. Nanoelectromechanical (NEM) relays are promising devices to overcome this voltage scaling issue because of their sharp on/off transition characteristics and zero off-state leakage. However, these devices have long switching times due to their long mechanical delays. By combining NEM relays with CMOS, it is possible to capitalize on the benefits of each technology.

In the first part of this work, a novel CMOS–NEM static random access memory (SRAM) cell design is proposed, in which three-terminal (3T) NEM relays replace the pull-down NMOS transistors of a conventional six-transistor (6T) CMOS SRAM cell. This SRAM cell utilizes the sharp on/off transition characteristics and hysteretic properties of NEM relays to dramatically increase the cell stability compared to the conventional CMOS 6T SRAM cells. It also utilizes the zero off-state leakage of NEM relays to significantly decrease static power dissipation. The structure is designed so that the relatively long mechanical delay of the NEM relays does not result in performance degradation. To simulate this novel design, various NEM relay parameters are modeled and calculated to build a Verilog-A model of a 3T NEM relay.

Compared to a 65 nm CMOS 6T SRAM cell, when 10 nm-gap NEM relays (pull-in voltage = 0.8 V, pull-out voltage = 0.2 V, on-resistance = 1 kΩ) are integrated, hold and read static noise margin (SNM) improve by approximately two-fold and three-fold, respectively. In addition, static power dissipation decreases by approximately 85 %. The write delay decreases by approximately 60 %, while read delay decreases by approximately 10 %. The advantages in SNM and static power dissipation are expected to increase with scaling.

Despite these advantages, this circuit has not yet been experimentally demonstrated; therefore, in the second part of this work, as an initial step towards the demonstration, the fabrication of NEM relays and their integration with CMOS, is experimentally demonstrated. NEM relays without CMOS are first fabricated and electrically characterized in two different versions: 1) optically patterned devices with larger dimensions, which have a polysilicon structural layer and a metal (platinum or titanium nitride) coating layer, with actuation voltages in the range of 10–80 V and 2) e-beam patterned devices with scaled-down dimensions, which have a single metal (platinum) layer, with actuation voltages in the range of 3–6 V. The scaled down devices are suitable for CMOS–NEM integration, since they have low actuation voltages and a CMOS-compatible fabrication process. With these devices, simple CMOS–NEM integrated circuits — an NMOS transistor driving a NEM relay and a CMOS inverter driving a NEM relay — are fabricated and electrically tested, for the first time, demonstrating the feasibility of CMOS–NEM integration.

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Chapter 1: Introduction

1.1. Limitations of CMOS

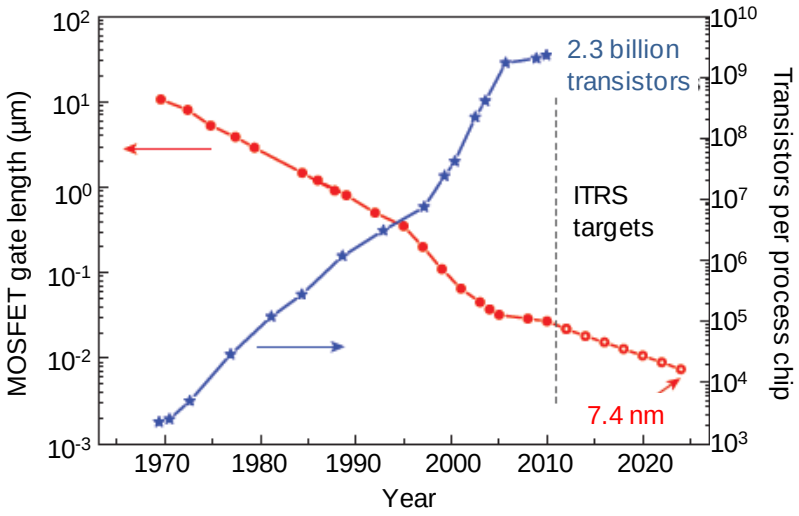

Figure 1-1 Plot showing the gate length of CMOS transistors scaling (red) and the number of transistors per integrated circuit increasing (blue) over several decades. (Adapted from [1].)

Ever since the introduction of integrated circuits in the late 1950s, CMOS transistors scaled according to Moore's prediction with the number of transistors per integrated circuit doubling every two years [2], [1] (Figure 1-1). Although there were some deviations, scaling largely followed the constant-field scaling presented by Dennard et al. in 1974 [3]. As shown Figure 1-2, according to this scaling rule, transistor dimensions, both horizontal and vertical, and operating voltage are all scaled by the same factor, κ. As a result, with scaling, density increases by κ^2, and performance increases by κ, while power density, dominated by the active power

density, remains constant. In other words, scaling brought along the benefit of lower cost (from higher density) and increased performance, without causing a power issue. However, with continued scaling, it has become increasingly difficult to strictly follow this "rule" and thus maintain these benefits simultaneously. One major reason for this is the increase in passive power dissipation.

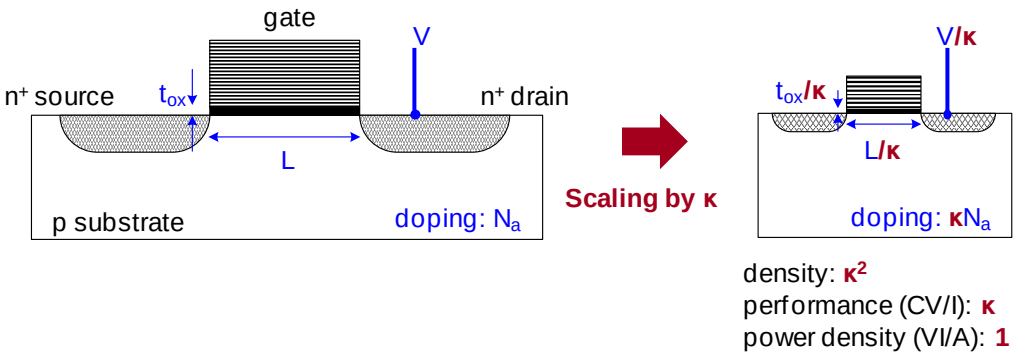

Figure 1-2 Schematic illustrating the constant-field scaling, proposed by Dennard in 1974 [3]. With scaling, density and performance increases, while power density remains constant.

The increased passive power dissipation is due to both increased gate leakage power dissipation and increased subthreshold leakage power dissipation, as shown in Figure 1-3. The power dissipation due to gate leakage increases with thinner gate dielectrics. This issue was alleviated by the transition from using the conventional silicon dioxide (SiO_2) for gate dielectrics to using high-κ materials [4], but the fundamental issue of tunneling current through dielectric remains.

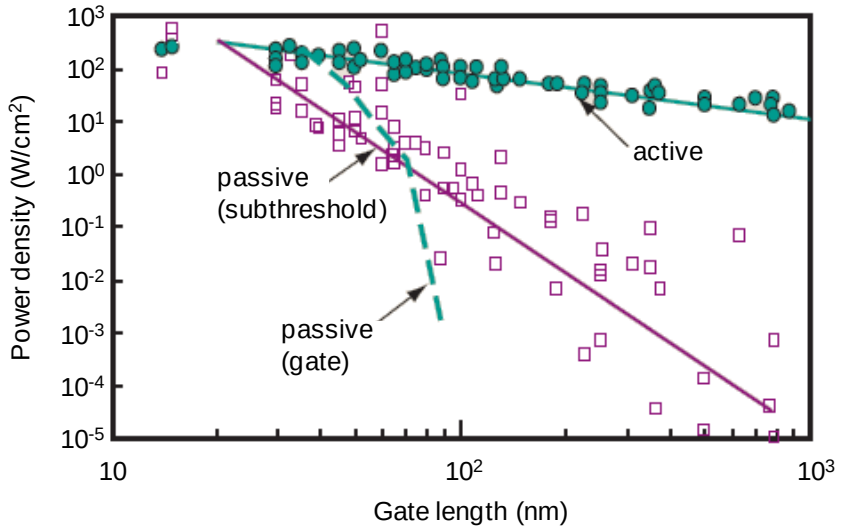

Figure 1-3 Plot of power density versus gate length with data collected from literature for active power density and passive power density. Passive power has become comparable to active power with gate length scaling. (Adapted from [5].)

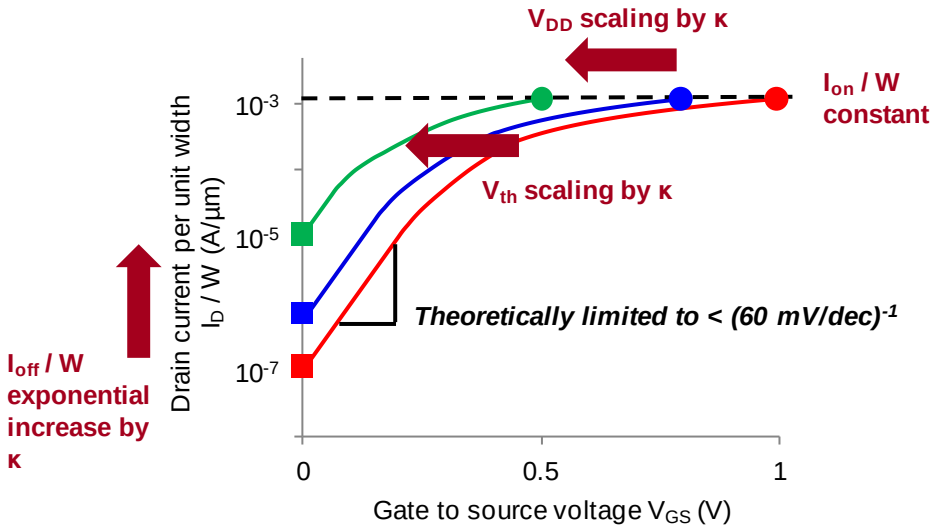

Figure 1-4 Schematic showing the limitation of CMOS voltage scaling. Scaling threshold voltage to maintain on-current (and thus performance) results in an exponential increase in off-current (red → blue → green). The subthreshold slope is limited to 60 mV/dec at room temperature.

The reason for the sharp increase in subthreshold leakage is illustrated in Figure 1-4. If the supply voltage (V_{DD}) scales by κ, in order to obtain the corresponding performance benefit of κ, the on-current per transistor width (I_{on}/W) needs to stay constant. Thus, the threshold voltage (V_{th}) needs to scale by the same factor. V_{th} does not scale by simply applying the constant-field scaling rules, and doping profiles need to be engineered to achieve the desired V_{th}. Even if V_{th} can be scaled, however, this leads to an exponential increase by κ in the off current per transistor width (I_{off}/W). This is a fundamental issue with CMOS transistors, since the subthreshold slope is theoretically limited to be no steeper than 60 mV/dec at room temperature by thermodynamic principles. Therefore, although a decrease in V_{DD} leads to a relatively constant active power density, the passive power density increases exponentially, so that the passive power density becomes comparable to the active power density with scaling, as shown in Figure 1-3. As a result, it has become increasingly difficult to scale V_{DD} as aggressively as in the past, eventually limiting the scalability of CMOS transistors.

Since the limited scalability is a fundamental issue with CMOS transistors that cannot be solved by design or material innovations, novel devices need to be introduced to solve this issue. The desirable electrical properties include an abrupt on–off switching and a large on-current to off-current ratio, as shown in Figure 1-5. With such a device, it is possible to obtain low leakage power dissipation even with scaling, and theoretically, to scale V_{DD} down to zero volts, resulting in ultra-low power dissipation. Electromechanical relays have such properties, making them promising devices for low power applications.

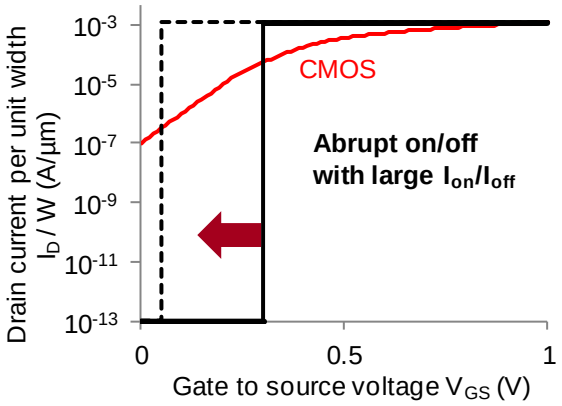

Figure 1-5 Schematic showing desired electrical properties of a novel device, namely 1) abrupt on/off transition and 2) large on-current to off-current ratio, that would allow continuous voltage scaling.

1.2. Electrostatically Actuated Micro/Nano-Electromechanical (M/NEM) Relays

Micro/nano-electromechanical (M/NEM) relays are electrical switches that turn on and off by the mechanical movement of a beam or a plate, with the smallest dimensions in the micro/nano-scale. There are various types of M/NEM relays. By actuation mode, they can be classified into electrostatic, magnetostatic, piezoelectric, and thermal relays [6], [7]. Of these, thermal and magnetostatic relays require a biasing current, which is undesirable for low power applications. Electrostatic relays have shown faster switching compared to piezoelectric relays and are chosen as the type of switches studied in this work.

Figure 1-6 shows a three-terminal (3T) electrostatically actuated M/NEM relay, which consists of a gate (G), a source (S), and a drain (D). In the off state, the beam, or the source, is mechanically separated from the gate and the drain, resulting in no

leakage current. Electrostatic force is applied between the gate and the source to turn the switch on, and, in the on-state, the source makes mechanical contact to the drain, forming a current path.

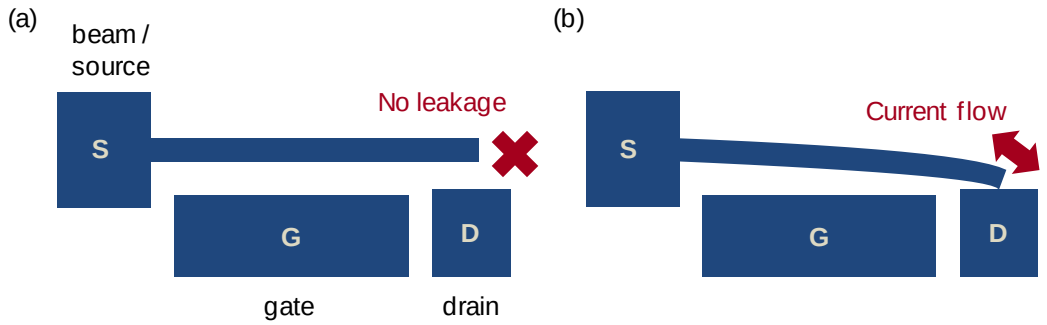

Figure 1-6 Electrostatically actuated three-terminal micro/nano-electromechanical (M/NEM) switches in (a) the off-state and (b) the on-state.

3T NEM relays operate similarly to CMOS transistors, with the current flow between the source and the drain terminals controlled by the bias on the gate. However, they differ in that they have: 1) zero off-state leakage, with all three terminals separated by an air gap in the off-state, 2) sharp on/off transition, performed by the making and breaking of the mechanical contact between the source and the drain, and 3) hysteresis, with the turn-on voltage being larger than the turn-off voltage. As described in Section 1.1, the first two properties are essential for continuous voltage scaling, making electrostatically actuated relays attractive devices for low standby power applications.

Despite the benefits, however, the relays have a low turn-on speed compared to CMOS transistors, because the beam needs to mechanically move in order to turn the device on. Switching speeds on the order of 100 ns have been measured [8], [9],

whereas that of scaled NEM relays with an operating voltage of around 1 V is projected to be on the order of 1 ns [10]. A 1 ns delay is still several orders of magnitude larger than the intrinsic delay of the state-of-the art MOSFETs, which is on the order of 1 ps[1].

1.3. CMOS–NEM Hybrid Circuits

Because of the long mechanical delay of NEM relays, a direct replacement of all CMOS transistors with NEM relays in current CMOS circuits is inherently too slow. To mitigate this limitation, optimized circuit topologies for all-NEM relay circuits have been proposed [11] and demonstrated [12]. Although these circuits reduce energy dissipation, comparable delay is expected only after assuming a 32-way parallelism. Another approach, the approach taken in this work, is to combine NEM relays with CMOS transistors to capitalize on the advantages of each technology, without the long mechanical delay of the relay being a critical issue.

Previous works include the use of NEM relays as sleep switches in CMOS circuits and CMOS–NEM field-programmable-gate-arrays (FPGAs). For NEM relay sleep switches, the zero off-state leakage of NEM relays allows three orders of magnitude lower off-current [13]. The slow switching speed is not a critical issue, since they do not switch often. For CMOS–NEM FPGAs, NEM relays are used as programmable

[1] According to the ITRS 2011 update [11], 2011 HP (high performance) 24 nm gate-length NMOSFETs and LSTP (low standby power) 30 nm gate-length NMOSFETs have intrinsic delays (CV/I) of 0.64 ps and 2.25 ps, respectively.

routing switches, one NEM relay replacing each SRAM and MOSFET pair in a CMOS-only FPGA [14]. Since the state of the NEM relay does not need to change once configured, the long switching time is not an issue, while the zero leakage of NEM relays enables a 37 % decrease in leakage power dissipation. These two works apply NEM relays to applications where the slow switching speed is not critical to the standard operation of a circuit.

In this work, a CMOS–NEM hybrid circuit, namely a CMOS–NEM static-random-access memory (SRAM) cell, was designed, where the combination of NEM relays with CMOS does not result in the overall performance degradation. In addition, the integration of NEM relays with CMOS, a technology that needs to be developed in order to realize the CMOS–NEM hybrid circuits, is experimentally demonstrated.

1.4. Thesis overview

In Chapter 2, modeling and calculation of various NEM relay parameters are discussed. Based on these parameters, a Verilog-A model of a 3T NEM relay is presented. In Chapter 3, a novel CMOS–NEM hybrid SRAM cell is introduced with simulation, results using this model. In the following chapters, the experimental demonstration of NEM relays is presented. Fabrication and electrical measurements of 1) optical lithography patterned, scaled-up devices are presented in Chapter 4, 2) e-beam lithography patterned, CMOS-compatible devices are presented in Chapter 5, and 3) simple CMOS–NEM integrated circuits are presented in Chapter 6.

Chapter 2: Nanoelectromechanical (NEM) Relay Modeling

2.1. Basic Operation

Figures 2-1 to 2-4 illustrate the basic operations of a three-terminal (3T) nanoelectromechanical (NEM) relay in detail. They demonstrate how the balance of forces, the movement of the beam, and the current change as the voltage between the gate and the source (V_{GS}) increases and decreases.

As shown in Figure 2-1, as V_{GS} initially increases from zero volts, the electrostatic force (F_{elec}) pulls the beam towards the gate, and the beam deflects to the point where the elastic force (F_{elas}) of the beam is equal to F_{elec}. Although the beam is moving towards the drain with increasing V_{GS}, because it is not contacting the drain, there is no current flow between the source and the drain.

As the beam deflects—that is, as the distance between the beam and the gate (g) decreases—F_{elec} increases inversely proportional to g^2, whereas F_{elas} increases inversely proportional to g. Because F_{elec} increases faster than F_{elas}, beyond a certain point, F_{elas} can no longer balance F_{elec}. Instability occurs, and the beam collapses to make contact with the drain, and the drain current (I_D) increases abruptly as shown in

Figure 2-2. This is called "pull-in" and the voltage at which this phenomenon occurs the "pull-in voltage" (V_{pi}). Notice that the drain electrode is designed to be closer to the beam than the gate electrode to ensure that the beam does not touch the gate when pulled-in.

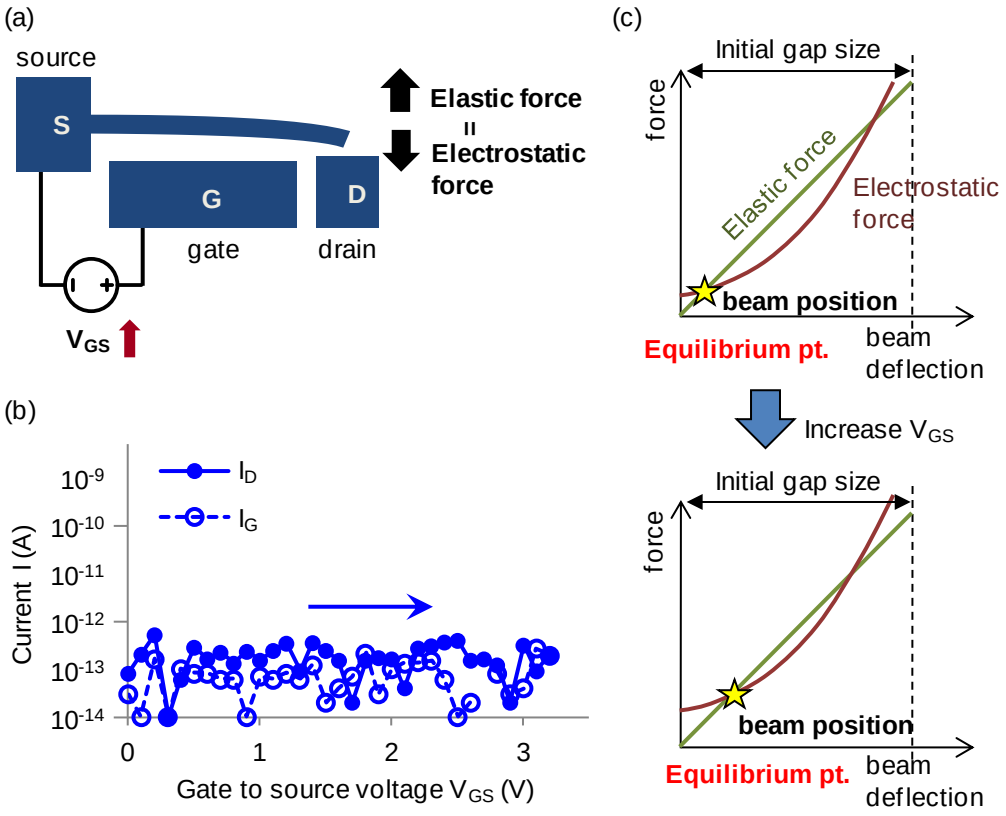

Figure 2-1 (a) Test setup and beam position, (b) electrical characteristics plotting drain and gate current (I_D and I_G) versus gate to source voltage (V_{GS}), and (c) plot of force versus beam deflection showing balance of forces, as V_{GS} increases from 0 V to a voltage less than the pull-in voltage (V_{pi}).

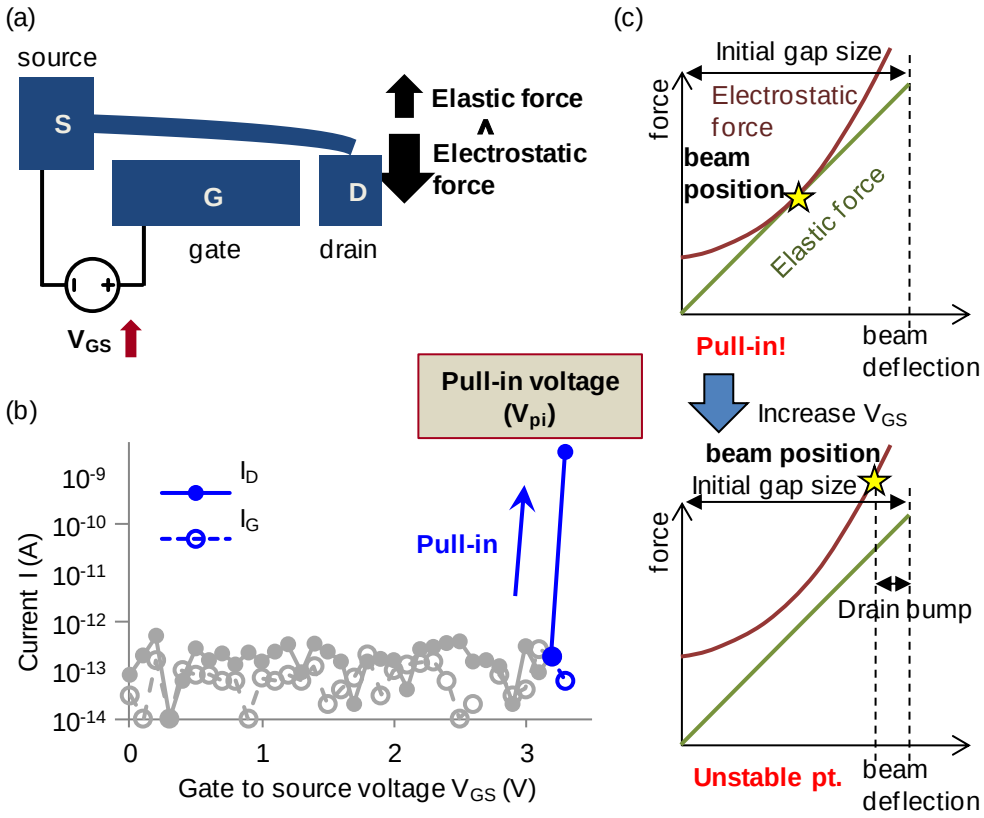

Figure 2-2 (a) Test setup and beam position, (b) electrical characteristics plotting I_D and I_G versus V_{GS}, and (c) plot of force versus beam deflection showing balance of forces, as V_{GS} increases from V_{pi} to the supply voltage (V_{DD}).

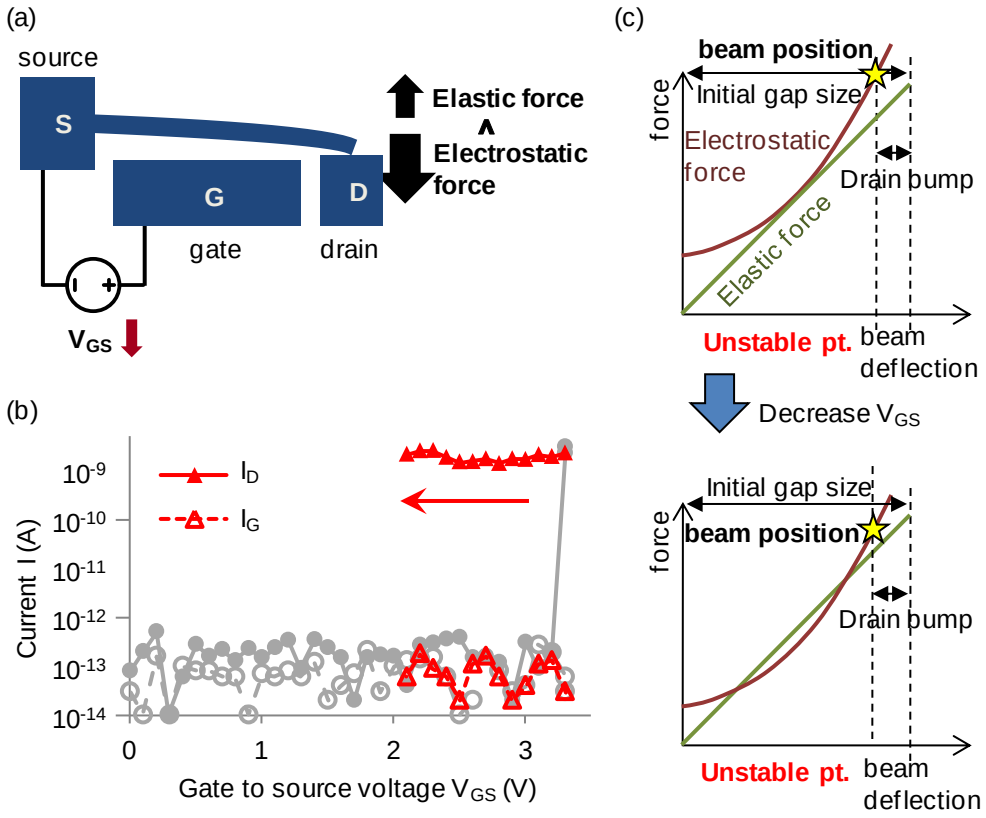

Figure 2-3 (a) Test setup and beam position, (b) electrical characteristics plotting I_D and I_G versus V_{GS}, and (c) plot of force versus beam deflection showing balance of forces, as V_{GS} decreases from V_{DD} to a voltage greater than the pull-out voltage (V_{po}).

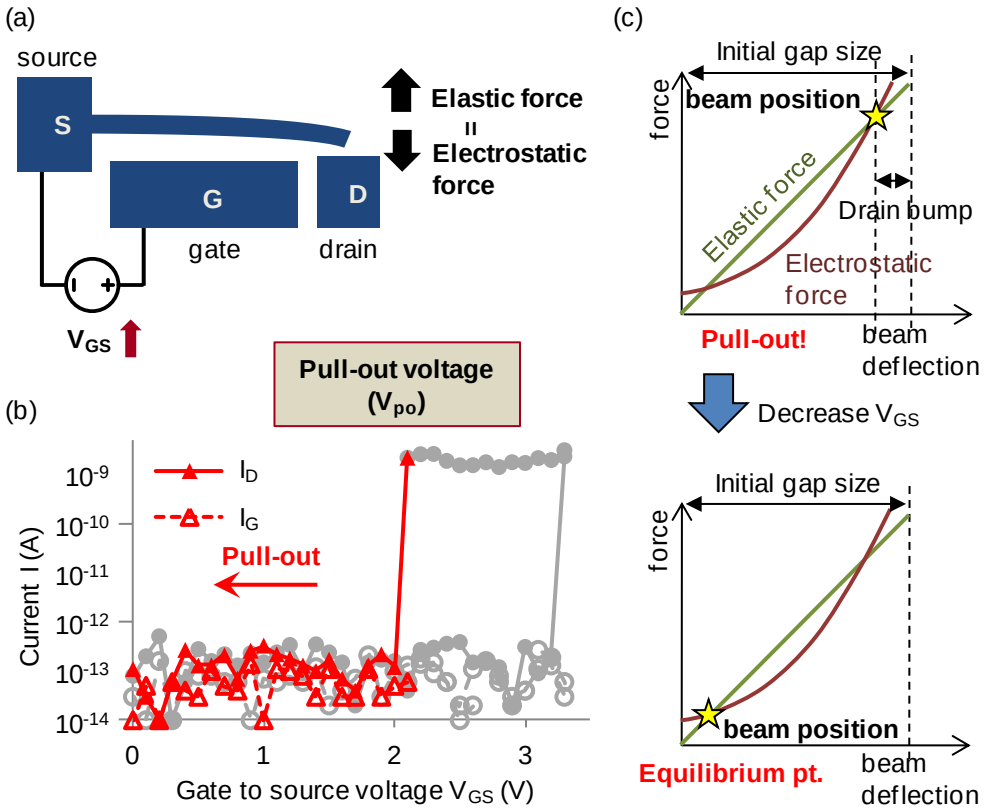

Figure 2-4 (a) Test setup and beam position, (b) electrical characteristics plotting I_D and I_G versus V_{GS}, and (c) plot of force versus beam deflection showing balance of forces, as V_{GS} decreases from V_{po} to 0 V.

As shown in Figure 2-3, as V_{GS} decreases from beyond V_{pi}, the beam stays in contact with the drain, even at $V_{GS} < V_{pi}$. This is because the beam was pulled in as a result of an instability, so that even at the same V_{GS}, the position of the beam is closer to the gate. Thus, F_{elec} is too large for F_{elas} to balance, and there is no equilibrium point.

When F_{elas} can finally balance F_{elec}, the beam loses contact with the drain, and there is no current between the source and the drain, as shown in Figure 2-4. This is called "pull-out" and the voltage at which this happens the "pull-out voltage" (V_{po}). Notice

that throughout this sweep, there is no gate leakage current, as expected, since there is no mechanical contact between the beam and the gate.

2.2. Modeling of NEM Relay Parameters[1]

2.2.1. Pull-in voltage (V_{pi})

As mentioned in Section 2.1, the position of the beam, and thus V_{pi}, is determined by a balance between F_{elec} and F_{elas}. With a one-dimensional (1D) model of MEM switches, F_{elec} is expressed as [15]

$$F_{elec} = \frac{1}{2} {V_{GS}}^2 \frac{d C_{GS}(g)}{dg} = -\frac{1}{2} \frac{\varepsilon t L {V_{GS}}^2}{g^2} \quad \text{Eq. 2-1}$$

where ε is the permittivity of air, C_{GS} is the capacitance between the gate and the source (or the beam), t is the thickness of the beam, L is the length of the beam, which is assumed to be equal to the length of the gate, and $g = (g_g - v)$ is the gap between the gate and the beam. The parameters are as labeled in Figure 2-5. This model assumes a constant gap between the beam and the gate electrode throughout the length of the beam, even as the beam deflects, as shown in Figure 2-5a, overestimating F_{elec}. F_{elas} of the beam is expressed as [6]

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[1] Part of this chapter is taken from S. Chong, K. Akarvardar, R. Parsa, J.-B. Yoon, R. T. Howe, S. Mitra, H.-S. P. Wong, "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," *IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, 2009, pp.478-484.

$$F_{ela} = k(g_g - g)$$ Eq. 2-2

where g_g is the gap between the gate and beam in the off-state, and k is the spring constant of the beam. k is calculated by

$$k = \frac{2Etw^3}{3L^3}$$ Eq. 2-3

where E is the Young's modulus, and w is the width of the beam.

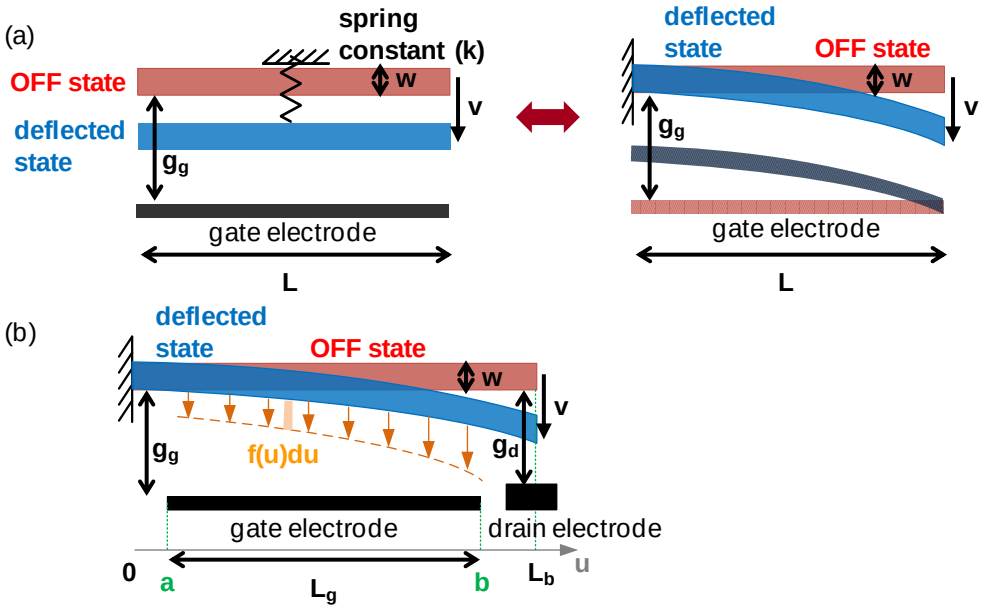

Figure 2-5 Schematic of (a) two equivalent one-dimensional (1D) beam deflection models, where equal attractive force between the beam and the actuating gate electrode is assumed throughout the length of the beam and (b) a two-dimensional (2D) beam deflection model, where a varying attractive force per unit length (f(u)) is assumed from u = a to u = b. Device dimension parameters are as labeled. t is the thickness of the beam (not shown in the schematic).

A simple 1D model of V_{pi} [6] is derived by setting $F_{elec} = F_{elas}$ and $\frac{dF_{elec}}{dg} = \frac{dF_{elas}}{dg}$. The resulting expression for V_{pi} is

$$V_{pi} = \sqrt{\frac{8k{g_g}^3}{27\varepsilon tL}} \qquad \text{Eq. 2-4}$$

Although the 1D model serves as a useful tool for a quick estimation, for a more accurate modeling, a two-dimensional (2D) model was used in this work. This model takes into account the varying attractive forces acting along the length of the beam and the resulting varying beam deflection along the length of the beam [16], as shown in Figure 2-5b. In this model, the deflection of the beam at point u = x, v(x), is determined by

$$v(x) = \begin{cases} \frac{x^2}{6EI}\int_a^b f(u)(3u-x)du & (0 \le x \le a) \\ \frac{x^2}{6EI}\int_x^b f(u)(3u-x)du + \frac{1}{6EI}\int_a^x f(u)u^2(3x-u)du & (a \le x \le b) \\ \frac{1}{6EI}\int_a^b f(u)u^2(3x-u)du & (b \le x \le L_b) \end{cases} \qquad \text{Eq. 2-5}$$

where the gate electrode spans from u = a to u = b. I is the moment of inertia, calculated by

$$I = \frac{tw^3}{12} \qquad \text{Eq. 2-6}$$

f(u) is the force per unit length, and for the electrostatic force per unit length (f_{elec}),

$$f_{elec}(u) = \frac{1}{2}{V_{GS}}^2 \frac{\varepsilon t}{(g_g - v(u))^2} \qquad \text{Eq. 2-7}$$

In order to determine the deflection of the tip of the beam at x = L_b, where L_b is the length of the beam, from Eq. 2-5,

$$v(L_b) = \frac{1}{6EI}\int_a^b f(u)u^2(3L_b - u)du \qquad \text{Eq. 2-8}$$

Eq. 2-8 cannot be solved analytically, because f(u) is a function of v(u). Therefore, Eq. 2-5 and Eq. 2-7 need to be solved iteratively until the solution converges to solve for v(L_b). As V_{GS} increases from zero volts, the smallest voltage at which there is no solution for v(L_b) is V_{pi}.

In addition to F_{elec}, van der Waals force (F_{vdw}) also needs to be accounted for when working with devices with dimensions in the tens of nanometer range. F_{vdw} is modeled as [17]

$$F_{vdw} = \frac{tL_gA_h}{6\pi(g_g - v)^3} \qquad \text{Eq. 2-9}$$

where A_h is the Hamaker constant, and L_g is the length of the gate electrode.

Figure 2-6 shows the difference in V_{pi} calculated using a 1D model and a 2D model, as well as the effect of including F_{vdw}. The calculation assumed a silicon beam, which has E = 170 GPa and A_h = 1.6 eV. L (in the 1D model) and L_g (in the 2D model) were both fixed to 260 nm. When w = g_g = 10 nm, including F_{vdw}, the 1D model V_{pi} was approximately 25 % smaller than the 2D model V_{pi}. By excluding F_{vdw} from the 2D model, V_{pi} increased by greater than 35 %. While the discrepancy between the 1D model and the 2D model decreased with scaling, the effect of F_{vdw} significantly increased as the gap becomes smaller than around 15 nm. In conclusion,

for relays with small gaps enabling a low-voltage operation, accounting for F_{vdw} is required, while the use of a 2D model is recommended for more accurate results.

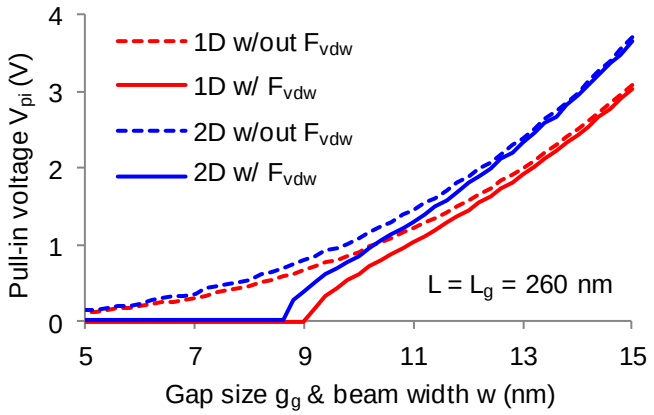

Figure 2-6 Plot of V_{pi} versus gap size (g_g), which is equal to beam width (w), comparing V_{pi} calculated using 1D and 2D models with and without van der Waals force (F_{vdw}). The length of the gate electrode (L = L_g) was fixed to 260 nm. A silicon beam beam was assumed with Young's modulus (E) of 170 GPa and Hamaker constant (A_h) of 1.6 eV. Accounting for F_{vdw} is required for small gaps relevant to low-voltage NEM relays, while using a 2D model is recommended for more accurate results.

2.2.2. Pull-out voltage (V_{po})

Using a simple 1D model of MEM switches, V_{po} is calculated with the following equation [6]

$$V_{po} = \sqrt{\frac{2k{g_d}^2(g_g - g_d)}{\varepsilon t L}} \qquad \text{Eq. 2-10}$$

where g_d is the gap between the beam and the drain in the off-state. However, while this 1D model takes into account only F_{elec} and F_{elas}, V_{po} heavily depends on surface forces that are exerted while the beam is in contact with the drain, decreasing V_{po}

below what is calculated with Eq. 2-10. These forces are dependent on the area of the contacting surface, as well as the material properties at the contact, which is difficult to predict and model. An accurate model becomes even more difficult to develop with current passing through the contact. Calculation of V_{po} requires specific details about the contact, which still need to be understood, and is beyond the scope of this work.

2.2.3. On resistance (R_{on})

The NEM relay on resistance (R_{on}) is a combination of the beam resistance and the contact resistance. Typically, the beam resistance can be made very small compared to the contact resistance by using materials with high conductivity, so that the contact resistance dominates R_{on}.

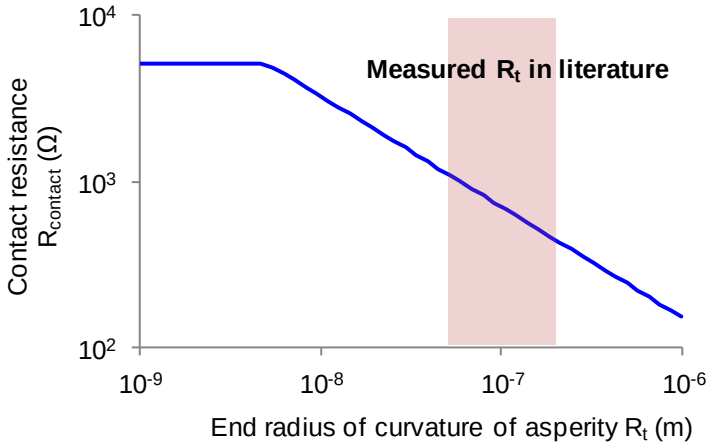

Figure 2-7 Plot of calculated gold-to-gold contact resistance ($R_{contact}$) for varying end radius of curvature of asperity (R_t), showing calculated $R_{contact}$ of around 1 kΩ, based on measured R_t in literature [18]. For gold, E = 78 GPa, Poisson's ratio = 0.44, mean free path = 38.3 nm, resistivity = 22.14 nΩ·m, and hardness = 1.77 GPa were used.

Contact resistance is dependent on many factors, such as the contact force, the number and radius of contact spots, and the end radius of curvature of asperities (R_t)

associated with the contact [18]. The calculated contact force [19] with g_d = 5 nm was in the 0.1 nN range, from which contact resistance could be estimated. The contact was assumed to be gold-to-gold, and only one contact spot was assumed to calculate an upper bound of the contact resistance, although multiple contact spots are possible. Depending on R_t, the contact resistance can significantly vary as shown in Figure 2-7. Detailed calculation of the contact force and contact resistance can be found in Appendix A. Based on measured R_t in [18], which was in the range of 50–200 nm, the calculated contact resistance was around 1 kΩ. Although a rough estimate was made using various assumptions, there can be a large difference in R_{on}, depending on the properties of the contact. Therefore, in this work, R_{on} was considered a variable with a wide range of values, being a device design parameter that must be optimized.

2.2.4. Capacitance ($C_{gs,on}$ and $C_{gs,off}$)

The gate to source (or beam) capacitance in the off-state ($C_{gs,off}$), neglecting fringing capacitance, was calculated using a parallel plate approximation, with

$$C_{gs,off} = \frac{W\varepsilon L_g}{g_g} \qquad \text{Eq. 2-11}$$

The gate to source capacitance in the on-state ($C_{gs,on}$) was calculated as

$$C_{gs,on} = \int_a^b \frac{W\varepsilon}{g_g - v(u)} du \qquad \text{Eq. 2-12}$$

where v(u) is the estimated beam deflection after pull-in, using the 2D model described in Section 2.2.1. The beam deflection after pull-in was estimated by finding a ratio γ between g_d and the beam tip deflection just before pull-in and multiplying γ to the deflection along the beam just before pull-in.

2.2.5. Mechanical delay (τ_{mech})

τ_{mech} was estimated using a 1D model of MEM switches as [6]

$$\tau_{mech} \sim 3.67 \frac{V_{pi}}{V_{DD}\omega_0} \quad \text{Eq. 2-13}$$

where V_{DD} is the supply voltage, and ω_0 is the resonant frequency of the beam, calculated by

$$\omega_0 = \sqrt{\frac{k}{m}} \quad \text{Eq. 2-14}$$

where m is the mass of the beam. The effective mass is around 0.35–0.45 of the actual mass of the beam.

2.3. NEM Relay Verilog-A Model

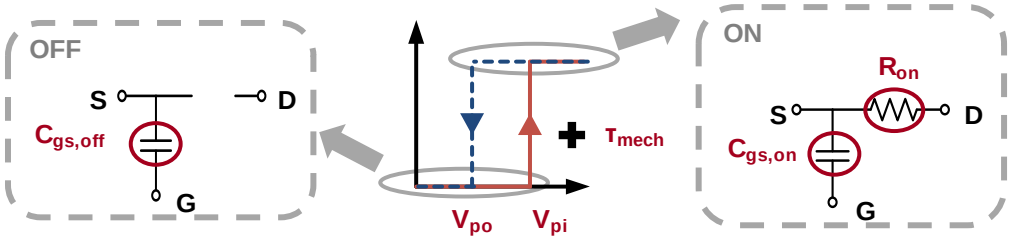

Figure 2-8 Schematic describing the Verilog-A model of a three-terminal (3T) NEM relay in the off-state and the on-state. The relay switches from the off-state to the on-state after a specified mechanical delay.

For a circuit analysis of CMOS–NEM hybrid circuits, a NEM relay model is needed. For this purpose, a simple NEM relay Verilog-A model was developed as

shown in Figure 2-8 (The Verilog-A code can be found in Appendix B[1]). In the off-state, the NEM relay was modeled as an open circuit between the source and the drain, with a capacitance $C_{gs,off}$, between the gate and the source. When the V_{GS} exceeds V_{pi}, it takes τ_{mech} for the relay to turn on. In the on-state, the NEM relay was modeled as having a resistor with resistance R_{on} between the source and the drain and a capacitance $C_{gs,on}$, between the gate and the source. When V_{GS} becomes smaller than V_{po}, the relay immediately switches to the off-state.

Based on the desired V_{DD}, and consequently the desired V_{pi}, the appropriate device dimensions and materials can be chosen. From these, $C_{gs,on}$, $C_{gs,off}$, and τ_{mech} can be calculated. For a lack of an accurate model, V_{po} is set to an arbitrary value smaller than V_{pi}, and R_{on} is set as a variable.

Future work includes a more detailed NEM relay model for a more accurate analysis. Improvements can be made in modeling the R_{on}. In this work, a constant R_{on} was assumed, but in reality, R_{on} changes with contact force and thus with the gate voltage overdrive (V_{GS}-V_{pi}).

2.4. Conclusion

The operation of a NEM relay is governed by the balance of forces, mainly F_{elec} and F_{elas}. Simple models and equations enable the estimation of NEM relay key parameters, including V_{pi}, $C_{gs,on}$, $C_{gs,off}$, and τ_{mech}, while it is more difficult to estimate

[1] Implementation of the Verilog-A model was done in collaboration with Kamal Aggarwal (Stanford University).

V_{po} and R_{on}. The key parameter, V_{pi}, can be estimated more accurately by using a 2D model, which takes into account different deflections along different points of the beam, and by including the effect of F_{vdw}. Based on these models, a Verilog-A model was developed, which can be used for simulations of CMOS–NEM hybrid circuits.

Chapter 3: CMOS–NEM Hybrid Applications – CMOS–NEM Static Random Access Memory (SRAM)[1]

3.1. Introduction

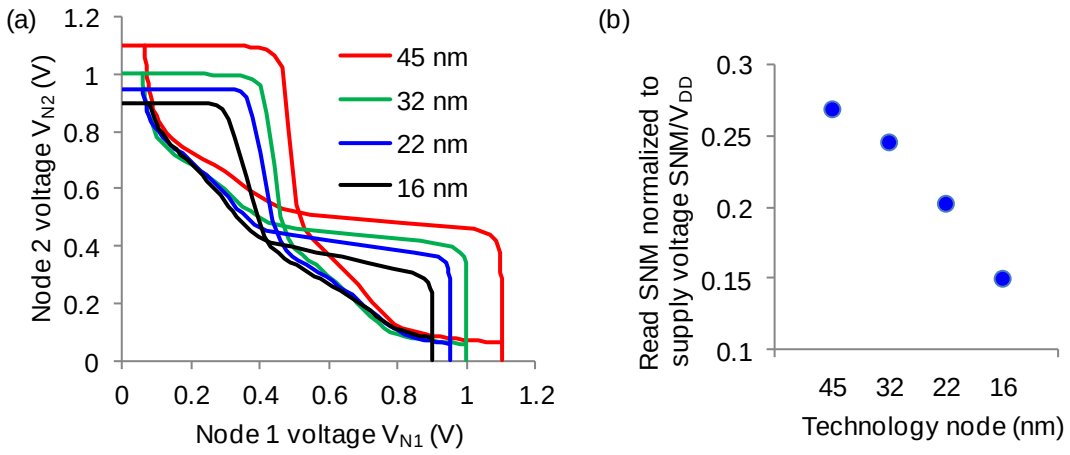

Figure 3-1 Simulation result showing the READ mode (a) butterfly curve and (b) static noise margin (SNM) normalized to the supply voltage (V_{DD}) versus technology node of a conventional CMOS six-transistor (6T) static random access memory (SRAM) cell. The noise margin with respect to V_{DD} is expected to decrease with scaling.

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[1] Part of this chapter is taken from S. Chong, K. Akarvardar, R. Parsa, J.-B. Yoon, R. T. Howe, S. Mitra, H.-S. P. Wong, "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," *IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, 2009, pp.478-484.

Scaling conventional CMOS six-transistor (6T) static random access memory (SRAM) cells while maintaining cell stability is becoming increasingly challenging, due to limitations inherent in the structure. Achieving both a stable read and a stable write, while maintaining a small cell size, has conflicting requirements, resulting in a small noise margin. This problem is aggravated at with scaling as shown with simulation results in Figure 3-1. To overcome these limitations and extend scalability, several approaches have been proposed, including (1) modifying the supply voltage (for example, using dual supplies, adaptive read/write supply, or word-line and bit-line pulsing[20]), (2) adding more transistors to decouple READ and WRITE (making it a 7T [21],[22], 8T [23],[24], or even a 10T [25] SRAM cell), (3) using asymmetric SRAM cells to decouple READ and WRITE [26], and (4) having additional transistors to implement hysteresis using CMOS [27],[28]. Although these methods are successful in improving the stability, it is at the cost of an increased cell size and/or the use of a different peripheral circuitry from a conventional CMOS 6T SRAM cell.

In this work, a non-CMOS device, a three-terminal (3T) nanoelectromechanical (NEM) relay, was incorporated to overcome the inherent limitations of conventional CMOS 6T SRAM cells. A hybrid integration of NEM relays and CMOS transistors is proposed, in which benefits can be gained by merely replacing the pull-down MOSFETs of a conventional CMOS 6T SRAM cell as shown in Figure 3-2. The infinite subthreshold slope and hysteretic properties of NEM relays can improve the cell stability, while the zero off-state leakage can decrease leakage power dissipation. In addition, by fabricating NEM relays on top of the CMOS devices, the cell area can be minimized. The advantages were verified through circuit simulations. The key

insight in this proposed design is that the relatively long mechanical delay of the NEM relay does not limit the performance of this hybrid CMOS-NEM SRAM cell.

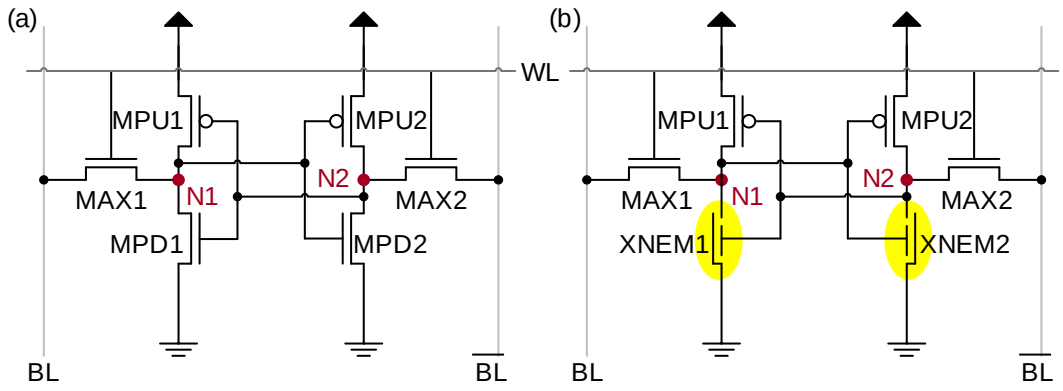


Figure 3-2 Schematic of (a) a conventional CMOS 6T SRAM cell and (b) a CMOS–NEM hybrid SRAM cell with NEM relays replacing the pull-down NMOSFETs.

3.2. Simulation Methodology

For CMOS transistors, 65 nm technology node CMOS (generated using the Predictive Technology Model (PTM) [29], based on [30]) with a physical gate length of 34 nm and an effective gate length of 22 nm was used. The threshold voltages were 400 mV and -400 mV for the NMOSFET and PMOSFET, respectively. For the conventional 6T SRAM cells, the widths of the pull-up PMOSFETs (MPU1 and MPU2) and the access NMOSFETs (MAX1 and MAX2) were minimum (65 nm), while the widths of pull-down NMOSFETS (MPD1 and MPD2) were 195 nm (i.e. $\beta = (W/L)_{pull\text{-}down}/(W/L)_{access} = 3$) to ensure a stable READ operation [23]. The transistors are labeled in Figure 3-2.

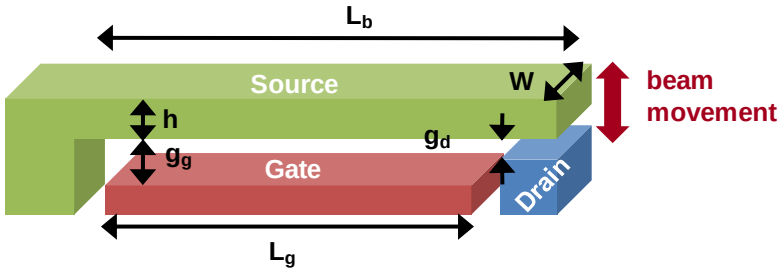


Figure 3-3 Schematic of a vertically actuated 3T NEM relay. Device dimension parameters are as labeled.

For the CMOS–NEM SRAM cells, only the pull-down NMOSFETs (MPD1 and MPD2) in a conventional CMOS 6T SRAM were replaced with NEM relays, using the Verilog-A model described in Section 2.3. No change was needed in the peripheral circuitry. For the NEM relay, a conductive beam or a non-conductive beam with a conductive coating can be used, and the specific material that would best suit this purpose is still under investigation. In this work, a silicon beam was assumed for mechanical properties, and a gold-to-gold contact was assumed for contact properties. Also, a vertically actuated NEM relay was assumed, because of the limitation in lithography to pattern the small gaps and beam widths that would yield the desired operating voltages. Vertically actuated relays operate similarly to laterally actuated relays, except that, for the analysis in Section 2.2, the thickness of the beam, t, becomes the width of the beam, W, and the width of the beam, w, becomes the height of the beam, h, as shown in Figure 3-3. For simulation with a supply voltage (V_{DD}) of 1 V, Table 3-1 summarizes the device dimensions and material properties, and Table 3-2 the resulting Verilog-A input parameters used in this work.

Table 3-1 Beam dimensions/properties that yields a pull-in voltage (V_{pi}) of 0.8 V for operation with V_{DD} = 1 V

Beam Dimensions/Properties					
$L_g = L_b$	W	$h = g_g$	E (Si)	A_h (Si)	ρ (Si)
260 nm	65 nm	10 nm	170 GPa	1.6 eV	2.32 g/cm^3

Table 3-2 Verilog-A input parameters

V_{pi}	V_{po}	$C_{gs,off}$	$C_{gs,on}$	τ_{mech}	R_{on}
0.8 V	0.2 V	15 aF	20 aF	3 ns[1]	10 Ω–100 kΩ

The static and transient characteristics of both the conventional CMOS SRAM cell and the novel CMOS–NEM hybrid SRAM cell were simulated using Cadence Spectre [31]. V_{DD} = 1V was used throughout the work.

3.3. HOLD Mode – Static Noise Margin (SNM)

In the HOLD mode, the two access transistors (MAX1 and MAX2) are turned off, and the values on the two storage nodes are maintained by the two back-to-back inverters. The HOLD static noise margin (SNM) is a metric used for quantifying the stability of an SRAM cell in the HOLD mode [32]. It can be determined from a

[1] The actual mass of the beam (ρ × L_b × W × h) was used for the calculation of the mechanical delay, serving as an upper limit. Using the effective mass of 0.4 × (actual mass) [6], the mechanical delay was around 2 ns.

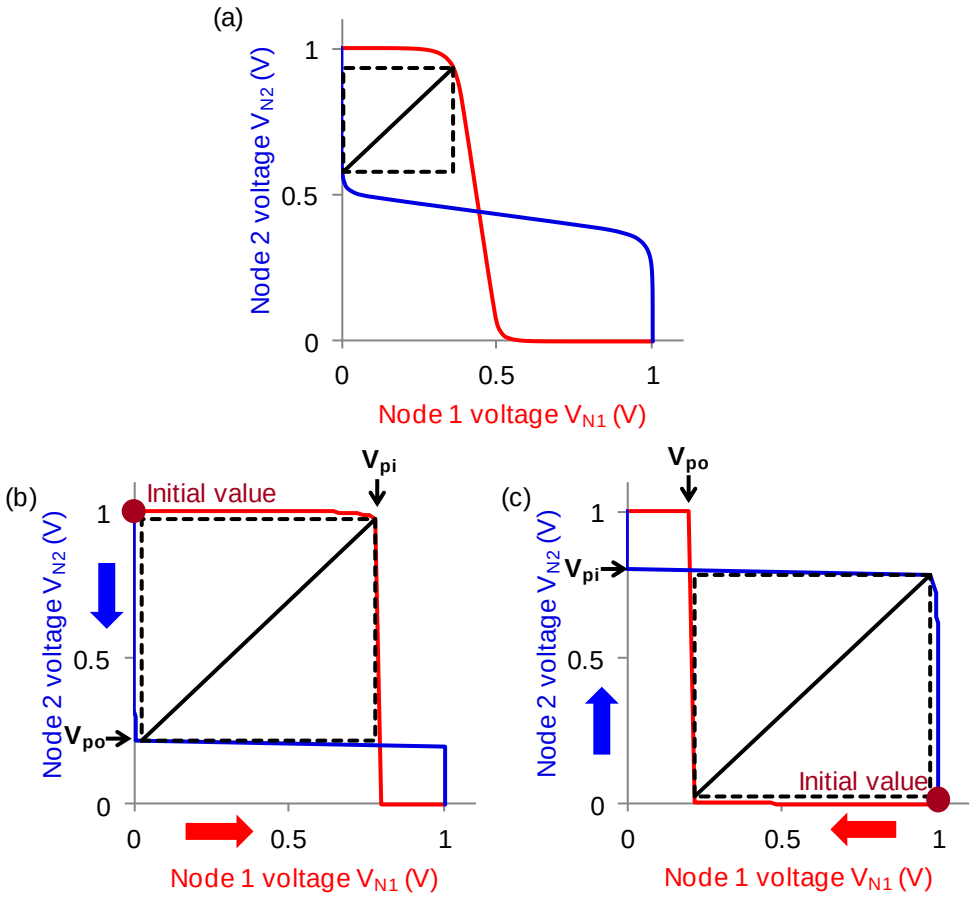


Figure 3-4 Butterfly curves in the HOLD mode for (a) a CMOS 6T SRAM cell, (b) a CMOS–NEM SRAM cell with increasing node 1 voltage (V_{N1}) and decreasing node 2 voltage (V_{N2}), and (c) CMOS–NEM SRAM cell with decreasing V_{N1} and increasing V_{N2}. (b) and (c) show the presence of directionality for the butterfly curve of a CMOS–NEM SRAM cell due to hysteresis and the resulting increase in SNM.

butterfly curve, which is drawn by sweeping the voltage at node 1 (V_{N1}) and plotting the voltage at node 2 (V_{N2}), as shown in red in Figure 3-4a, and sweeping V_{N2} and plotting V_{N1} on the same plot, shown in blue in Figure 3-4a (See Figure 3-2 for notations). The access transistors (MAX1 and MAX2) are turned off to emulate the HOLD mode. From the butterfly curve, the length of the side of the largest square that

can fit into the opening is defined as the SNM. It is the amount of static noise the cell can tolerate before the stored value flips to opposite values.

For the CMOS SRAM cell, the butterfly curve does not depend on the stored values, because the direction of the voltage sweep does not affect the shape of the curve. However, for the CMOS–NEM SRAM, the butterfly curve has directionality due to hysteresis. The butterfly curve in Figure 3-4b considers the case when $V_{N1} = 0$ and $V_{N2} = V_{DD}$ and thus is obtained by sweeping V_{N1} from 0 to V_{DD} and V_{N2} from V_{DD} to 0. In the opposite case, the butterfly curve would be reflected along $V_{N1} = V_{N2}$ as in Figure 3-4c.

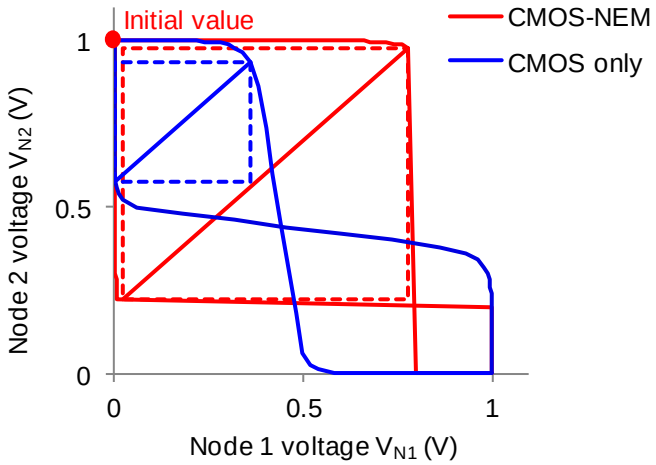


Figure 3-5 Butterfly curve in the HOLD mode for increasing V_{N1} and decreasing V_{N2} with $R_{on,NEM}$ = 1 kΩ, showing significantly increased SNM for the CMOS–NEM SRAM cell. This is due to the infinite subthreshold slope and hysteretic behavior of NEM relays.

Figure 3-5 shows the butterfly curve for the 6T CMOS SRAM cell and the CMOS–NEM SRAM cell, when $V_{N1} = 0$ and $V_{N2} = V_{DD}$. The CMOS–NEM SRAM cell with

a NEM relay on-resistance ($R_{on,NEM}$) of 1 kΩ had a SNM that is about two times larger than that of a CMOS SRAM cell. This increase can be attributed to not only the infinite subthreshold slope but also the hysteretic behavior of NEM relays. The trip voltage of the '0' node and the '1' node are decoupled into V_{pi} and V_{po}, respectively, so that the SNM can be increased by increasing V_{pi} and decreasing V_{po}. The extent to which this can be done is limited only by the variation in V_{pi} and V_{po} to ensure $V_{pi} < V_{DD}$ and $V_{po} > 0$.

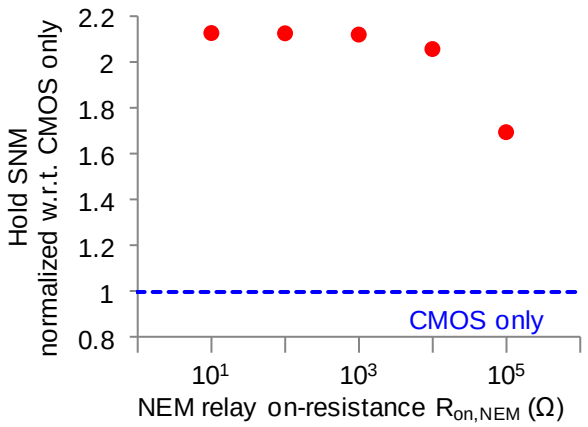


Figure 3-6 Normalized HOLD SNM of a CMOS–NEM SRAM cell with respect to a CMOS 6T SRAM cell for different $R_{on,NEM}$. When $R_{on,NEM}$ = 10 kΩ, HOLD SNM increased by more than two-fold, and decrease in $R_{on,NEM}$ below ~10 kΩ had diminishing return for improving the HOLD SNM. Even when $R_{on,NEM}$ = 100 kΩ, SNM increased by about 70 %.

The HOLD SNM decreased as $R_{on,NEM}$ increased from 10 Ω to 100 kΩ as shown in Figure 3-6. To understand why, consider the case when V_{N2} is swept from V_{DD} to 0 (i.e. when the stored values are V_{N1} = 0 and $V_{N2} = V_{DD}$). Between ($V_{DD} - |V_{th,PMOS}|$) and V_{po}, both the MPU1 and the XNEM1 are turned on, so that a higher $R_{on,NEM}$ with respect to the PMOSFET on-resistance results in a higher V_{N1}. When $R_{on,NEM}$ = 10

kΩ, HOLD SNM increased by more than two-fold, and decrease in $R_{on,NEM}$ below around 10 kΩ had diminishing return for improving the HOLD SNM. Even when $R_{on,NEM}$ = 100 kΩ, SNM increased by about 70%. This suggests that $R_{on,NEM}$ does not need to be smaller than ~10 kΩ in order to obtain a two-fold benefit in the HOLD SNM.

3.4. READ Mode – SNM and Speed

In the READ mode, the two bitlines are precharged to V_{DD}, and the access transistors (MAX1 and MAX2) are turned on. The bitline on the side with the '0' stored discharges, creating a voltage difference between the two bitlines, which is detected by the sense amplifier. The READ SNM is determined the same way as with the HOLD SNM, except that the SRAM cell is biased in a way that emulates the READ mode [32]. That is, the access transistors are turned on, and both bitlines are biased at V_{DD}. Because the voltage of the '0' node rises above 0 V when the bitline discharges, the READ mode is less stable than the HOLD mode. Therefore, the READ SNM is a more critical parameter than the HOLD SNM.

As in the HOLD case, the infinite subthreshold slope and hysteretic behavior of NEM relays significantly improved the READ SNM as shown in Figure 3-7. The CMOS–NEM SRAM with $R_{on,NEM}$ = 1 kΩ had a SNM that is about three times larger than that of the CMOS only SRAM. The benefit is larger than that for the HOLD SNM, because there is an additional benefit coming from the low $R_{on,NEM}$ compared to the on resistance of the pull-down NMOS transistors (MPDs). With pull-down

devices with lower resistance, the rise in the voltage of the node storing a '0' during the bitline discharge is less, resulting in a more stable cell.

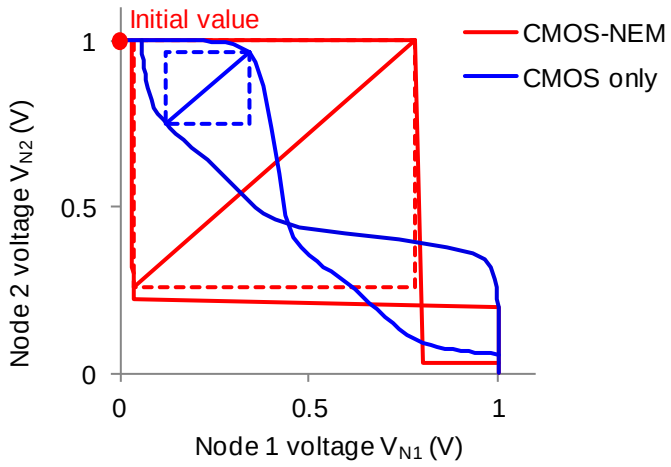


Figure 3-7 Butterfly curve in the READ mode for increasing V_{N1} and decreasing V_{N2} with $R_{on,NEM}$ = 1 kΩ, showing significantly increased SNM for the CMOS–NEM SRAM cell. This is due to the infinite subthreshold slope, hysteretic behavior, and low on-resistance of NEM relays.

As with the HOLD SNM, the READ SNM decreased as $R_{on,NEM}$ increased from 10 Ω to 100 kΩ (Figure 3-8). When $R_{on,NEM}$ = 1 kΩ, READ SNM increased by more than three-fold, and decrease in $R_{on,NEM}$ below around 1 kΩ had diminishing return for improving the READ SNM. Even without the $R_{on,NEM}$ being smaller than the NMOS pull-down transistor, which is roughly in the 10 kΩ range, the SNM increases by more than two-fold. This suggests that $R_{on,NEM}$ does not need to be smaller than around 1 kΩ in order to obtain a three-fold benefit in the READ SNM, and that it can be as large as 100 kΩ and still obtain a two-fold benefit.

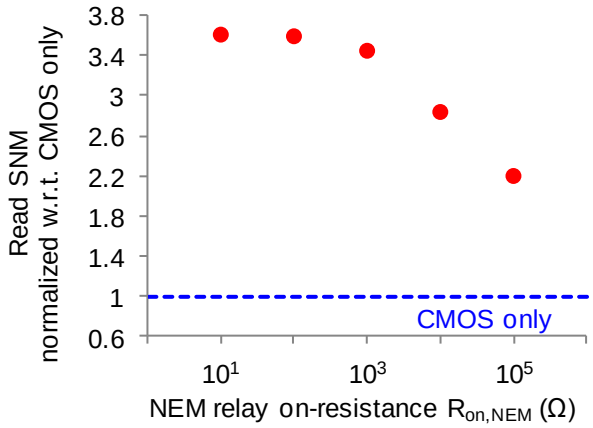


Figure 3-8 Normalized READ SNM of a CMOS–NEM SRAM cell with respect to a CMOS 6T SRAM cell for different $R_{on,NEM}$. When $R_{on,NEM}$ =1 kΩ, READ SNM increased by more than three-fold, and decrease in $R_{on,NEM}$ below ~1 kΩ had diminishing return for improving the READ SNM. Even when $R_{on,NEM}$ = 100 kΩ, SNM increased by more than two-fold.

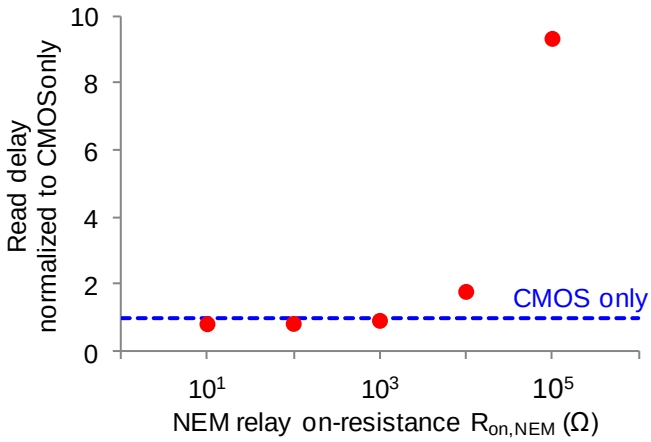


Figure 3-9 Normalized READ delay of a CMOS–NEM SRAM with respect to a CMOS 6T SRAM cell for different $R_{on,NEM}$. A reasonable READ delay was obtained for $R_{on,NEM}$ below ~10 kΩ. READ delay was defined as the time it takes for the V_{BL} or V_{BL_B} to decrease to $0.9 \times V_{DD}$. C_{BL} = 80 fF was assumed.

With the READ delay defined as the time it takes for the bitline on the side with the '0' stored to decrease to 0.9 × V_{DD}, transient analysis showed that a READ can be achieved without a significant degradation in speed compared to the CMOS 6T SRAM cell by keeping $R_{on,NEM}$ below around 10 kΩ (Figure 3-9). This is expected since the READ delay is determined by the resistance in the bitline discharge path, which is the sum of the on-resistance of the access transistor (MAX) and that of the pull-down device (MPD or XNEM). The READ delay of the CMOS-NEM SRAM cell becomes larger than that of the CMOS SRAM cell, when $R_{on,NEM}$ becomes larger than the on-resistance of the pull-down transistor (MPD), which is around 10 kΩ.

3.5. WRITE Mode – Speed

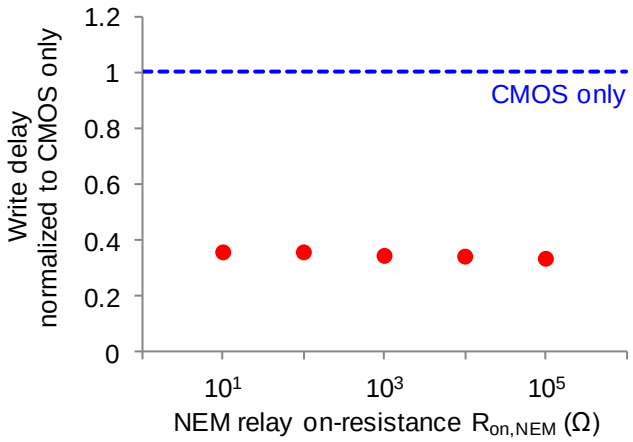


Figure 3-10 Normalized WRITE delay of a CMOS–NEM SRAM cell with respect to a CMOS 6T SRAM cell for different $R_{on,NEM}$. A large reduction in WRITE delay was maintained for a large range of $R_{on,NEM}$.

The WRITE operation is the only case that the beam mechanically moves, and hence the only case that the large τ_{mech} of the beam may be a concern. Both HOLD

and READ do not involve the movement of the beam. However, transient analysis showed that a WRITE can be achieved about 60 % faster than with a CMOS 6T cell throughout a wide range of $R_{on,NEM}$, from 10 Ω to 100 kΩ as shown in Figure 3-10. Also, the WRITE delay did not depend on the magnitude of the $R_{on,NEM}$ within that range.

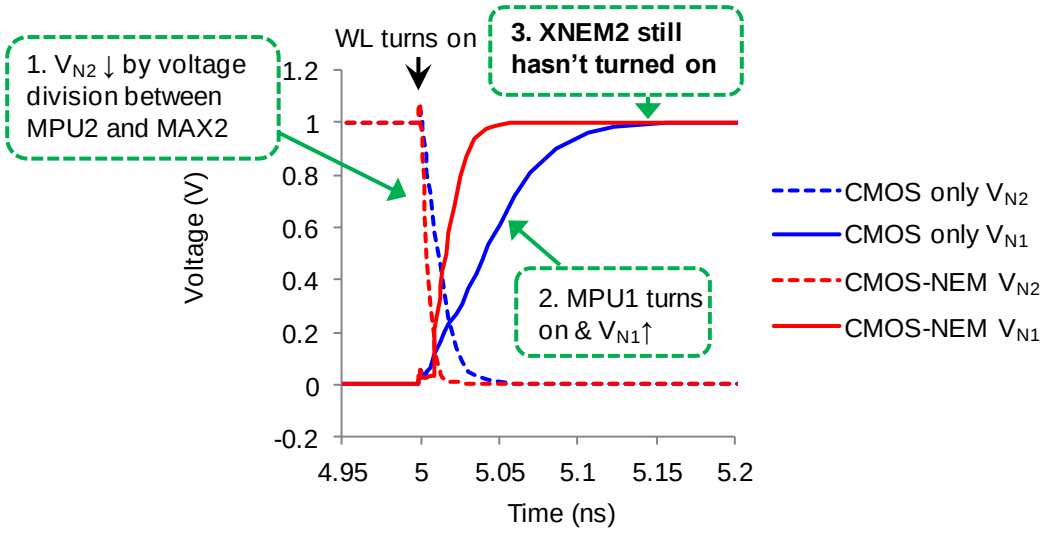


Figure 3-11 Transient characteristics of a WRITE operation of a CMOS–NEM SRAM cell, showing successful WRITE without degradation in performance, confirming that the NEM relay mechanical delay does not limit the WRITE performance. The WRITE sequence explains how the conduction of the pull-down transistor is not critical in achieving a successful WRITE.

This can be understood by analyzing the sequence in which a WRITE occurs as explained in Figure 3-11. Consider the case of writing a '1' to node 1 and '0' to node 2. Initially, $V_{N1} = 0$ and $V_{N2} = V_{DD}$. BL is connected to V_{DD} to pull V_{N1} up to V_{DD}, but the cell is designed to ensure that this transition does not occur (so that a READ can be performed without disturbing the stored values). Therefore, it is BL_B,

connected to 0 V, that initiates the writing process. The strengths of the MPU and MAX are designed so that V_{N2} becomes lower than the trip voltage of the inverter consisting of MPU1 and XNEM1, turning on MPU1, which in turn increases V_{N1}. When V_{N1} increases beyond V_{pi}, XNEM2 turns on after τ_{mech}. However, τ_{mech} does not limit the speed of the WRITE process, because most of the current that discharges node 2 flows through MAX2. The WRITE is faster with the CMOS–NEM SRAM cell, because there is less charge to discharge due to the smaller capacitance of the NEM relay compared to CMOS, and hence a smaller capacitance on the storage node. Even in the CMOS 6T SRAM structure, where MPD2 turns on without a large delay, current through MAX2 is significantly larger than current through MPD2. Thus, the absence of conduction through the pull-down device connected to N2 did not significantly affect the speed of the WRITE operation.

Considering the case when the MAXs turn off before XNEM2 turns on, node 2 becomes a floating node and drops below 0 due to feedthrough of the WL signal. However, because the capacitance from node 2 to the gate of MAX2 is generally smaller than that to the other nodes with fixed voltages, this voltage is not large enough to cause a write failure. Also, even if XNEM2 does not turn on before another WRITE occurs after a WRITE, a successful WRITE after WRITE can be achieved, since the NEM relays do not play a critical role in the WRITE operation. READ after WRITE is the only case when the NEM relay needs to be conducting for the operation to be successful and is thus limited by τ_{mech} of the NEM relay.

It is also worth noting that, although hysteresis decreases the trip voltage of the WRITE operation for the node transitioning from a ‘1’ to a ‘0’, the WRITE speed is

not significantly degraded by this. As shown in Figure 3-11a, because the '1' to '0' transition of node 2 occurs much faster than the '0' to '1' transition of node 1, the decrease in the write trip voltage of node 2 does not have a significant impact on the overall WRITE speed of the cell.

3.6. Leakage Power

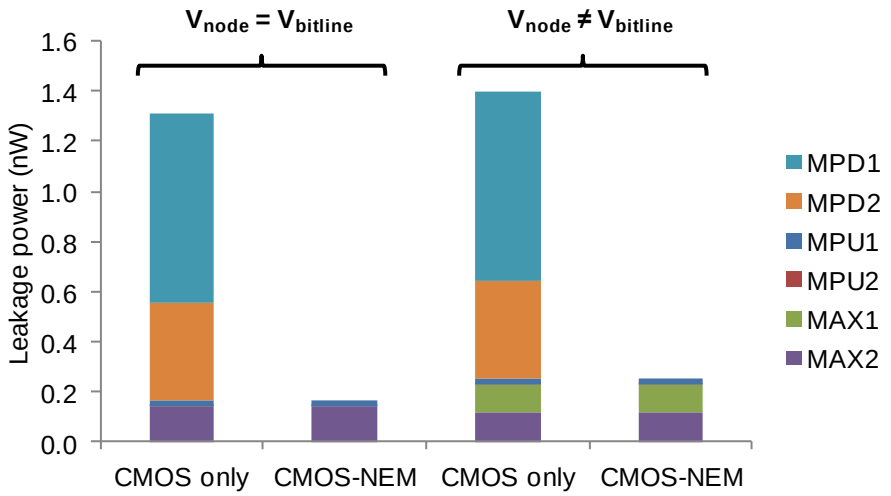


Figure 3-12 Leakage power dissipation comparison for both $V_{node} = V_{bitline}$ (i.e. $V_{BL} = V_{N1} = 0$; $V_{BL\_B} = V_{N2} = V_{DD}$) and $V_{node} \neq V_{bitline}$ (i.e. $V_{BL} = V_{DD}$; $V_{N1} = 0$; $V_{BL\_B} = 0$; $V_{N2} = V_{DD}$), showing a significant decrease in leakage power dissipation with the CMOS-NEM SRAM cell.

The zero leakage characteristic of NEM relays resulted in a dramatic reduction in static power dissipation in the HOLD mode as shown in Figure 3-12. The reduction in static power dissipation was 80–90 %, when only two transistors, MPD1 and MPD2, of the six transistors were removed from the cell. This is because the MPDs in a conventional CMOS 6T SRAM cell consume the most leakage power. This can be

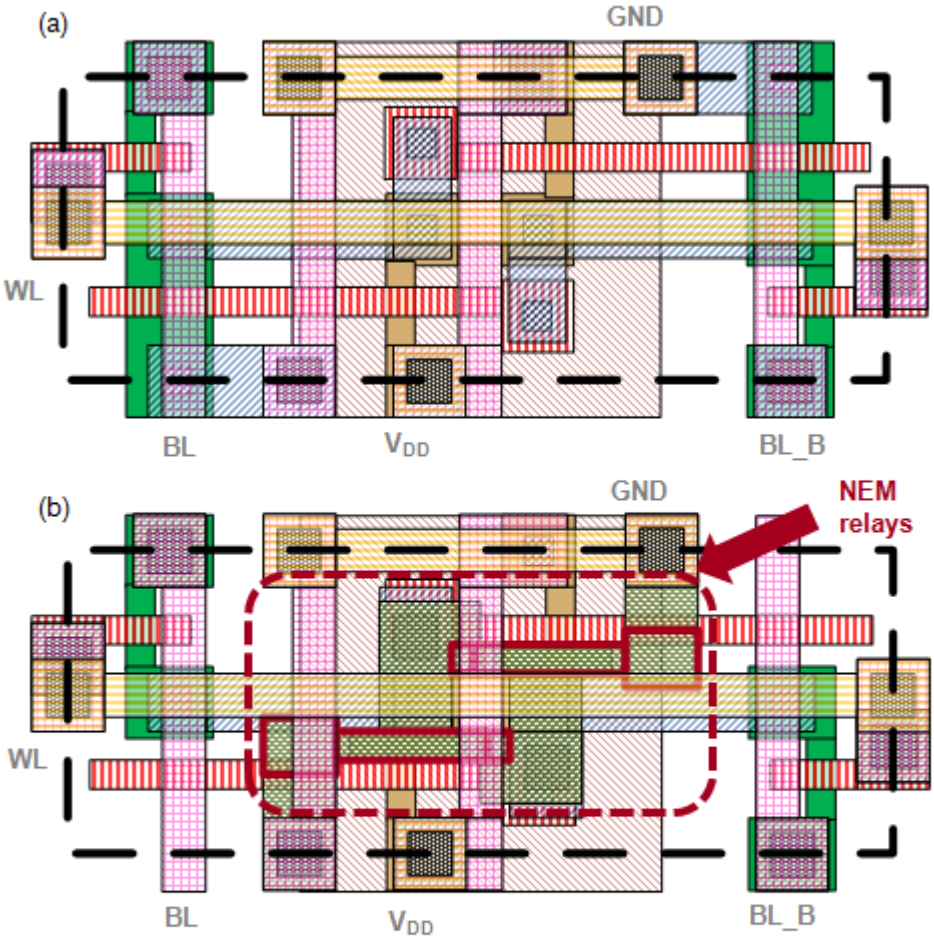
understood from the fact that 1) NMOSFETs have gate leakage (which can be larger than the source to drain subthreshold current [33]) that is significantly higher than PMOSFETs [34], and 2) MPD widths are larger than other minimum sized transistors (i.e. $\beta > 1$) to ensure stability. Eliminating this leakage path by replacing the MPDs with NEM relays resulted in a significant leakage power reduction.

3.7. Cell Area

Although the NEM relay itself may consume a larger area than a CMOS device, this does not directly translate into a larger SRAM cell size, if NEM relays are fabricated on top of CMOS devices. An example of a possible layout is shown in Figure 3-13, where the 6T CMOS SRAM and the CMOS–NEM SRAM had the same cell size. Note that, although pushed rules are commonly used for SRAM cells to obtain minimum cell sizes, since these rules are technology dependent, design rules applicable to random logic—MOSIS scalable CMOS (SCMOS) design rules [35]—were used for this example. It should also be noted that the additional area consumption needed for NEM relay encapsulation was not included in this design.

3.8. Effects of Scaling

The above analyses were performed at the 65 nm technology node in order to have CMOS parameters based on experimental data; however, it is important to study the effects of technology scaling to ensure that the major benefits, namely SNM increase and leakage power dissipation decrease, remain with further scaling. Simulations were performed with PTM of high-κ/metal-gate LP (low power) devices from 45 nm



CMOS	n-well	p-diffusion	n-diffusion	poly-Si	metal 1	N/A	metal 2	metal 3	contact /via
NEM/ CMOS						metal 2	metal 3	metal 4	

Figure 3-13 Cell layout (size ~300 F^2) of (a) a 6T CMOS SRAM cell and (b) a CMOS–NEM SRAM cell, based on the MOSIS scalable CMOS (SCMOS) design rules [35], showing no area penalty incurred by replacing the pull-down NMOS transistors with NEM relays. NEM relays were placed in the metal2 layer, pushing metal2/3 layers up to metal3/4 layers.

to 16 nm nodes [29]. For the NEM relays, only the widths were scaled according to the minimum possible width of each technology node.

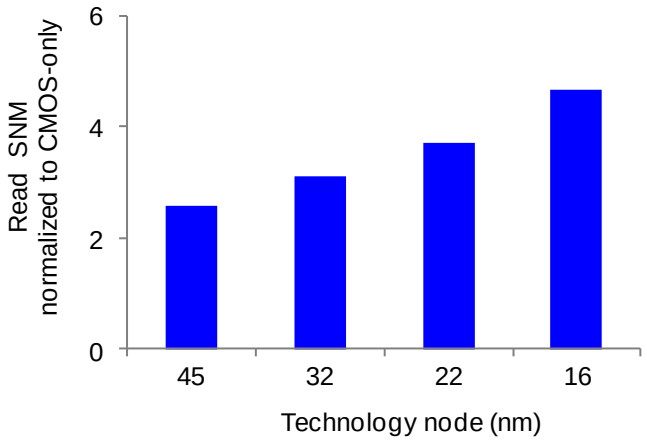


Figure 3-14 Normalized READ SNM of a CMOS-NEM SRAM cell ($R_{on,NEM}$ = 1 kΩ) with respect to a CMOS 6T SRAM cell with technology scaling, showing increased benefits with scaling.

As V_{DD} scales with technology scaling, the SNM decreased rapidly. Although this applied to both the CMOS 6T SRAM cells and the CMOS–NEM SRAM cells, the effect was not as detrimental in the CMOS–NEM SRAM cells, because of the sharp on/off transition characteristics of the NEM relays. Simulation results showed increasing benefits of the CMOS–NEM SRAM cells with further scaling as shown in Figure 3-14.

The leakage power advantage was also increased with scaling. With a thinner gate dielectric, and thus more gate leakage, a greater proportion of the leakage power was dissipated in the MPDs. This leakage path was eliminated in the CMOS–NEM SRAM cell, resulting in a larger reduction in leakage power with scaling as shown in Figure

3-15. Note that, although the advantage was still significant, changing to a high-κ dielectric decreased the power advantage, since gate leakage was reduced.

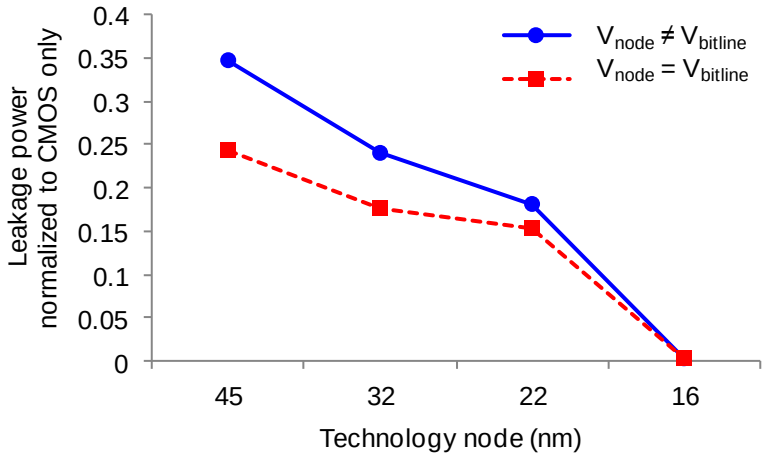


Figure 3-15 Normalized leakage power of a CMOS–NEM SRAM cell ($R_{on,NEM}$ = 1 kΩ) with respect to a CMOS 6T SRAM cell with technology scaling, showing increased benefits with scaling.

3.9. Other CMOS-NEM SRAM Configurations – Why They Don't Work

Unlike the SRAM cell structure with the NEM relay as pull-down devices, when NEM relays replaced the pull-up devices (MPUs) of a conventional CMOS 6T SRAM cell [13], the WRITE speed was limited by the large τ_{mech} of the pull-up NEM relay as shown in Figure 3-16. Recall from Section 3.5 that a WRITE operation is triggered by the voltage of the node transitioning from a '1' to a '0' reaching a voltage that turns on the pull-up device. When the pull-up device turns on, the voltage at the storage node increases to become a '1,' completing a WRITE. Therefore, the large τ_{mech} of a NEM relay is in the critical write path, and the WRITE operation cannot be completed until

the relay turns on. Therefore, the WRITE delay is always greater than τ_{mech} of the NEM relay, significantly degrading the WRITE performance.

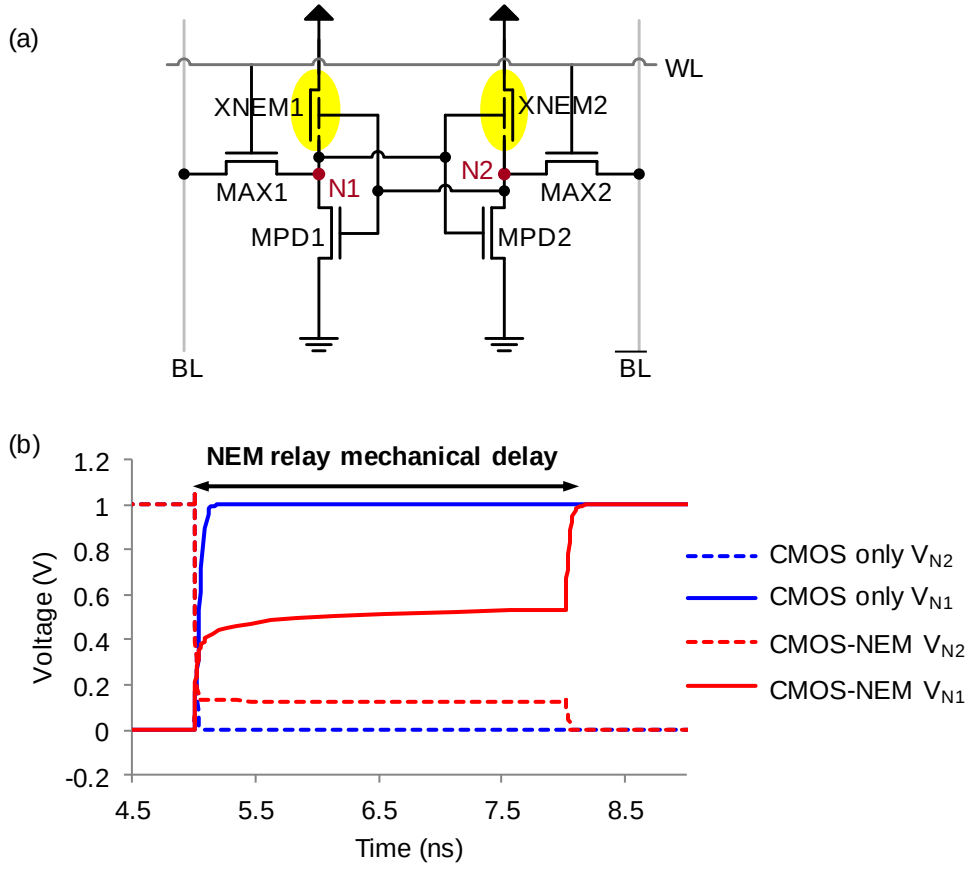


Figure 3-16 (a) Schematic of a CMOS–NEM SRAM with NEM relays as pull-up devices and (b) transient characteristic of a WRITE operation, showing a successful WRITE but with performance limited by NEM relay mechanical delay ($R_{on,NEM}$ = 50 kΩ).

3.10. Conclusion

A novel hybrid CMOS–NEM SRAM cell structure was designed and studied to utilize the sharp on/off transition, hysteretic behavior, and zero leakage current of the NEM relays to overcome the inherent limitations of conventional CMOS 6T SRAM

cells. In the CMOS 65 nm technology node under consideration, replacing the pull-down NMOSFETs with NEM relays resulted in over a two-fold and a three-fold increase in the HOLD and READ SNM, respectively, assuming $R_{on,NEM}$ = 1 kΩ. The main leakage path of the storage node was eliminated by the pull-down NEM relays, so that leakage power reduction was up to around 85 %. In addition, because the NEM relay was not in the critical path that determines the WRITE speed, its long mechanical delay did not limit the CMOS–NEM SRAM WRITE speed. Finally, unlike previous works that modify the SRAM cell structure and/or peripheral circuitry to improve the stability at the cost of area, the increased stability of this structure did not require a larger overall SRAM cell array area. The increased SNM and decreased leakage power advantages of this novel structure are predicted to increase with further scaling. This work provides motivation to develop the NEM relay fabrication technology into a more mature technology, with devices having lower operating voltages (with V_{pi} < 1 V) and better reliability.

In order to predict the stability of the SRAM cell more accurately, variability also needs to be evaluated. Although this hybrid CMOS–NEM SRAM cell structure significantly increases noise margin compared to the conventional CMOS 6T SRAM cell, it is unclear what the variability of the NEM relay parameters will be in the dimensions of interest compared to that of CMOS transistor parameters. Variability in NEMS is beginning to be studied [36] and requires more analysis.

Chapter 4: Optical Lithography Patterned Relays[1,2]

4.1. Introduction

As a first step towards realizing the CMOS–NEM hybrid circuits, scaled-up relays alone, without CMOS, were fabricated using optical lithography as a proof of concept. Previous works for the fabrication of electrostatically actuated M/NEM relays are summarized in Table 4-1. The devices in these works have at least one of the following properties: 1) they are vertically actuated, which results in limited design flexibility and more complicated fabrication process; 2) they are fabricated using a structure that requires more area than a cantilever switch; and 3) they have less than three terminals, which have limited use as a switch. In this chapter, a laterally actuated three terminal (3T) cantilever type NEM relay was fabricated and electrically tested.

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[1] Part of this chapter is taken from R. Parsa, S. Chong, N. Patil, K. Akarvardar J Provine, D. Lee, D. Elata, S. Mitra, H.-S. P. Wong, R. T. Howe, "Composite polysilicon-platinum lateral nanoelectromechanical relays," Solid-State Sensors, Actuators, and Microsystems Workshop, Hilton Head, SC, 2010, pp. 7-10.

[2] This work was done in collaboration with Roozbeh Parsa (Stanford University). More details can be found in [61].

Table 4-1 Previous works of fabrication of electrostatically actuated M/NEM relays (in order of publication date from least to most recent)

Structure	act.*	# of T†	Dimensions	V_{pi} / V_{po}	Material	Speed‡	cycling	Ref
cantilever beam	V	3T	h = 210 nm; g_g = 430 nm; g_d = 210 nm; L = 10 μm; W = 4 μm	27.5 V / 25 V	Ni + Au + Al	N/A	10^9	[37]
cantilever beam	V	3T	h = 1 μm; g_g = 500 nm; g_d = 200 nm; L = 30 μm; W = 8 μm	24.6 V / N/A	polySi	3 μs	N/A	[38]
cantilever beam	V	2T	h = 35 nm; g_g = 15 nm; L = 1 μm; W = 200 nm	13 V / 8 V	TiN	N/A	500	[39]
cantilever beam	V	3T	h = 1.7 μm; g_g = 500 nm; g_d = 150 nm; L = 40 μm; W = 8 μm	22 V / 18 V	Ni + Au	N/A	10^5	[40]

* Actuation direction: H (horizontal) or V (vertical)

† T = terminals

‡ Switching speed

cantilever beam	V	2T	h = 30 nm; g_g = 20 nm; L = 300 nm; W = 200 nm	13 V / 8 V	TiN	N/A	300	[41]
clamped-clamped beam	V	2T	h = 30 nm; g_g = 20 nm; L = 1 μm; W = 200 nm	11 V / 6 V	TiN	N/A	N/A	[41]
clamped-clamped beam	L	5T*	W = 100 nm; g_g = 75 nm; g_d = 50 nm; L = 10 μm; t = 200 nm	5V / N/A	Ru	400 ns	2×10^6	[9]
folded flexure plate	V	4T	h = 1 μm; g_g = 200 nm; g_d = 100 nm; L = 27 μm; W = 30 μm	6.1 V / 5.9 V	polySiGe + Al_2O_3 + W	0.2–1.8 μs	10^9	[42]
cantilever beam	V	3T	h = 50 nm; g_g = 40 nm; g_d = 20 nm; L = 900 nm; W = 200 nm	8 V / N/A	TiN	N/A	50 (in oil)	[43]

* Double-sided 3T

clamped-clamped beam	V	3T*	h = 32 nm; g_g = 55 nm; g_d = 18 nm; L = 1.83 μm; W = 500 nm	2.52 V / N/A	W	N/A	N/A	[44]
seesaw-like plate	V	6T†	h = 1 μm; g_g = 200 nm; g_d = 100 nm; L = 86 μm; W = 40 μm	7.14 V / 3.16 V	polySiGe + Al_2O_3 + W	N/A	400	[45]

* Operates like a 2T

† Double-sided 4T

4.2. Device Structure

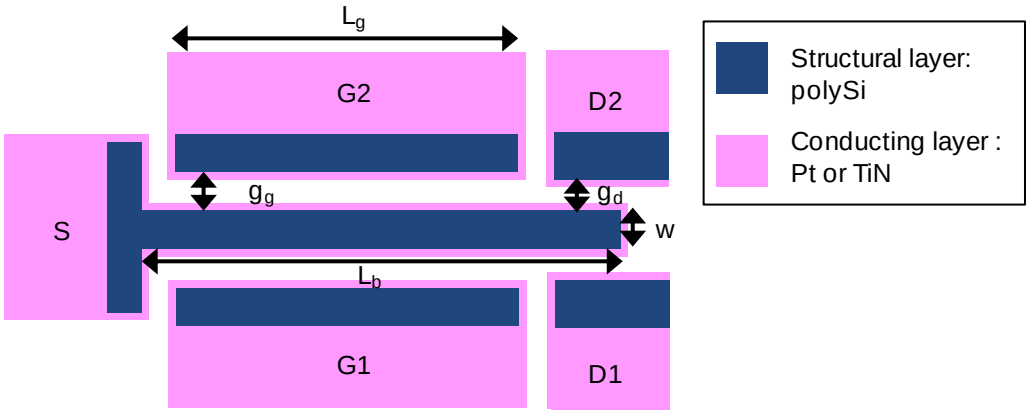

Figure 4-1 Schematic of a double-sided three-terminal (3T) cantilever relay, or a five-terminal (5T) relay. The polysilicon (polySi) structural layer is coated with a conducting layer, for which platinum (Pt) or titanium nitride (TiN) was used in this work.

In this work, a double-sided 3T relay, or a five-terminal (5T) relay was used. The schematic of the device is shown in Figure 4-1. If desired, the device can be operated as a 3T device by biasing the gate and drain on one side (G1 and D1, for example) at the same voltage as the source (S) and actuating the beam to the other side (the side with G2 and D2). By using a 5T structure, benefits are gained in terms of both fabrication and functionality of the device.

In terms of fabrication, a 5T device allows achieving symmetry of the beam easier to attain. Having an electrode on one side and not on the other would result in a difference in exposure during lithography between the two sides of the beam, which can lead to a beam that is laterally asymmetric. This can result in a beam that is not laterally flat.

In terms of functionality, the beam being able to actuate to both sides opens up possibilities of achieving more complex functions with a single device. For example, this device can perform the function of an inverter, by biasing one of the gates (G1, for example) at V_{DD} and the other gate (G2) at 0 and switching the voltage on the source (S) between 0 and V_{DD}. By connecting D1 and D2 and taking the output from this node, this device performs the function of an inverter. Another example is the use of this device for energy-reversible operations [46]. In this scheme, the energy stored in the beam when actuated to one side, is utilized in actuating the beam to the other side. This enables actuation at a voltage smaller than V_{pi} (and larger than V_{po}), resulting in low operating voltage and thus low power dissipation.

The moving body was a cantilever that was laterally actuated. Compared with vertically actuated devices, laterally actuated devices have the advantage of having a simpler fabrication process. The lithography is simpler, since the structural layer, including the beam, the two gates, and the two drains, can be patterned in one lithography step. This leads to an additional advantage of having more design flexibility. Also, it facilitates obtaining symmetry for the double-sided 5T structures.

Polysilicon (polySi) was used as the structural layer, with a conducting coating layer, for which platinum (Pt) or titanium nitride (TiN) was used in this work. polySi is a material that has been used extensively for MEMS devices as a structural material based on its good material properties of having a high melting temperature (around 1400 ºC), having a reasonable Young's modulus (around 170 GPa), and being able to be processed using silicon microfabrication techniques [47]. A conducting layer was needed, however, because polySi forms a native oxide, which serves as a conduction

barrier. Pt and TiN were chosen as the conductive material due to their low resistivity (17 μΩ·cm and 24–40 μΩ·cm, respectively), high melting temperature (1768 ºC and 2930 ºC, respectively), and excellent chemical inertness [48], [49]. The structural layer itself was not made of the conducting material, because it is desirable to have the thickness of the device (t) be at least as thick as the width of the beam (w) for stable operation. The minimum feature size was limited to around 500 nm, due to the limited optical lithography tool capability of the Stanford Nanofabrication Facility (SNF), and it was not feasible both capability-wise and cost-wise to deposit 500 nm of Pt or TiN.

4.3. Process Flow

The fabrication process of a Pt-coated polySi NEM relay was as follows (Figure 4-2). A silicon dioxide (SiO_2) and polySi stack was made on a bare silicon (Si) wafer by depositing 2 μm of a SiO_2 insulating layer at 400 °C and 1.2 μm of a phosphorous-doped polySi structural layer at 580 °C and annealing at 1075 °C for 30 seconds. Next, 300 nm of SiO_2 was deposited at 400 °C to be used as a hard mask. Then, photoresist (PR) was patterned by optical lithography, using an i-line stepper, defining the NEM relay gate, drain, and source. The minimum feature size was limited to around 500 nm, due to the limited capability of the fabrication facility at SNF. The SiO_2 was etched, and using the patterned SiO_2 as a hard mask, the polySi structural layer was etched. Having fabricated the NEM relay structural layer, 50 nm of Pt was sputtered to serve as the conductive coating layer. Then, the Pt was anisotropically etched unmasked, so that the bottom of the trench was opened up, while leaving Pt on the sidewalls. One more lithography step was performed to have Pt on top of the pads,

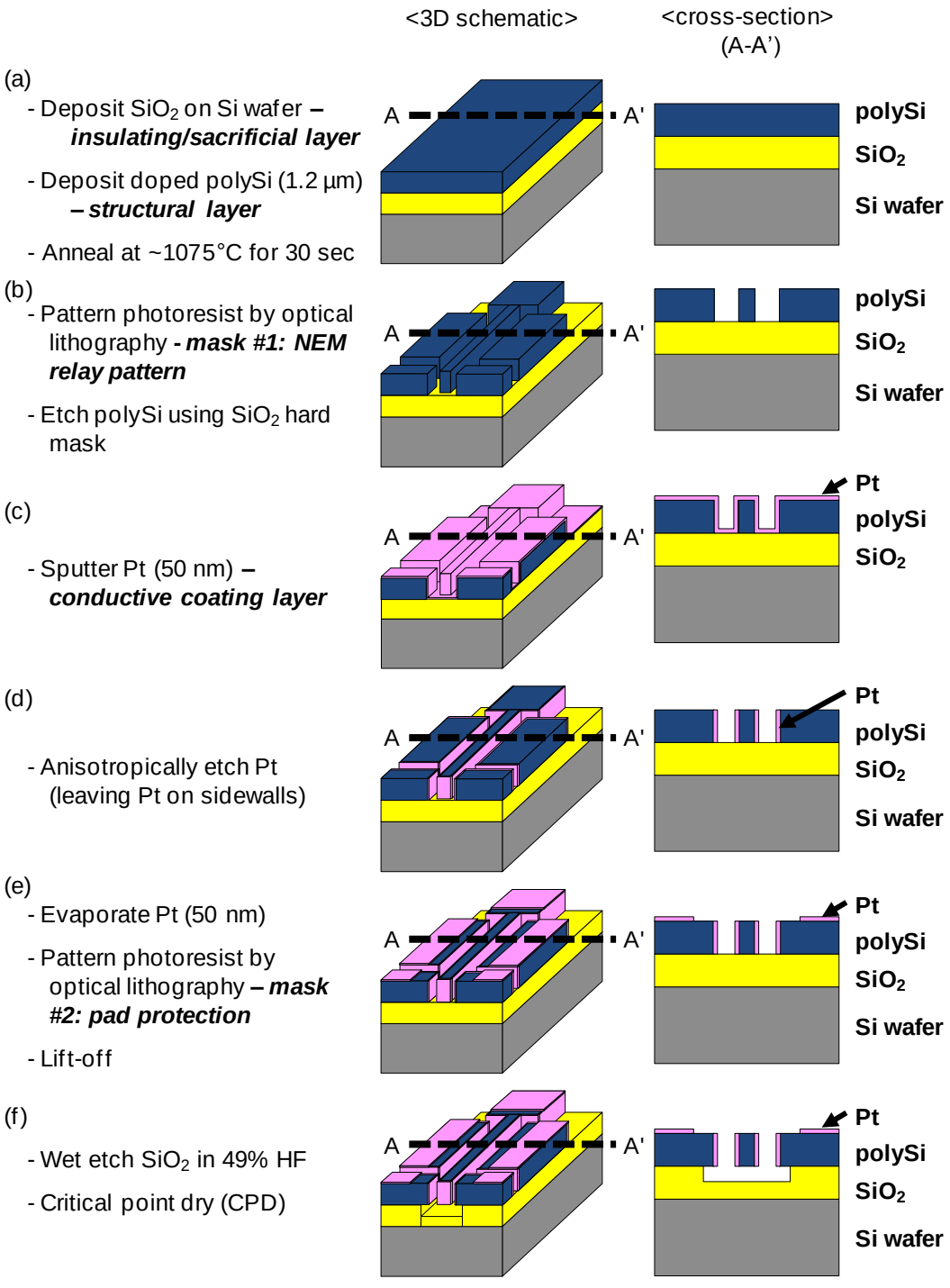

Figure 4-2 Process flow of the fabrication of a laterally actuated Pt-coated polySi NEM relay patterned by optical lithography and etching.

so that there is conduction along the Pt from the contacting sidewalls to the pads during measurements. For this, PR was patterned via optical lithography, 50 nm of Pt was evaporated, and a lift-off was performed in acetone. Finally, using a timed wet etch in 49 % hydrofluoric acid (HF), the oxide underneath the beam was removed, so that the beam was released and able to move. The last step was a critical point dry (CPD) to avoid stiction during drying. Note that, because of the polySi deposition and anneal, the process temperature was not CMOS-compatible.

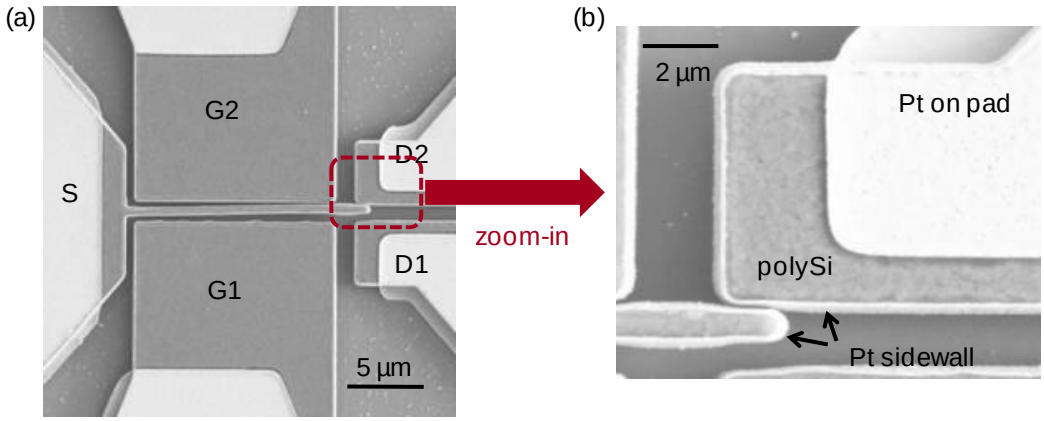

Figure 4-3 (a) A scanning electron microscope (SEM) image of a Pt-coated polySi 5T NEM relay patterned via optical lithography, showing the beam actuated to one side due to charging during imaging. (b) A zoomed-in image shows the polySi layer and the Pt on the pad and on the sidewalls. Drawn dimensions: L_b = 16 µm; g_g = 600 nm.

A scanning electron microscope (SEM) image of a fabricated device is shown in Figure 4-3. The beam had actuated during SEM imaging, which often happened due to charge build-up during imaging. The zoomed-in image shows the polySi structural layer, as well as the Pt sidewall and the Pt on the pads.

The process flow for the devices with a TiN conducting coating layer was similar to the process flow described above[1]. The difference was that 150 nm of TiN was deposited using metal organic chemical vapor deposition (MOCVD)[2]. Also, the sidewall and pad TiN was deposited, patterned, and etched simultaneously.

4.4. Electrical Measurements

4.4.1. Quasi-Static Measurement

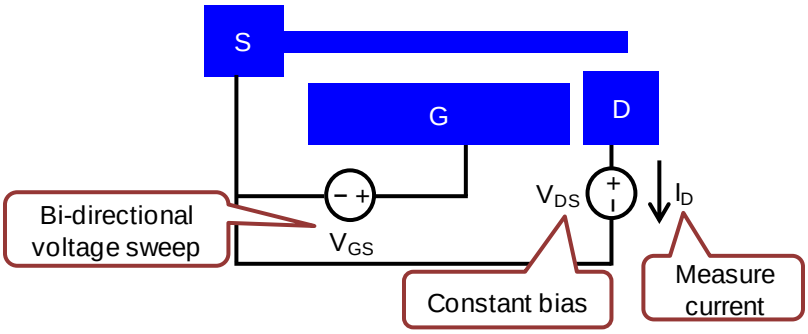

Figure 4-4 Schematic of a quasi-static measurement setup. Using a parameter analyzer, the voltage between the gate and the source (V_{GS}) was quasi-statically swept in both directions, the voltage between the drain and the source (V_{DS}) was biased at a constant voltage, and the current through the drain (I_D) was measured.

A quasi-static measurement was performed to find out the pull-in/out characteristics. Using an Agilent 4156C parameter analyzer, V_{GS} was swept in both

[1] The fabrication of TiN-coated polySi devices was done by Dae Sung Lee (Stanford University).

[2] The deposition was done by J.-O. Lee at the Korea Advanced Institute of Science and Technology, Daejeon, Korea.

directions, and V_{DS} was biased at a constant voltage, while current was measured on the drain as shown in Figure 4-4. Since excessive current can undesirably modify the contacting surface, the current was limited to 1 nA by setting a current compliance. Measurement was done in air with nitrogen flow.

The device without a conducting layer was first measured. The drawn dimensions of the device were L_b = 14.6 μm, L_g = 11.5 μm, g_g = 600 nm, g_d = 500 nm, and w = 500 nm. The results are shown in Figure 4-5. The device successfully pulled in at around 60 V and pulled out at 40–50 V. The voltage between the drain and the source (V_{DS}) needed to be as high as 3–5 V for a stable contact measured with a 1 nA current compliance. However, even at V_{DS} = 5V, a stable contact was not consistent. This is expected to be due to the native oxide that formed on the polySi structural layer before and during testing. By removing the current compliance, the approximate on-resistance, simply calculated by I_{on}/V_{DS} ($R_{NEM,approx}$), was measured to be in the GΩ range with V_{DS} = 3–5 V.

Figure 4-6 shows the quasi-static measurement result of a Pt-coated polySi 5T relay with drawn dimensions of L_g = 18 μm, w = 600 nm, and g_g = 600 nm and a 50 nm Pt coating. The device was actuated to one side, operating like a 3T relay. The device pulled in at around 12 V and pulled out at around 5 V, demonstrating hysteresis. Unlike the polySi devices, a stable contact was achieved, with a 1 nA current compliance, at V_{DS} as low as 15 mV. The on/off transition was sharp, and the off-state current was limited by the noise level of the measurement tool. By removing the current compliance, $R_{NEM,approx}$ was measured to be less than 3 kΩ with V_{DS} = 0.01–1 V.

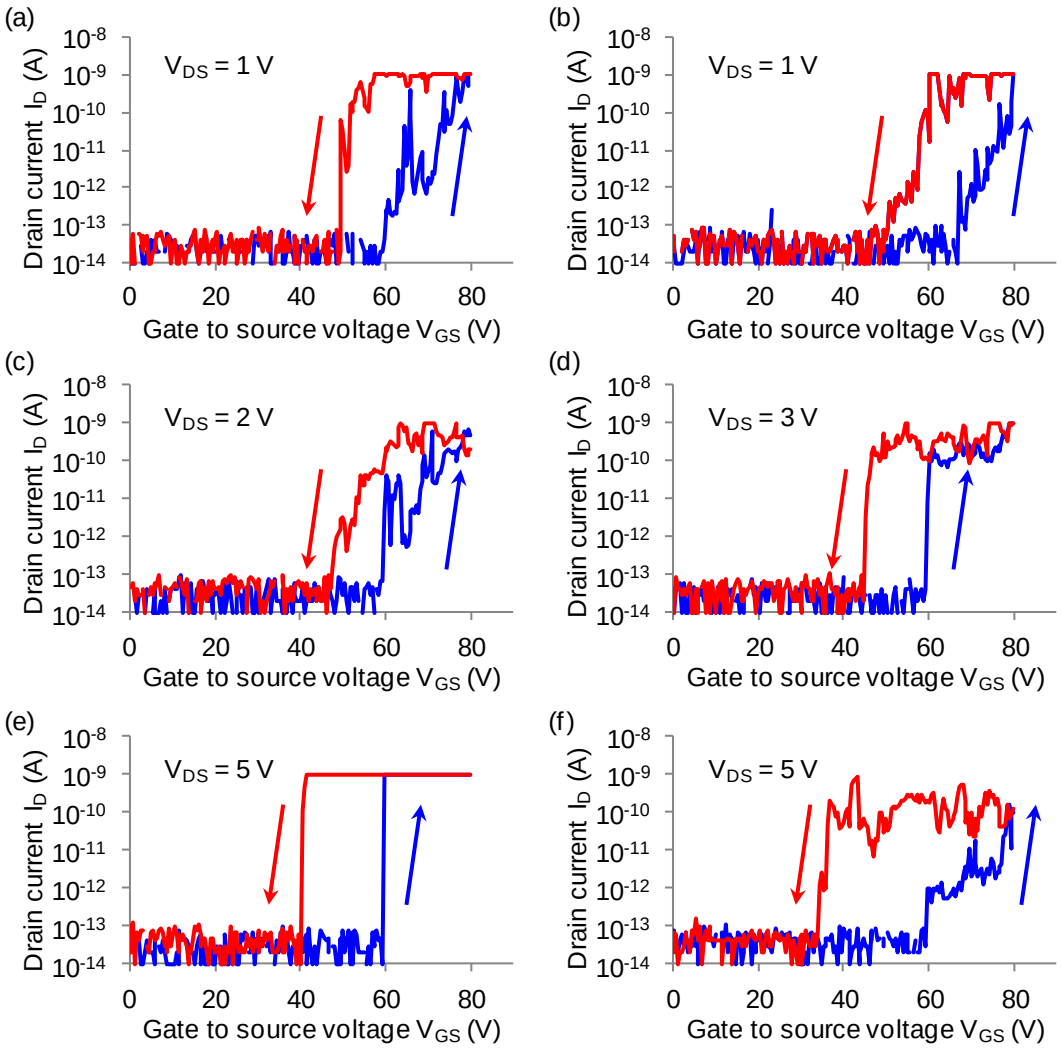

Figure 4-5 Quasi-static measurement results of a polySi 5T relay (with no conductive layer coating) plotting I_D versus V_{GS} with a current compliance of 1 nA. The test was repeated several times at (a) V_{DS} = 1 V, (b) V_{DS} = 1 V, (c) V_{DS} = 2 V; (d) V_{DS} = 3V; (e) V_{DS} = 5 V, (f) V_{DS} = 5 V, showing that a V_{DS} as high as 3–5 V was needed for a stable contact. However, stable contact was not repeatable at the next cycle. This is expected to be due to the native oxide that forms on the polySi surfaces. Drawn dimensions: L_b = 14.6 µm; L_g = 11.5 µm; g_g = 600 nm; g_d = 500 nm; w = 500 nm.

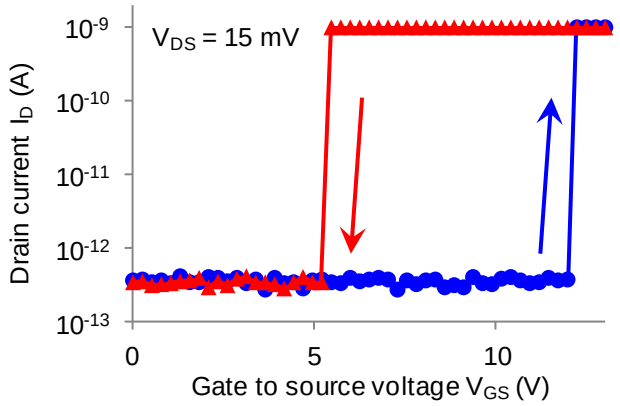

Figure 4-6 Quasi-static measurement result of a Pt-coated polySi 5T relay, actuated to one side, operating like a 3T relay. I_D versus V_{GS} is plotted with a 1 nA current compliance. Sharp pull-in and pull-out, zero off-state leakage, and hysteresis were demonstrated with V_{DS} = 15 mV. Drawn dimensions: L_g = 18 µm; w = 600 nm; g_g = 600 nm. Pt coating layer thickness was 50 nm.

4.4.2. Dynamic Measurement

A dynamic measurement was performed to measure the switching time of the device. The test setup was as shown in Figure 4-7a. Using a Keithley dual-channel pulse generator (4205-PG2), the beam was biased at a constant voltage $V_{B\text{-}sub} = V_{low}$, and the gate voltage ($V_{G\text{-}sub}$) was pulsed between V_{low} and V_{high}, where $V_{high} - V_{low} > V_{pi}$. Using a Keithley 1.25 GS Dual-Channel Oscilloscope (4200-SCP2), the voltage on the drain ($V_{D\text{-}sub}$) was measured.

With an oscilloscope internal resistance (R_{osc}) of 1 MΩ, the measured $V_{D\text{-}sub}$ is

$$V_{D-sub} = \frac{R_{osc}}{R_{osc} + R_{NEM}} \times V_{B-sub} \qquad \text{Eq. 4-1}$$

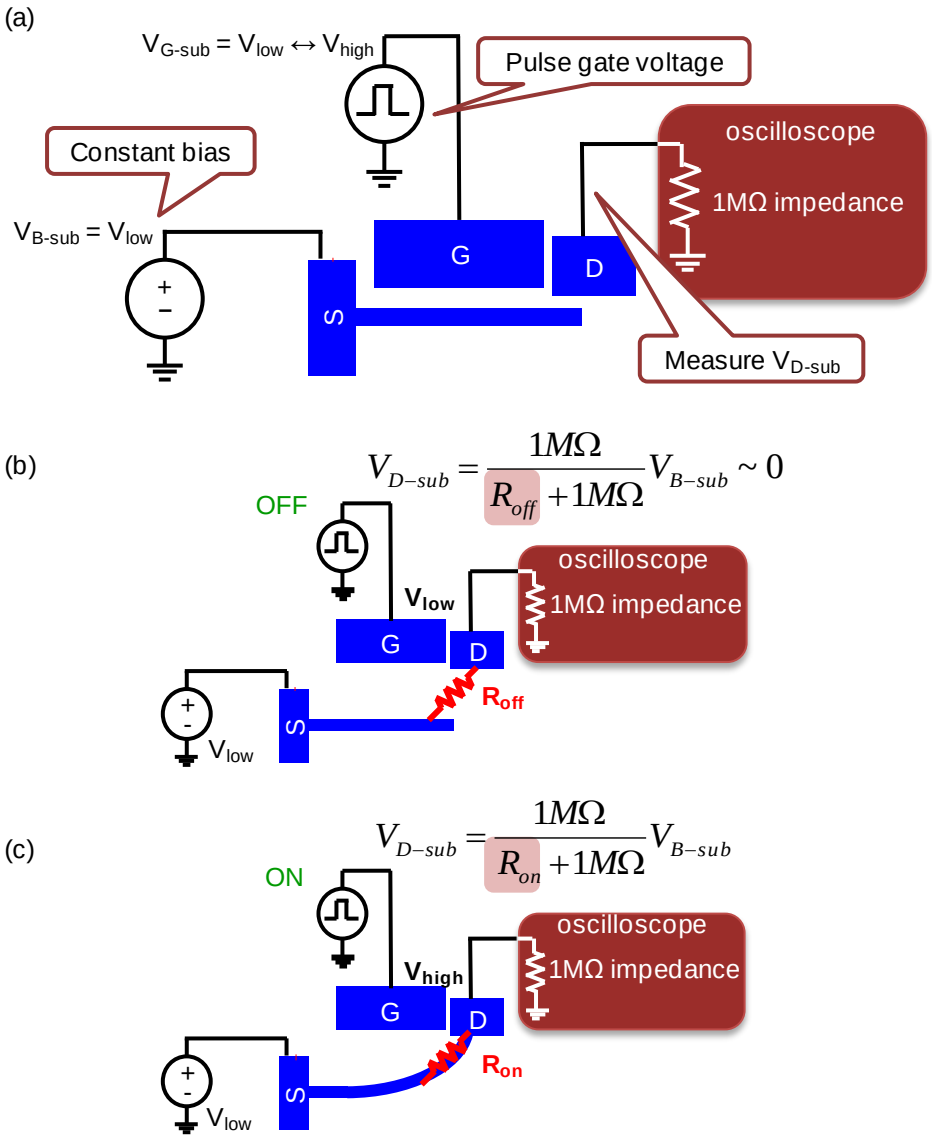

Figure 4-7 (a) Test setup for a dynamic test to measure the switching time of a 3T relay. The beam is biased at a constant voltage of $V_{B\text{-}sub} = V_{low}$, the gate voltage ($V_{G\text{-}sub}$) is pulsed between V_{low} and V_{high}, and the voltage at the drain ($V_{D\text{-}sub}$) is measured with an oscilloscope. (b) In the off-state, the drain node would discharge to approximately 0 V. (c) In the on-state, the drain node would charge to a non-zero voltage.

In the off-state (Figure 4-7b), $R_{NEM} = R_{off,NEM} >> R_{osc}$, so that $V_{D\text{-}sub}$ discharges to approximately 0 V. In the on-state (Figure 4-7c), $V_{D\text{-}sub}$ charges to a non-zero voltage, $R_{osc} / (R_{osc} + R_{on,NEM}) \times V_{B\text{-}sub}$. The device was tested in a nitrogen glove-box (Figure 4-8).

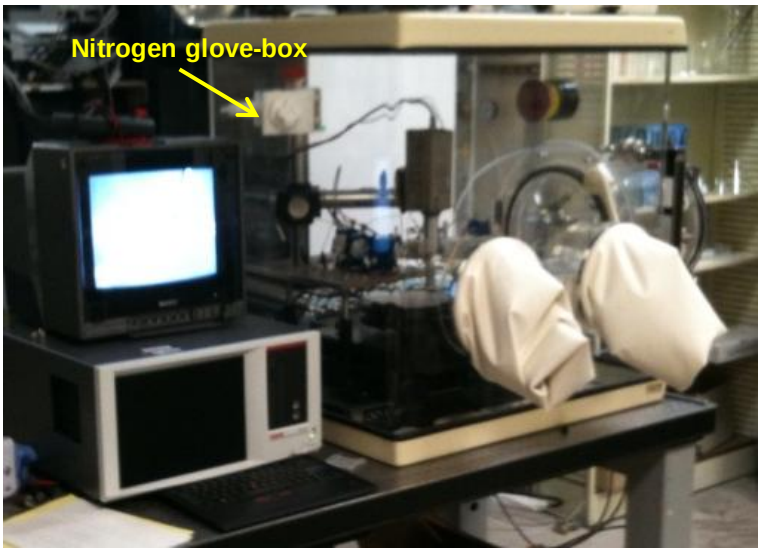

Figure 4-8 Photo of the nitrogen-filled glove-box, used for dynamic and cycling testing.

Figure 4-9 shows the dynamic measurement result of a TiN-coated polySi 5T relay, with drawn dimensions of L_b = 22 μm, w = 600 nm, and g_g = 750 nm and a 150 nm TiN coating. The device was actuated to one side, operating like a 3T relay. After $V_{G\text{-}sub}$ increased to V_{high} (20 V), the device pulled in, and $V_{D\text{-}sub}$ started charging after about 200 ns; that is, the device had a mechanical delay, or switching time, of around 200 ns. The mechanical delay calculated with the 1D model using Eq. 2-3 was 100–200 ns, in good agreement with the measured delay. When $V_{G\text{-}sub}$ decreased to V_{low} (-5V), the device pulled out, and $V_{D\text{-}sub}$ started discharging to zero. The slower charge

and discharge than what is predicted from the capacitance and resistance of the device, pad, and oscilloscope, is expected to be due to the large parasitic capacitance in the test setup.

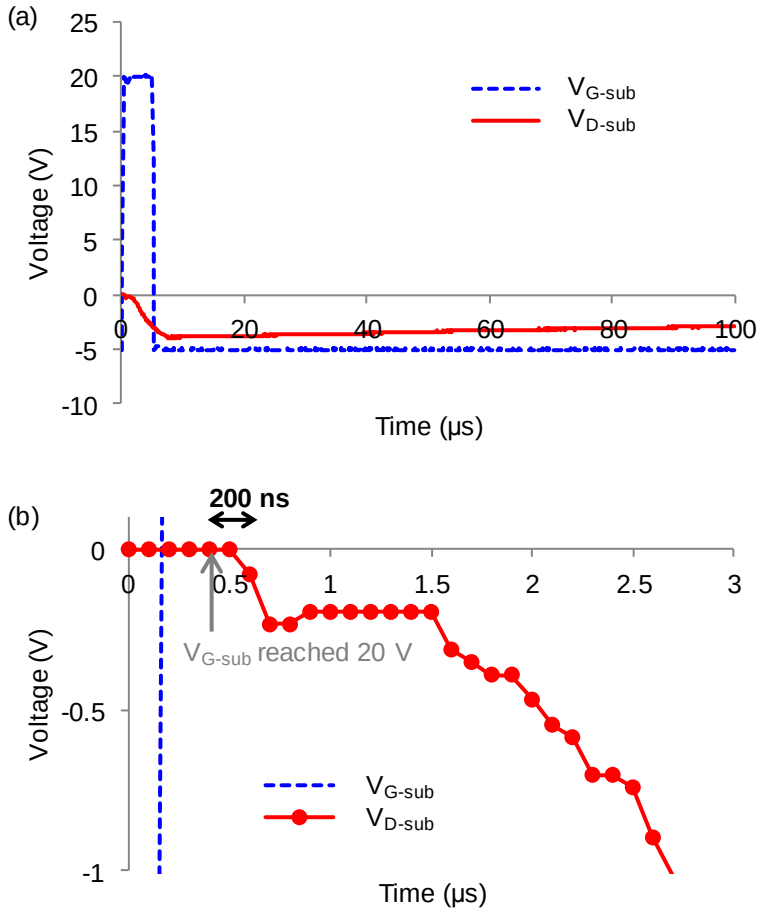

Figure 4-9 Dynamic measurement result of a TiN-coated polySi 5T relay, actuated to one side, operating like a 3T relay. $V_{D\text{-}sub}$ versus time is plotted. V_{low} = -5 V and V_{high} = 20 V were used. The device had a mechanical delay of around 200 ns. Drawn dimensions: L_b = 22 µm; w = 600 nm; g_g = 750 nm. TiN coating layer was 150 nm..

4.4.3. Cycling Measurement

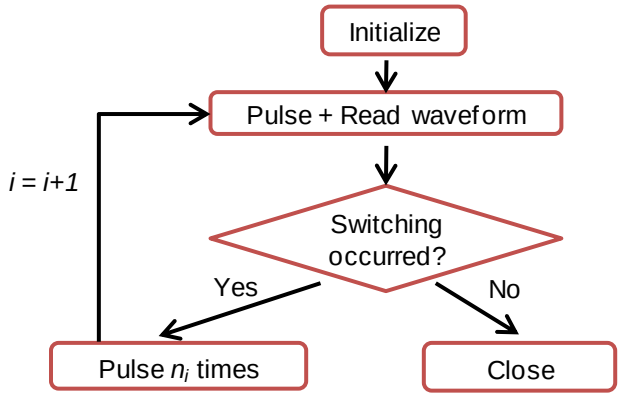

Figure 4-10 Flow chart of method used for the cycling test. A waveform was taken to check if successful switching occurred after n_i (i=1, 2, 3, …) cycles. n_i was an input parameter which was an array of numbers, corresponding to the number of cycles after which a successful switching would be tested. If the switching was successful, i increased and cycling continued, whereas if the switching failed, the program ended.

A cycling measurement was performed to test the reliability of the device. The device was tested as shown in the flow chart in Figure 4-10. The test was automated by creating C-language subroutine libraries. The measurement setup for the "pulse and read waveform" step was the same as that for the dynamic measurement in Figure 4-7. If the ratio between the on-resistance and the off-resistance was smaller than a certain threshold value, the switching was considered to be unsuccessful.

Figure 4-11 shows the cycling measurement result for the same TiN-coated polySi 5T relay used for the mechanical delay measurement in Section 4.4.2. With the measured $V_{D\text{-}sub}$, an approximate value of $R_{on,NEM}$ can be estimated from Eq. 4-1. The device was actuated to one side, operating like a 3T relay. $V_{G\text{-}sub}$ was pulsed between V_{low} = -5 V and V_{high} = 20 V, and $V_{S\text{-}sub}$ was biased at V_{low} = -5 V. The device

switched up to 4×10^8 cycles, at which point the beam did not pull out. However, the stiction was temporary, and the device was functional at the next sweep. The variation in on-resistance with cycling is an issue that needs to be studied in the future.

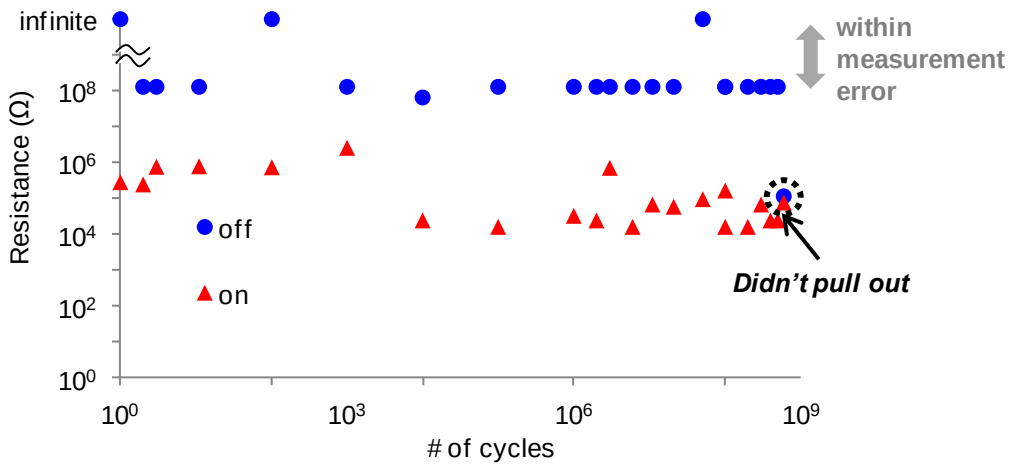

Figure 4-11 Cycling measurement of a TiN-coated polySi 5T relay, actuated to one side, operating like a 3T relay. The device successfully switched up to 4×10^8 cycles. Drawn dimensions: L_b = 22 μm; w = 600 nm; g_g = 750 nm. TiN coating layer was 150 nm.

4.5. Variation – Isolated Beam Structures

In order to decouple the actuating voltage and the voltage at the contacts, the relay can be designed as a six terminal (6T), or a double-sided four terminal (4T) device as shown in Figure 4-12. By electrically isolating part of the beam, the part of the beam overlapping with the gate electrode, relevant to the electrostatic actuation, is isolated from the source and drain that conduct. When the beam is actuated, the source and drain are electrically connected, while there is no current flow to/from the beam. This design allows the contacting voltage to be made independent of the actuating voltage,

enabling a wider range of functions to be performed with a single device. For example, by different biasing schemes, the same device can be used both as a buffer and as an inverter as illustrated in Figure 4-13 (Recall that only an inverter function was possible with the 5T relay without isolation in the beam).

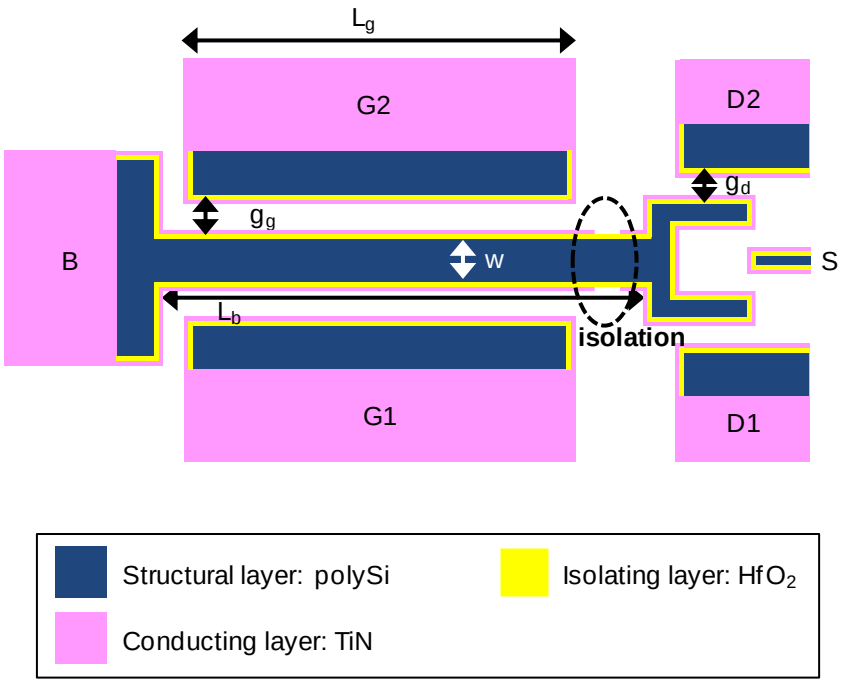

Figure 4-12 Schematic of a six-terminal (6T), or a double-sided four-terminal (4T), isolated beam relay. The beam has an isolation region, so that the area relevant to the electrostatic actuation overlapping with the gate electrodes is electrically isolated from the area between the source and the drains that conducts when actuated.

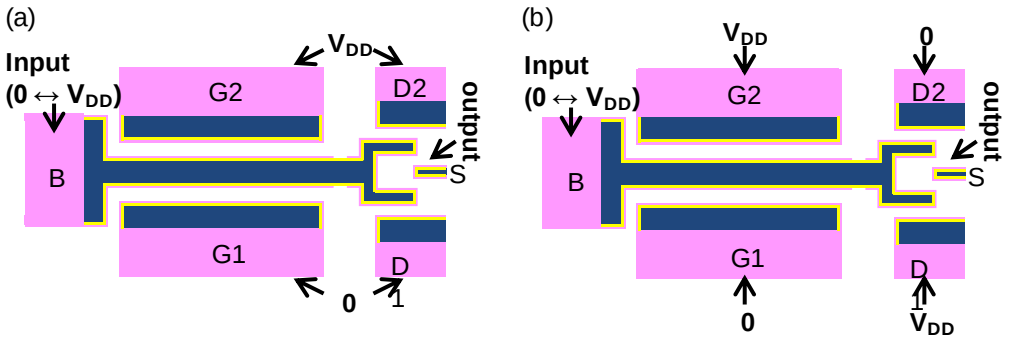

Figure 4-13 Schematic of a single 6T relay design with beam isolation performing the function of (a) an inverter and (b) a buffer, by simply changing the biasing scheme.

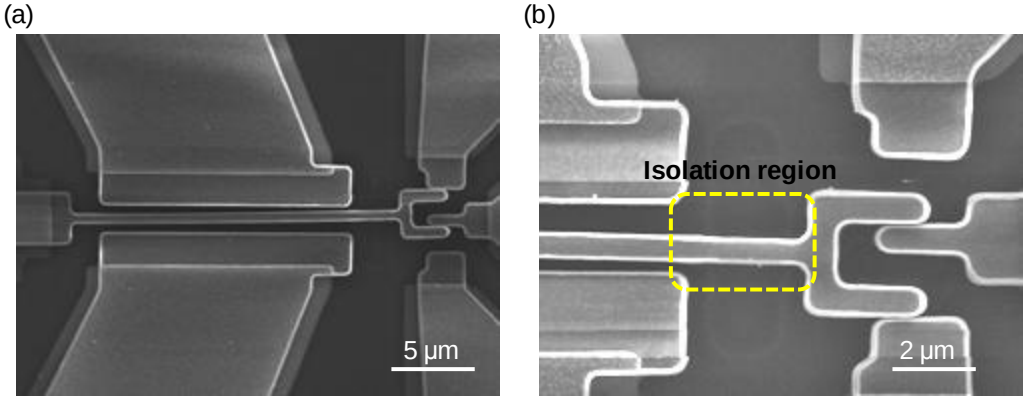

Figure 4-14 SEM image of (a) a 6T isolated beam relay and (b) a zoomed-in view, where the beam isolation region can be seen.

The device was fabricated using polySi as the structural layer, HfO_2 as the isolating layer, and TiN as the conducting layer[1]. An additional mask was used to open up the isolating region on the beam and selectively etch the TiN. Figure 4-14 shows an SEM of the fabricated device. The beam was slightly thinner in the area where the TiN had been etched for isolation. The beam made contact to either the top drain (D1) and the

[1] Device fabrication was done by Daesung Lee (Stanford University).

source (S) (Figure 4-14a), or the bottom drain (D2) and the source (S) (Figure 4-14b) by charging during imaging.

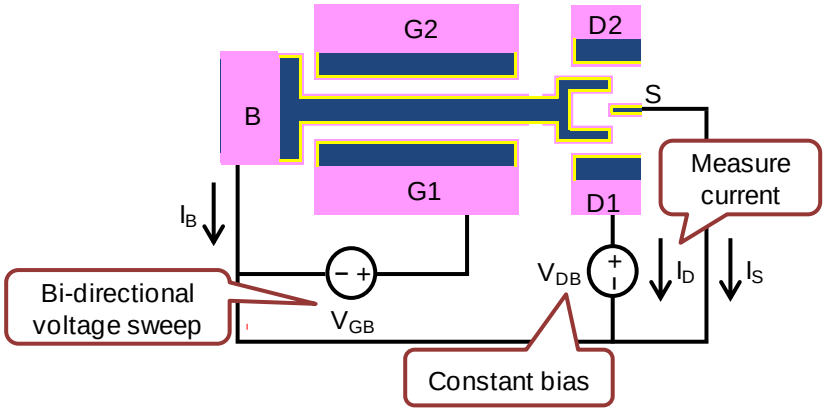

Figure 4-15 Schematic of a quasi-static measurement setup for a 4T isolated beam relay. Using a parameter analyzer, V_{GB} was quasi-statically swept in both directions, V_{DB} was biased at a constant voltage, and I_D and I_S were measured. I_B was also measured to confirm beam isolation.

A quasi-static sweep of V_{GB} in both directions was performed on a 6T isolated beam relay actuating to one side, operating the device like a 4T relay, to pull the beam in and out of contact with the source and the drain as shown in Figure 4-15. Current on all four terminals was measured. Electrical measurement result in Figure 4-16 shows current between the source and the drain, when the beam was actuated, while there was no current through the beam, confirming successful electrical isolation of the beam.

SEM images, as shown in Figure 4-17, revealed that one of the failure mechanisms was damage of the contacting surfaces. Peeling of the coating materials was observed, which is presumed to be caused by a voltage that is too high across the contact.

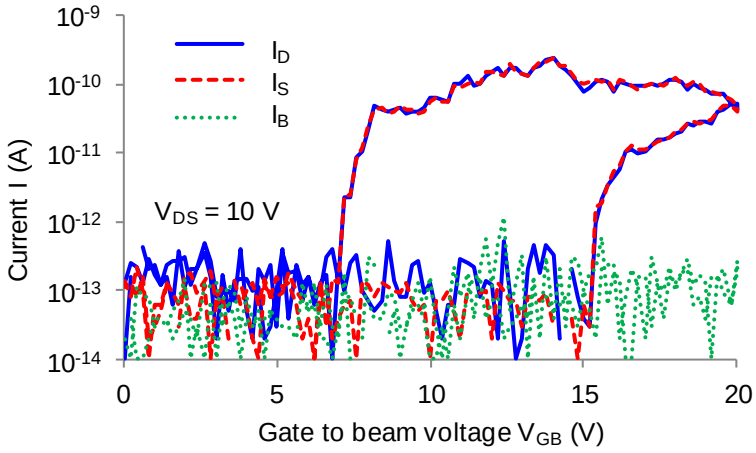

Figure 4-16 Quasi-static measurement result of an isolated beam 6T relay, actuated to one side, operating like a 4T relay. The beam successfully pulled in at 15 V and pulled out a 7 V, with zero beam current. Drawn dimensions: L_b = 30 µm; g_g = 700 nm. TiN coating layer was 50 nm.

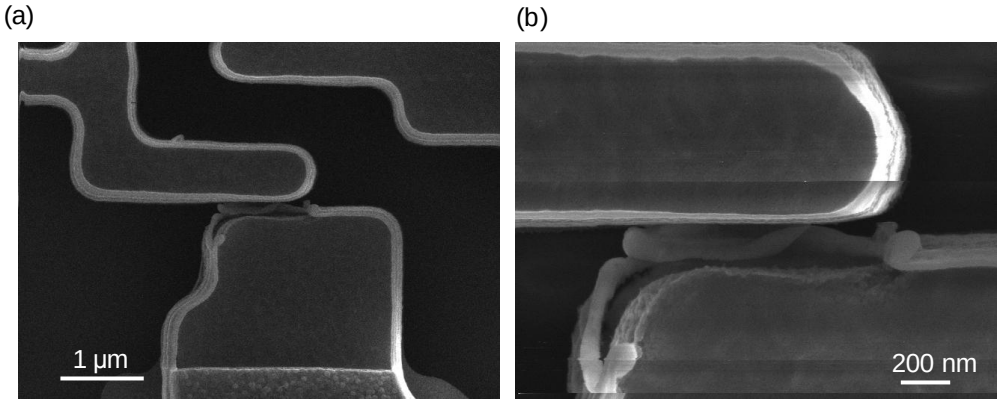

Figure 4-17 SEM images of a failed device. The conducting layer was peeled off, which is presumed to be due to the high voltage across the contact (V_{DS} = 12.5 V).

Possible solutions to this problem include using a conducting layer that can withstand higher current by changing the type of material and/or increasing the layer thickness.

4.6. Conclusion

This chapter demonstrates the feasibility of fabricating NEM relays using optical lithography with separate structural layers and conductive layers. Quasi-static, dynamic, and cycling measurements were performed to confirm the functionality of the device, as well as to test the reliability. A variation of the device structure was also fabricated and tested, which allows for a single device to perform various logic functions with different biasing. However, these device fabricated using optical lithography are unsuitable for demonstration of CMOS–NEM hybrid circuits, because the operating voltage is too high, and, more importantly, because the process temperature is too high to be CMOS-compatible.

Chapter 5: E-beam Lithography (EBL) Patterned Relays[1,2]

5.1. Introduction

One method of scaling down the operating voltage of laterally actuated relays with the limited optical lithography capabilities is using e-beam lithography (EBL). Previously, laterally actuated clamped-clamped relays have been fabricated using EBL, where ruthenium was used as the structural material and was patterned by etching [9] (Table 4-1). However, a clamped-clamped beam structure has the disadvantage of having a higher V_{pi} compared to the cantilever beam structure with the similar dimensions. In this chapter, laterally actuated three-terminal (3T) cantilever type relays were fabricated using EBL to decrease the operating voltage. In addition, CMOS-compatible temperatures were used for fabrication, making the device suitable for CMOS–NEM integration.

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[1] Part of this chapter is taken from S. Chong, B. Lee, K. B. Parizi, J Provine, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit," *IEEE International Electron Devices Meeting*, Washington D.C., 2011, pp. 701-704 and S. Chong, B. Lee, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical relays with silicon nMOS," *IEEE Transactions on Electron Devices,* vol. 59, pp. 255-258, Jan. 2012..

[2] This work was done in collaboration with Byoungil Lee at Stanford University.

5.2. Device Structure

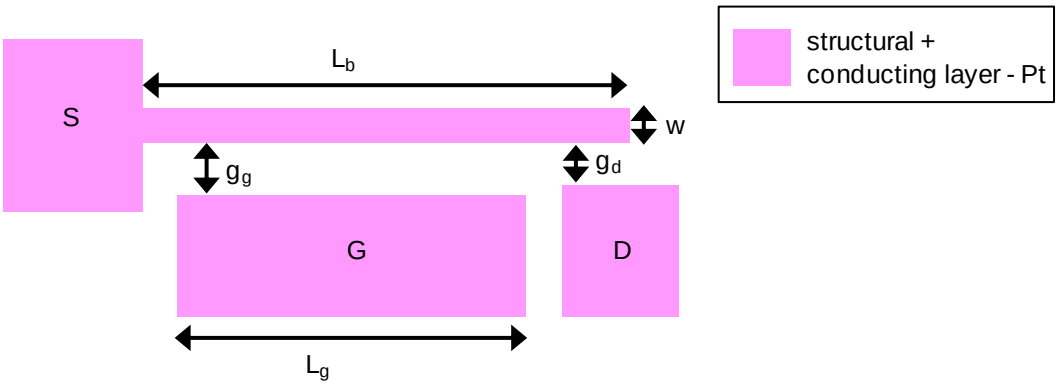

Figure 5-1 Schematic of a three-terminal (3T) NEM relay fabricated using e-beam lithography (EBL). The structural layer is made of a single material, platinum (Pt).

Using EBL, a laterally actuated 3T cantilever NEM relay, as shown in Figure 5-1, was fabricated. A beam width (w) of around 60 nm was achieved. Because a deposition of 60 nm of platinum (Pt) was feasible, the device could be made all-Pt, instead of having a separate structural layer and a conducting layer. Pt was used as the structural material, because, in addition to its desirable conductivity and stability in air, it is a material well-suited for a lift-off process, the process used in combination with EBL for patterning structures.

5.3. Process Flow

Having an all-metal relay, the process flow is even simpler than that of the optically patterned NEM relays (Figure 4-2). The process flow was as follows (Figure 5-2). On a bare Si wafer, around 700 nm of insulating SiO_2 layer was deposited by thermal oxidation at 1000 ºC. For efficiency, the pads for probing during electrical testing were patterned by optical lithography using Pt lift-off. 1 µm of Shipley 3612

photoresist was spun, exposed with an i-line stepper, and developed. Then, 1 nm of titanium (Ti; adhesion layer) and 55 nm of Pt was deposited by evaporation, and lift-off was done by first soaking in acetone, followed by sonication.

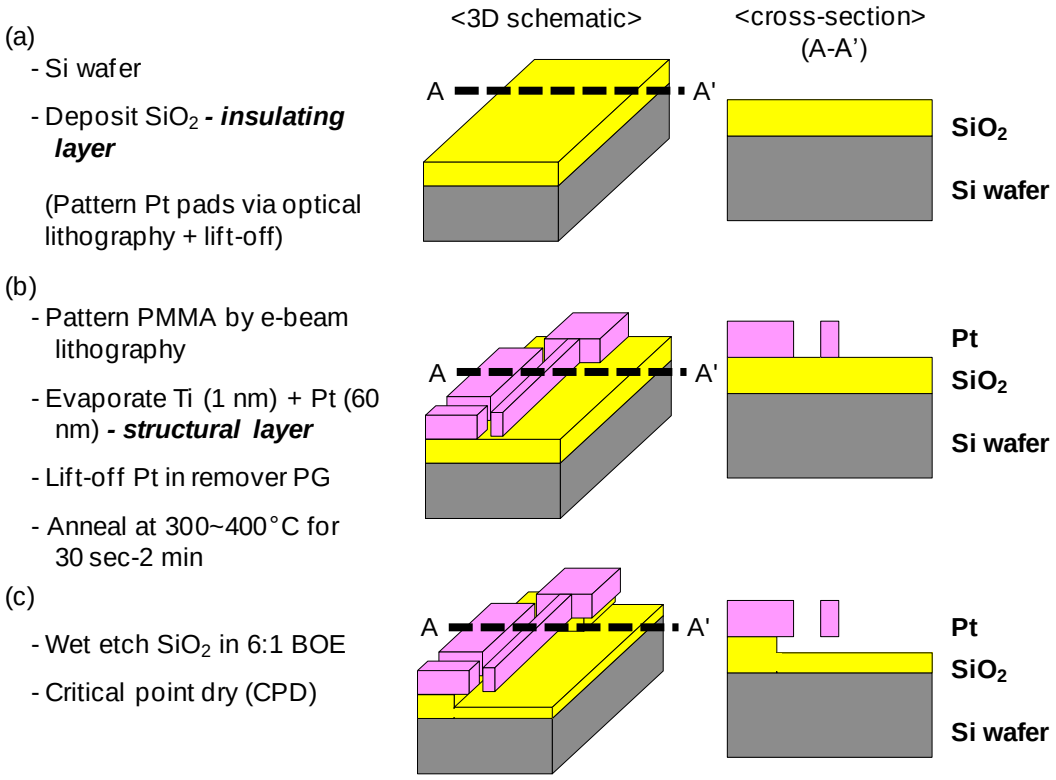

Figure 5-2 Process flow of the fabrication of a laterally actuated Pt NEM relay patterned using EBL and lift-off.

Next, 100 nm of 2 % 950K poly(methyl methacrylate) (PMMA) resist was spun, and the NEM relay gate, source, and drain were patterned by EBL, aligning to the pads. The beam energy was 10 keV, the aperture size was 7.5 µm or 10 µm, the beam current was around 10 pA, and the working distance was around 5 mm. The resist was developed by soaking in 1:3 Methyl isobutyl ketone (MIBK):isopropanol (IPA) for 40 seconds and rinsing in IPA for 20 seconds. Then, 1 nm of Ti (adhesion layer) and 60–

70 nm of Pt was evaporated, and a lift-off was done by first soaking in remover PG, followed by sonication.

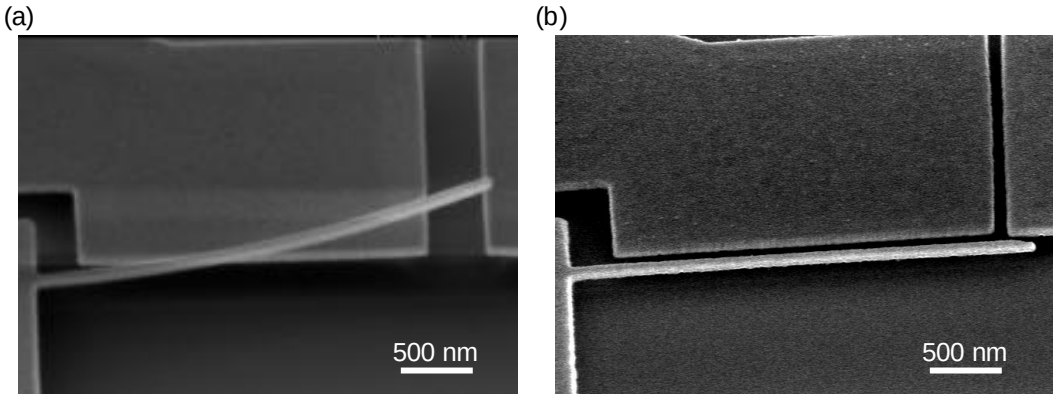

Figure 5-3 SEM images showing Pt beams (a) without anneal and (b) with a rapid thermal anneal (RTA) at 300 °C for 2 min in N_2. The anneal step reduced the stress gradient in the beam.

Then the device was annealed at 300–400 °C for 30 seconds to 2 minutes to release the stress gradient of the beam, which was a critical step. Without this anneal, the beams were found to curl upwards after release as shown in Figure 5-3a. However, performing a rapid thermal anneal (RTA) in N_2 released the stress gradient of the beam and resulted in flat beams as shown in Figure 5-3b. The final step was releasing the beam, where a timed SiO_2 etch in 6:1 buffered oxide etch (BOE) was performed, followed by a critical point dry (CPD). Notice that the temperature never went above 400 °C during NEM relay fabrication; that is, the fabrication can be done at CMOS-compatible temperatures.

Figure 5-4 shows SEM images of the e-beam patterned fabricated devices from a 45 degree tilted view. The e-beam patterned NEM relay is aligned so that it is

connected to the optically patterned pads. A zoomed in image shows the NEM relay in the on-state, as well as the tip of the beam.

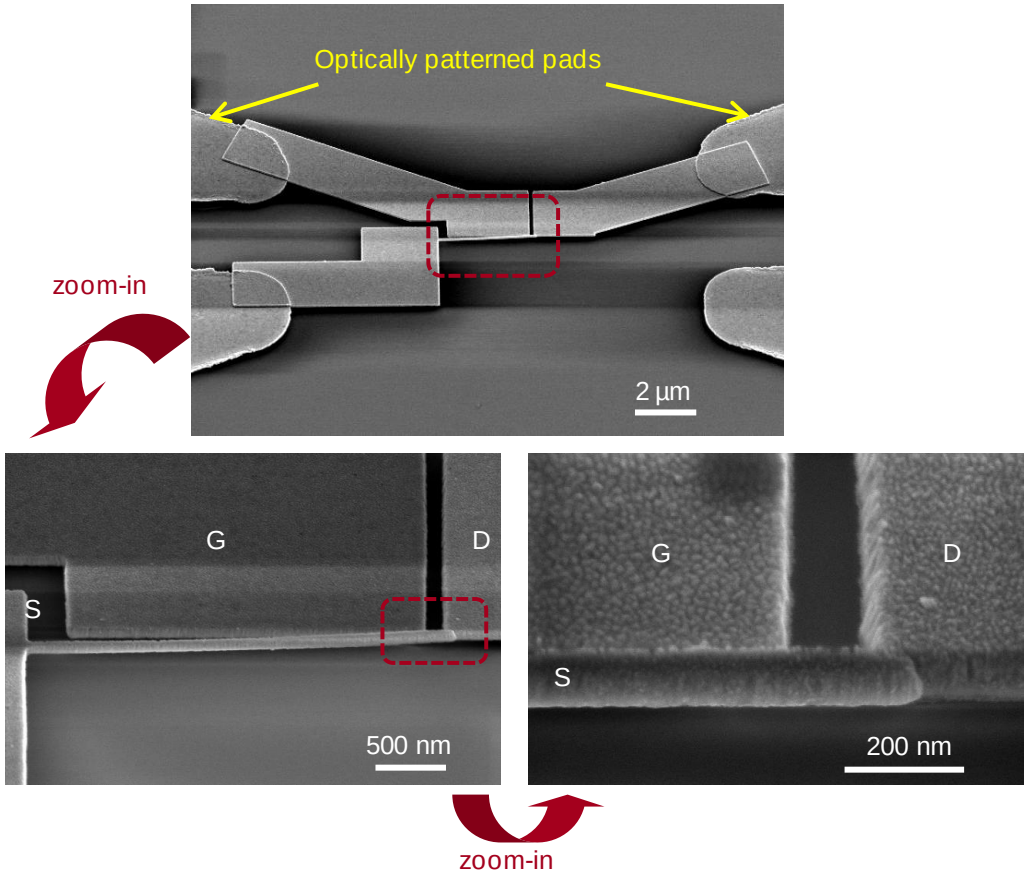

Figure 5-4 SEM images of fabricated e-beam patterned NEM relays, (a) showing the relay aligned to the optically patterned pads, (b) zooming in on the device itself, and (c) zooming in to the tip of the beam.

5.4. Electrical Measurements

The pull-in/out characteristics were measured using the quasi-static test setup shown in Figure 4-4. There was no current compliance in order to measure the on-current level of the device. The device with drawn dimensions of w = 60 nm, L_b = 3.2

µm, and g_g = 100 nm pulled-in at 3.3 V and pulled out at around 2 V with V_{DS} = 1 V. The device demonstrated noise-level off-state current and sharp on/off transitions.

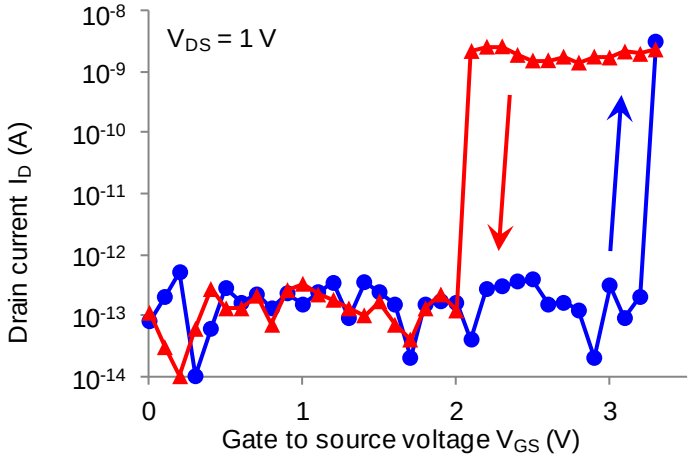

Figure 5-5 Quasi-static measurement result plotting drain current (I_D) versus the gate to source voltage (V_{GS}) of an e-beam patterned 3T NEM relay with drain to source voltage (V_{DS}) of 1 V. Noise-level off-state current and sharp on/off transitions are demonstrated. The beam successfully pulled in and out at 3.3 V and 2 V, respectively. Design parameters as drawn are: w = 60 nm, L_b = 3.2 µm, and g_g = 100 nm.

5.5. Issues

Although a successful pull-in/out was demonstrated, the device had various issues that are discussed below. Methods that were attempted to solve the issues are also listed; however, they were not successful in solving the problems.

5.5.1. High $R_{on,NEM}$

An approximate on-resistance, calculated by V_{DS}/I_D, was in the order of GΩs. The reason for the high on-resistance is attributed to the high contact resistance of the NEM relay, which is an issue that is still under investigation. It is suspected that it

could be caused by modification of Pt surfaces during processing and/or testing. One possible cause is organic deposits due to friction on Pt surfaces, which have been reported [50], [51]. Various methods were attempted to solve this issue, as listed below, but none of these methods consistently yielded lower resistance.

A. *Testing in the N_2 glovebox* to avoid moisture from gathering on the contacting surfaces and/or oxidation of possible contaminants on the contacting surfaces during testing, which could affect the contact properties.

B. Testing at low temperatures to avoid oxidation of possible contaminants on the contacting surfaces. The probe station chamber was cooled down to -40 °C.

C. Testing at high temperatures to eliminate possible contaminants on the contacting surfaces. The probe station chamber was heated up to 110 °C.

D. *Coating the relay with another layer of Pt after release* to have a fresh coat of Pt. The original Pt could have been contaminated during the lift-off, RTA, and/or BOE etch. Three methods were attempted:

1) A thin layer (target thickness of around 10 nm) of Pt was sputtered after release to coat the sidewalls while not electrically connecting the different electrodes.

2) A thin layer of Pt (target thickness of around 10 nm) was deposited by plasma atomic layer deposition (ALD) and etched (using plasma reactive ion etch) unmasked to leave Pt on the sidewalls.

3) A thin layer of Pt (target thickness of around 2.5 nm) was deposited by thermal ALD, where Pt is known to nucleate more easily on Pt than on SiO_2. This process was not extensively studied and needs further investigation.

E. *Isotropically etching Pt after lift-off* to remove Pt with possible contaminants on the surface. The Pt was dipped in aqua regia ($HCl:HNO_3:H_20$ = 3:1:2) for 1–2 minutes with an expected etch of around 5 nm.

F. *Doing a longer soak in remover PG, a soak at higher temperatures (40 °C) and/or a longer sonication for lift-off* to remove PMMA more thoroughly which could be left over on the Pt contacting surfaces.

G. Rinsing the device in water after the soak in remover PG for lift-off to remove the residues of PMMA, acetone, and/or IPA. Acetone and IPA were always sprayed on the samples after lift-off to rinse the samples.

H. Plasma clean after release to eliminate possible contaminants on the contacting surfaces.

Pt-coated polySi optical lithography devices showed an on-resistance less than 3 kΩ (Section 4.4.1), and previous works using different materials and/or structures have shown an on-resistance less than 100 kΩ [8]. Therefore, although the issue has not been solved, these works suggest that gaining further fundamental understanding of material issues coupled with optimized mechanical design may lead to a satisfactory solution. Also, controlling the environment in which the device operates may lead to a lower, more consistent resistance.

5.5.2. Low Operable V_{DS}

Another issue with the relays was that they could not consistently withstand a V_{DS} as high as V_{pi}, which is a condition that needs to be met in some NEM–CMOS applications, including the NEM-CMOS SRAM cell. Increasing V_{DS} resulted in

failure to pull-out, as shown in Figure 5-6. The quasi-static measurement with the same 3T NEM relay used in Figure 5-5 showed that, while the device successfully pulled in and out at V_{DS} = 1 V and 2 V, it did not pull out at V_{DS} = 2.5 V. This was smaller than V_{pi}, which was around 3 V.

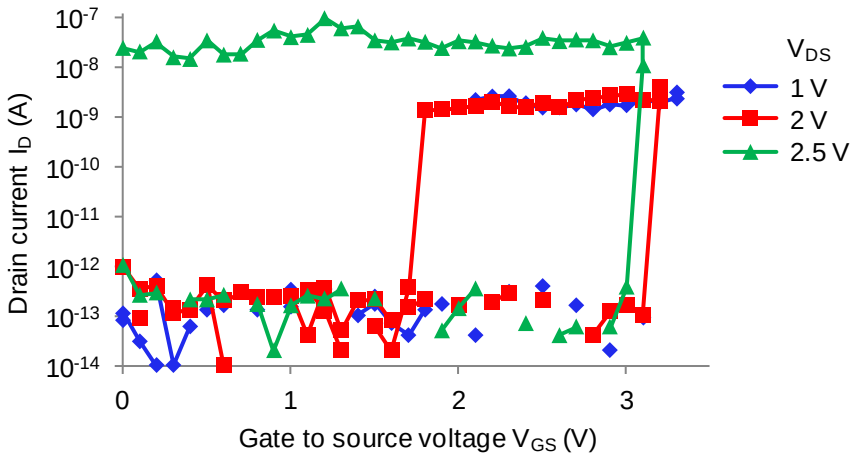

Figure 5-6 Quasi-static measurement result, plotting I_D versus V_{GS} of a 3T NEM relay with different V_{DS} of V_{DS} = 1 V, 2 V, and 2.5 V. As V_{DS} increased, the beam failed to pull out at V_{DS} = 2.5 V, which was still smaller than V_{pi} of around 3 V. The device under test was the same as that used for Figure 5-5.

Various variations of device structure have been attempted to increase V_{po}. As shown in Figure 5-7, beams with triangular tips were designed to decrease the surface force by decreasing the contact area, and beams with extruding tips were designed to decrease the electrostatic force in the on-state by increasing the distance between the gate and the source in the on-state; however, these variations did not yield a consistent increase in the maximum operable V_{DS}.

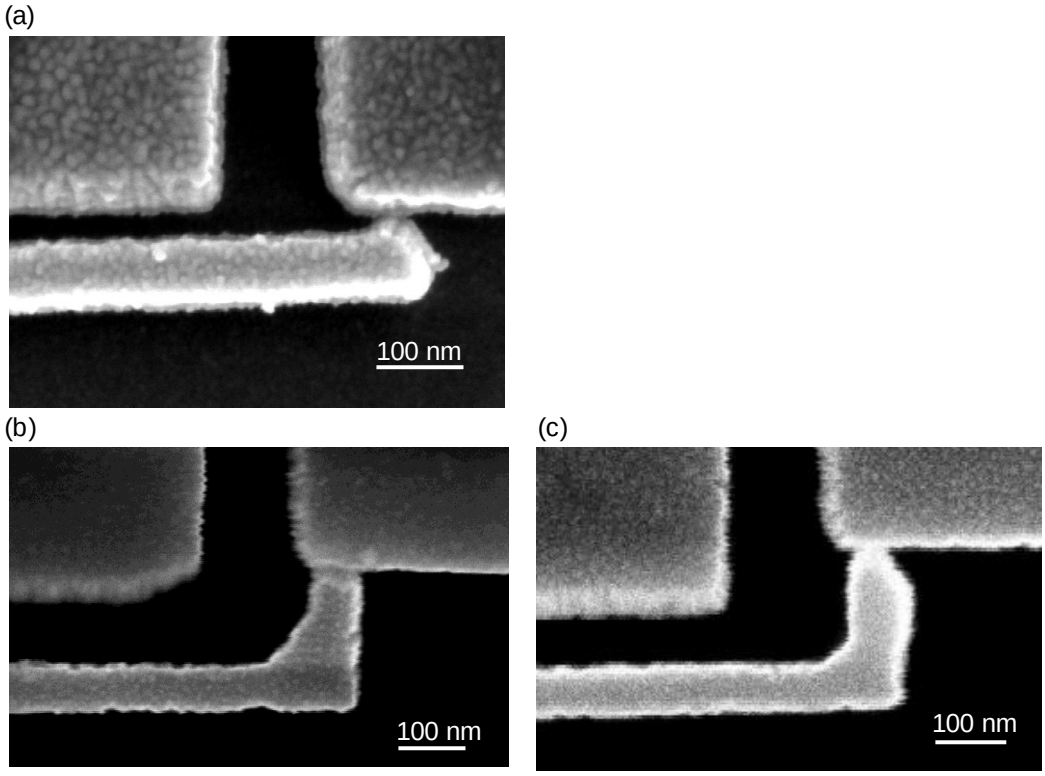

Figure 5-7 SEM images of the tip of the NEM relay, showing design variations to increase V_{po} by having (a) a triangular tip, and (b), (c) extruding tips. However, these did not result in consistent increase in the maximum V_{DS} at which the beam successfully pulled out.

5.6. Scaling to Sub-1 V Supply Voltage

Although V_{pi} is still in the 3–5 V range even with EBL, with continued scaling, the operating voltages of NEM relays are expected to reduce down to sub-1 V. With these devices, conventional CMOS with a 1 V power supply could be used together. Based on the two dimensional numerical simulation using MATLAB (with and without the inclusion of the van der Waals force), as described in Section 2.2.1, it was predicted that V_{pi} below 1 V can be achieved by scaling all dimensions of the current fabricated

device by a factor of 0.2 as shown in Figure 5-8. This required a beam width of 12 nm and a beam-to-gate gap of 20 nm. This was consistent with the predictions made in [8] and [10].

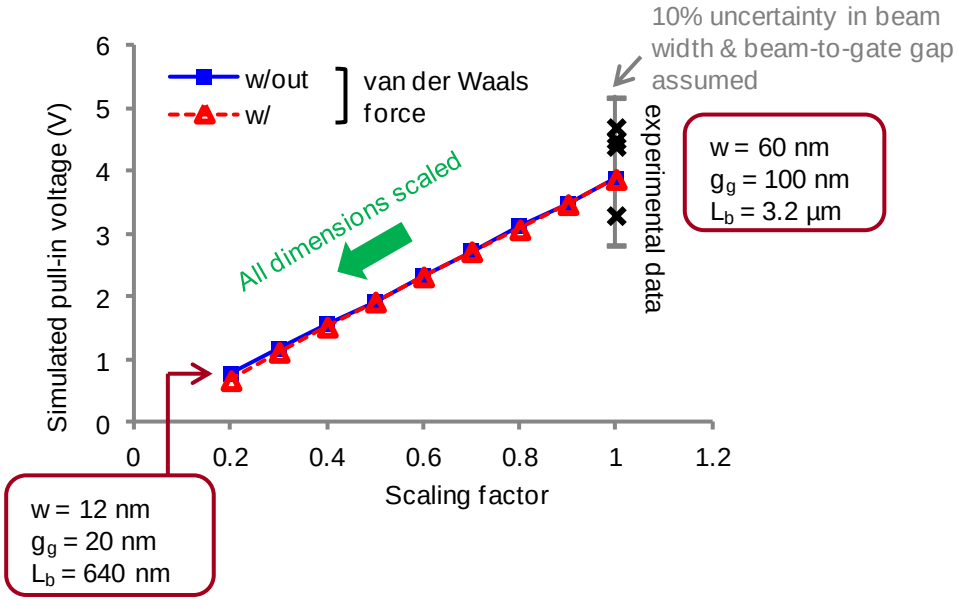

Figure 5-8 Two-dimensional (2D) simulation result of V_{pi} scaling by scaling all dimensions of the NEM relay design in by a scaling factor. V_{pi} including the van der Waals force (F_{vdw}) (Δ in red) were not significantly different from those without F_{vdw} (o in blue) at these dimensions. Experimental results (× in black) were within the error bar, which accounts for the difference between the drawn w and g_g and their actual fabricated sizes (~10 % uncertainty assumed). With w = 12 nm, g_g = 20 nm, and L_b = 640 nm, V_{pi} < 1 V was achieved.

5.7. Conclusion

The EBL patterned NEM relays were fabricated using Pt lift-off. These devices are suitable for demonstration of CMOS–NEM integration, because their fabrication can be done at CMOS-compatible temperatures (below 400 °C), and the operating

voltages are low enough to operate with outdated CMOS at the same supply voltage. Electrical results showed a successful pull-in at around 3 V, sharp on/off transition, and zero off-state leakage. Various attempts have been made to resolve the issues of a high $R_{on,NEM}$ and the operable V_{DS} being smaller the V_{pi}, but no successful solution has been found. Simulations predict that a NEM relay with beam widths and gap sizes in the 10–20 nm range would yield a sub-1 V V_{pi}, with which integration with state-of-the art CMOS operating at sub-1 V V_{DD} would be possible.

Chapter 6: CMOS–NEM Integration[1]

6.1. Introduction

Despite the promising projections made for CMOS–NEM hybrid circuits, there has been no experimental demonstration of these circuits. More generally, electrostatically actuated MEM/NEM resistive switches have never been demonstrated to operate with on-chip CMOS. Past work is limited to low temperature CMOS-compatible processes for fabricating NEM relays [8], [9], [52] including actual fabrication of contacting switches in the CMOS back-end-of-line [52]. However, experimental demonstrations of electrical interaction between CMOS and integrated M/NEMS have been limited to contact-less MEMS devices [53], [54], which do not convey DC signals, and thermally actuated resistive switches [55], which consume static DC current. This work demonstrates, for the first time, a functioning CMOS-electrostatically actuated NEM relay integrated circuit with electrical results.

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[1] Part of this chapter is taken from S. Chong, B. Lee, K. B. Parizi, J Provine, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit," *IEEE International Electron Devices Meeting*, Washington D.C., 2011, pp. 701-704 and S. Chong, B. Lee, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical relays with silicon nMOS," *IEEE Transactions on Electron Devices,* vol. 59, pp. 255-258, Jan. 2012.

6.2. Process Flow

Laterally actuated platinum (Pt) three-terminal (3T) NEM relays were fabricated using e-beam lithography (EBL) on top of CMOS fabricated at the Stanford Nanofabrication Facility (SNF)[1]. The CMOS had a gate length of 1–2 μm and a supply voltage of around 5 V. A silicon MOS technology capable of a relatively high power supply voltage was used so that the same supply voltage can used for both the MOSFETs and the NEM relays, whose supply voltage scaling is currently limited by lithographical limits.

The process flow of the CMOS–NEM hybrid circuit after CMOS fabrication was as follows (Figure 6-1). First, a low temperature silicon dioxide (LTO) passivation layer was deposited on top of unpassivated silicon MOSFETs by low pressure chemical vapor deposition (LPCVD) at 400 °C and densified at 950 °C. Via holes were then etched into the LTO down to the CMOS layer. The vias, interconnects, and pads were simultaneously formed by optical lithography, 5 nm titanium (Ti; adhesion layer) and 80 nm Pt sputter deposition, and lift-off in acetone. Pt was chosen as the material for the via for convenience, since this would allow the processing of vias and the Pt pads to occur at the same time. Then, an anneal step was performed for 10 minutes at 400 °C to improve the contacts to CMOS. This step resulted in a significant improvement in contacts to the PMOSFETs.

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[1] CMOS fabrication process flow was based on the process flow used for the Stanford University EE410 class, "Integrated Circuit Fabrication Laboratory." The fabrication of CMOS was done in collaboration with Kokab B. Parizi.

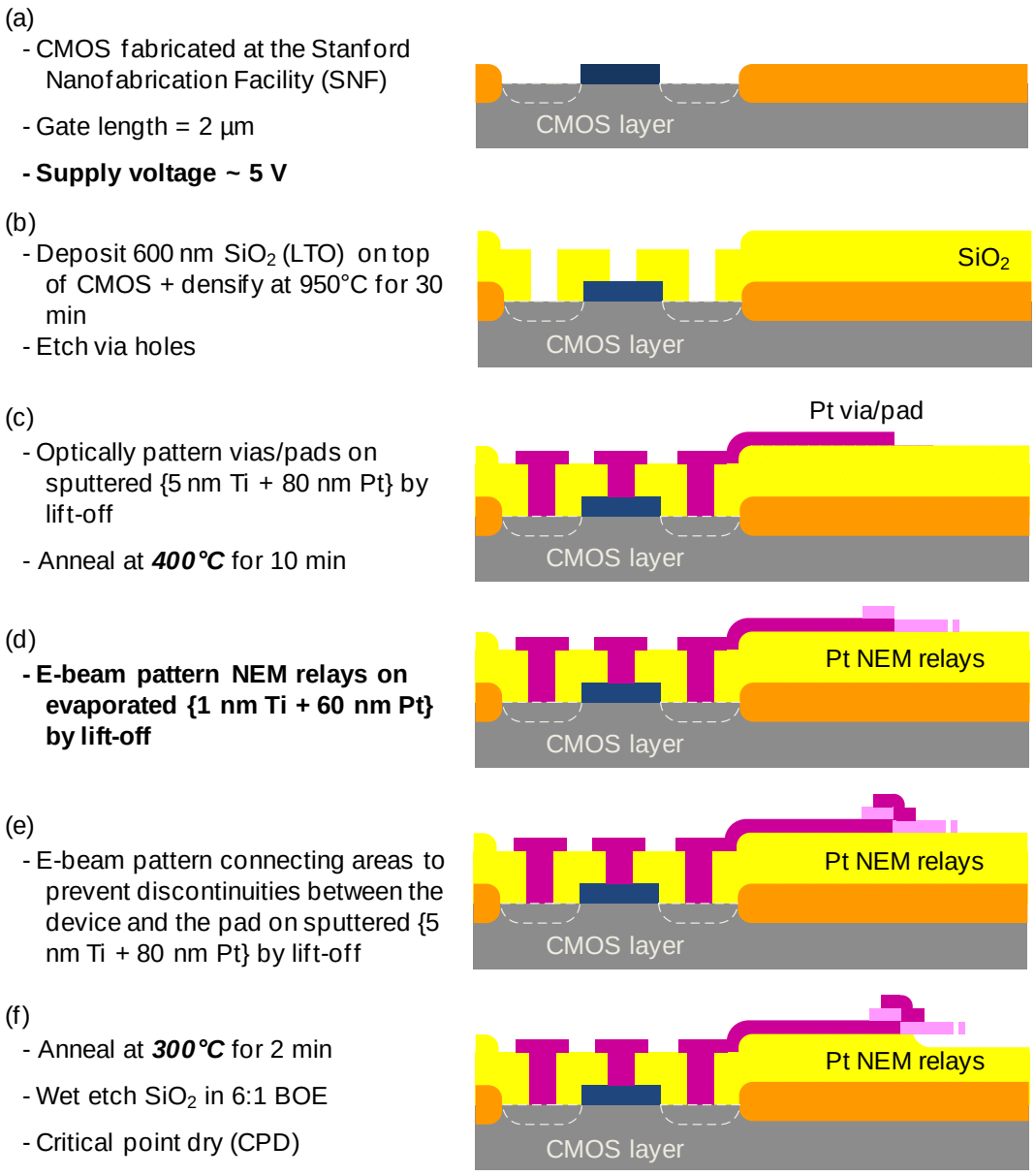

Figure 6-1 Process flow of a laterally actuated Pt NEM relay (demonstrated in Chapter 5) on pre-fabricated CMOS.

Next, the NEM relays were fabricated by EBL, 1 nm Ti (adhesion layer) and 60 nm Pt evaporation deposition, and lift-off in remover PG (Details can be found in Section 5.3). The evaporation deposition method was used for EBL patterning and lift-off,

because an anisotropic deposition is favorable for lift-off of small feature sizes as illustrated in Figure 6-2a. However, as shown in Figure 6-2b, because it is anisotropic, it can result in a poor connection between the optically patterned pads and the e-beam patterned devices. Thus, a second EBL, Pt sputtering deposition, and lift-off were performed to ensure good electrical connection between these areas.

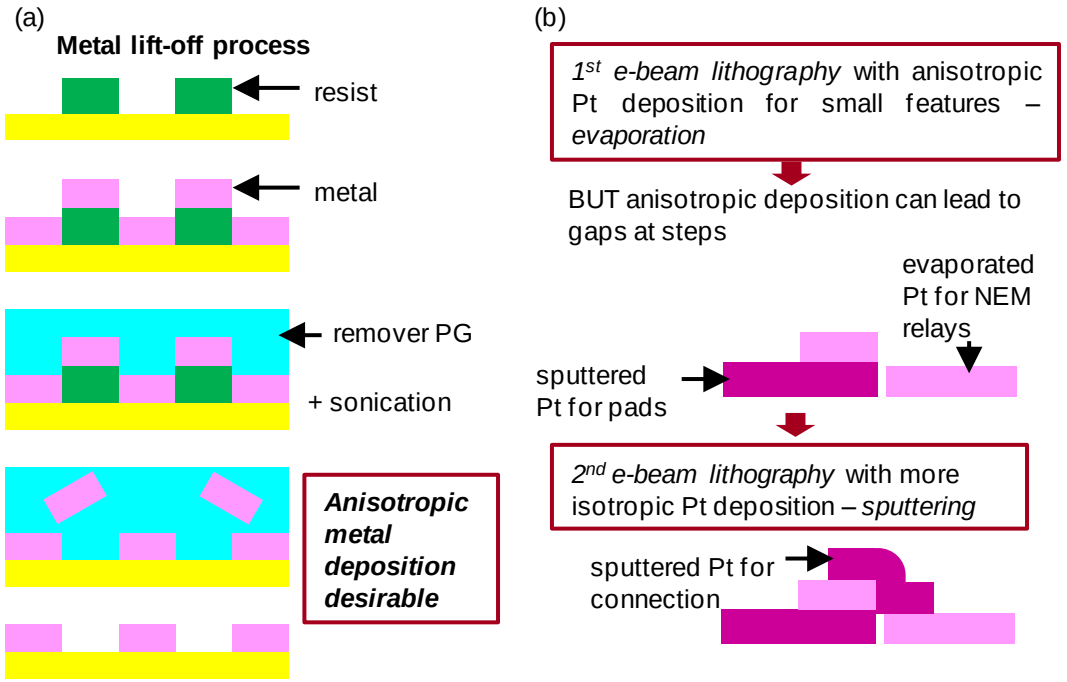

Figure 6-2 Schematic explaining (a) the metal lift-off process and why an anisotropic metal deposition is desirable and (b) the need for a second EBL step.

These lithography steps were followed by a 2 minute rapid thermal anneal (RTA) at 300 ºC to reduce the stress gradient of the Pt beam. Finally, a 1–2 minute timed etch in 6:1 buffered oxide etch (BOE) was used to release the beam, followed by critical point drying (CPD) to avoid stiction. Note that the processing temperature never went above 400 °C throughout the NEM relay fabrication.

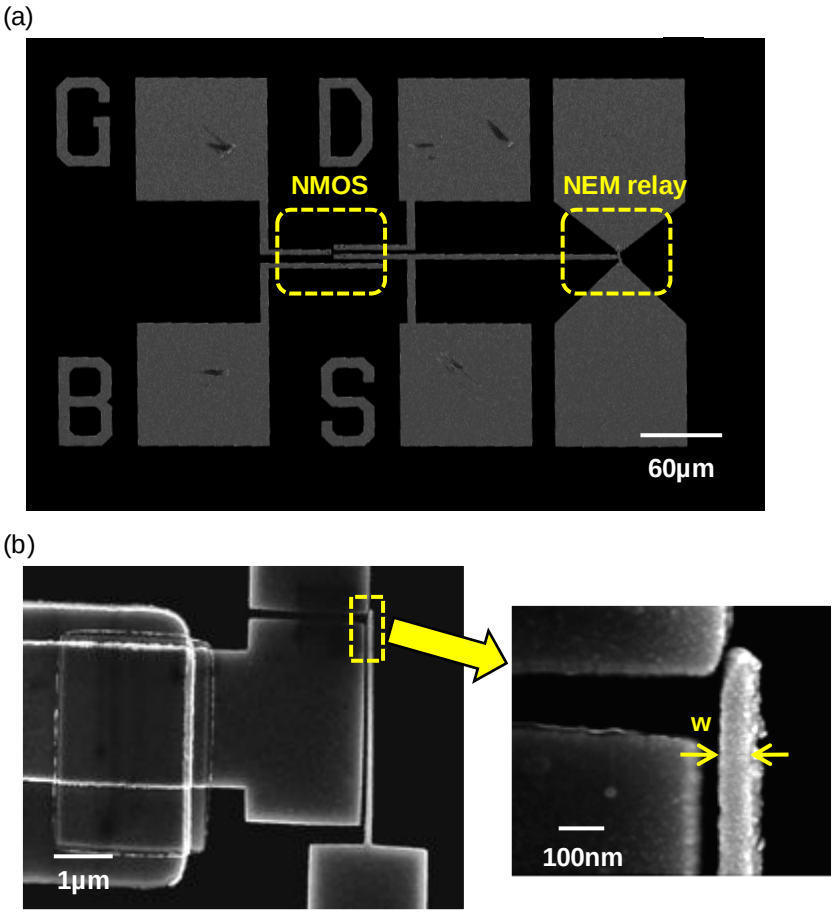

Figure 6-3 Top-down view SEM images of (a) a NEM relay fabricated on NMOS and (b) the NEM relay zoomed-in. Drawn beam length was 3.5 µm, and measured beam width (w) was around 80 nm.

Figure 6-3 and Figure 6-4 show SEMs of NEM relays fabricated on NMOS and CMOS, respectively. For the NEM relay in Figure 6-3, the fabricated relay had w = 80 nm, g_g = 100 nm, and L_b = 3.5 µm. For the NEM relay in Figure 6-4, design parameters as drawn were: w = 60 nm, L_b = 3.54 µm, and g_g = 100 nm, and measured w was around 70 nm.

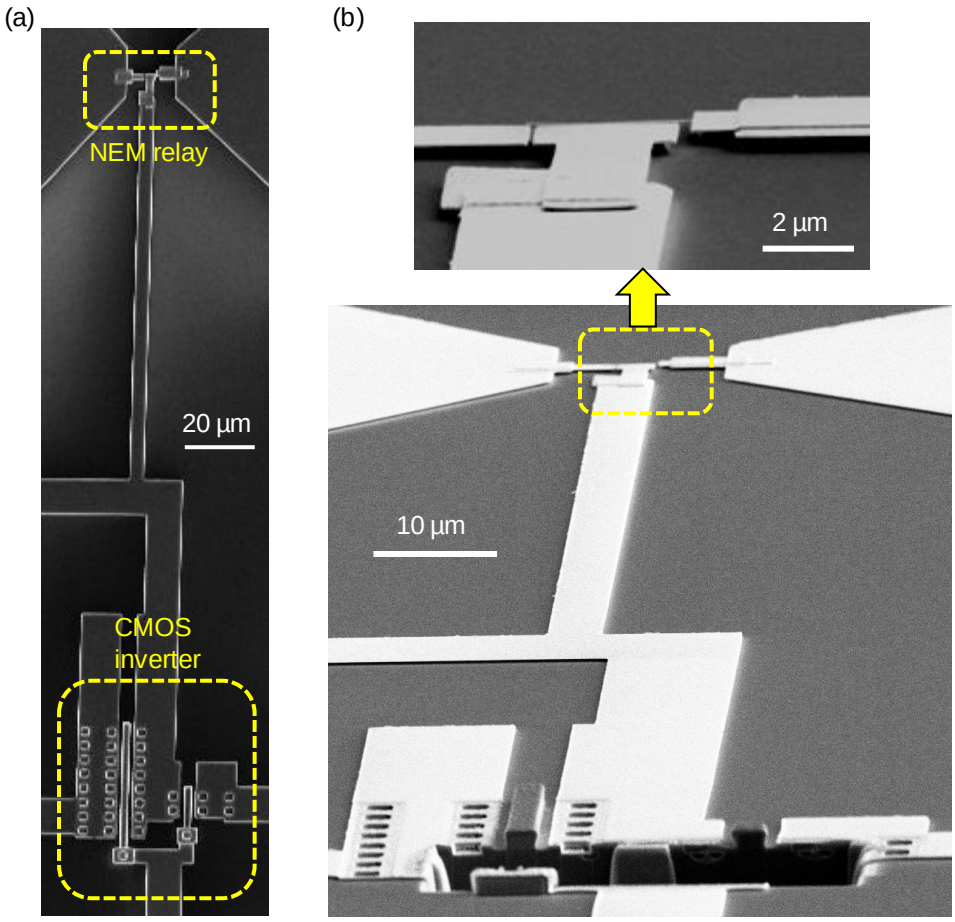

Figure 6-4 (a) Top-down view and (b) 80º tilted view (with CMOS cross-section shown by etching with a focused ion beam) SEM images of a NEM relay fabricated on CMOS. Design parameters as drawn were: w = 60 nm, L_b = 3.54 µm, and g_g = 100 nm. Measured w was around 70 nm.

Although the NEM relay was on a layer above Si MOSFETs, it was not placed directly over the MOSFETs, because a flat surface was needed for EBL. Area reduction by stacking relays directly above MOSFETs can be achieved by depositing a thicker LTO layer and adding an additional chemical-mechanical polishing (CMP) step to planarize the surface before NEM relay fabrication. Planarization by CMP is a common practice for CMOS technologies in production.

6.3. Electrical Measurements

6.3.1. NMOS Driving NEM Relay

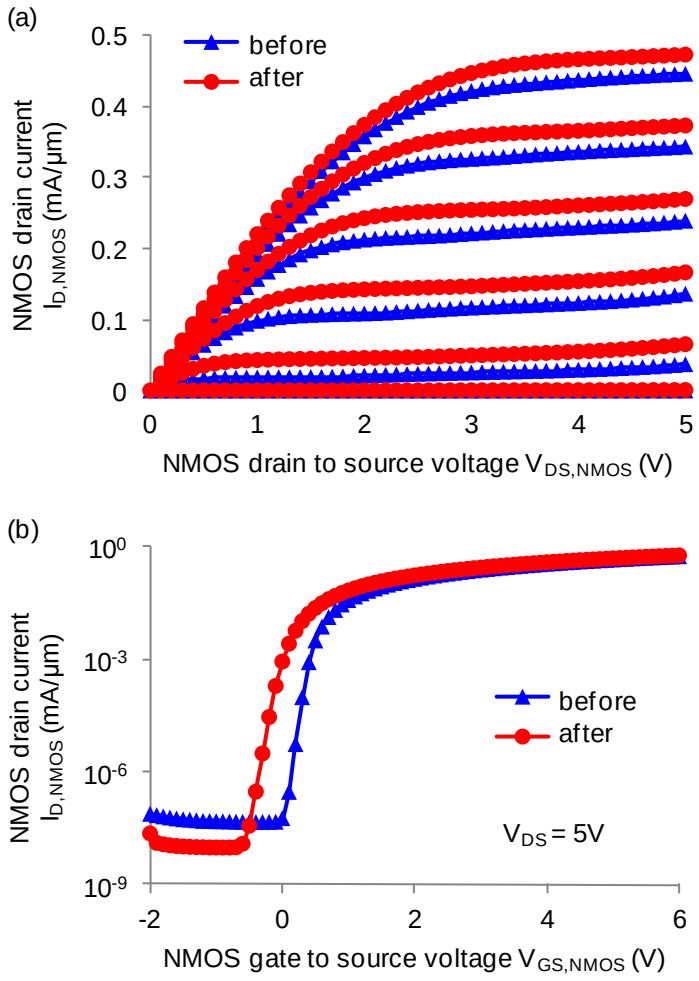

Figure 6-5 (a) $I_{D,NMOS}$ versus $V_{DS,NMOS}$ and (b) $I_{D,NMOS}$ versus $V_{GS,NMOS}$ before and after NEM relay fabrication by post-processing. The NMOS transistor was shown to be functional with good gate control. $I_{D,NMOS}$ vs $V_{GS,NMOS}$ shows a V_{th} shift of ~0.3 V.

NEM integration with only NMOS was initially demonstrated, by showing an NMOSFET drive a NEM relay. First, the NMOS was tested before and after NEM relay fabrication, and the $I_{D,NMOS}$-$V_{DS,NMOS}$ and $I_{D,NMOS}$-$V_{GS,NMOS}$ characteristics were

compared as shown in Figure 6-5. It confirmed that the NMOS maintained functionality and good gate control even after processing, although the threshold voltage shifted by approximately 0.3 V (Figure 6-5b). The NMOS characteristics showed changes throughout the processing steps, but no apparent trend has been observed, requiring further investigation.

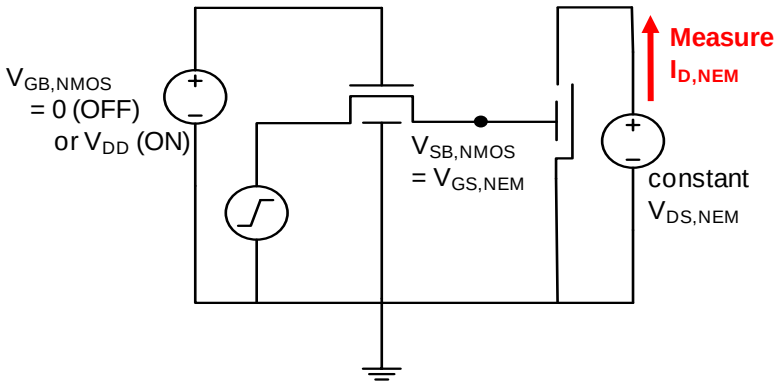

Figure 6-6 Test setup to demonstrate successful NMOS–NEM relay integration, with an NMOSFET serving as a pass transistor and driving the NEM relay. A bidirectional quasi-static sweep of $V_{DB,NMOS}$ with $V_{GB,NMOS} = V_{DD} + V_{th,NMOS} = 6$ V, turns the NEM relay on/off, which can be detected by measuring $I_{D,NEM}$. $V_{DS,NEM}$ was biased at a constant voltage.

The test setup used to demonstrate the combined functionality of the NEM relay and NMOS is shown in Figure 6-6. The NMOS served as a pass transistor and drove the gate of the NEM relay. When the NMOS is turned off (with $V_{GB,NMOS} = 0$), the NMOS source, or the NEM relay gate, becomes a floating node, leaving the NEM relay in the off-state. The capacitance of the floating node, dominated by the pad capacitance, is on the order of 1 pF. When the NMOS is turned on, with $V_{GB,NMOS} = 6$ V ~ $(V_{DD} + V_{th,NMOS})$, the NMOS source, or the NEM relay gate, charges/discharges to

$V_{DB,NMOS}$. When $V_{DB,NMOS} > V_{pi}$, the beam actuates, and current flows between the drain and source of the NEM relay ($I_{D,NEM}$). $V_{DS,NEM} < V_{DD}$ is applied, because the contacts are susceptible to failure, with the beam failing to pull-out when switched off, when a high bias is applied between the contacts as described in Section 5.5.2. As explained earlier, this issue needs to be resolved for the hybrid circuits, such as CMOS–NEM SRAM cells, to be realized.

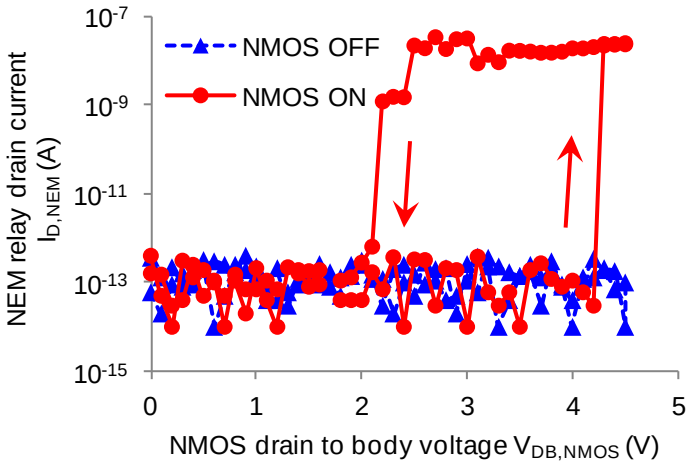

Figure 6-7 Quasi-static measurement result plotting $I_{D,NEM}$ versus $V_{DB,NMOS}$ with $V_{DS,NEM}$ = 0.5V. When $V_{GB,NMOS}$ = 0, the NEM relay stayed in the off-state, whereas when $V_{GB,NMOS}$ = 6 V, $V_{DB,NMOS}$ was passed onto $V_{SB,NMOS}$ = $V_{GS,NEM}$, and the NEM relay actuated with V_{pi} = 4.3 V and V_{po} = 2.1 V.

The $I_{D,NEM}$-$V_{DB,NMOS}$ characteristics, shown in Figure 6-7, demonstrate successful integration of NEM relays with NMOS. When the NMOS was turned off, the relay did not actuate. However, when the NMOS was turned on, the relay turned on at $V_{DB,NMOS}$ = 4.3 V (cf. 2D simulated V_{pi} of 4.8 V, using the method described in Section 2.2.1) and turned off at $V_{DB,NMOS}$ = 2.1 V with $V_{DS,NEM}$ = 0.5 V. The test was repeatable up to

8 cycles (with $V_{DS,NEM}$ = 0.1 V or 0.5 V) with consistent V_{pi} and varying V_{po}. The beam failed to pull out on the 9th cycle but was functional on the following cycle.

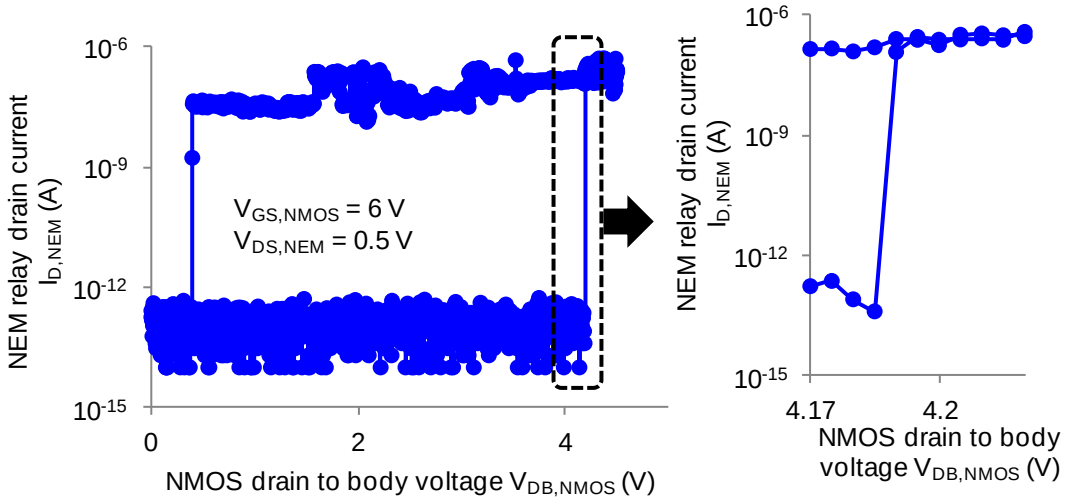

Figure 6-8 Quasi-static measurement result plotting $I_{D,NEM}$ versus $V_{DB,NMOS}$ with a finer voltage steps of 5 mV. An inverse subthreshold slope of approximately 0.8 mV/dec was measured, limited by the noise level of the measurement setup.

The leakage current in the off-state was a few hundred fA (noise level of the measurement setup). The turn-on and turn-off transitions were abrupt, changing by 4–6 orders of magnitudes, when measured in 100 mV steps. As shown in Figure 6-8, finer voltage steps of 5 mV showed an inverse subthreshold slope of approximately 0.8 mV/dec, limited by the noise level of the measurement setup.

6.3.2. CMOS Driving NEM Relay

NEM integration with CMOS was demonstrated next, by showing a CMOS inverter drive a NEM relay. The CMOS inverter characteristics were measured before and after NEM relay fabrication as shown in Figure 6-9. The CMOS inverter

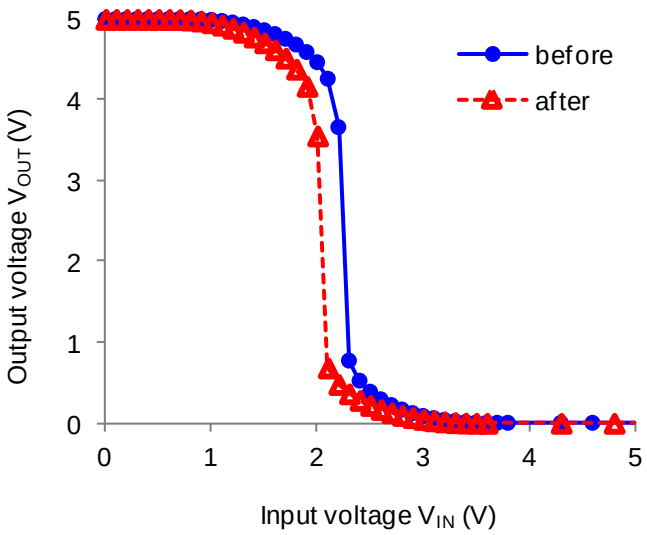

Figure 6-9 Plot showing the CMOS inverter characteristics before and after NEM relay fabrication. Although there was a shift in transition voltage of ~200 mV, the functionality of the CMOS inverter was confirmed after NEM relay fabrication.

remained functional after the relay fabrication, although a shift in the transition voltage was present. This is consistent with the change in NMOSFET threshold voltage in Section 6.3.1. The transition voltage shift was around 200 mV for this run, but the direction and magnitude of the shift were not consistent from run to run. CMOS characteristics showed slight variations after each EBL, RTA, and BOE etch step, during which changes in the gate oxide and/or contact properties were possible.

The test setup used to demonstrate the combined functionality of the NEM relay and CMOS is shown in Figure 6-10. A bidirectional voltage sweep was performed to the input of the CMOS inverter from V_{DD} to 0 to V_{DD}. The output of the CMOS inverter, expected to transition from 0 to V_{DD} to 0, was connected to the gate of the NEM relay. Therefore, with the source (beam) at ground, the relay would start from the off-state, pull-in during the sweep from V_{DD} to 0 at the CMOS input and pull-out

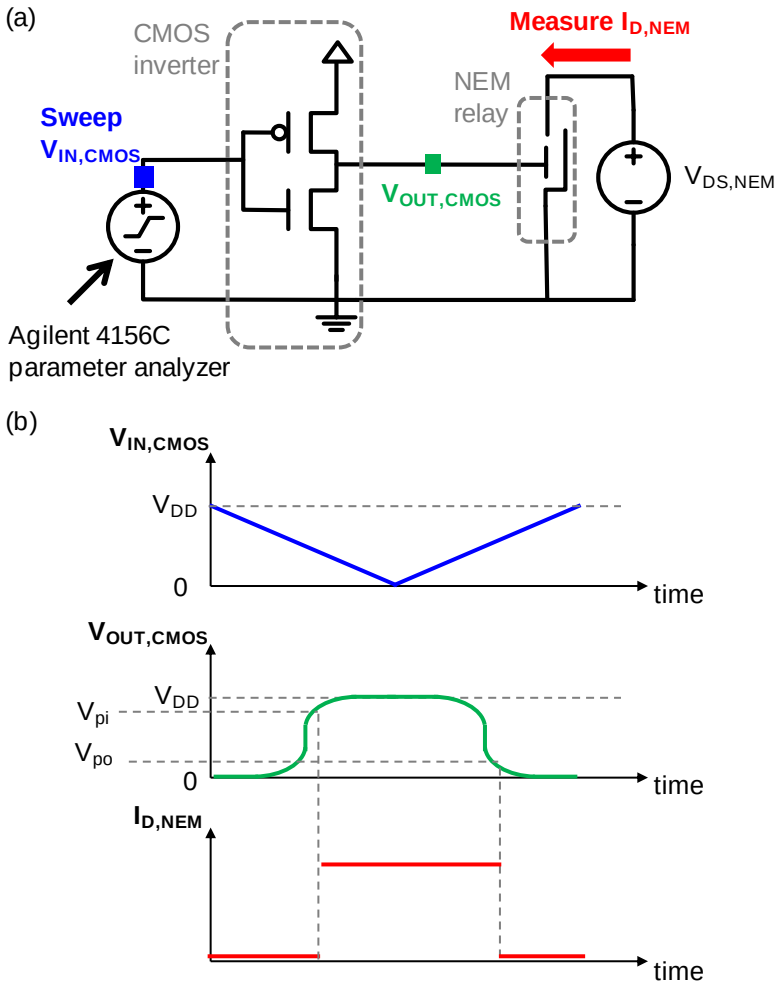

Figure 6-10 (a) Test setup to demonstrate successful CMOS–NEM relay integration, with an inverter driving a NEM relay. (b) Waveforms of the voltage applied to the input of the inverter (blue) and of the expected voltage at the output of the inverter (green) and the expected current through the NEM relay drain (red). $V_{DS,NEM}$ was biased at a constant voltage.

during the sweep from 0 to V_{DD} at the CMOS input. The resulting on/off state of the NEM relay was detected by measuring the current between the drain, biased at a constant voltage, and the source of the relay. The devices were tested in air with N_2 flow.

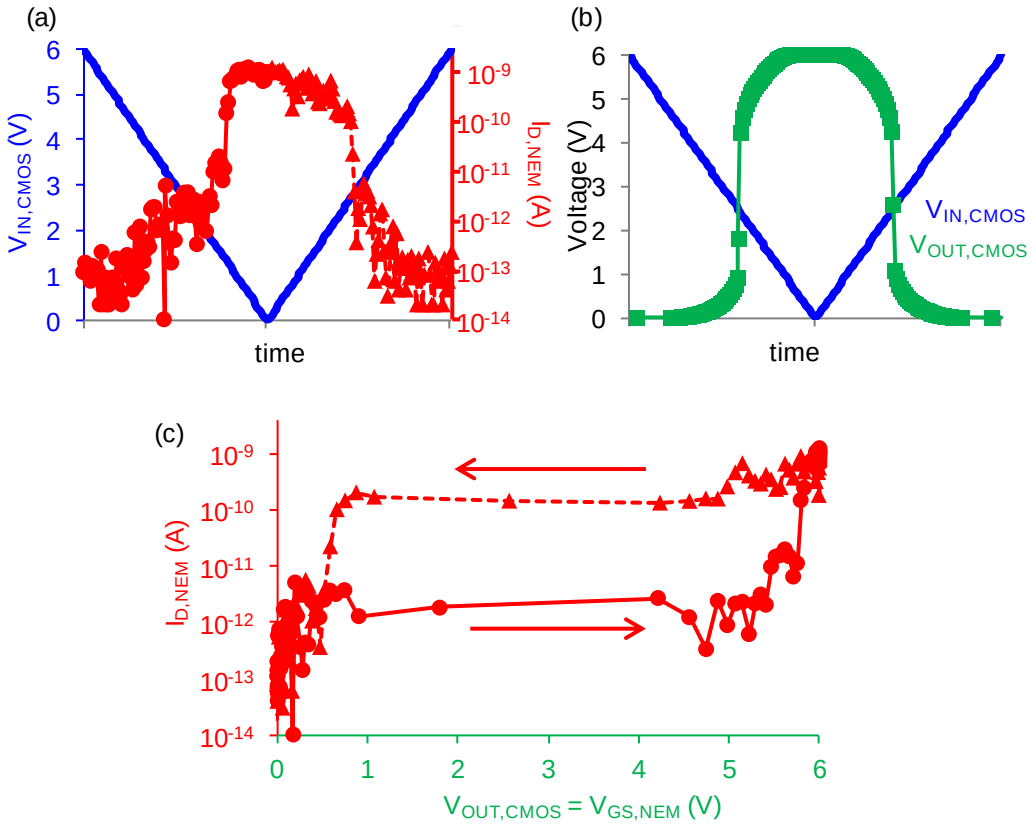

Figure 6-11 Quasi-static measurement results plotting (a) $I_{D,NEM}$ versus $V_{IN,CMOS}$ with $V_{DS,NEM}$ = 0.1 V and (b) the CMOS inverter characteristics at V_{DD} = 6 V. (c) $I_{D,NEM}$ versus $V_{GS,NEM}$ (=$V_{OUT,CMOS}$) deduced from (a) and (b). A CMOS inverter successfully drove a NEM relay, both operating at V_{DD} = 6 V, with the NEM relay having V_{pi} = 5–6 V and V_{po} = 0–1 V.

The measured $I_{D,NEM}$ while sweeping $V_{IN,CMOS}$, shown in Figure 6-11a, demonstrated the CMOS inverter successfully driving a NEM relay at V_{DD} = 6 V. The NEM relay turned on (high $I_{D,NEM}$) as the CMOS inverter input was swept from V_{DD} to 0 and turned off (low $I_{D,NEM}$) as the input was swept from 0 to V_{DD}. From the CMOS inverter characteristics (Figure 6-11b), the NEM relay $I_{D,NEM}$-$V_{GS,NEM}$ characteristics can be deduced as Figure 6-11c. The device had V_{pi} = 5–6 V, and V_{po} = 0–1 V.

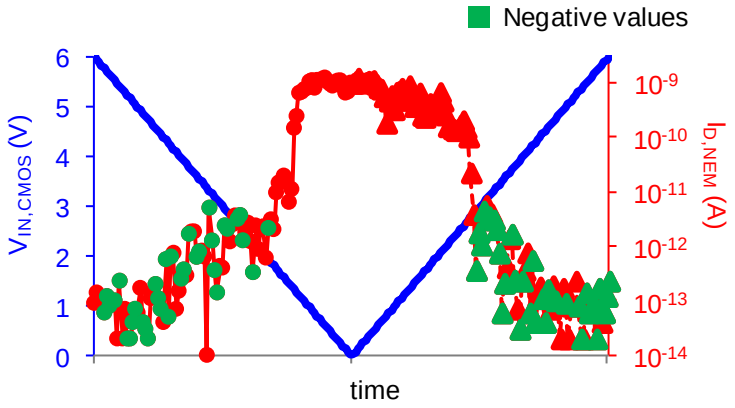

Figure 6-12 Plot of the same data in Figure 6-11a, but showing negative current values in green. This confirms that the increase in the magnitude of the current in the off-state was not leakage, but increased noise.

Plotting the negative values in green, as in Figure 6-12, it was confirmed that the on/off transition was abrupt, and that the increase in the magnitude of the current in the off-state was not due to leakage, but was caused by an increase in the noise level. The source of this noise has not been identified.

6.4. Summary

The first experimental demonstration of the integration of electrostatically actuated NEM relay with CMOS with electrical data is presented, enabled by e-beam patterned scaled NEM relay fabrication process at CMOS compatible temperatures. Electrical results for an NMOSFET driving a NEM relay and a CMOS inverter driving a NEM relay are demonstrated. This is an initial step towards realizing CMOS–NEM relay hybrid circuits that have various benefits, including low leakage power dissipation, that are unattainable with CMOS only circuits. To complete the realization of specific CMOS–NEM hybrid circuits, further work needs to be done to achieve the desired

NEM relay characteristics. Also, encapsulation of the NEM relays [52] needs to be included to complete the integration and have reliably operating switches.

Chapter 7: Conclusion

A simple NEM relay model was developed using simple calculations of NEM relay parameters and implemented using Verilog-A. Using this Verilog-A model, a newly proposed CMOS–NEM SRAM cell was simulated to confirm the benefits compared to a conventional 6T CMOS SRAM cell. Promising results were found, showing benefits in stability and power without the mechanical delay of the NEM relay limiting the performance. This work is meaningful, not only in that a novel CMOS–NEM SRAM cell design with various benefits was proposed, but also in that the possibility of designing CMOS–NEM hybrid circuits in general was demonstrated, that can capitalize on the unique properties of NEM relays, without sacrificing speed.

Having demonstrated promising properties of CMOS-NEM hybrid circuits, the next step was to experimentally demonstrate the simulated circuits. A scaled-up version of the NEM relay was first fabricated and tested to check the feasibility of the operation of a laterally and electrostatically actuated three terminal NEM relay. Then, a scaled-down version, suitable for integration with CMOS, was fabricated and tested. Finally, simple CMOS–NEM circuits were fabricated and tested. This work is an initial step towards achieving the benefits promised by CMOS–NEM hybrid circuits.

In order to advance to fabricating useful CMOS–NEM hybrid circuits, such as the CMOS–NEM SRAM cell, there are various hurdles. Of these, getting more reliable and predictable contact resistances that are in at least the kΩ range is one of the most important tasks to be completed. Contact properties need to be studied in greater

depth. Precisely controlled contact surfaces need to be fabricated with various materials to find the optimal material to use and extensively tested to gain a good understanding of the contact under different conditions. With this knowledge, we would be much closer to achieving the proposed CMOS–NEM hybrid circuits.

APPENDIX A: Calculation of NEM Relay Contact Resistance

The methodology used to calculate and the NEM relay contact resistance was as follows:

1. Use the 2D model described in Section 2.2.1 to find the position of the beam immediately before pull-in.
2. Estimate the beam deflection after pull-in by finding a ratio γ between g_d and the beam tip deflection just before pull-in and multiplying γ to the beam deflection found in Step 1.
3. Use the estimated beam deflection found in Step 2 to calculate the electrostatic force along the length of the beam and find the beam deflection according to this electrostatic force. The deflection of the tip of the beam will be greater than the initial gap between the beam and the drain (g_d), since beam deflection is not limited by the presence of the electrodes in the model.
4. Calculate the contact force with [19]

$$F_{contact} = \frac{3EI(v_{tip} - g_d)}{{L_g}^3} \quad \text{Eq. A–1}$$

where E is the Young's modulus of the beam, I is the moment of inertia (defined in Eq. 2-6), v_{tip} is the deflection at the beam tip found in Step 3, and L_g is the length of the gate electrode.

5. Assuming an elastic deformation, calculate the effective contact area radius with [18]

$$r_{eff} = \sqrt[3]{\frac{3F_{contact}R_t}{4E'}}$$ Eq. A–2

where R_t is the end radius of curvature of asperities, and E' is the effective modulus of elasticity defined as

$$\frac{1}{E'} = \frac{2 \cdot (1 - \nu^2)}{E}$$ Eq. A–3

where ν is the Poisson's ratio.

6. Calculate the $F_{contact}$ threshold with [18]

$$F_{threshold} = 0.6\pi H {r_{eff}}^2$$ Eq. A–4

where H is the hardness of the contacting material.

7. If $F_{contact} > F_{threshold}$, the contact is predicted to result in a plastic deformation, in which case r_{eff} is recalculated as [18]

$$r_{eff} = \sqrt{\frac{F_{contact}}{0.6\pi H}}$$ Eq. A–5

8. Calculate the contact resistance with [18]

$$R_{contact} = \frac{4\rho l_e}{3\pi {r_{eff}}^2}$$ Eq. A–6

where ρ is the resistivity, and l_e is the electron mean free path length.

APPENDIX B: Verilog-A Code for NEM Relay

```
module NEM(drain,gate,source);
            //Input variable Definition
            parameter real Vpi  = 0.8; // pull-in voltage
            parameter real Vpo = 0.2; // pull-out voltage
            parameter real rch = 1e+3 from [0:inf); // resistance
            parameter real tdmec = 1e-9; // mechanical delay
            parameter real tr=1e-18; // small nonzero value
            parameter real tf=1e-18; // small nonzero value
            parameter real Cgson=2e-17; // on-capacitance
            parameter real Cgsoff=1.5e-17; // off-capacitance

            real Vgs;
            real Cgs;
            real on_flg; // "1" when device is on
            real td; // switching delay

            inout drain, gate, source;
            electrical drain, gate, source;

            analog begin
                        //Initialization
```

```
@(initial_step("tran","dc")) begin
            on_flg = 1;
            td = tdmec;
end

Vgs = abs(V(gate,source));
if ((Vgs >= Vpi) && (on_flg == 0))  begin
            on_flg = 1;
            Cgs=Cgson;
            td = tdmec;
end

else if ((Vgs > Vpo) && (on_flg == 1))  begin
            on_flg = 1;
            Cgs=Cgson;
            td = tdmec;
end

else if ((Vgs <= Vpo) && (on_flg == 1))  begin
            on_flg = 0;
            Cgs=Cgsoff;
            td = 0;
end

else if ((Vgs < Vpi) && (on_flg == 0))  begin
            on_flg = 0;
```

```
                                    Cgs=Cgsoff;

                                    td = 0;

                            end


            I(drain,source) <+
                     transition(on_flg,td,tr,tf)*V(drain,source)/rch;

            I(gate,source) <+ (transition(on_flg,0,td,tf)*

                        (Cgson-Cgsoff)+Cgsoff)*ddt(V(gate,source));

            end // end of analog begin

endmodule
```

Bibliography

[1] F. Schwierz, "Graphene Transistors," *Nature Nanotechnology*, vol. 5, no. 7, pp. 487-496, July 2010.

[2] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114-117, Apr. 1965.

[3] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256-268, Oct. 1974.

[4] R. Chau, S. Datta, M. Doczy, J. Kavalieros, and M. Metz, "Gate dielectric scaling for high-performance CMOS: from SiO2 to high-K," in *International Workshop on Gate Insulator*, Tokyo, Japan, 2003, pp. 124-126.

[5] W. Haensch et al., "Silicon CMOS devices beyond scaling," *IBM Journal of Research & Development*, vol. 50, no. 4/5, pp. 339-361, Jul./Sep. 2006.

[6] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology*. Hoboken, N.J.: John Wiley and Sons, 2003.

[7] A. Raychowdhury, J. I. Kim, D. Peroulis, and K. Roy, "Integrated MEMS Switches for Leakage Control of Battery Operated Systems," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2006, pp. 457-460.

[8] H. Kam et al., "Design and Reliability of a Micro-Relay Technology for

Zero-Standby-Power Digital Logic Applications," in *IEEE International Electron Devices Meeting*, Baltimore, MD, 2009, pp. 809-812.

[9] D. A. Czaplewski et al., "A Nanoelectromechanical Switch for Integration with CMOS Logic," *Journal of Micromechanics and Microengineering*, vol. 19, no. 8, p. 085003, Aug. 2009.

[10] K. Akarvardar et al., "Design Considerations for Complementary Nanoelectromechanical Logic Gates," in *IEEE International Electron Devices Meeting*, Washington DC, 2007, pp. 299-302.

[11] F. Chen et al., "Integrated Circuit Design with NEM Relays," in *IEEE/ACM International Conference on Computer-Aided Design* , San Jose, CA, 2008, pp. 750-757.

[12] F. Chen et al., "Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2010, pp. 150-151.

[13] H.F. Dadgour and K. Banerjee, "Design and Analysis of Hybrid NEMS-CMOS Circuits for Ultra Low-Power Applications," in *ACM/IEEE Design Automation Conference*, San Deigo, CA, 2007, pp. 306-311.

[14] C. Chen et al., "Efficient FPGAs Using Nanoelectromchanical Relays," in *ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, 2010, pp. 273-282.

[15] M. Zahn, *Electromagnetic Field Theory: A Problem Solving Approach*. New

York: John Wiley & Sons, 1979.

[16] J. M. Gere, *Mechanics of Materials*. Belmont, CA: Brooks/Cole-Thomas Learning, 2004.

[17] R. Maboudian and R. T. Howe, "Critical Review: Adhesion in Surface Micromechanical Structures," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 15, no. 1, pp. 1-20, Jan. 1997.

[18] S. Majumder et al., "Measurement and Modeling of Surface Micromachined, Electrostatically Actuated Microswitches," in *International Conference on Solid State Sensors and Actuators*, Chicago, IL, 1997, pp. 1145-1148.

[19] R. A. Coutu Jr. and P. E. Kladitis, "Contact Force Models, including Electric Contact Deformation, for Electrostatically Actuated, Cantilever-Style, RF MEMS Switches," in *NSTI-Nanotech*, 2004, pp. 219-222.

[20] C.-T. Chuang, S. Mukhopadhyay, J.-J. Kim, K. Kim, and R.l Rao, "High-Performance SRAM in Nanoscale CMOS: Design Challenges and Techniques," in *IEEE International Workshop on Memory Technology, Design and Testing*, Taipei, 2007, pp. 4-12.

[21] R.E. Aly, M. I. Faisal, and M. A. Bayoumi, "Novel 7T SRAM Cell for Low Power Cache Design," in *IEEE SOC Conference*, Herndon, VA, 2005, pp. 171-174.

[22] K. Takeda et al., "A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications," *IEEE Journal of Solid-State Circuits*, vol.

41, no. 1, pp. 113-121, Jan. 2006.

[23] L. Chang et al., "Stable SRAM cell design for the 32 nm node and beyond," in *Symposium on VLSI Technology*, Kyoto, 2005, pp. 128-129.

[24] L. Chang et al., "A 5.3 GHz 8T-SRAM with Operation Down to 0.41 V in 65 nm CMOS," in *Symposium on VLSI Circuits*, Kyoto, 2007, pp. 252-253.

[25] B. H. Calhoun and A. Chandrakasan, "A 256 kb Sub-threshold SRAM in 65 nm CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2006, pp. 259-2601.

[26] K. Kim, J.-J. Kim, and C.-T. Chuang, "Asymmetrical SRAM Cells with Enhanced Read and Write Margins," in *International Symposium on VLSI Technology, Systems and Applications*, Hsinchu, 2007, pp. 1-2.

[27] J.P. Kulkarni, K. Kim, and K. Roy, "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303-2313, Oct. 2007.

[28] J.P. Kulkarni, K. Kim, S.P. Park, and K. Roy, "Process variation tolerant SRAM array for ultra low voltage applications," in *ACM/IEEE Design Automation Conference*, Anaheim, CA, 2008, pp. 108-113.

[29] [Online]. http://www.eas.asu.edu/~ptm

[30] H. Nii et al., "A 45nm High Performance Bulk Logic Platform Technology (CMOS6) using Ultra High NA (1.07) Immersion Lithography with Hybrid Dual-Damascene Structure and Porous Low-k BEOL," in *IEEE International*

Electron Devices Meeting, San Francisco, CA, 2006, pp. 1-4.

[31] *Virtuoso® Spectre® Circuit Simulator User Guide*. San Jose, CA: Cadence Design Systems, 2004.

[32] E. Seevinck, F. J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, Oct. 1987.

[33] S. Mukhopadhyay and K. Roy, "Modeling and Estimation of Total Leakage Current in Nano-scaled CMOS Devices Considering the Effect of Parameter Variation," in *International Symposium on Low Power Electronics and Design*, Seoul, 2003, pp. 172-175.

[34] Y. C. Yeo et al., "Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 540-542, Nov. 2000.

[35] [Online]. http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html

[36] H. Dadgour, A.M. Cassell, and K. Banerjee, "Scaling and Variability Analysis of CNT-Based NEMS Devices and Circuits with Implications for Process Design," in *IEEE International Electron Devices Meeting*, San Francisco, CA, 2008, pp. 1-4.

[37] W. H. Teh, J. K. Luo, M. R. Graham, A. Pavlov, and C. G. Smith, "Near-Zero Curvature Fabrication of Miniaturized Micromechanical Ni Switches Using

Electron Beam Cross-Linked PMMA ," *Journal of Micromechanics and Microengineering*, vol. 13, no. 5, pp. 591-598, May 2003.

[38] W. W. Jang, J. O. Lee, and J.-B. Yoon, "A DRAM-Like Mechanical Non-Volatile Memory," in *Transducers & Eurosensors*, Lyon, France, 2007, pp. 2187-2190.

[39] W. W. Jang et al., "Fabrication and Characterization of a Nanoelectromechanical Switch with 15-nm-Thick Suspension Air Gap," *Applied Physics Letters*, vol. 92, no. 10, pp. 103110-1-3, Mar. 2008.

[40] W. W. Jang, J. O. Lee, H.-H. Yang, and J.-B. Yoon, "Mechanically Operated Random Access Memory (MORAM) Based on an Electrostatic Microswitch for Nonvolatile Memory Applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2785-2789, Oct. 2008.

[41] W. W. Jang et al., "NEMS Switch with 30 nm-Thick Beam and 20 nm-Thick Air Gap for High Density Non-Volatile Memory Applications," *Solid-State Electronics*, vol. 52, no. 10, pp. 1578-1583, Oct. 2008.

[42] R. Nathanael, V. Pott, H. Kam, J. Jeon, and T.-J. K. Liu, "4-Terminal Relay Technology for Complementary Logic," in *IEEE International Electron Devices Meeting*, Baltimore, MD, 2009, pp. 223-226.

[43] J.-O. Lee et al., "3-Terminal Nanelectromechanical Switching Device in Insulating Liquid Media for Low Voltage Operation and Reliability Improvement," in *IEEE International Electron Devices Meeting*, Baltimore,

MD, 2009, pp. 227-230.

[44] B. D. Davidson, S. M. George, and V. M. Bright, "Atomic Layer Deposition (ALD) Tungsten Nano-Electromechanical Transistors," in *IEEE International Conference on Micro Electro Mechanical Systems*, Wanchai, Hong Kong, 2010, pp. 424-427.

[45] J. Jeon et al., "Perfectly Complementary Relay Design for Digital Logic Applications," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 371-373, April 2010.

[46] K. Akarvardar, D. Elata, R. T. Howe, and H.-S. P. Wong, "Energy-Reversible Complementary NEM Logic Gates," in *Device Research Conference*, Santa Barbara, CA, 2008, pp. 69-70.

[47] B. Bhushan and X. Li, "Micromechanical and tribological characterization of doped single-crystal silicon and polysilicon films for microelectromechanical systems devices," *Journal of Materials Research*, vol. 12, no. 1, pp. 54-63, Jan. 1997.

[48] H. Lee, R. A. Coutu, S. Mall, and K. D. Leedy, "Characterization of Metal and Metal Alloy Films as Contact Materials in MEMS Switches," *Journal of Micromechanical Microengineering*, vol. 16, no. 3, pp. 557-563, Feb. 2006.

[49] D. Seneviratne, G. N. Nielson, S. Takahashi, G. Barbastathis, and H. L. Tuller, "On the Use of Titanium Nitride as Structural Material for Nano-Electro-Mechanical Systems (NEMS)," in *IEEE Conference on Nanotechnology*,

Nagoya, Japan, 2005, pp. 138-141.

[50] H. W. Hermance and T. F. Egan, "Organic Deposits on Precious Metal Contacts," *The Bell System Technical Journal*, vol. 37, pp. 739-776, May 1958.

[51] D. A. Czaplewski et al., "Lifetime limitations of ohmic, contacting RF MEMS switches with Au, Pt and Ir contact materials due to accumulation of 'friction polymer' on the contacts," *Journal of Micromechanics and Microengineering*, vol. 22, no. 10, p. 105005, October 2012.

[52] R. Gaddi et al., "MEMS Technoogy Integrated in the CMOS Back End," *Microelectronics Reliability*, vol. 50, no. 9-11, pp. 1593-1598, Sep.-Nov. 2010.

[53] K. A. Honer and G. T. A. Kovacs, "Integration of Sputtered Silicon Microstructures with Pre-Fabricated CMOS Circuitry," *Sensors and Actuators A: Physical*, vol. 91, no. 3, pp. 386-397, July 2001.

[54] A. E. Franke, J. M. Heck, T.-J. King, and R. T. Howe, "Polycrystalline Silicon-Germanium Films for Integrated Microsystems," *Journal of Microelectormechanical Systems*, vol. 12, no. 2, pp. 160-171, Apr. 2003.

[55] D. Saias et al., "An Above IC MEMS RF Switch," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2318-2324, Dec. 2003.

[56] [Online]. http://www.cavendish-kinetics.com/

[57] E. J. Nowak, "Maintaining the Benefits of CMOS Scaling When Scaling Bogs Down," *IBM Journal of Research and Development*, vol. 46, no. 2/3, pp. 169-180, Mar./May 2002.

[58] R. Parsa et al., "Composite Polysilicon-Platinum Lateral Nanoelectromechanical Relays," in *Hilton Head Workshop: A Solid-State Sensors, Actuators and Microsystems Workshop*, Hilton Head Island, SC, 2010.

[59] J. Jeon et al., "Seesaw Relay Logic and Memory Circuits," *Journal of Microelectromechanical Systems*, vol. 19, no. 4, pp. 1012-1014, Aug. 2010.

[60] International Technology Roadmap for Semiconductors 2011 Edition. [Online]. http://www.itrs.net/Links/2011ITRS/Home2011.htm

[61] W. H. Teh, J. K. Luo, M. R. Graham, A. Pavlov, and C. G. Smith, "Switching characteristics of electrostatically actuated miniaturized micromechanical metallic cantilevers," *Journal of Vacuum Science & Technology B*, vol. 21, no. 6, pp. 2360-2367, Nov./ Dec. 2003.

[62] M. A. Beunder, R. van Kampen, D. Lacey, M. Renault, and C. G. Smith, "A New Embedded NVM Technology for Low-Power, High Temperature, Rad-Hard Applications," in *Non-volatile Memory Technology Symposium*, Dallas, TX, 2005, pp. 65-68.

[63] R. Parsa, "Nanoelectromechanical Relays for Low Power Applications", Ph.D. dissertation, Department of Electrical Engineering, Stanford University, Stanford, CA, 2011.

List of Publications

C. Chen, W. S. Lee, R. Parsa, S. Chong, J Provine, J. Watt, R. T. Howe, H.-S. P. Wong, and S. Mitra, "Nano-Electro-Mechanical Relays for FPGA Routing: Experimental Demonstration and a Design Technique," *Design, Automation & Test in Europe Conference & Exhibition*, Dresden, Germany, 2012, pp.1361-1366.

C. Chen, W. S. Lee, J Provine, S. Chong, R. Parsa, D. Lee, R. T. Howe, H.-S. P. Wong, and S. Mitra, "Nano-Electro-Mechanical (NEM) Relays and Their Application to FPGA Routing," *Asia and South Pacific Design Automation Conference*, Sydney, Australia, 2012, pp. 639.

S. Chong, B. Lee, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical relays with silicon nMOS," *IEEE Transactions on Electron Devices,* vol. 59, pp. 255-258, Jan. 2012.

S. Chong, B. Lee, K. B. Parizi, J Provine, S. Mitra, R. T. Howe, H.-S. P. Wong, "Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit," *IEEE International Electron Devices Meeting*, Washington D.C., 2011, pp. 701-704.

X. Shen, S. Chong, D. Lee, R. Parsa, R. T. Howe, H.-S. P. Wong, "2D analytical model for the study of NEM relay device scaling," *International Conference on Simulation of Semiconductor Processes and Devices*, Osaka, Japan, 2011, p. 243-246.

W. S. Lee, S. Chong, R. Parsa, J. Provine, D. Lee, S. Mitra, H.-S P. Wong, R. T. Howe, "Dual sidewall lateral nanoelectromechanical relays with beam isolation," *16th*

International Solid-State Sensors, Actuators and Microsystems Conference, Beijing, China, 2011, pp. 2606-2609.

R. Parsa, M. Shavezipur, W. S. Lee, S. Chong, D. Lee, H.-S. P. Wong, R. Maboudian, R. T. Howe, "Nanoelectromechanical relays with decoupled electrode and suspension," *IEEE 24th International Conference on Micro Electro Mechanical Systems,* Cancun, Mexico, 2011, pp. 1361-1364.

S. Oh, L. Wei, S. Chong, J. Luo, H.-S. P. Wong, "Device and circuit interactive design and optimization beyond the conventional scaling era," *IEEE International Electron Devices Meeting*, San Francisco, CA, 2010, p. 412.

C. Chen, R. Parsa, N. Patil, S. Chong, K. Akarvardar, J. Provine, D. Lewis, J. Watt, R. T. Howe, H.-S. P. Wong, S. Mitra, "Efficient FPGAs using nanoelectromechanical relays," *Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays,* Monterey, CA, 2010, pp. 273-282.

R. Parsa, S. Chong, N. Patil, K. Akarvardar J Provine, D. Lee, D. Elata, S. Mitra, H.-S. P. Wong, R. T. Howe, "Composite polysilicon-platinum lateral nanoelectromechanical relays," Solid-State Sensors, Actuators, and Microsystems Workshop, Hilton Head, SC, 2010, pp. 7-10.

S. Chong, K. Akarvardar, R. Parsa, J.-B. Yoon, R. T. Howe, S. Mitra, H.-S. P. Wong, "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," *IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, 2009, pp.478-484.

H.-S. P. Wong, L. Wei, S. Oh, A. Lin, J. Deng, S. Chong, K. Akarvardar, "Technology projection using simple compact models," *International Conference on Simulation of Semiconductor Processes and Devices*, San Diego, CA, 2009, pp.1-8.

D. Akinwande, J. Liang, S. Chong, Y. Nishi, H.-S. P. Wong, "Analytical ballistic theory of carbon nanotube transistors: Experimental validation, device physics, parameter extraction, and performance projection," *Journal of Applied Physics,* vol. 104, pp. 124514 - 124514-7, Dec. 2008.