

Topics for the orals 2025

1. Basic MOSFET operation: the charge sheet model, ohmic and saturation regime. Channel modulation and finite output resistance. Modulation voltage and dependence on channel length. Resistive coupling between source and drain terminals.
2. Subthreshold operation. Diffusion regime. Limit to the maximum voltage gain. Moderate inversion. Inversion coefficient. EKV model.
3. MOSFET's figures of merit: maximum voltage gain and cut-off frequency. Dependences on bias (strong, moderate and weak inversion).
4. BJT basics: The planar npn structure. Current gain and transconductance. Early effect, maximum current gain. Gummel plot and beta dependence on current. High injection-low injection effects. Optimal bias. Options for pnp devices (lateral and substrate devices).
5. BJT equivalent circuit. Resistance values at the BJT terminals accounting for the resistive coupling between emitter and collector. Cut-off frequency in BJTs: diffusion capacitance and dependence on current density.
6. Independent/interacting capacitors and poles. Extension of the time constant method. Middlebrook's theorem. Examples with RC networks.
7. Quantitative description of noise: noise variance and noise power spectral density.
8. Noise transfer in circuits. Input referred noise sources of a two-port network. Definitions and derivation.
9. Noise models: Thermal noise of resistors. The Nyquist argument for the thermal noise power spectral density.
10. Noise models: Shot noise model. Application to p-n junctions, BJTs and MOSFETs in weak inversion.
11. Trapping noise: trapping noise in a resistor
12. McWorther model of the 1/f noise in MOSFETs. Tvidis formula.
13. The prototypical differential stage: from resistive to active loads. Common mode feedback and single ended option.
14. Single ended differential stage with mirror: Bias, input and output voltage swings, differential gain, Common mode gain.
15. Input referred noise sources of a differential stage with MOSFETs and BJTs. Power-noise trade-off.
16. Two-stage CMOS OTA: topology, frequency response using the time constant method, Miller compensation. Pole splitting vs. compensation capacitance value. The RHP zero and the high frequency pole. OTA compensation and FoM.
17. Two-stage CMOS OTA: frequency compensation with the nulling resistor. Implementing the nulling resistor.
18. Two-stage CMOS OTA: frequency compensation with ideal voltage and current buffers. Impact of the buffer finite resistance.
19. Two stage bipolar amplifier: input resistance, input referred voltage and current noise, sizing example and compensation.
20. uA741 - first stage, bias and common mode feedback, output resistance, differential gain. Mirror with emitter follower and bleeding resistor. Wilson's mirror.
21. uA741 second stage. Setting the bias: trade-off between gain and input impedance. Frequency response.
22. Single-stage CMOS OTAs: telescopic cascode topology, differential gain, input and output voltage swing, power dissipation, frequency response.
23. Folded cascode topology, enhanced mirrors, voltage dynamics, power dissipation. Folded cascode with bipolar transistors. Feed-forward compensation.
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25. OTA Linear response. In-band zero-pole doublets and features of the settling response.
26. The slew rate limit. Impact on settling time. CMOS-OTA: Internal and external slew rate limits. Improving SR with class AB output stages.
27. Output stages: Emitter follower as output stage. Emitter follower efficiency. Push-pull. Efficiency. Cross-over distortion. Class A-B stage. Total harmonic distortion. Distortion reduction by feedback.
28. Output stages in bipolar technology (uA741). Short-circuit protections.

29. Variability and matching: Relative matching of threshold voltage values. Common centroid. Pelgrom's formula
30. Variability and matching: Relative matching of resistors. Common centroid. Pelgrom's formula
31. OTA: Offset. Deterministic and statistical contributions to input referred offset. Input referred offset in bipolar differential stages. Temperature effects.
32. OTA: Common-mode rejection ratio. Deterministic and statistical limits to CMRR

I DO NOT GUARANTEE THE ACCURACY OF THE ANSWERS, NOR MY ENGLISH

1. Basic MOSFET operation: the charge sheet model, ohmic and saturation regime. Channel modulation and finite output resistance. Modulation voltage and dependence on channel length. Resistive coupling between source and drain terminals. (L01_24)

Given the structure of a mosfet, we can write the Ohm Law and in particular, the voltage across a section of the channel. $dV_c = I_{DS} dR$. We know that the resistance from the second Ohm Law is given by: $dR = \rho \frac{dx}{Wd}$ where the resistivity is given by: $\rho = \frac{1}{q\mu n(x)}$

The mobility indicates how easily carriers move under an electric field and n indicates the number of carriers per unit volume. We can rewrite the voltage drop across a section as: $dV_c = I_{DS} \frac{dx}{q n(x) W d} = I_{DS} \frac{dx}{q C_{ox} \mu W}$ with $Q_n(x)$ the free charge per unit area in the channel.

Now we adopt the approximation of the charge sheet model: we assume that the charge carriers in the channel are concentrated in very thin layer, "sheet", near the oxide. Given this model, the charge can be expressed by: $\begin{cases} Q_n(x) = C_{ox} (V_{GS} - V_T) \\ Q'_n(x) = C_{ox} (V_{GS} - V_{DS} - V_T) \end{cases} \Rightarrow Q'_n(x) = C_{ox} (V_{GS} - V_T(x) - V_T)$

Now, doing some math...

$$dV_c = I_{DS} \frac{dx}{C_{ox} (V_{GS} - V_T(x) - V_T) \mu W} \Rightarrow \int_0^{V_{DS}} \mu C_{ox} W (V_{GS} - V_T(x) - V_T) dx = \int_0^{V_{DS}} I_{DS} dx \Rightarrow I_{DS} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}$$

Finding the classic relationship of a MOSFET in the ohmic region. Studying this function, we can see that the current has a parabolic dependence on V_{DS} and reaches a maximum when: $\frac{\partial I_{DS}}{\partial V_{DS}} = 0 \Rightarrow \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T) - V_{DS}] = 0 \Rightarrow V_{DS} = V_{GS} - V_T \Rightarrow I_{DS} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T)(V_{GS} - V_T) - \frac{(V_{GS} - V_T)^2}{2}] \Rightarrow I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$

Finding the classic expression of the saturation regime.

After the vertex of the parabola, the ohmic expression is no longer valid, in fact it makes no sense that increasing V_{DS} makes the electron density decrease. To understand better what happens, we should remember that a current continuity should always remain: all the carriers leaving the source per unit time has to be equal to the electrons reaching the drain. Given that, as the carriers density decrease along the channel, there's a need of increasing the electric field (so the velocity of the carriers) to keep the carriers per unit time constant.

When we reach the saturation of the electric field, we reach the so-called "pinch-off", where the charge at the drain is "zero" (not true, given by charge sheet approx).

However, increasing V_{DS} even more, we notice that the current increases a bit. This can be explained by taking into account that the pinch-off moves back to the source by a small amount. Calling L' the new channel length, and knowing that it depends on the voltage across V_{DS} , we can describe L' with a first order approximation: $L'(V_{DS}) = L'(V_{GS}) \Big|_{V_{DS}=V_{DS,SAT}} + \frac{\partial L'(V_{GS})}{\partial V_{DS}} \Big|_{V_{DS}=V_{DS,SAT}} (V_{DS} - V_{DS,SAT}) = L - \left| \frac{\partial L'(V_{GS})}{\partial V_{DS}} \right| (V_{DS} - V_{DS,SAT}) \Rightarrow L'(V_{DS}) = L \left(1 - \frac{1}{L} \left| \frac{\partial L'(V_{GS})}{\partial V_{DS}} \right| (V_{DS} - V_{DS,SAT}) \right)$

$$\Rightarrow I_{DS} = \frac{1}{2} \mu C_{ox} \frac{W}{L \left[1 - \lambda (V_{DS} - V_{DS,SAT}) \right]} (V_{GS} - V_T)^2 \Rightarrow \left[\frac{1}{1-x} \approx 1+x \right] \Rightarrow I_{DS} = I_{DS,SAT} [1 + \lambda (V_{DS} - V_{DS,SAT})]$$

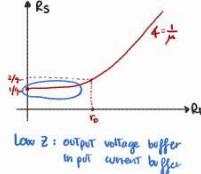
$$\Rightarrow \frac{1}{r_o} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right) = I_{DS} \lambda = \frac{I_{DS,SAT}}{V_A} \Rightarrow r_o = \frac{V_A}{I_{DS,SAT}} \quad V_A: \text{channel modulation voltage}$$

So, we can model a MOSFET in saturation as an ideal current generator with a finite output resistance, leading to a maximum gain of :

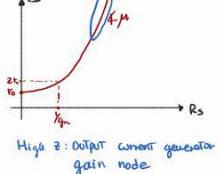
$$G_{max} = g_m r_o = \frac{2Z}{V_{ov}} \cdot \frac{V_A}{Z} \approx 2 \frac{V_A}{V_{ov}}$$

Resistive coupling: source resistance

$$\begin{aligned} & \left\{ \begin{aligned} i_m &= V_{GS} g_m \\ i_T &= \frac{V_{GS}}{r_o} = \frac{V_{GS} R_o}{r_o} \\ i_T &= i_m \end{aligned} \right. \Rightarrow i_m = \frac{V_{GS}}{r_o} - \frac{i_m R_o}{r_o} + V_T g_m \\ & R_S = \frac{V_{GS}}{i_m} = \frac{1 + \frac{R_o}{r_o}}{1 + g_m r_o} = \frac{r_o + R_o}{r_o + g_m r_o} \end{aligned}$$



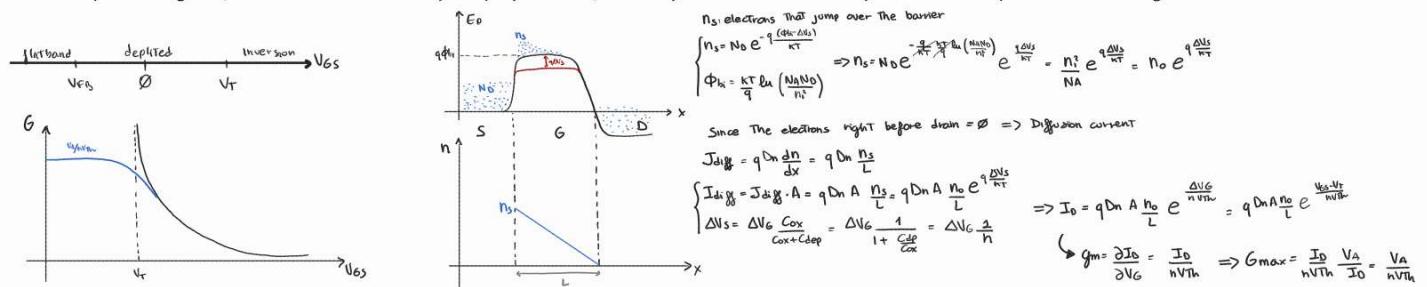
$$\begin{aligned} & \left\{ \begin{aligned} i_m &= -(i_S R_S) g_m \\ i_o &= \frac{V_S - i_S R_S}{r_o} \\ i_S &= i_o + i_m \end{aligned} \right. \Rightarrow i_m = \frac{V_S}{r_o} - \frac{i_S R_S}{r_o} - i_S R_S g_m \\ & i_S \left(\frac{1}{r_o} + g_m r_o \right) = \frac{V_S}{r_o} \\ & \frac{V_S}{r_o} = \left(\frac{1}{r_o} + g_m r_o \right) r_o \\ & R_o = r_o + R_S \left(\frac{1}{r_o} + g_m r_o \right) \\ & R_o = r_o + R_S \left(1 + g_m r_o \right) \end{aligned}$$



We have found before that the maximum gain for a mosfet is given by: $G_{max} = gm \frac{V_0}{2} = \frac{2I}{V_{DD}} \cdot \frac{V_A}{2I} = \frac{V_A}{V_{DD}}$, suggesting that decreasing the overdrive can lead to a very large gain! Let's study what happens when $V_{GS} \rightarrow V_t$.

We always said that $V_{GS} > V_t$ was needed to be on, but actually it is just the inversion condition at the source to create a channel. Actually, even if $V_g = 0$, there's a Φ_m given by the metal junction (because of Fermi). Part of this voltage will drop on the "fake" channel, making the majority carriers to move down and create a depleted region where the current may flows. $\Delta V_s = \Delta V_G \frac{C_{ox}}{C_{ox} + C_{dep}}$

In the depleted regime, the mosfet is made by an npn junction, like a bjt! We can now study the carriers profile according to Boltzman:



In the moderate inversion regime, the current is both given by a drift and a diffusion, so we can adopt a model, called EKV model (Enz-Krumanacher-Vittoz model) to describe the behaviour of a mosfet both by a drift contribution and a diffusion one. We introduce an inversion coefficient IC that measures the level of inversion:

$$\begin{cases} I_D = I_S e^{\frac{V_{GS}-V_t}{nV_{th}}} \\ I_S = 4n K' \frac{W}{L} (V_m)^2 \\ IC = \frac{I_D}{I_S} \end{cases} \xrightarrow[IC > 10]{\text{Strong}} \xrightarrow[0 < IC < 10]{\text{Moderate}} \xrightarrow{IC < 10} \text{Weak}$$

$$gm = \frac{I_D}{nV_{th}} \left(\frac{2}{1 + \sqrt{4IC + 1}} \right)$$

	BJT	V_S	MOSFET
G	V_A/V_{th}	V_A/nV_{th}	V_A/V_{th}
gm	I/V_{th}	I/nV_{th}	I/nV_{th}
V_A	$\sim 100 \text{ mV}$	$\propto L$	V_A/I
R_o	V_A/I		V_A/I

BJT > MOS
BJT > MOS
BJT ~ MOS (if $L(\text{mos}) \gg 1$)

3. MOSFET's figures of merit: maximum voltage gain and cut-off frequency. Dependences on bias (strong, moderate and weak inversion). (L01_24)

There are three key points that define the efficiency of a transistor: gain, bandwidth and noise. Let's dive deep into the trade off between the gain and the bandwidth. As we saw before, the gain goes like $1/V_{th}$ and reach a max gain of $V_a/n V_{th}$ (check answer 2). Now we want to see if and how the bandwidth has a dependence on bias in weak, moderate and strong inversion regime.

In a mosfet we can define two intrinsic capacitances: C_{gs} , between gate and source, due to the charge accumulated in the channel, and a C_{gd} , between gate and drain, mainly because there's a overlap between gain and drain.

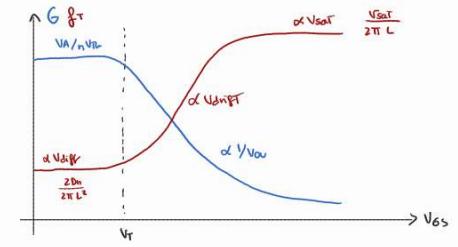
The cut-off frequency is the frequency for a unit current gain, so we can derive:

$$\begin{aligned}
 & \text{Circuit diagram: } \text{V}_{DD} \text{ is connected to the drain, } \text{V}_{GS} \text{ is connected to the gate, } \text{V}_{DS} \text{ is connected to the drain and source, } \text{I}_{DS} \text{ is the drain current.} \\
 & \text{Equations: } I_{DS} = i_{in} R \cdot g_{m} \Rightarrow \frac{I_{DS}}{i_{in}} = \frac{g_{m} R}{2\pi(C_{gs} + C_{gd})R} = \frac{g_{m}}{2\pi(C_{gs} + C_{gd})} \\
 & \left[\begin{array}{l} C_{gs} = \frac{2}{3} C_{ox} WL \\ C_{gd} \propto C_{gs} \\ \Rightarrow C_{gs} + C_{gd} \approx C_{ox} WL \end{array} \right] \Rightarrow f_T = \frac{\mu C_{ox} \frac{W}{L} V_{DD}}{2\pi C_{ox} WL} = \frac{1}{2\pi} \mu \frac{V_{DD}}{L} \frac{1}{L} = \frac{1}{2\pi} \mu F \frac{1}{L} = \frac{1}{2\pi} \frac{V}{L} = \frac{1}{2\pi} \frac{V}{C}
 \end{aligned}$$

Now that we have derived the value of the cut-off frequency, we have to evaluate it under different bias.

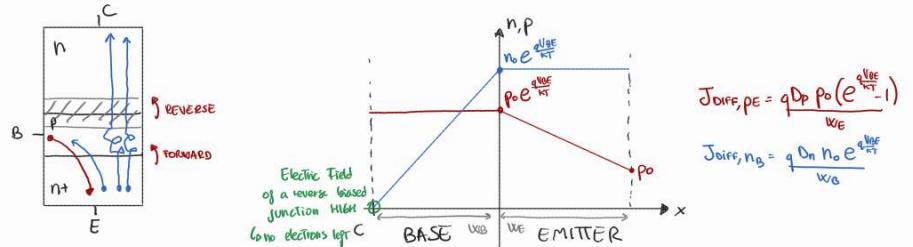
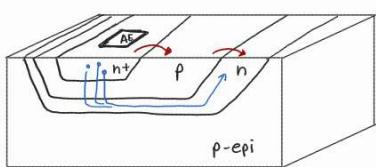
In strong inversion, $\tau = t_{\text{drift}}$, increasing when V_{DD} increase, until the velocity reach the saturation value. In weak inversion $\tau = t_{\text{diff}}$.

$$\begin{aligned}
 & \text{Graph: } n(x) \text{ vs } x \quad n(x) = n_s - \frac{n_s}{L} x \quad Q = \frac{n_s L}{2} \\
 & J_{DS} = q D_n \frac{n(x)}{L} \Rightarrow \tau_{\text{diff}} = \frac{Q}{J_{DS}} = \frac{Q' A}{J_{DS} A} = \frac{q n(x) L / 2}{q D_n \frac{n(x)}{L}} = \frac{L^2}{2 D_n} \parallel \text{const}
 \end{aligned}$$



4. BJT basics: The planar npn structure. Current gain and transconductance. Early effect, maximum current gain. Gummel plot and beta dependence on current. High injection-low injection effects. Optimal bias. Options for pnp devices (lateral and substrate devices). (L01B_24)

Let's start with the physics of the npn bjt transistor. Our goal is to inject from the base and collect electrons from the collector. To do so, we need this polarization:



$$\begin{cases} I_E = I_E + I_C \\ I_E = I_B = qD_p A_E \frac{p_0}{V_{BE}} e^{\frac{qV_{BE}}{kT}} \\ I_C = I_C = qD_n A_E \frac{n_0}{V_{BE}} e^{\frac{qV_{BE}}{kT}} \end{cases}$$

NB Designer can change A_E

$$Goal: I_B \ll I_C$$

$$J_C = \beta J_B$$

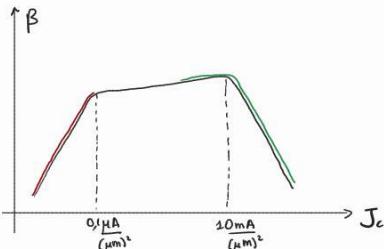
$$I_E = (\beta + 1) I_B$$

$$\beta = \frac{I_C}{I_B} = \frac{D_n}{D_p} \cdot \frac{N_p}{N_A} \cdot \frac{N_e}{N_h} \cdot \frac{V_{BE}}{V_{WB}} \Rightarrow N_e \gg N_h \quad V_{WB} \text{ short}$$

$$\frac{\partial I}{\partial V_{BE}} = g_m = \frac{I}{V_{TH}} \quad G_{MOS} = g_m R_o = \frac{I}{V_{TH}} \cdot \frac{V_A}{V_{TH}} = \frac{V_A}{V_{TH}}$$

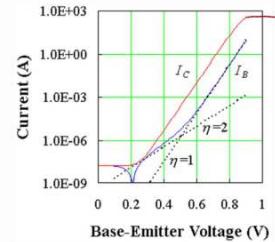
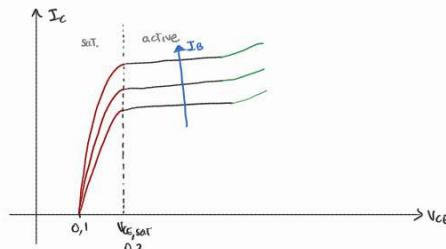
- emitter n+ heavily doped
- n+ an p short for less recombination
- collector less doped to avoid avalanche effect
(more doped \rightarrow smaller ZCS \rightarrow higher F)

Now that we derived the current, let's plot its dependence with V_{CE} :



$$I_c = I_s e^{\frac{qV_{CE}}{kT}}$$

$$I_c \approx \beta I_B$$



Let's first comment the beta plot. We can distinguish three zones: the red one, for low values of I_c , the recombination of carriers in the base zone is relevant, a flat zone where the device works properly and a green zone where the kirk effect (base modulation effect) takes place: when the ZCS starts increasing (we are increasing the reverse bias voltage), at first the main relevant effect is the decreasing of W_b , leading to less recombination, increasing the current. After a certain value, the beta drops down (max electric field?) not required

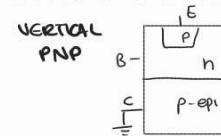
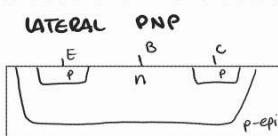
We can see the same effect in the Current x V_{CE} plot. An important details is that the I_c plot may not start from (0,0)! This is due to the fact that: $I_c = 0 \Rightarrow \text{holes in } E = \text{holes in } C \Rightarrow qA_C e^{\frac{qV_{CE}}{kT}} = qA_E e^{\frac{qV_{CE}}{kT}}$. Since $A_E \ll A_C \Rightarrow V_{BE} > V_{CE} \Rightarrow V_{CE} = V_{EE} - V_{BE} > 0 \ (\approx 0.1)$

Then we enter the saturation region in red, where the np junction isn't reverse biased yet and holes both flow in E and C. As soon as it is reverse biased, we enter the active region very similar to the saturation region of a MOSFET, and then when the kirk effect kicks in, we have an increasing current and then drops down.

The third graph, is the well-known Gummel Plot, where I_c and I_b are plot in logarithm (so the beta is the difference) and the x axis is V_{BE} . Between 0.5 and 0.8 we have that their values are in the correct regime and everything is fine. As V_{BE} becomes less, the recombination of carriers in the base becomes more relevant (because the ZCS of the base-emitter junction becomes a relevant site of recombination). For high V_{BE} , I_c reach a sort of saturation because we arrive of a certain saturation of the reversed biased junction (?) not required

Since we've studied that we cannot rely on beta, it is better not to bias the BJT with the base current! Let's see how to correctly bias it:

$$\begin{aligned} &G_x: I \text{ want } 100 \mu\text{A} \text{ of current} \\ &I \text{ place } R_B = 20 \text{ k}\Omega \\ &\Rightarrow V_B = R_B \cdot I_B = 2 \text{ V} \\ &V_B = V_S - 0.7 = 1.3 \text{ V} \\ &\text{Decide } R_1 \text{ and } R_2 \text{ to have } 1,3 \text{ V} \\ &\text{ex: } V_{DD} = 3 \text{ V}, R_1 = 17 \text{ k}\Omega, R_2 = 13 \text{ k}\Omega \end{aligned}$$



Let's now discuss about pnp BJT. Since the price of a device depends on the number of steps, industries usually adapt the same steps of a npn fabrication to do pnp. This means that also the doping is the same!

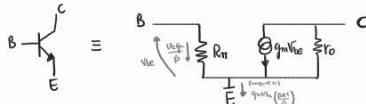
Let's first focus on lateral pnp. We start from a p-epi and then we build a device similar to a MOSFET. Since we have the same dopants, we do not have $N_c \ll N_b$ as we should, so the ZCS will extend into the collector and not the base \rightarrow large $W_b \rightarrow$ lot of recombination!!

A vertical pnp is an upgrade version, but not always possible. In this case we use the substrate to have $N_c \ll N_b$ and have less recombination.

NB: since we are using the substrate, we do not have an isolation layer, so we should keep the collector connected to the ground!!! Even if we have the correct doping, since the working principle is linked to the holes and not electrons, the beta will be lower than npn device (the mobility of holes is always less than the mobility of electrons)

5. BJT equivalent circuit. Resistance values at the BJT terminals accounting for the resistive coupling between emitter and collector. Cut-off frequency in BJTs: diffusion capacitance and dependence on current density. (L01B_24)

The BJT equivalent circuit is:



Let's now find the resistive coupling:

$$\begin{aligned} \text{BASE-EMITTER: } I_B &= \frac{I_C}{\beta} = \frac{I_C}{\beta} e^{\frac{qV_{BE}}{kT}} \\ \frac{1}{R_B} = \frac{\partial I_B}{\partial V_{BE}} &= \frac{1}{\beta} \frac{\partial I_C}{\partial V_{BE}} = \frac{1}{\beta} \frac{I_C}{V_{BE}} = \frac{g_m}{\beta} \end{aligned}$$

BASE RESISTANCE:

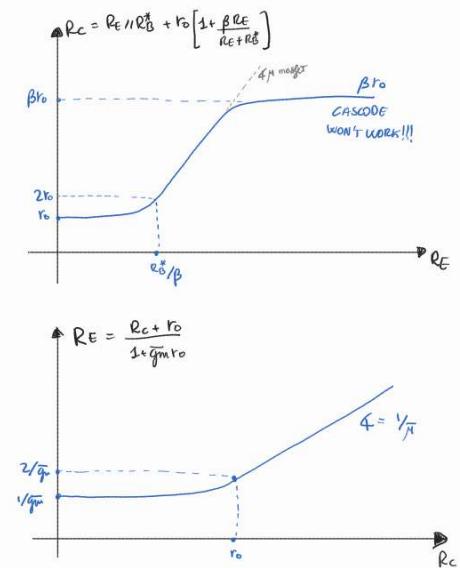
$$V_T = V_{BE} - V_{BE} \ln(\beta) \Rightarrow V_{BE} = \frac{V_T}{1 + g_m \beta}$$

$$R_{BE} = \frac{V_T}{I_C} = R_E + \beta R_E$$

$$\begin{aligned} \text{COLLECTOR RESISTANCE: } & \left\{ \begin{array}{l} i_T = i_C - i_E \\ i_O = \frac{V_T}{R_C + R_E + R_O} \\ i_E = i_O \frac{\beta}{\beta+1} \\ i_C = i_O \frac{R_E}{R_E + R_O} \end{array} \right. \Rightarrow \left\{ \begin{array}{l} i_T = i_O \left(1 - \frac{R_E}{R_E + R_O} \frac{\beta}{\beta+1} \right) \\ i_T = i_O \left(\frac{R_E + R_O - R_E \beta}{(\beta+1)R_E + R_O} \right) \end{array} \right. \\ & i_T = \frac{V_T}{R_O \left((\beta+1)R_E + R_O \right)} \cdot \frac{R_E + R_O}{(\beta+1)R_E + R_O} \end{aligned}$$

$$i_T = \frac{V_T}{R_O \left((\beta+1)R_E + R_O \right)} \cdot \frac{R_E + R_O}{(\beta+1)R_E + R_O}$$

$$R_C = \frac{V_T}{I_C} = \frac{R_E + R_O}{\frac{R_E + R_O}{R_E + R_O} + \frac{R_O}{R_E + R_O}} = R_E / R_O + R_O \left[\frac{1 + \frac{R_E}{R_O}}{R_E + R_O} \right]$$



EMITTER RESISTANCE

$$\begin{aligned} \left\{ \begin{array}{l} i_T = -i_E - i_O \\ i_E = -\frac{V_T}{R_E} \\ i_O = \frac{(V_T - V_T)}{R_O} \end{array} \right. & \Rightarrow i_T = V_T \frac{R_E + R_O}{R_E} + V_T \frac{1}{R_O} - i_T \frac{V_T}{R_O} \\ & i_T \left(1 + \frac{R_E}{R_O} \right) = V_T \left(\frac{R_E + 1}{R_E} + \frac{1}{R_O} \right) \\ R_E = \frac{V_T}{I_C} &= \frac{1 + \frac{R_E}{R_O}}{\frac{R_E + 1}{R_E} + \frac{1}{R_O}} = \frac{R_O + R_C}{R_O \left(\frac{R_E + 1}{R_E} + 1 \right)} = \frac{R_C + R_O}{1 + R_O \frac{R_E}{R_O}} \end{aligned}$$

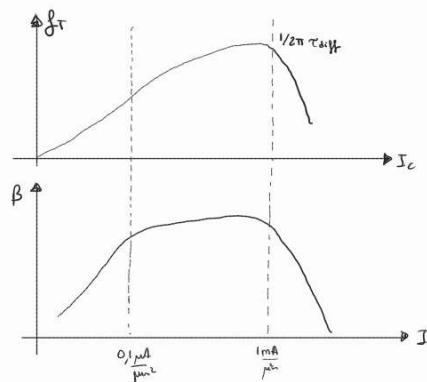
in questo caso i_C è circa zero senza contare la corrente di fondo

Let's now derive the cut-off frequency. As in the mosfet, the cut-off frequency is defined as the frequency of a unitary current gain.

$$\frac{i_{in}(o)}{i_{in}(0)} = \beta$$

$$f_T = \frac{1}{2\pi(C_{in} + C_{in})R_{in}}$$

$$\Rightarrow f_T = \frac{g_m}{2\pi(g_m^2 C_{in} + C_{in})} = \frac{1}{2\pi(\tau_{diff} + \frac{C_{in}}{g_m})} = \frac{1}{2\pi(\tau_{diff} + C_{in} \frac{V_{BE}}{I_C})}$$



$$\begin{aligned} & C_{in}: \text{reverse biased capacitance} \\ & C_{in} = E_S \cdot A \\ & C_{in}: \text{conducting path capacitance} \\ & C_{in} = \frac{\partial Q}{\partial V_{BE}} \\ & Q: \text{charge of a single "plate" or p zone, or n zone} \\ & Q = N(o) \cdot W_B \cdot q \\ & Q = N(o) \cdot W_B \cdot A E \cdot e^{\frac{V_{BE}}{kT}} \\ & \left\{ \begin{array}{l} C_{in} = \frac{\partial Q}{\partial V} = \frac{Q}{V_{in}} \\ I_C = \frac{Q}{\tau_{diff}} \end{array} \right. \Rightarrow \left\{ \begin{array}{l} C_{in} = \frac{I_C}{V_{in}} \tau_{diff} = g_m \tau_{diff} \\ I_C = \frac{Q}{\tau_{diff}} = \frac{Q}{I_C} = \frac{N(o) W_B A E q / 2}{g_m \tau_{diff}} = \frac{W_B^2}{2 g_m \tau_{diff}} \end{array} \right. \end{aligned}$$

In conclusion, we know that to guarantee a low power dissipation, we prefer a low bias, but it means also that the cut-off frequency (the speed of the device) decrease!! (and we should also remember that the noise also depends on I_C, but that is a story for another time)

6. Independent/interacting capacitors and poles. Extension of the time constant method. Middlebrook's theorem. Examples with RC networks.

It is known that a transfer function in Laplace Domain is written as: $T(s) = A_0 \frac{b_m s^m + b_{m-1} s^{m-1} + \dots + b_1 s + 1}{a_n s^n + a_{n-1} s^{n-1} + \dots + a_1 s + 1}$

For an electronic circuit, A_0 is the DC gain, the roots of the numerator (so when $T(s)=0$) are called zeros and the roots of the denominator ($T(s)\rightarrow\infty$) are called poles. Our goal is to find an algorithm to find all the coefficients.

First of all, we should define what's a independent or interactive capacitor. We define two or more capacitors as independent when they can be analyse separately because they are isolated to each other (ex: there's a gate in between or a buffer), while we call two or more capacitors interactive when they influence each other.

The coefficient n is given by the number of independent capacitors of the circuit, while the coefficient m is always less or equal to n .

Let's start with a single capacitor network to set the basics to find the coefficients b and a . Since the network is linear, we can write:

$$\begin{aligned} \text{Circuit: } & V_{out} = A_0 V_{in} + R_m i_C \\ & V_C = R_0 V_{in} + R_0 i_C \Rightarrow [i_C = -s C V_C] \Rightarrow V_{out} = A_0 V_{in} - s C R_m V_C \\ & V_C (1 + s C R_0) = R_0 V_{in} \Rightarrow V_{out} = A_0 V_{in} - \frac{R_m R_0 V_{in}}{1 + s C R_0} = V_{in} A_0 \left(1 - \frac{s C (R_m R_0)}{1 + s C R_0} \right) = V_{in} A_0 \left(\frac{1 + s C (R_m R_0)}{1 + s C R_0} \right) \\ & \text{Zero when } V_{out} = 0 = A_0 V_{in} + R_m i_C \Rightarrow V_{in} = -\frac{R_m i_C}{A_0} \Rightarrow \frac{V_C}{i_C} = R_0 - \frac{R_m R_0}{A_0} = R_{01} \\ & V_{out} = A_0 V_{in} \left(\frac{1 + s C R_{01}}{1 + s C R_0} \right) \end{aligned}$$

R_1 is the resistance seen across C when $V_{in}=0$
↳ $V_C = R_0 V_{in} + R_0 i_C \Rightarrow \frac{V_C}{i_C} = R_0$ (That's why we put it in V_C) like a generator

So, the DC gain, is the gain between v_{in} and v_{out} when C_1 is open, the pole is given by the resistance seen across C_1 terminals when v_{in} is a short and the zero is the resistance seen across C_1 terminals when v_{out} is zero.

In a two capacitors network, if the two capacitors are independent, we can derive some other rules. Let's take this circuit:

$$\begin{aligned} \text{Circuit: } & V_{out} = A_0 \frac{(1 + s C_1 R_0)(1 + s C_2 R_0)}{(1 + s C_1 R_1)(1 + s C_2 R_2)} \quad \text{The poles: } S^2 C_1 C_2 R_1 R_2 + S(C_1 R_1 + C_2 R_2) + 1 \\ & \text{DC: } S(C_1 R_1 + C_2 R_2) + 1 = 0 \Rightarrow Z_{DC} = C_1 R_1 + C_2 R_2 = \sum \frac{1}{R} \\ & \text{Middlebrook: } S(C_1 C_2 R_1 R_2 + C_1 R_1 + C_2 R_2) = 0 \Rightarrow T_{DC} = \frac{C_1 C_2 R_1 R_2}{C_1 R_1 + C_2 R_2} = \left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} \right)^{-1} = \sum \frac{1}{C} \end{aligned}$$

Let's now derive a general rule to find coefficients (also known as Middlebrook theorem): Given a three capacitor network:

$$\begin{aligned} T(s) = A_0 \frac{a_3 s^3 + a_2 s^2 + a_1 s + 1}{b_3 s^3 + b_2 s^2 + b_1 s + 1} \quad & b_2 = C_1 R_2^0 + C_2 R_1^0 + C_3 R_0^0 \\ & b_2 = C_1 C_2 R_0^0 R_1^0 + C_1 C_3 R_0^0 R_2^0 + C_2 C_3 R_0^0 R_1^0 \\ & b_3 = C_1 C_2 C_3 R_0^0 R_1^0 R_2^0 \\ & a_2 = C_1 R_2^0 + C_2 R_1^0 + C_3 R_0^0 \\ & a_3 = C_1 C_2 C_3 R_0^0 R_1^0 R_2^0 \end{aligned}$$

An easy example of a RC network with a single capacitor can be:

$$\begin{aligned} \text{Circuit: } & V_{out} = A_0 \frac{\frac{1 + s C R_{01}}{1 + s C R_0}}{R_0} \\ & \left\{ \begin{array}{l} A_0 = \frac{R_0}{R_0 + R_b} \\ R_{01} = R_0 // R_b \\ R_{01} = R_a \end{array} \right. \end{aligned}$$

(can be added also the calculation of $\frac{1 + s C R_{01}}{1 + s C R_0}$ for interactive capacitors)

Actually, you should do...

$$\begin{aligned} \text{Circuit: } & V_{out} = A_0 \frac{\frac{1 + s C_1 R_{01}}{1 + s C_1 R_0} \cdot \frac{1 + s C_2 R_{02}}{1 + s C_2 R_0}}{R_0} \\ & \Rightarrow T(s) = T_0 \frac{s^2 a_2 + s a_1 + 1}{s^2 b_2 + s b_1 + 1} = T_0 \frac{s^2 (C_1 C_2 d_1) + s (C_1 d_1 + C_2 d_2) + 1}{s^2 (C_1 C_2 \beta_1) + s (C_1 \beta_1 + C_2 \beta_2) + 1} \\ & C_2 = \emptyset \Rightarrow \frac{s C_2 d_2 + 1}{s C_2 \beta_2 + 1} \rightarrow d_2 = R_0^{(0)} \quad \beta_2 = R_0^{(0)} \\ & C_2 = \emptyset \Rightarrow \frac{s C_2 d_1 + 1}{s C_1 \beta_2 + 1} \rightarrow d_1 = R_0^{(0)} \quad \beta_1 = R_0^{(0)} \\ & C_2 \rightarrow 0 \Rightarrow \frac{s^2 C_2 C_1 d_1 + s C_1 d_1}{s^2 C_2 C_1 \beta_1 + s C_2 \beta_1} = \frac{s C_1 d_1}{s C_2 \beta_1} \cdot \frac{(1 + s C_2 \frac{d_1}{d_1})}{(1 + s C_2 \frac{\beta_1}{\beta_1})} \rightarrow \frac{d_1}{d_1} = R_0^{(0)} \rightarrow d_{12} = R_0^{(0)} R_0^{(0)} \\ & C_2 \rightarrow \infty \Rightarrow \text{same} \end{aligned}$$

7. Quantitative description of noise: noise variance and noise power spectral density. (L02_16) 🎧

In a electronic circuit, we do not only have our signal that propagates but also a contribution of electronic noise and disturb. Disturb is given by external sources and can be filtered by taking appropriate actions while we cannot separate the noise from our signal, so we should quantify the average value of the noise, so that derive the minimum signal that we should apply. Since a noise is a fluctuation in time, it can be considered as a gaussian with zero mean value and with parameters not depending on time. To have a quantitative measure, we can take σ^2 , so where 68% of samples fall.

By definition, $\sigma^2 = E\langle x^2(t) \rangle - (E\langle x(t) \rangle)^2$ but keeping in mind that in our case, the mean value is zero!

Since the noise can be described as a superposition of orthogonal harmonics:

$$x(t) = A \sin(\omega_1 t + \varphi_1) + B \sin(\omega_2 t + \varphi_2)$$

$$\langle x^2(t) \rangle = \langle A^2 \sin^2(\omega_1 t + \varphi_1) + B^2 \sin^2(\omega_2 t + \varphi_2) + 2AB \sin(\omega_1 t + \varphi_1) \sin(\omega_2 t + \varphi_2) \rangle = \frac{A^2}{2} + \frac{B^2}{2}$$

So, we can derived that the variance is equal to the sum of variance values of single component. More in general, we can say: $\sigma^2 = \sum_i \sigma_i^2 = \int S_n(f) df$. Calling $S_n(f)$ the noise power spectral density, describing how this power is distributed across different frequencies

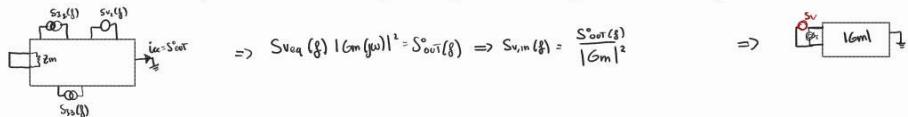
Conclusions:

1) Knowing the noise (voltage or current) power spectral density in a node of a circuit, we can know the noise in another node of the circuit (input, output, etc) just by multiply by the transfer function squared and sum with the other variance square of the other noise in that node.

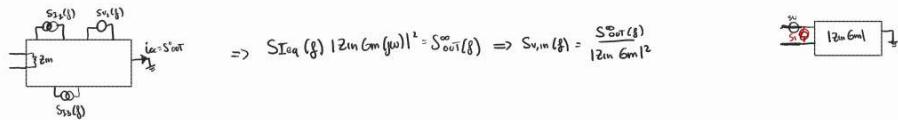
2) Knowing that the variance comes from the integral in frequency, if we know that a signal has a limited bandwidth, we should ALWAYS filter the signal + noise around the bandwisth of our interest in order to reduce the noise.

8. Noise transfer in circuits. Input referred noise sources of a two-port network. Definitions and derivation. ()

Noise in electrical circuits propagates through components and systems, influencing performance. A **two-port network** is a convenient model to analyze how noise sources within a circuit contribute to the overall noise at the output or are referred back to the input. This model consists on replacing the circuit with an ideal, noiseless circuit with equivalent noise sources at the input terminals. Deriving the equivalent noise source is a simple algorithm of few steps: to derive the input-referred voltage noise, we short both input and output and finds i_{cc} at the output and devide it by the square of the gain G_m (voltage \rightarrow current)



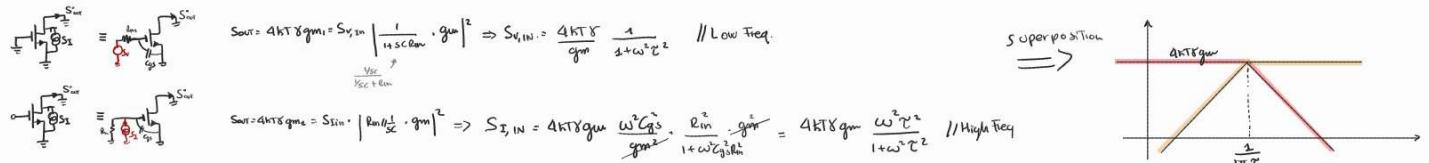
Instead to derive the input-referred current noise, we keep short the output and keep the input open. This time we divide S_{out} by the square of the current gain (current \rightarrow current) or simply $Z_{in} * G_m$



Let's use the two port network theorem for a mosfet:

$$\begin{aligned} \text{Left: } & \frac{S_{out}}{S_{11}} \equiv \frac{S_{out}}{S_{11}} \quad S_{out} = 4kTg_{m1} = S_{11}g_{m1}^2 \Rightarrow S_{11} = \frac{4kTg}{g_{m1}} \\ \text{Right: } & \frac{S_{out}}{S_{11}} \equiv \frac{S_{out}}{S_{11}} \quad S_{out} = 4kTg_{m1} = S_{11} \left| \frac{g_m}{s(C_{gs}C_{gd})} \right|^2 \Rightarrow S_{11} = 4kTg_{m1} \frac{\omega^2 C_{gs}^2}{g_{m1}^2} \Rightarrow \left[\omega_1 = \frac{g_{m1}}{C_{gs}} \right] \Rightarrow S_{11} = 4kTg_{m1} \left(\frac{\omega}{\omega_1} \right)^2 \end{aligned}$$

Let's have a confirm that the two port theorem is valid for every input resistance:



Overall, the input resistance will shift the pole, so where the current or the voltage input referred noise is dominant.

9. Noise models: Thermal noise of resistors. The Nyquist argument for the thermal noise power spectral density. (L02_17)

Since noise is given by random walk of carriers that may invert their direction due to scattering with ions (<1ps), we can consider their contributions as spike, so their spectrum is expected to be constant (at least in our range of frequencies). This type of noise is called White Noise because of its spectrum. Considering a simple network with a capacitor, we try to exploit the variance:

$$\text{Circuit diagram: } \frac{R}{2} \parallel \frac{1}{j\omega C} \parallel V_n \Rightarrow \left\{ \begin{array}{l} S_V(f) = W \\ T(\omega) = \frac{1/SC}{1+j\omega R} = \frac{1}{1+j\omega RC} \Rightarrow T(j\omega) = \frac{1}{1+j\omega C} \\ \sigma^2 = \langle V_c^2 \rangle = \int_{-\infty}^{\infty} S_V(f) |T(j\omega)|^2 df \end{array} \right. \Rightarrow \sigma^2 = \int_{-\infty}^{\infty} W \left| \frac{1}{1+j\omega C} \right|^2 df = W \int_{-\infty}^{\infty} \frac{1}{1+\omega^2 C^2} d\omega = \frac{W}{2\pi C} \int_0^{+\infty} \frac{d(\omega C)}{1+\omega^2 C^2} = \frac{W}{2\pi C} [\arctan(\omega C)]_0^{+\infty} = \frac{W}{2\pi C} \cdot \frac{\pi}{2} = \frac{W}{4C}$$

Now we should derive the value W based on thermodynamic argument. In a single capacitor network, the energy can be stored only there and the only variable that set it is the voltage across the capacitor. Since the system has a single degree of freedom, we can say:

$$\frac{1}{2} C \langle V_c^2 \rangle = \frac{1}{2} k_B T \Rightarrow \langle V_c^2 \rangle = \frac{k_B T}{C} \Rightarrow W = 4k_B T R \Rightarrow S_V(f) = \frac{4k_B T}{R}$$

In a mosfet in ohmic regime, we can use the same result, considering that the resistance seen is the resistive channel:

$$\frac{1}{R_{ch}} = G_{ch} = \frac{\partial I}{\partial V_{ds}} \Big|_{V_{ds}=0} = \mu C_{ox} \left(\frac{W}{L} \right) (V_{ds} - V_t) = g_{m0} \quad S_V(f) = \frac{4k_B T R_{ch}}{g_{m0}}$$

In the saturation region, since the channel is not uniform anymore, we can consider a correction factor: $S_V(f) = \frac{4kT\delta}{g_{m0}}$ $S_I(f) = 4kT\delta g_{m0}$

NYQUIST

R with thermal noise

At a certain time
R = short circuit
(then solution eq. onde con condizioni al contorno
 $V(x) = V(t)$)

$\left\{ \begin{array}{l} \text{Eq. Onde: } \frac{\partial^2 V(x,t)}{\partial x^2} = \frac{1}{v^2} \frac{\partial^2 V(x,t)}{\partial t^2} \\ V(0,t) = \nabla V(x,t) = \emptyset \end{array} \right.$

Hip: $\nabla V(x,t) = X(x) T(t)$ ipotizzo che sia scindibile come due eq. indipend.

$X''(x) T(t) = \frac{1}{v^2} X(x) T''(t) \Rightarrow \frac{X''(x)}{X(x)} v^2 = \frac{T''(t)}{T(t)}$ che è valida solo se le due espressioni sono costanti al variare delle incognite.
Chiamo la costante $-\gamma^2$ (dove essere negativo sono i numeri complessi ma non le loro parti reali)
(quindi questo stabilisce per imposto $v > 0$)

$\Rightarrow \left\{ \begin{array}{l} V(x,t) = X(x) T(t) = C \operatorname{seu}(\gamma t + \phi) \left[A \cos \left(\frac{\gamma x}{v} \right) + B \sin \left(\frac{\gamma x}{v} \right) \right] \\ V(0,t) = \emptyset \Rightarrow T(t) \cdot A = \emptyset \Rightarrow A = \emptyset \\ V'(0,t) = \emptyset \Rightarrow T(t) B \operatorname{seu}' \left(\frac{\gamma L}{v} \right) = \emptyset \Rightarrow \frac{\gamma L}{v} = n\pi \Rightarrow \gamma = n\pi \frac{v}{L} \end{array} \right.$

$\omega = \frac{n\pi v}{L} \Rightarrow \theta = \frac{n\pi}{2L} \quad (\text{frequenze che possono esistere nel canale costante})$

$Energia = \# \text{gradi libri} \cdot 2 \cdot \frac{E^2}{2} \Rightarrow \left[\# \text{modi} = \text{gradi libri} = \frac{\Delta \theta}{\frac{\pi}{L}} \right] = \frac{2L \Delta \theta}{\pi} \cdot \frac{E^2}{2}$

Potenza imposta

$P = \frac{1}{2} \bar{V} \bar{I}^2 = \frac{1}{2} \frac{1}{R} \frac{1}{2} \left(\operatorname{seu} \frac{\theta}{2} \right)^2 \cdot \frac{1}{2} \frac{1}{2} = \frac{C_0^2}{8R} \cdot \frac{1}{4R} \cdot \frac{\theta^2}{2} \Rightarrow \left[\theta = \frac{E}{T} \Rightarrow E = P \cdot T = \frac{P L}{v} \right] \Rightarrow E = \frac{1}{2R} \frac{C_0^2}{2} \frac{L}{v}$

questo perché $S_f df = S_f \text{ di una singola sin. (Fourier = } \sum \sin)$
 $\hookrightarrow S_f \text{ di una singola sin. } = \frac{A^2}{2}$

$\left\{ \begin{array}{l} E = \Delta f \frac{2L}{v} K T \\ E = \frac{1}{2R} S_f \Delta f \frac{L}{v} \end{array} \right. \Rightarrow \Delta f \frac{2L}{v} K T = \frac{1}{2R} S_f \Delta f \frac{L}{v} \Rightarrow S_f = 4KTR$

10. Noise models: Shot noise model. Application to p-n junctions, BJTs and MOSFETs in weak inversion. (L02B_24)

Now we analyse the carriers in a pn junction. The bias current is defined as the average number of carriers crossing the junction per unit time, but since it can be affected by statistical fluctuations, it is also a source of noise, called "shot noise". To describe it, we want to find the variance (in current): $\sigma_i^2 = \langle i^2 \rangle - \langle i \rangle^2$

Our first goal is to determinate the current. Let's start considering the pn junction as a parallel plate capacitor where each carrier is a charge moving between the plates. An electron at distance x from the first plate gives a contribution of charge of Q_1 for the first plate and Q_2 for the second one, with $Q_1+Q_2=q$ always. $Q_1 = q \frac{(L-x)}{L}$ $Q_2 = \frac{qx}{L}$

The current is given by: $i(t) = \frac{dQ_1}{dt} = \left| \frac{\partial Q_1}{\partial t} \right| = \frac{dq}{dx} \frac{dx}{dt} = \frac{q}{L} V(t)$

We find that the current is proportional to the instantaneous carrier speed. In vacuum, the carrier over time will give a triangular pulse contribution, instead, in our case, we imagine that the velocity has saturated and the pulse has a rectangular shape with $i(t)=qh(t)$.

Overall the shot noise is given by all these pulses that occur at a certain time.

We denote λ as the average rate of carriers across the junction per unit time, so we have that the number of pulses starting from t and $t+\delta t$ is given by $\lambda \delta t$

The current measured at an instant t will be given by the superposition of all the pulses before t .

Using an additional coordinate x , we can write:

$$\begin{aligned} i(t) &= qh(x_0) + qh(x_1) + qh(x_2) + \dots \\ \langle i(t) \rangle &= \int h(x) \lambda q dx \Rightarrow [\int h(x) dx = 1] \Rightarrow \langle i(t) \rangle = \lambda q \Rightarrow \langle i^2 \rangle = (\lambda q)^2 \\ i(t) &= q^2 h^2(x_0) + q^2 h^2(x_1) + q^2 h^2(x_2) + \dots + q^2 h(x_0)h(x_1) + q^2 h(x_0)h(x_2) + \dots \\ \langle i^2(t) \rangle &= \int \lambda q^2 h^2(x) dx + \iint q h(x) \lambda dx \cdot q h(y) \lambda dy = \lambda q^2 \int h^2(x) dx + (\lambda q)^2 \end{aligned}$$

(NB: $\lambda \ll q$ in room temp.)

$[I = \lambda q]$



Figure 1. a) Electron transit in the depleted region of a p-n junction. b) Electron transit between the plates of a parallel plate capacitor.

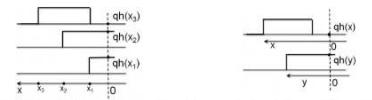
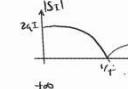


Figure 2. a) evaluation of the mean value of the current described as a random superposition of elementary pulses with the same form and area. b) evaluation of the square mean value.

$$\begin{aligned} \text{Paraxial: } \int |h(x)|^2 dx &\approx \int h(x)^2 dx = \int h^2(x) dx \quad \text{[because even]} \\ \sigma_I^2 = \langle i^2 \rangle - \langle i \rangle^2 &= \lambda q^2 \int h^2(x) dx + (\lambda q)^2 - (\lambda q)^2 \Rightarrow S_I = \sigma_I^2 = 2q \int_0^\infty |h(x)| dx \end{aligned}$$



We know from the basics that the Fourier Transform of a rect is a sinc. Since a sinc is zero at $1/T$ (in our case around 100GHz), for our range of frequency, we can consider the noise constant of $2qI$.

The shot noise can be seen in three device that we have studied: the diode, the mosfet in weak inversion and in a bjt because each of them has a pn junction where the current should flow. For each of them, we should define which current takes place.

For a diode, we have the shot noise both if forward and reverse biased junction.

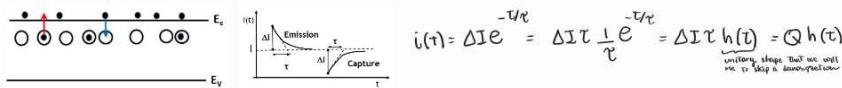
For a mosfet in weak inversion we have the current noise at the source-drain terminals: $S_I = 2qI_D \Rightarrow [g_{mS} = \frac{I_D}{nV_T}] \Rightarrow 2A' g_{mS} \frac{kT}{X} \Rightarrow 4kT \delta g_{mS} \left[\delta = \frac{n}{2} \right]$

For a bjt, we have a current from base to emitter and one from collector to emitter. In addition, since there's an ohmic path in the base, we can define a "spreading resistance" (around 250 ohm) that contributes to the noise with its resistance. Overall, in a bjt transistor, we can define three noise contributions. As we have done with a mosfet, we can use the two port theorem to find two single generators that represent the noise.

$$\begin{aligned} \text{Top: } & S_{out} = 2qI_B\beta l^2 + 2qI_C = S_I |\beta|^2 \Rightarrow S_I = 2qI_B \left(1 + \frac{1}{\beta} \right) \approx 2qIB \\ \text{Bottom: } & S_{out} = 4kTR_{bb} \left(\frac{R_{bb}}{R_E + R_{bb}} \right)^2 + 2qI_C = S_V \left(\frac{R_{bb}}{R_E + R_{bb}} \right)^2 \Rightarrow S_V = 4kTR_{bb} + 2qI_C \left(\frac{R_E + R_{bb}}{R_E} \frac{1}{g_m} \right)^2 \approx 4kTR_{bb} + 2q \frac{I_C}{g_m} \Rightarrow [I_C = g_{mV}V_{BE}] \Rightarrow 4kTR_{bb} + \frac{2kT}{g_{mV}} \end{aligned}$$

11. Trapping noise: trapping noise in a resistor (L13C_24)

In our technology we use doped silicon. This means that we will likely have defects, especially at the interface, that acts as a centre of recombination and generation. Since the current is proportional to the number of free carriers in a resistor, we can say that $\frac{\Delta I}{I} = \frac{\Delta N}{N}$. When a capture event occurs, we register a ΔI in the current, while when an emission event occurs, we register a $-\Delta I$. After a while, the defect will emit again (or capture again) the carrier. Since the emission (capture) can take place after a different amount of time, it can be shown that we can describe it with an exponential function:



Since the current of the noise is a superposition of pulses, we can use what we have derived in the shot noise:

$$S_I(f) = 2\lambda Q^2 |H(f)|^2 \quad \left\{ \begin{array}{l} \lambda = \beta \frac{N_T}{\tau} \quad // \text{Trapping rate} \\ Q^2 = (\Delta I \tau)^2 \end{array} \right. \Rightarrow S_I(f) = 2\beta \frac{N_T}{\tau} \Delta I^2 \tau^2 \frac{1}{(1+\omega^2 \tau^2)} \Rightarrow \left[\frac{\Delta I}{I} = \frac{\Delta N}{N} \right] \Rightarrow S_I(f) = 2\beta N_T \left(\frac{I}{N} \right)^2 \frac{\tau}{1+\omega^2 \tau^2} \Rightarrow \left[\beta \approx \frac{1}{Q} \right] \Rightarrow S_I(f) = N_T \left(\frac{I}{N} \right)^2 \frac{\tau}{1+\omega^2 \tau^2}$$

positive and negative spikes

NB: The base current of a bjt is very sensitive to traps because it has to cross the centre of recombination!

$$\text{PDE: In a resistor } V=RI \Rightarrow I = \frac{V}{R} \quad \left[Q = \frac{I}{q N_A N_D} \frac{1}{W D} \right] \Rightarrow I \propto N$$

12. McWhorter model of the 1/f noise in MOSFETs. Tvidis formula. (L13_24) 🍒

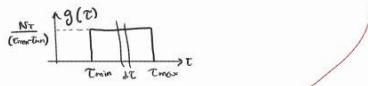
We have found that the power spectral density of the noise caused by defects is $S_I(f) = N_T \left(\frac{I}{N}\right)^2 \frac{\pi}{1 + \omega^2 \tau^2}$

But tau is not a single value! tau depends on where's the energy level of the traps!

We can introduce an additional function $g(\tau)$ to represent the link between tau and N_T :

$dN_T(\tau) = N_T g(\tau) d\tau$ with $d\tau$ the portion of traps with a specific τ .

$$\Rightarrow S_I(f) = \int_{\tau_{min}}^{\tau_{max}} dN_T \left(\frac{I}{N}\right)^2 \frac{\pi}{1 + \omega^2 \tau^2} = N_T \left(\frac{I}{N}\right)^2 \int_{\tau_{min}}^{\tau_{max}} \frac{g(\tau) d\tau}{(1 + \omega^2 \tau^2)}$$

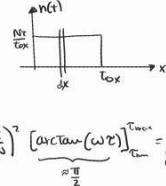


Now, our goal is to find out what's $g(\tau)$.

McWhorter pointed out that in a mosfet, the carriers that travel in the channel can be trapped by defects both at the interface channel-oxide and by tunneling inside the oxide. The average tunneling time is $\tau = \tau_0 e^{V_x}$ where V_x depends on the height of the barrier and τ_0 is the capture time for the same energy level of traps.

We can approximate that the traps along the oxide are uniformly distributed, so that

$$\begin{aligned} \Rightarrow \begin{cases} dN_T = N_T g(\tau) d\tau \\ dN_T > \frac{N_T}{t_{ox}} dx \\ \tau = \tau_0 e^{V_x} \\ S_I(f) = N_T \left(\frac{I}{N}\right)^2 \int_{\tau_{min}}^{\tau_{max}} g(\tau) d\tau \end{cases} &\Rightarrow \frac{N_T}{t_{ox}} g(\tau) d\tau = \frac{dx}{t_{ox} d\tau} \Rightarrow g(\tau) = \frac{dx}{t_{ox} d\tau} = \frac{1}{\tau_0 t_{ox}} \\ &\Rightarrow d\tau = \tau_0 V_x e^{V_x} dx = \tau_0 dx \Rightarrow dx = \frac{1}{\tau_0} d\tau \\ &\Rightarrow S_I(f) = \frac{N_T}{t_{ox}} \left(\frac{I}{N}\right)^2 \int_{\tau_{min}}^{\tau_{max}} \frac{1}{\tau} \frac{\tau}{1 + \omega^2 \tau^2} d\tau \cdot \omega = \frac{N_T}{\omega t_{ox}} \left(\frac{I}{N}\right)^2 \left[\arctan(\omega \tau) \right]_{\tau_{min}}^{\tau_{max}} = \frac{N_T}{\omega t_{ox}} \left(\frac{I}{N}\right)^2 \frac{\pi}{2} = \frac{N_T}{4 \omega t_{ox}} \left(\frac{I}{N}\right)^2 \frac{1}{8} \end{aligned}$$



The Tsividis formula help us to use the result of McWhorter in a easier way:

$$\begin{aligned} \begin{cases} N = C_{ox} V_{ds} = C_{ox} W L \left(V_{ds} - V_t\right) \\ I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{ds} - V_t)^2 \\ N_T = n_T W L t_{ox} \end{cases} &\Rightarrow S_I(f) = \frac{n_T}{4 \omega t_{ox}} \left(\frac{I}{N}\right)^2 \frac{1}{8} = \frac{n_T W L t_{ox}}{4 \omega t_{ox}} \left(\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{q}{C_{ox} W L t_{ox}} \right)^2 \frac{1}{8} = \frac{n_T q^2 \mu_n^2}{8 \times 2 \times \frac{1}{2} \times \frac{W}{L} \times \frac{q}{L} \times \frac{C_{ox}}{C_{ox}}} \frac{1}{t_{ox}^2} = \frac{n_T q^2 \mu_n^2}{8 \times C_{ox}} \frac{1}{L^2} \frac{I^2}{8} = K_3 \frac{q^2 \mu_n^2}{L^2} \frac{I^2}{8} \\ &\Rightarrow S_V(f) = \frac{S_I(f)}{g_{th}} = \frac{n_T q^2 \mu_n^2}{8 \times C_{ox}} \frac{1}{L^2} \frac{\frac{1}{8} \mu_n C_{ox} \frac{W}{L} V_{ds}^2}{\frac{1}{8} \mu_n^2 C_{ox}^2 \frac{W^2}{L^2} V_{ds}^2} \frac{1}{g_{th}} = \frac{n_T q^2 \mu_n^2}{16 \times C_{ox}^2 \frac{W^2}{L^2} V_{ds}^2} \frac{1}{g_{th}} = K_4 \frac{q^2 \mu_n^2}{C_{ox}^2} \frac{1}{L^2} \frac{1}{g_{th}} \end{aligned}$$

// better to use because it doesn't depend on I

13. The prototypical differential stage: from resistive to active loads. Common mode feedback and single ended option. (L03_17)

Our goal is to design a differential amplifier that has a high differential gain and a high Common Mode Rejection Ratio (Gd>>Gcm). To do so, our first step is to design a differential input stage. The easiest circuit we can think is a differential stage with resistive loads:

First of all, we should understand how to set the bias of this circuit: we decide the current that flows in the tail and the overdrive of the two input mosfet (Vov=0.1, the lower the overdrive, the higher gm and so the gain). After that, we may set Vg=Vdd/2 and then we also find the value of Re = (Vg-Vgs)/2I.

Let's now derive the Gd and Gcm to see if this circuit is appropriate.

The differential gain of this stage is given by $G_d = g_m R_L$. We should underline that we cannot rise RL too much to amplify the gain, because increasing RL means increasing the voltage drop across it and risk that the mosfet enter the ohmic region. Now we derive the Gcm. In common mode, the input transistors act like source followers, so the current that flows in RE is V_{cm}/R_E . This current will split in half, giving $G_{cm} = RL/2R_E$. Overall we have:

$$G_{d,max} = \frac{g_m R_L}{2} = \frac{2I}{V_{ov}} \cdot \frac{R_L}{2} = \frac{V_{RL,max}}{V_{ov,min}}$$

$$G_{cm} = \frac{R_L}{2R_E} = \frac{I_{RL}}{2I_{RE}} = \frac{V_{RL,max}}{V_E}$$

$$CMRR = \frac{G_d}{G_{cm}} = \frac{V_E}{V_{ov}}$$

NB Both $G_{cm}, G_d \propto V_{IL,max}$

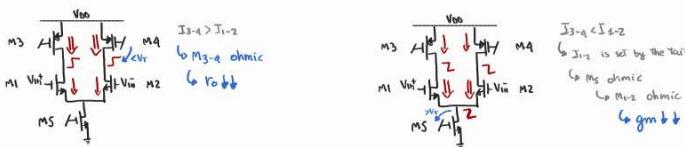


Our main limitation is due to the voltage drop across R_L . We should replace them with a device that provides a high impedance independent on the voltage drop across it. To do so, we should replace all the resistors with current sources: Let's analyse the differential stage with active loads.

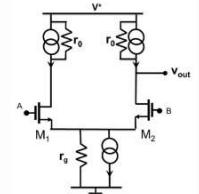
In this case $G_d=g_m r_o/2$, that can be set changing the lenght of the transistor! While $G_{cm}=r_o/2rg$, giving $CMRR=g_m * rg$.

We have quite good results! But the problem of this stage is setting the bias considering possible mismatch!

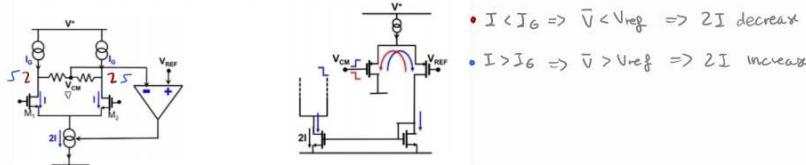
We know consider a possible mismatch of M3-M4.



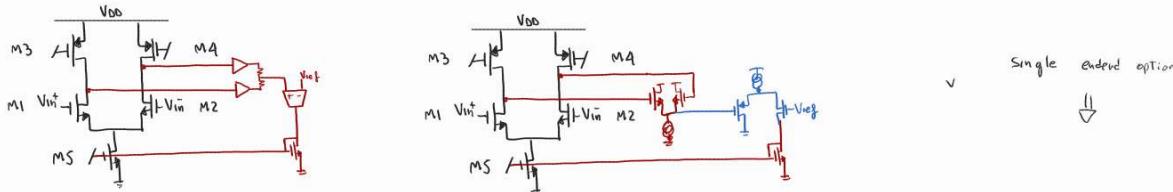
=> In both cases The gain drop down!!



To solve this issue, we introduce a common mode feedback:



Actually in this way we change G_d , so we should do...

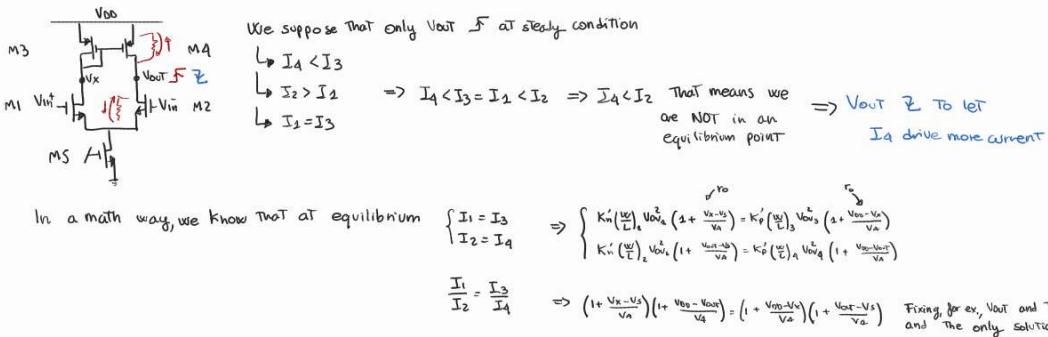


14. Single ended differential stage with mirror: Bias, input and output voltage swings, differential gain, common mode gain. (L04_17) 🏠

Another way to guarantee that a mismatch between the pair of transistor won't influence the differential gain, is using a differential stage with a mirror, also called single ended configuration (because having the other node at low impedance means that we cannot have a double ended anymore).

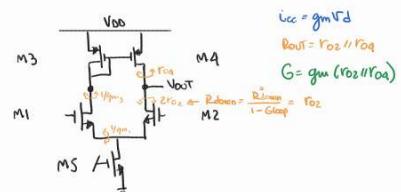
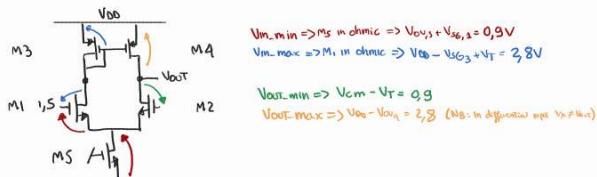
Let's first show that the mismatch won't cause troubles and then we derive how to set the bias, the voltage swing and gains.

Our goal is to demonstrate that V_x (drain of M3) and V_{out} follow each other. We use a proof by contradiction first and then the math proof.



For the bias we set the current of the tail (according to noise requirements) and we decide mosfet overdrives (both based on dynamics and noise). Some values may be $I_{tail} = 50\mu\text{A}$, $V_{ov_1} = 0.1\text{V}$, $V_{ov_3} = 0.2\text{V}$, $V_{ov_5} = 0.2$.

Now let's study the dynamics considering $V_{cm} = 1.5\text{V}$ and $V_{out} = 2.2\text{V}$ ($V_{dd} - V_{gs3}$):



To derive the differential gain, we use Norton Theorem. This theorem says that $G = i_{cc} * R_{out}$. Finally, we derive G_{cm} , still given by $i_{cc} * R_{out}$

$i_{cc} = \frac{i_{tail}}{2} \cdot E$

$i_{tail} = \frac{V_{cm}}{R_{og}}$

$\begin{cases} i_1 = i_{tail} \frac{R_2}{R_1 R_2} = \frac{R_2}{\frac{r_{ds1} + r_{ds2}}{g_{m1} g_{m2}} + \frac{r_{ds1} + r_{ds2}}{g_{m1} g_{m3}}} i_{tail} = \frac{V_{cm}}{R_{og}} \frac{R_{01}}{2 R_{01} + \frac{1}{g_{m3} r_{ds3}}} \\ i_2 = i_{tail} \frac{R_1}{R_1 + R_2} = \frac{\frac{1}{g_{m1} r_{ds1}}}{r_{ds1} + \frac{1}{g_{m2} r_{ds2}} + R_{01}} i_{tail} = \frac{V_{cm}}{R_{og}} \frac{\frac{1}{g_{m3}} + \frac{1}{R_{01}}}{2 R_{01} + \frac{1}{g_{m3} r_{ds3}}} \end{cases} \Rightarrow i_2 = i_1 \left(1 + \frac{1}{g_{m3} r_{ds3}}\right)$

$i_4 = i_1 \frac{R_2}{R_{03} + \frac{1}{g_{m3}}} = i_1 \frac{1}{1 + \frac{1}{g_{m3} r_{ds3}}} \approx i_1 \left(1 - \frac{1}{g_{m3} r_{ds3}}\right)$

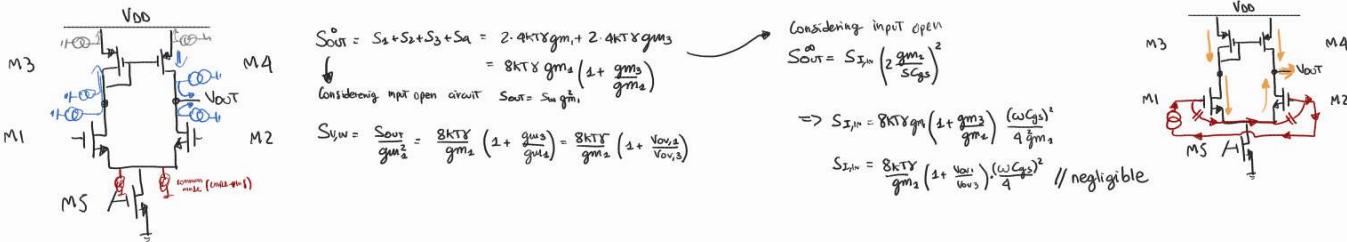
$i_{cc} = i_2 - i_4 = i_1 \left(1 + \frac{1}{g_{m3} r_{ds3}} - 1 + \frac{1}{g_{m3} r_{ds3}}\right) \Rightarrow E = \frac{1}{g_{m3} r_{ds3}} + \frac{1}{g_{m3} r_{ds3}}$

$$\Rightarrow G_{cm} = \frac{E}{2 R_{og}} \cdot R_{out} = \frac{E}{2 R_{og}} (R_{02} // R_{04})$$

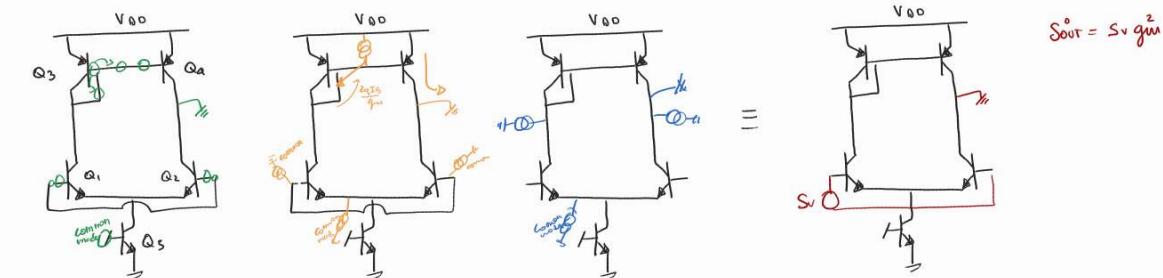
$$\Rightarrow CMRR = \frac{G_d}{G_{cm}} = \frac{g_m (R_{02} // R_{04}) 2 R_{og}}{E (R_{02} // R_{04})} = 2 \frac{R_{og} g_m}{E}$$

15. Input referred noise sources of a differential stage with MOSFETs and BJTs. Power-noise trade-off. ()

In theory, an OTA is not a two port network because $V_{out}(v_d, v_{cm})$, but under the assumption of $CMRR \rightarrow \infty$, we can consider it a two port network and derive the input referred noise. We will use the split theorem to analyse all the noises.



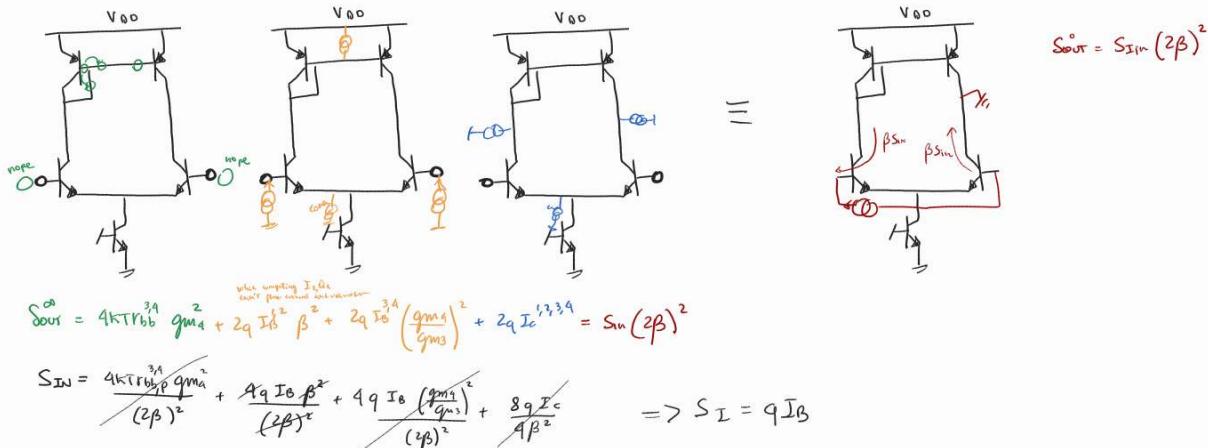
Overall, the noise set a minimum current for the bias!



$$S_{out} = E_n^{3/2} g_m^2 + E_n^{3/4} g_m^2 + 2qI_c^{3/4} \cdot \left(\frac{g_{m3}}{g_{m2}} \right)^2 + 2qI_c^{1/2, 3/4} = S_v g_m^2$$

$$S_v g_m^2 = 8kTg_m^2 + 8kTg_m^2 + 4qI_c \left(\frac{g_{m3}}{g_{m2}} \right)^2 + 8qI_c g_m^2$$

$$S_v = 8kTg_m^2 + 4qI_c + \frac{8qI_c}{g_m^2} \Rightarrow S_v = 8kTg_m^2 + \frac{8qI_c}{g_m^2} \left(1 + \frac{1}{\beta} \right) \quad [I_c = g_m \frac{kT}{q}] \Rightarrow S_v = 8kT \left(r_{bb,n} + \frac{1}{g_m^2} \right)$$



16. Two-stage CMOS OTA: topology, frequency response using the time constant method, Miller compensation. Pole splitting vs. compensation capacitance value. The RHP zero and the high frequency pole. OTA compensation and FoM. (L04_17) 🚨

First of all, we derive the overall circuit and how to set the bias. We saw that increasing the channel length (to increase the gain) both influence the area needed and the cut-off frequency decrease. Not to limit the speed of the circuit, we decide to use an additional stage, a common source to gain what we need.

$$G_{tot} = g_{m1} R_{out1} \cdot g_{m2} R_{out2}$$

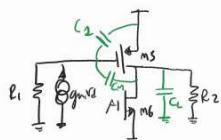
$$V_{out,1} = V_{out,4} \quad // \text{to match}$$

$$I_S = 2I_1 \quad (\text{if not other requirement})$$

$$V_{out,5} = V_{out,6} \quad // \text{to set the same current}$$

$$K_S = K_6 \quad // \text{with good dynamics}$$

Since the circuit has two high impedance nodes, at the output of the first and second stage, there's a risk to have two poles before the GBWP! Because of that, we need a proper compensation. Let's first analyse the Miller Compensation:



$$T(s) = g_{m1} R_{out1} g_{m2} R_{out2} \frac{a_1 s + 1}{b_1 s^2 + b_2 s + 1} \quad \begin{matrix} 3 \text{ poles interactive (2 poles)} \\ 1 \text{ zero (the others at } \infty\text{)} \end{matrix}$$

$$\begin{aligned} V_1 &= R_1 - I_S \\ V_2 &= (V_1 g_{m3} - I_S) R_2 \\ V_3 &= V_2 - V_1 = R_2 I_S + R_1 I_S g_{m2} + R_2 I_S \\ V_4 &= I_S (R_3 + R_2 + R_1 R_2 g_{m2}) \\ Req &= \frac{V_3}{I_S} = R_1 + R_2 + R_1 R_2 g_{m2} \end{aligned}$$

$$\Rightarrow T(s) = -A_0 \frac{(1 - s \frac{C}{g_{m2}})}{b_1 s^2 + b_2 s + 1}$$

$$\Rightarrow P_C \approx -\frac{1}{b_2} = -\frac{1}{C_1 R_1 + C_2 R_2 + C_m (R_1 + R_2 + g_{m2} R_2)} \approx -\frac{1}{C_2 R_2 + R_2 (C_1 + C_m) + C_m R_2 (1 + g_{m2} R_2)} \approx -\frac{1}{C_m R_2 (1 + g_{m2} R_2)}$$

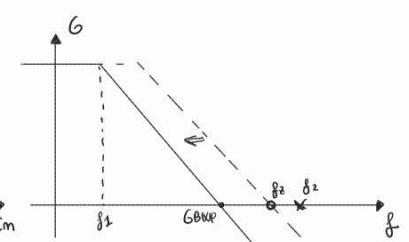
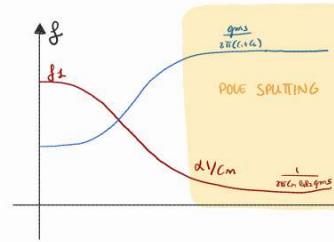
$$\Rightarrow P_H \approx -\frac{b_1}{b_2} = -\frac{C_m R_1 g_{m2} R_2}{R_1 R_2 (C_1 C_m + C_1 C_m + C_m)} \approx -\frac{C_m R_1 R_2 g_{m2}}{R_1 R_2 g_{m1} (C_1 + C_2)} = -\frac{g_{m2}}{C_1 + C_2}$$

(since I want the two poles to be far away, I can use the splitting approx)

$$\left\{ \begin{array}{l} f_1 = \frac{1}{2\pi C_m (1 + g_{m2} R_2)} \\ f_2 = \frac{g_{m2}}{2\pi (C_1 + C_2)} \\ f_3 = \frac{g_{m2}}{2\pi C_m} (+) \\ G_{BWIP} = f_2 A_0 = \frac{g_{m1} R_1 g_{m2} R_2}{2\pi C_m R_1 R_2 g_{m2}} = \frac{g_{m1}}{2\pi C_m} \end{array} \right.$$

$$\Rightarrow GBWP < f_2 \Rightarrow C_m > \frac{g_{m1}}{g_{m2}} (C_1 + C_2)$$

$$\Delta = 180 - 90 - \arctan\left(\frac{GBWP}{f_2}\right) - \arctan\left(\frac{GBWP}{f_3}\right) \Rightarrow f_2, f_3 \gg GBWP$$



Having $I_S > I_2 \Rightarrow$ move f_2, f_3 at HF
Increasing $C_m \Rightarrow$ move $f_2, GBWP$ down

$FoM = \frac{GBWP \cdot C_m}{I_{TOT}}$

17. Two-stage CMOS OTA: frequency compensation with the nulling resistor. Implementing the nulling resistor. (L06_19)

The Miller compensation solves the compensation problem but in some cases the power penalty is not acceptable. The main problem is due to the positive zero that contributes like a pole in the phase margin. The first and intuitive way to make the zero negative, is to add a resistance in series to the Miller capacitance. Let's study again where the zero and the poles are:

$$\text{Zero } \frac{V_S}{R_N + \frac{1}{SC_m}} = V_S g_{mS} \Rightarrow s = -\frac{1}{C(R_N + \frac{1}{g_{mS}})} \Rightarrow f_z = \frac{1}{2\pi C_m (R_N + \frac{1}{g_{mS}})}$$

There are two ways of implementation of R_N : the first is to bring f_z to infinite (do not do that, there's variability in fabrication), or to use it to make a zero-pole cancellation with the second pole. (THE DOUBLES ALWAYS AFTER THE GBWP if possible).

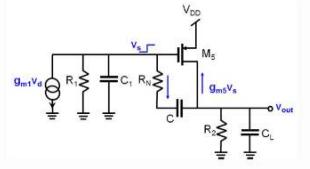
$$T_{low,2} = \sum T^o = R_1 C_1 + R_2 C_L + C_m (R_1 + R_2 + R_N + g_{mS} R_2) \approx C_m R_1 (1 + g_{mS} R_2) \quad // \text{NOT CHANGED}$$

Now there are three poles since the capacitors are independent and interactive. Since the pole due to the miller capacitor is way lower than the others, we can consider C_m as short when computing the other two.

$$T_{low,2} = \sum T^o = C_2 \frac{R_N + R_2}{1 + g_{mS} R_2} + C_2 \frac{R_N + R_1}{1 + g_{mS} R_1} \approx \frac{1}{g_{mS}} (C_1 + C_2)$$

$$\frac{1}{T_{max,3}} = \sum \frac{1}{T^o} = \frac{1}{C_2 (R_2 / R_N)} + \frac{1}{C_2 R_N} + \frac{1}{C_m R_N} \approx \frac{1}{R_N} \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_m} \right) \Rightarrow T_{max,3} = R_N (C_1 \parallel C_2 \parallel C_m)$$

$$\Rightarrow \begin{cases} f_1 = \frac{1}{2\pi C_m R_1 (1 + g_{mS} R_2)} \\ f_2 = \frac{g_{mS}}{2\pi (C_1 + C_2)} \\ f_3 = \frac{1}{2\pi C_m (R_N - \frac{1}{g_{mS}})} \\ f_4 = \frac{1}{2\pi R_N (C_1 \parallel C_2 \parallel C_m)} \end{cases} \quad] \text{Set } R_N | f_2 = f_3 \geq GBWP$$



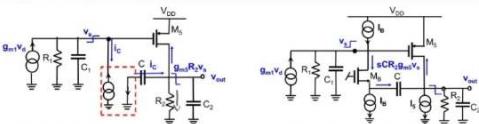
Note that R_N is often implemented with a MOS transistor in ohmic regime

Another way to remove the zero in the Miller Compensation is to stop the current in the Cm branch. There are two ways: using a voltage buffer or a current buffer. We first analyse the two ways considering them ideal. (Ideal case → interactive and not independent)

$$T_{\text{low}} = \sum T^0 = C_1 R_1 + C_2 R_2 + C_m R_i (1 + g_{\text{MS}} R_2) \Rightarrow j\omega = \frac{1}{2\pi C_1 R_1 (1 + g_{\text{MS}} R_2)} \quad \text{STILL.}$$

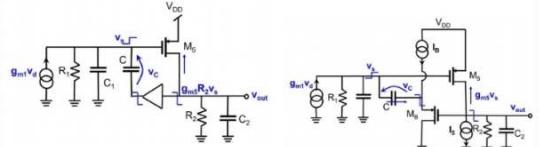
$$T_{\text{low}} = \sum T^0 = C_1 (R_1 // 0) + C_2 (R_2 // \frac{1}{g_{\text{MS}}}) \Rightarrow j\omega = \frac{g_{\text{MS}}}{2\pi C_2} \quad \text{DEPENDS ON } C_2 \quad (\text{NOT THAT GOOD})$$

no zero, no 3rd pole



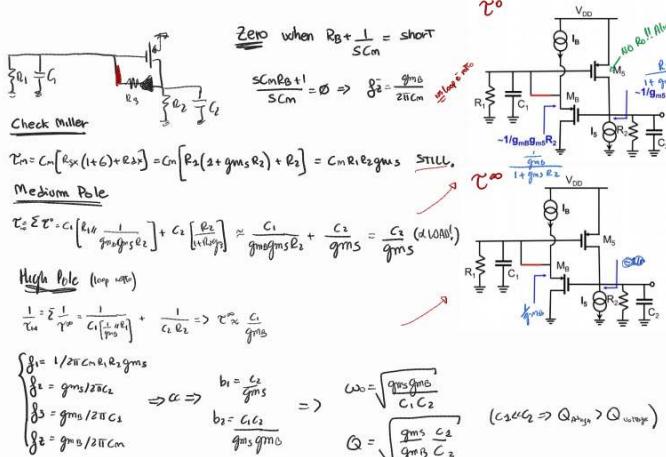
$$T_{\text{low}} = R_1 C_1 + R_2 C_2 + C_m R_i g_{\text{MS}} R_2 \Rightarrow \frac{1}{j\omega} = \frac{1}{2\pi C_1 R_1 (1 + g_{\text{MS}} R_2)} \quad \text{STILL. (≈)}$$

$$T_{\text{low}} = R_1 C_1 + R_2 C_2 + C_m R_i g_{\text{MS}} R_2 \Rightarrow \frac{1}{j\omega} = \frac{1}{2\pi C_2} \quad \text{NB INDEPENDENT ON } C_1$$



Now we discuss the impact of a buffer finite resistance. The capacitors, because of the source resistance, become independent and interactive and the zero re-appears!

REAL VOLTAGE BUFFER



REAL CURRENT BUFFER - AHUJA

$$\text{Zero when } R_B + \frac{1}{g_{\text{MS}}} = \text{short}$$

$$\Rightarrow \frac{sC_m R_B + 1}{sC_m} = 0 \Rightarrow j\omega = \frac{g_{\text{MS}}}{2\pi C_m} \quad \text{NO ZERO! ALREADY IN } T^0$$

Check Miller Effect

$$Z_m = C_m \left(R_B (1 + g_{\text{MS}}) + R_2 \right) = C_m \left[\frac{1}{g_{\text{MS}}} \left(1 + g_{\text{MS}} R_2 \right) + R_2 \right] \approx C_m R_2 g_{\text{MS}} \quad \text{STILL.}$$

Medium Pole

$$T_m = \sum T^0 = C_1 \left[R_1 \frac{1}{g_{\text{MS}} g_m R_2} + C_2 \left[\frac{R_2}{g_{\text{MS}} g_m} \right] \right] \approx \frac{C_1}{g_{\text{MS}} g_m R_2} + \frac{C_2}{g_{\text{MS}}} = \frac{C_2 (1 + g_{\text{MS}} R_2)}{g_{\text{MS}}}$$

High Pole (loop with)

$$\frac{1}{j\omega} = \sum \frac{1}{j\omega} + \frac{1}{C_1 \frac{1}{g_{\text{MS}} g_m} + \frac{1}{C_2 R_2}} = \frac{j\omega}{g_{\text{MS}}} \frac{C_1}{g_{\text{MS}}} + \frac{1}{g_{\text{MS}} g_m R_2}$$

$$\begin{cases} j\omega = 1/(2\pi C_1 R_1 g_m g_{\text{MS}}) \\ j\omega = g_{\text{MS}}/2\pi C_1 \\ j\omega = g_{\text{MS}}/2\pi C_2 \\ j\omega = g_{\text{MS}}/2\pi C_m \end{cases} \Rightarrow \omega = \frac{1}{g_{\text{MS}} g_m} = \frac{\omega_0}{C_1 C_2} \Rightarrow \omega_0 = \sqrt{\frac{g_{\text{MS}} g_m}{C_1 C_2}} \quad (C_2 < C_1 \Rightarrow Q_{\text{MS}} > Q_{\text{VFB}})$$

$$T^0 = C_1 \left(\frac{1}{g_{\text{MS}}} \right) + C_2 \left(\frac{1}{g_{\text{MS}} g_m R_2} \right) \approx \frac{C_1}{g_{\text{MS}}} \Rightarrow j\omega = \frac{g_{\text{MS}}}{2\pi C_1}$$

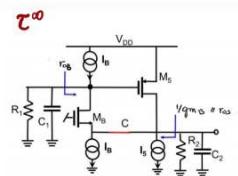
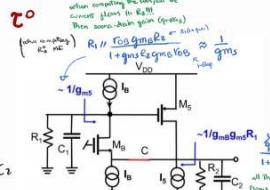
High Pole

$$\frac{1}{j\omega} = \sum \frac{1}{j\omega} + \frac{1}{C_1 (g_{\text{MS}} R_2)} + \frac{1}{C_2 \frac{1}{g_{\text{MS}}}} \Rightarrow T^0 = \frac{C_2}{g_{\text{MS}}} \Rightarrow j\omega_H = \frac{g_{\text{MS}}}{2\pi C_2}$$

TIME CONSTANT METHOD WITH C_1 AND C_2

$$\begin{cases} s^2 b_1 + s b_2 + 1 = \frac{1}{C_1 C_2 (g_{\text{MS}} R_2)} \\ b_2 = \frac{C_1}{g_{\text{MS}}} (T^0)^2 \\ b_2 = C_1 C_2 R^2 R_2 = C_1 \frac{1}{g_{\text{MS}} g_m} \end{cases} \Rightarrow \omega_0 = \sqrt{\frac{g_{\text{MS}} g_m}{C_1 C_2}} \Rightarrow Q = \frac{g_{\text{MS}}}{g_m} \sqrt{\frac{C_1 C_2}{g_{\text{MS}} g_m}} = \frac{\sqrt{g_{\text{MS}} C_1}}{g_{\text{MS}} C_2} \quad [Q = \frac{1}{\sqrt{1+Q^2}}]$$

// They are likely cc and the pick may > 0dB ⇒ May drop negative phase margin



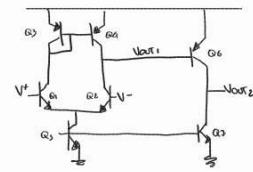
19. Two stage bipolar amplifier: input resistance, input referred voltage and current noise, sizing example and compensation. (L04B_14)

Let's assume that what we derive from MOSFET works with BJT. We use at first the same configuration of the MOSFET OTA and see its parameters:

$$G = G_1 G_2 = \frac{g_{m1} \beta_{mp}}{g_{m1}} \frac{g_{m6} (r_{o6} \parallel r_{o7})}{g_{m6}} \quad \text{and} \quad g_{m1} \frac{\beta_{mp}}{g_{m1}} \frac{I_c}{V_{TH}} \frac{V_A \sqrt{V_A}}{I_C} > G_{TOT} \Rightarrow g_{m6} < g_{m1}, \beta_{mp} \frac{V_A \sqrt{V_A}}{V_{TH}}$$

// second stage with low current

$$\frac{E}{g_{m3} r_{o3}} + \frac{1}{g_{m3} r_{o2}} + \frac{2}{\beta} \approx \frac{2}{\beta} \quad (\text{need to improve mirror}) \Rightarrow CMRR = \frac{2 g_{m1} r_{o2}}{E}$$



RESISTANCE

$$R_{in} = 2r_{bb} = \frac{2\beta_{mp}}{g_{m1}}$$

$$R_{out} = 2r_{bb} \text{ from}$$

NOISE

$$S_{out} = E_n^2 g_{m1}^2 + E_n^2 g_{m6}^2 + 2q I_o^2 \left(\frac{g_{m1}}{g_{m3}} \right)^2 + 2q I_c^{1/2,1} = S_v g_{m1}^2$$

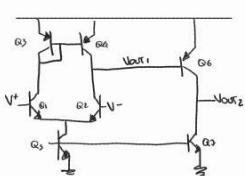
$$S_v g_{m1}^2 = 8kT r_{bb,n} g_{m1}^2 + 8kT r_{bb,n}^2 g_{m4}^2 + 4q I_B \left(\frac{g_{m1}}{g_{m3}} \right)^2 + 8q I_{C_e}$$

$$S_v = 8kT r_{bb,n} + \frac{q I_c}{\beta g_{m3}} + \frac{8q I_c}{g_{m1}} \Rightarrow S_v = 8kT r_{bb,n} + \frac{8q I_c}{g_{m1}} \left(1 + \frac{1}{\beta} \right) \Rightarrow S_v = 8kT \left(r_{bb,n} + \frac{1}{g_{m1}} \right)$$

$$S_{out} = 4kT r_{bb,n} g_{m1}^2 + 2q I_o^2 \beta^2 + 2q I_o^{1/2,1} \left(\frac{g_{m1}}{g_{m3}} \right)^2 + 2q I_c^{1/2,1} = S_v (2\beta)^2$$

$$S_{IN} = \frac{4kT r_{bb,n} g_{m1}^2}{(2\beta)^2} + \frac{4q I_B \beta^2}{(2\beta)^2} + \frac{4q I_B \left(\frac{g_{m1}}{g_{m3}} \right)^2}{(2\beta)^2} + \frac{8q I_c}{4\beta^2} \Rightarrow S_I = q I_B$$

SIZING



$$\begin{cases} S_v = 8kT \left(r_{bb,n} + \frac{1}{g_{m1}} \right) < (S_v N / \sqrt{N})^2 \\ S_I = 4q I_B < (2\beta N / \sqrt{N})^2 \end{cases} \Rightarrow \text{SET a min } g_{m1} \quad (\text{Trade-off between Noise and } R_{in})$$

* choose $g_{m1} \rightarrow I$

$$\{ G = G_1 \cdot G_2 > 80dB \Rightarrow g_{m1} \cdot r_{T6} \cdot g_{m6} (r_{o6} \parallel r_{o7}) \Rightarrow \text{SET } g_{m6} \rightarrow I_6 \quad (!! g_{m6} < g_{m1} \text{ NEEDED} \Rightarrow \text{BALANCE}) \}$$

\Rightarrow All current and g_{m1} and r_o SET.

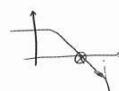
* Derive C_T , C_{ph} and find a compensation

→ Miller

$$\begin{cases} f_T = \frac{1}{2\pi (R_{in} + R_o) C_T (1 + \beta)} \\ f_{z1} = \frac{g_{m1}}{2\pi C_T (1 + \beta)} \\ f_{z2} = \frac{g_{m6}}{2\pi C_T} \end{cases} \Rightarrow f_{z1} < f_{z2} \Rightarrow \text{! NOTE}$$

NUCLEAR RESISTANCE

$$\begin{cases} f_{z1} = \text{Same} \\ f_{z2} = \frac{g_{m6}}{2\pi C_T (1 + \beta)} \\ f_{z3} = \frac{1}{2\pi C_T} \\ f_{z4} = \frac{1}{2\pi C_T (1 + \frac{1}{g_{m6}})} \Rightarrow \text{SET } f_{z3} = f_{z4} = 66\mu\text{P} \\ f_{BBNP} = \frac{g_{m6}}{2\pi C_T} \end{cases}$$



Wilson's mirror. (L05B_15)

In a bipolar OTA, we could start with the same input differential MOSFET stage, but then we will occur in a trade-off. The input resistance (that a MOSFET has infinite because of the gate) is finite, of $2R_{pi}$. Since R_{pi} is proportional to beta, we would like to have a npn as an input stage.

In trade off with this requirement, there's the CMRR that, in this case, is the mirror error, since the current bias needed is $2/\beta$. So, also in this case, we would like to have a npn mirror to decrease the error. Having input bjt and mirror as npn, keeping the output node with an high impedance, means that we should add a current buffer in between.

Now we encounter another problem: A bjt should have a base current to be biased, not a voltage. We then have to build a feedback network to bias it properly. (if we bias with voltage, the current will change as e^{-V_b})

If we decide to bias with a normal current generator, we have a problem that beta is found after the fabrication and the current won't be decided by us but by variability fabrication. We build a feedback in order to have a stable current in our brench with a small error:

$$G = \frac{A}{1+AF} \Rightarrow dG = \frac{dG}{dA} + \frac{dG}{dF} \Rightarrow dG = \frac{dA}{(1+AF)^2} - \frac{A^2}{(1+AF)^2} dF$$

$$\begin{cases} \frac{dG}{dA} = \frac{1}{(1+AF)^2} - FA \\ \frac{dG}{dF} = \frac{-A^2}{(1+AF)^2} \end{cases}$$

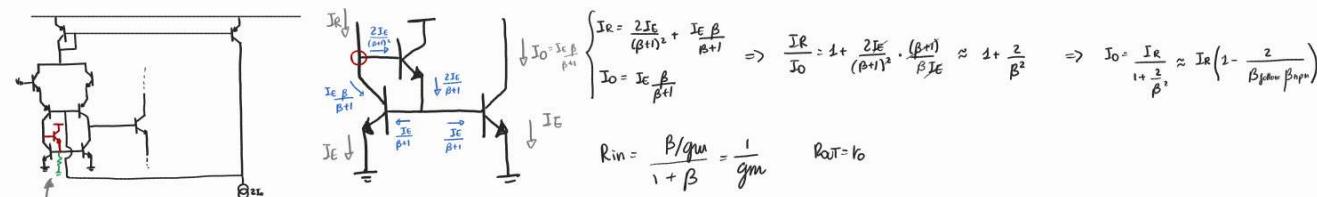
$$\frac{dG}{G} = \frac{dA}{(1+AF)^2} - \frac{A^2}{(1+AF)^2} dF \approx \frac{dA}{A(1+AF)} - \frac{A}{(1+AF)} dF \approx \frac{dA}{A(1+AF)} - \frac{dF}{F}$$

Feedback!

$$\frac{dI_L}{I_L} = \frac{d((\beta_{p+1}) d_n)}{\beta_{p+1}} \frac{d\beta_p}{\beta_p} \frac{1}{1+AF} - \frac{d(\frac{2}{\beta_p})}{d\beta_p} \frac{d\beta_p}{\beta_p} = \frac{\frac{2}{\beta_p} \frac{1}{1+AF}}{\frac{2}{\beta_p} + \frac{2}{\beta_p} \frac{1}{1+AF}} = \frac{\frac{2}{\beta_p}}{\frac{2}{\beta_p} + \frac{2}{\beta_p} \frac{1}{1+AF}} = \frac{1}{1+\frac{1}{1+AF}}$$

The same issue can be also solved with a Darlington stage using pnp as input stage, without the need of this feedback brench. The drawback of the Darlington is the input noise amplified by B^2 .

Once we set the current buffer, we may decide to improve also the CMRR because the mirror error is still degrading it. To improve it, we have at least two solutions: using a mirror with an emitter follower or a Wilson's mirror. Let's analyse the first solution.



Since the current is very low, there's a risk of β_{p+1} The bleeding resistance offer an alternative path and help to maintain the desired current (Note V_{BE} is fixed 0.7V) (We fix R_B in order to have the right amount of current)

$$I_R = \frac{2I_E}{(\beta_{p+1})^2} + \frac{I_E \beta}{\beta+1} \Rightarrow \frac{I_R}{I_E} = 1 + \frac{2I_E}{(\beta_{p+1})^2} \cdot \frac{(\beta+1)}{\beta_{p+1}} = \frac{\frac{\beta}{\beta+1} + \frac{\beta}{(\beta+1)^2}}{\frac{1}{\beta_{p+1}} + \frac{1}{\beta_{p+1}(\beta+1)} + \frac{\beta}{\beta_{p+1}}} = \frac{\beta(\beta+1) + \beta}{\beta^2 + 2\beta + 2} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$$



Let's now analyse a Wilson's Mirror:

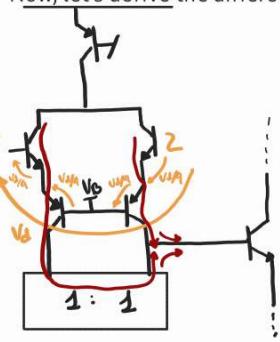
$$I_R = \frac{2I_E}{(\beta_{p+1})^2} + \frac{I_E \beta}{\beta+1} \Rightarrow \frac{I_R}{I_E} = 1 + \frac{2I_E}{(\beta_{p+1})^2} \cdot \frac{(\beta+1)}{\beta_{p+1}} = \frac{\frac{\beta}{\beta+1} + \frac{\beta}{(\beta+1)^2}}{\frac{1}{\beta_{p+1}} + \frac{1}{\beta_{p+1}(\beta+1)} + \frac{\beta}{\beta_{p+1}}} = \frac{\beta(\beta+1) + \beta}{\beta^2 + 2\beta + 2} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$$

$$R_{in} = \frac{2\beta}{gm} // R_o = \frac{2\beta}{\beta} = \frac{2}{gm}$$

$$R_{out} = \frac{\beta R_o}{2} \quad (\text{with } V_{BE})$$

$$\text{Otherwise } \left(\frac{1}{gm} + \frac{1}{\beta}\right) \approx \frac{1}{gm} \approx \frac{1}{\beta}$$

Now, let's derive the differential gain and the output resistance:

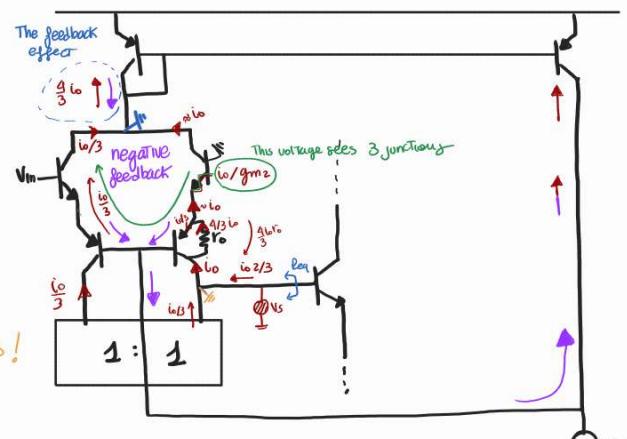


$$I_{out} = 2 \cdot \frac{V_o}{4} \cdot R_{in}$$

$$R_{in} = \frac{1}{gm} + \frac{1}{\beta} \approx \frac{1}{gm}$$

$$R_{in} = \frac{V_o}{2I_o} = \frac{4}{2} \frac{V_o}{I_o} = 2R_o$$

$$\text{The common mode feedback won't affect } R_{in} \text{ but stabilize } \Delta\beta \text{ in AC!}$$



21. uA741 second stage. Setting the bias: trade-off between gain and input impedance. Frequency response. (L06B_15)

After the single differential stage, we need to add a second stage that gain. The uA741 is designed to have a resistive load, so after a gain transistor, we place an emitter follower as a buffer, in order to have a low resistance output.

The second gain is given by $gm_{11} \cdot Rout_1$

$$G_2 = gm_{11} \cdot R_{out_1} = gm_{11} \beta_{nph} R_L \quad (\beta_{nph} R_L + \beta_{pnp} R_L \ll V_{DD} - V_{GS1}) \approx \beta_{nph} R_L$$

Since the gain depends on the load resistance, we should ask for a minimum one that the user shoud use.

$$G_2 = gm_{11} \cdot \beta_{nph} R_{L\min} \Rightarrow gm_{11} \geq \frac{G_2}{\beta_{nph} R_{L\min}} \quad gm_{11} \uparrow \leftrightarrow R_{in2} \downarrow \quad R_{in2} = \frac{\beta_{nph}}{gm_{11}}$$

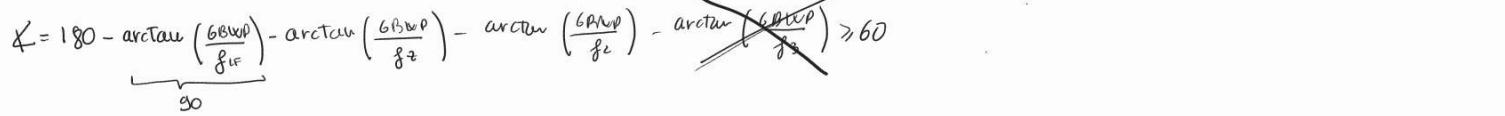
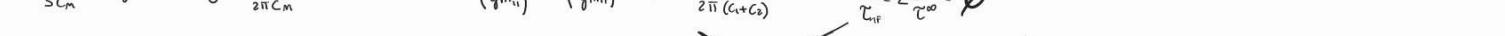
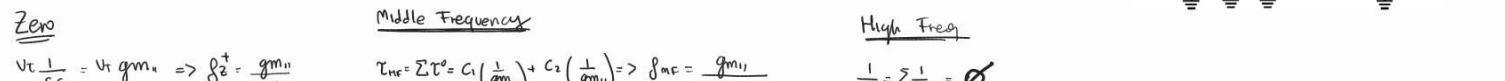
As we see, we end up with a minimum gm required, that may degrade Rin2. We should remember that in order not to degrade the gain of the first stage, we need to have $Rin2 > Rout_1$. Then we should add an emitter follower.

NB: We should also add a "bleeding resistance" in order to have bias properly Q11 and avoid Q10 operating in low injection regime. We also achieve an important result: we reach the symmetry of (B) and (A)!

Placing an emitter follower degrades the gain a little bit (0.9) but it's needed for the input resistance.

Now we check the frequency response of the circuit. Since we have two high impedance nodes (A) and (C), we expect to have two main pole in the transfer function. $C_a = C_{coll-sub(4-9)}$ (not Q10 because follower and the voltage across the capacitor is constant) and $C_c = C_{mu(11)}$. Since both the capacitors and the resistances they see are in the same order of magnitude, a compensation is needed.

We place the compensation capacitance C between node (A) and (C). In this case the Miller compensation is fine because we had to increase the current of the second stage to fulfill the gain.

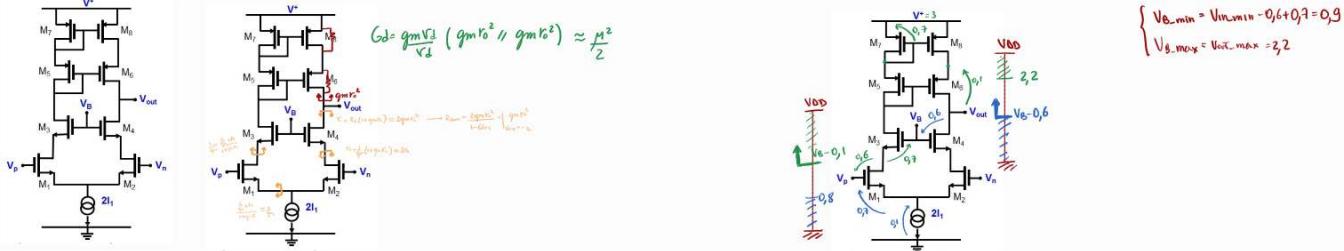


$$\begin{aligned} G_1 &= \frac{gm_{11}}{4} \cdot 2 \cdot 2R_0 = gm_{11}R_0 \\ G_2 &= gm_{11} \beta_{nph} R_L \end{aligned} \quad \left\{ \begin{array}{l} G_{tot} = gm_{11}R_0 gm_{11} \beta_{nph} R_L \Rightarrow GBWIP = \frac{gm_{11}/2}{2\pi C_m} \\ f_{Miller} = \frac{1}{2\pi C_m 2R_0 \cdot gm_{11} \beta_{nph} R_L} \end{array} \right.$$

22. Single-stage CMOS OTAs: telescopic cascode topology, differential gain, input and output voltage swing, power dissipation, frequency response.
 (LEZ 20, L07_19, ESE 14) 🎉

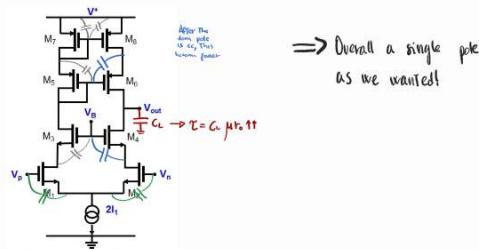
The main problem of a two stage amplifier, even if it has beautiful performance, is the need for compensation. We try now to find a way to elaborate a single stage amplifier so that we have just a single dominant pole and the speed of it is increasing, in trade off, maybe, with other performances. The first configuration we finds, comes from the natural flow of implementing the first stage of the two stage amplifier. Our major issue, is to reach the proper gain, and to do so, we implement Rout with two cascode stage, one on top of the mirror, with an additional mirror, and one with a common gate on the bottom. (We need two cascodes because Rout is given by R_{top}/R_{bottom} and we need to improve both in order to see the result on the output). This improvement gives birth to the Telescopic cascode amplifier.

Let's calculate the overall R_{out} and then we will try to catch the CONS of this config:



As we saw, the gain is large enough, but the real "issue" is the input and output swing (that is caused by the series of many transistors), since the upper voltage input and the lower voltage output both depends on V_b . This configuration works quite well in an inverting configuration with feedback, but for buffers or other, the performance are very poor.

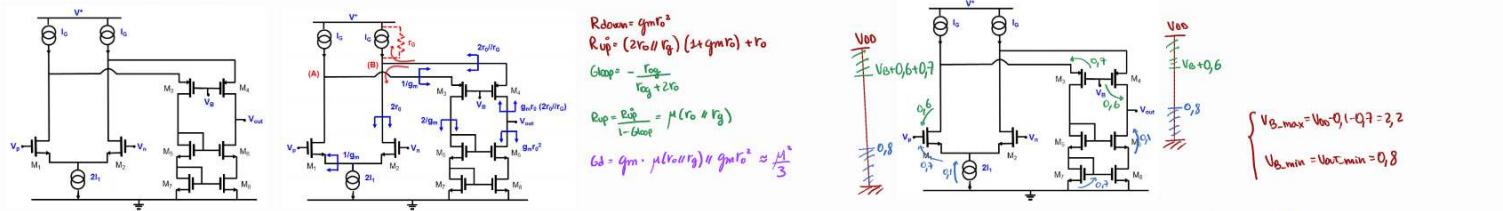
Let's now look at the frequency response:



23. Folded cascode topology, enhanced mirrors, voltage dynamics, power dissipation. Folded cascode with bipolar transistors. Feed-forward compensation. (LEZ 20, L07_19, ESE 14)

Since the telescopic cascode has a poor dynamics, we now look for a config with a larger swing. We change the configuration using pmos, giving birth to the Folded Cascode Amplifier.

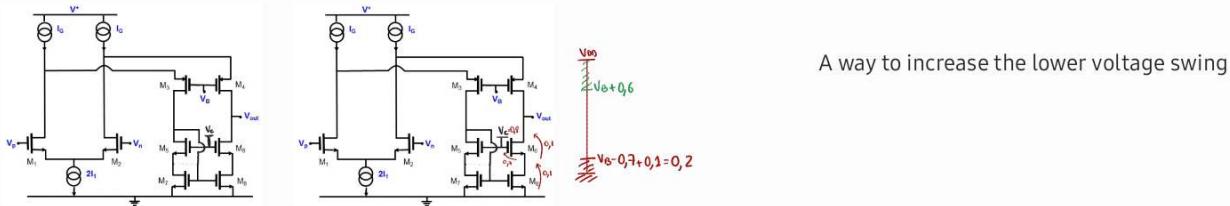
Let's see if it still has an high gain and how the voltage swing changed:



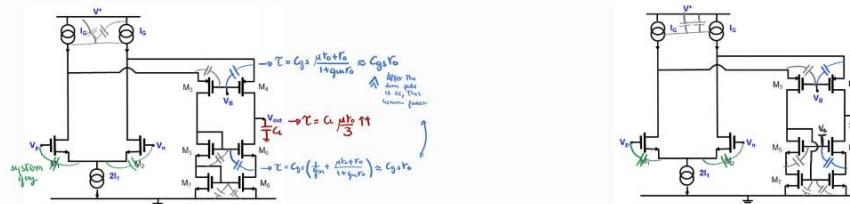
As we can see, the voltage range improved a lot, but we payed for power consumption: now we have two different branches that dissipate!! We can easily evaluate that the power consumption is at least twice as the telescopic ($2 \times 2I$) because the second branch needs at least the same current of the first one, here's why: considering the case where $V_{cm} \gg$ and all the current of the first stage flows in $M1$, we would first switch off $M3$ and then require current from it in opposite direction! Since this case is not possible, $M1$ enters in ohmic region to let less current and the node (A) will go down. In case we change the input again, in order to have a functional circuit, we have to wait a certain amount of time to let $M1$ re-enter in the saturation region and to fix the potential of (A) to have a proper output. Not to have this, we want that $Ig + I2 \geq 2I$, so $I2$ is at least equal to $I1$.

Apart from this lost in performance in power dissipation, this folded stage works well, but we can improve the voltage swing even more!

We can add an additional reference voltage so that $M7$ and $M8$ works with the minimum Vds and the source potential of $M5$ and $M6$ is even lower. We call this configuration Folded Stage with Enhanced Mirror or simply the Enhanced Mirror Stage:



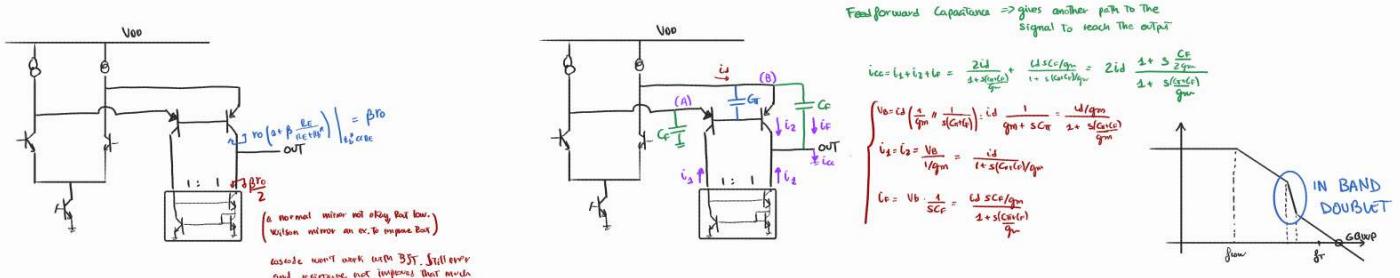
For both these two configurations, we can study the frequency response. Taking to account a capacitive load CL , we can evaluate the poles in DC given by all the capacitors.



From this fast deduction, we can expect that these configurations have just a single pole due to the load capacitor and the other C_{gs} capacitors, once the load is short circuited, give a pole contribution very far away. We will see that this won't happen in the bjt configurations.

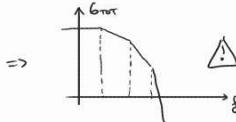
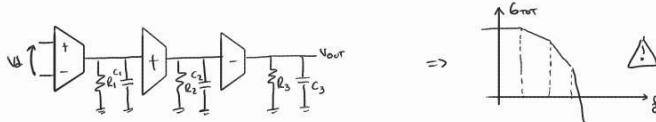
Let's now derive the Folded Cascode with BJT.

The output resistance can be derived easily, but now we encounter a big problem! Since the cut frequency of pnp is quite low, it may happen that $f_T < GBWP$ and in that case, our amplifier won't work anymore. That's why we need to introduce the Feedforward Compensation

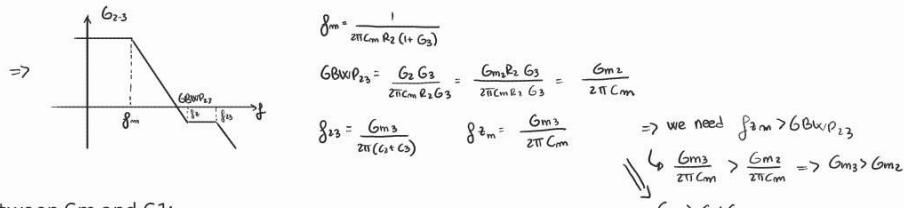
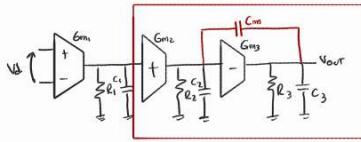


24. Three-stage CMOS OTA: Nested Miller Compensation (L08_23)

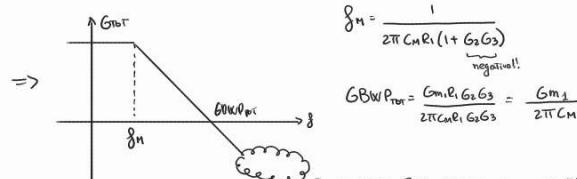
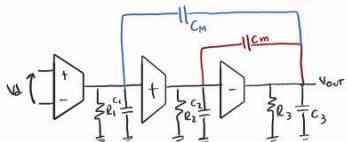
For some application we need very high gain (120dB) and as the supply voltage decrease (tech scales down), we cannot use cascode structure because of the limited voltage range. The other solution is to add another stage to gain. Three stages means three node with high impedance ad a required compensation. As we will see later, the first stage has to be differential, the second one non inverting and the third one inverting.



We start from the usual Miller Compensation only considering the second and third stage:



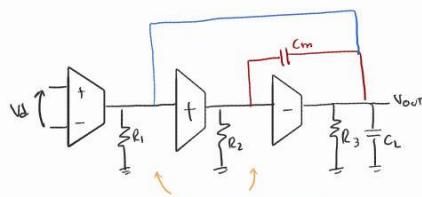
Now we use another Miller compensation between Cm and C1:



SIZING EX:

$$\begin{aligned} \text{GBWP} = \frac{Gm_2}{2\pi f} &= 10 \text{ GBWP} \Rightarrow Gm_2 = 1,6 \text{ mA/V} \\ C_L = S_p F & \\ Gm_2 = Gm_3 / 5 &= 0,5 \text{ mA/V} \\ \text{GBWP} = \frac{Gm_2}{2\pi f_m} &= 2 \text{ GBWP} = \frac{Gm_2}{2\pi f_m} \Rightarrow C_m = S_p F \\ \text{GBWP} = \frac{Gm_2}{2\pi f_m} &\rightarrow Gm_2 \text{ set by the noise } (Gm_2 > 1,3 \text{ mA/V}) \\ &\rightarrow C_m = \frac{Gm_2}{2\pi f_m} = 48 \text{ pF} \end{aligned}$$

Now we derive the whole transfer function with the time constant method:



$$\begin{aligned} T(s) &= T(\omega) \frac{s^2 a_2 + s a_1 + 1}{(s + s_1)(s^2 b_2 + s b_1 + 1)} \\ b_1 &= C_m R_m^{(o)} + C_L R_L^{(o)} = C_m \frac{Gm_2 Gm_3}{Gm_2 Gm_3} + C_L \frac{1}{Gm_2 Gm_3 R_2} \approx C_m \frac{Gm_2 - Gm_3}{Gm_2 Gm_3} \\ b_2 &= C_m C_L R_m^{(o)} R_L^{(o)} = C_m C_L \frac{Gm_2 Gm_3}{Gm_2 Gm_3} \frac{1}{Gm_2 Gm_3} = \frac{C_m C_L}{Gm_2 Gm_3} \end{aligned}$$

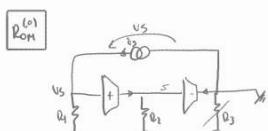
=> (check if complex con) ---)



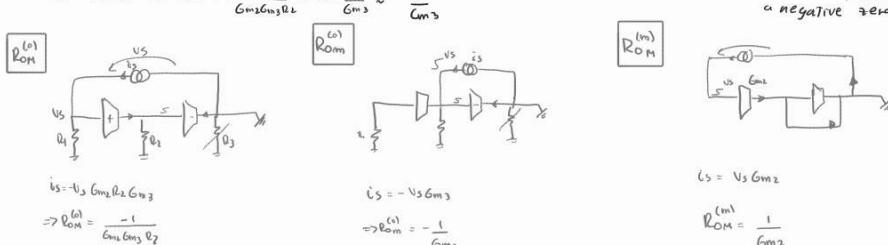
$$\begin{aligned} i_S &= V_{S2} Gm_2 Gm_3 + \frac{V_S}{R_1} + \frac{V_S}{R_2} \\ R_L^{(o)} &= \frac{V_S}{i_S} \approx \frac{1}{Gm_2 Gm_3} \\ i_S &= V_{S2} - V_S \\ i_S &= \frac{V_S}{R_2} + V_S Gm_3 \approx V_S Gm_3 \rightarrow V_S = \frac{i_S}{Gm_3} \\ i_S &= \frac{V_S}{R_2} + V_S Gm_2 \approx V_S Gm_2 \rightarrow V_S = \frac{i_S}{Gm_2} \\ V_S &= V_{S2} - i_S \left(\frac{1}{Gm_2} - \frac{1}{Gm_3} \right) \Rightarrow \frac{V_S}{i_S} = \left(\frac{1}{Gm_2} - \frac{1}{Gm_3} \right) = \frac{Gm_3 - Gm_2}{Gm_2 Gm_3} \end{aligned}$$

$$\begin{aligned} a_2 &= C_m C_m R_m^{(o)} R_L^{(o)} = C_m C_m \frac{-1}{Gm_2 Gm_3 R_2} \cdot \frac{1}{Gm_2} \approx -\frac{C_m C_m}{Gm_2 Gm_3} \\ a_1 &= C_m R_m^{(o)} + C_m R_L^{(o)} = C_m \frac{-1}{Gm_2 Gm_3 R_2} + C_m \frac{-1}{Gm_3} \approx -\frac{C_m}{Gm_3} \end{aligned}$$

=> $s^2(a_2) - s |a_1| s + 1 = 0$ \rightarrow Because of the signs, we will have a positive and a negative zero!!



$$\begin{aligned} i_S &= V_{S2} Gm_2 Gm_3 \\ R_{OM}^{(o)} &= \frac{-1}{Gm_2 Gm_3 V_2} \end{aligned}$$



$$\begin{aligned} i_S &= V_{S2} Gm_3 \\ R_{OM}^{(o)} &= -\frac{1}{Gm_3} \end{aligned}$$

$$R_{OM}^{(o)} = \frac{1}{Gm_2}$$

25. OTA Linear response. In-band zero-pole doublets and features of the settling response. (LEZ 21, L09_21)

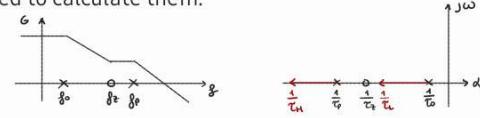
In Analog Circuit Design, in-band zero-pole doublets refer to a pair of closely located zeros and poles in the frequency response of our interest (before GBWP). These can derive from an error in a slightly different value of C_{load} that can lead to a split of a perfect zero-pole cancellation or from a feed-forward compensation. We can devide the study in two cases: the zero comes before or after the pole of the doublet. At first impact we may say that, since they are very close, their effect nearly cancel out in the magnitude response and the gain has a minimal alteration, not giving any issues, but it actually degrades the transient response of the circuit.

Let's first study the case of pole-zero-pole:

The transfer function of an amplifier with two poles and a zero can be written as (a), with a closed loop transfer function as (b), and as we know, the zero of the open and closed loop are the same, but the poles will vary and we need to calculate them.

$$(a) \quad A(s) = \frac{A_0(1+sT_z)}{(1+sT_u)(1+sT_p)}$$

$$(b) \quad H(s) = \frac{A(s)}{1+A(s)} = \frac{\frac{A_0(1+sT_z)}{(1+sT_u)(1+sT_p)}}{\frac{(1+sT_u)(1+sT_p) + A_0(1+sT_z)}{(1+sT_u)(1+sT_p)}} \Rightarrow \frac{(1+sT_z)}{(1+sT_u)(1+sT_p)}$$



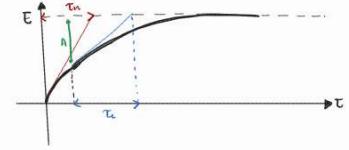
The root locus will help us to see the relative position of the new poles. As the Gloop increase, the low frequency pole will approach the zero, while the high frequency one will move approaching GBWP. From this we can see that if the doublet is at low frequency, with the right gain, we will have a pole of the close loop at the frequency of the zero. We have to figure out whenever we prefer the doublet at low or high frequency and its relative effect on the transient.



Let's now study the response of this stage to a step function E . In Laplace domain we can write:

$$V_{out}(s) = \frac{E}{s} \left[\frac{(1+sT_z)}{(1+sT_u)(1+sT_p)} \right] = \frac{E}{s} \left[\frac{A}{1+sT_u} + \frac{B}{1+sT_p} \right] = \frac{E}{s} \left[A(1-e^{-T_u}) + B(1-e^{-T_p}) \right] = \begin{cases} \frac{E}{s} \left[1 - A e^{-T_u} - B e^{-T_p} \right] \\ \text{FAST EXP + SLOW EXP} \end{cases}$$

$$\left\{ \begin{array}{l} \lim_{s \rightarrow -1/T_u} \frac{A(1+sT_z)}{(1+sT_u)(1+sT_p)} = A \\ \lim_{s \rightarrow -1/T_p} \frac{B(1+sT_z)}{(1+sT_u)(1+sT_p)} = B \end{array} \right. \quad \left\{ \begin{array}{l} \lim_{s \rightarrow -1/T_u} \frac{A(1+sT_z)}{(1+sT_u)(1+sT_p)} = \frac{A(1-sT_u)}{(1-sT_u)(1+sT_p)} = \frac{T_u}{T_u - T_p} \\ \lim_{s \rightarrow -1/T_p} \frac{B(1+sT_z)}{(1+sT_u)(1+sT_p)} = \frac{B(1-sT_p)}{(1-sT_u)(1+sT_p)} = \frac{T_p}{T_u - T_p} \end{array} \right. \Rightarrow A:B = 1:1$$



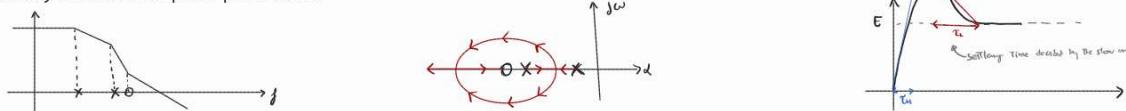
Now we want to estimate the two poles:

$$H(s) = \frac{A(s)}{1+A(s)} = \frac{A_0(1+sT_z)}{(1+sT_u)(1+sT_p) + A_0(1+sT_z)} \Rightarrow s^2 T_u T_p + s(T_u + T_p + A_0 T_z) + A_0 + 1 = 0 \Rightarrow \begin{cases} p_u = -\frac{1}{T_u} = -\frac{c}{b} = -\frac{A_0 + 1}{T_u + T_p + A_0 T_z} \approx -\frac{1}{T_u + \frac{T_p}{A_0}} \\ p_p = -\frac{1}{T_p} = -\frac{b}{a} = -\frac{T_u + A_0 T_z}{T_u T_p} \approx -\frac{A_0 T_z}{T_u T_p} \end{cases} \quad \begin{cases} T_u \approx T_p + \frac{T_p}{A_0} \\ T_p \approx \frac{T_u T_p}{A_0 T_z} \approx \frac{T_u}{A_0} \end{cases} \Rightarrow A = \frac{T_u - T_p}{T_u - T_p} \approx \frac{T_u/A_0}{T_p/A_0} = \frac{1}{GBWP}$$

At first, we may say that we want $f_z \ll GBWP$ so that A is high and the fast pole covers the majority of the exponential, but if we think twice, we notice that the slow pole has a proportional dependency with f_z , so if we try to increase the velocity of the fast pole, we slow down the slow one! Overall we will have a worse solution! (also because due to fab errors, A may appear bigger than expected and the slow pole not be so marginal)

We find out that it's actually better to have an high frequency zero pole so that the fast pole covers a small portion of the exponential (but still quite fast) and the slow pole, overall, not so slow.

Let's now study the case of pole-pole-zero:

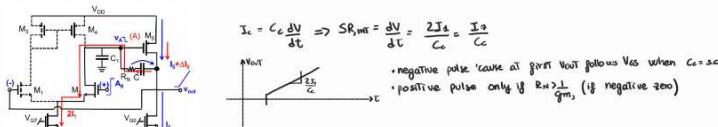


N.B.: per T_{min} A↑ e alta sonodragnazione, può esplodere tutto. Non sempre il sistema può essere fatto per ottimizzare la velocità.

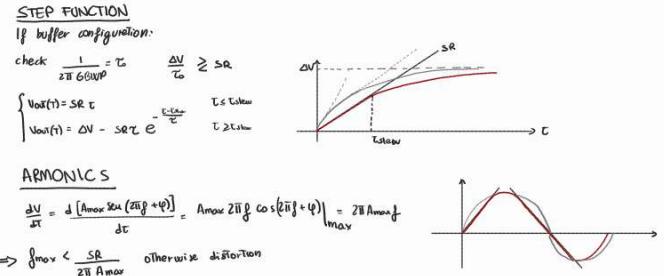
Now as A_0 increase, the poles become complex conjugate. For large values of A_0 , the poles become real again. The response of the sistem has an overshoot whose amplitude depends on the distance between the pole and the zero of the doublet (since the position is not so precise, you should avoid this config). The system will settle down with the slow pole, so, once again, we want the slow pole to be faster as possible, with a f_z at high frequency

26. The slew rate limit. Impact on settling time. CMOS-OTA: Internal and external slew rate limits. Improving SR with class AB output stages. (LEZ 22, L09_21, ESE 13) 

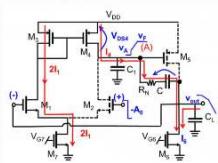
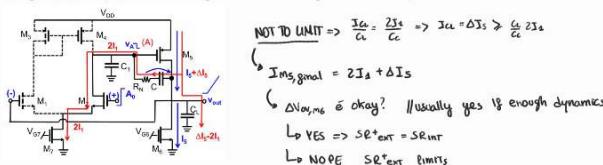
For what concern the time response of a real amplifier, we should take into account, in addition to doublets, the slew rate. The slew rate describes how quickly the output node can vary in response to a rapid change of the input. Let's study the SR of a CMOS-OTA, considering first the internal slew rate and then how the external slew rate should be in order not to limit the circuit performance. The internal slew rate is related to the first stage and the maximum current it can provide to charge the capacitors. We can study separately the upper and lower SR (even if they are the same for a standard OTA due to the symmetry of the differential stage). Imaging a large positive input, the situation is the one in figure:



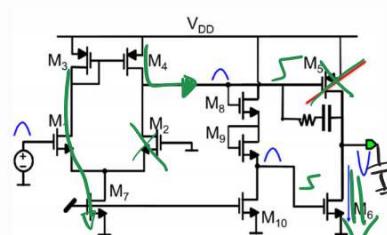
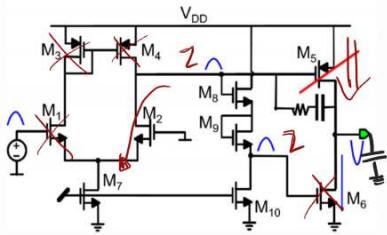
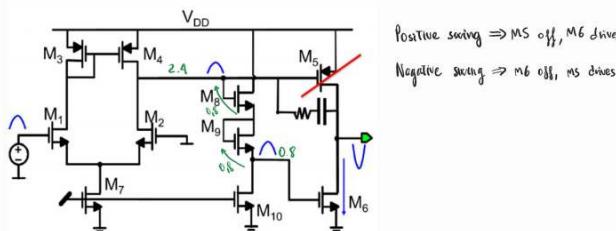
$$SR = 2\pi f_{max} G_{BWP}$$



The external slew rate upper and bottom are very different. Let's focus on the one that doesn't give problems first: positive swing when the second stage is p-type (or negative swing with n-type). On the side the one that may give issues.



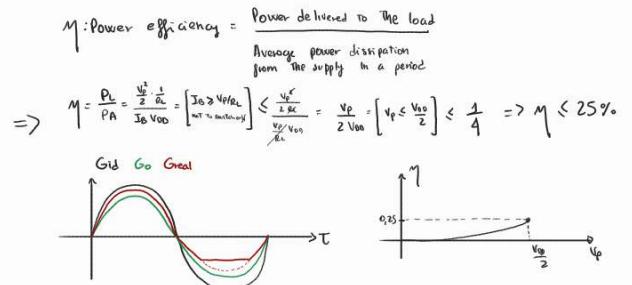
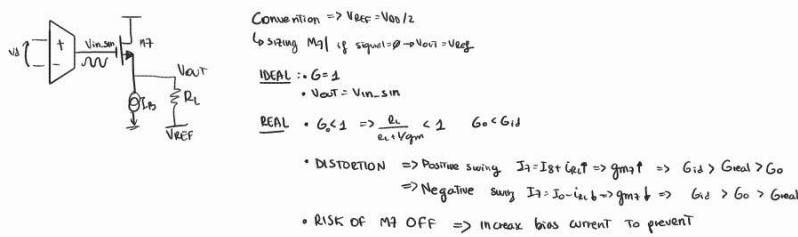
If we want to have a better external SR, we may build an AB circuit that raise the current of M6 only on negative swings (power consumption!):



27. Output stages: Emitter follower as output stage. Emitter follower efficiency. Push-pull. Efficiency. Cross-over distortion. Class A-B stage. Total harmonic distortion. Distortion reduction by feedback. (L11_21)

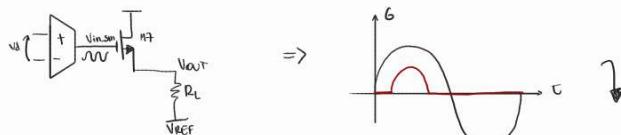
When we have a resistive load, our OTA cannot be used! This is due to the fact that the OTA has a high impedance not ad connecting it to a low resistive load will degrade the gain. We should add an additional stage to decouple the gain and the output. The first configuration we can think about is a simple source follower.

CLASS A - Source Follower



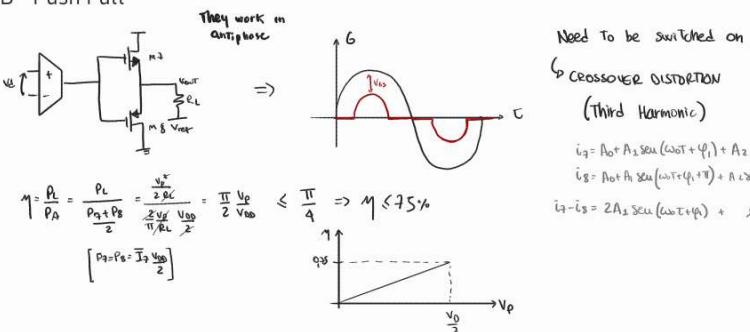
Thinking a way to reduce the static power to improve power efficiency is to use a ideal source follower.

CLASS B - Ideal Source Follower



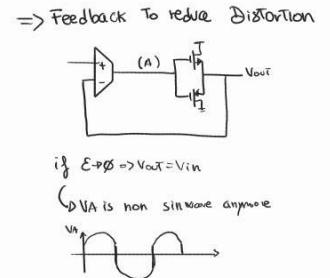
We noticed that we need to add a transistor switching on for negative swing:

CLASS B - Push Pull



\hookrightarrow CROSSOVER DISTORTION (Third Harmonic)

 $i_3 = I_{D1} + A_1 \sin(\omega_0 t + \varphi_1) + A_2 \sin(2\omega_0 t + \varphi_2) + A_3 \sin(3\omega_0 t + \varphi_3) + \dots$
 $i_8 = A_1 \sin(\omega_0 t + \varphi_1) + A_2 \sin(2(\omega_0 t + \pi) + \varphi_2) + A_3 \sin(3(\omega_0 t + \pi) + \varphi_3) + \dots$
 $i_2 - i_3 = 2A_1 \sin(\omega_0 t + \varphi_1) + \underbrace{A_2 \sin(2\omega_0 t + \varphi_2)}_{3^{rd} \text{ Harmonic Distortion}}$

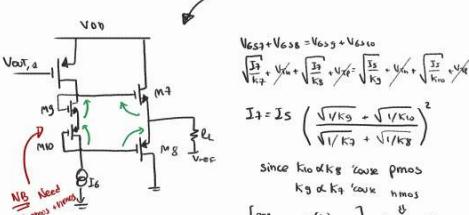
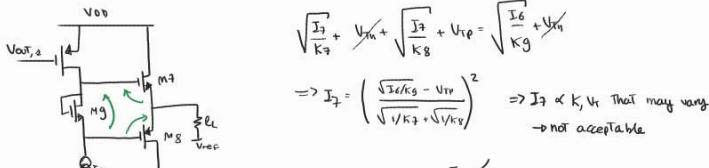


DISTORTION

Total Harmonic Distortion (THD) $= \sqrt{D_2^2 + D_3^2 + D_4^2 + \dots}$
 $= \sqrt{\frac{A_2^2}{A_1^2} + \frac{A_3^2}{A_1^2} + \frac{A_4^2}{A_1^2} + \dots}$

The crossover distortion is due to the fact that the mosfet are not biased yet. We can implement the circuit in order to have a almost on mosfet.

CLASS AB - AB stage

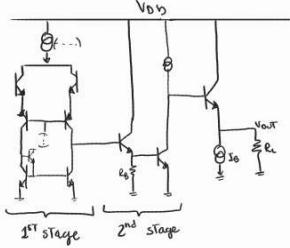


Transistor biasing

28. Output stages in bipolar technology (uA741). Short-circuit protections. (no file :() 🥰

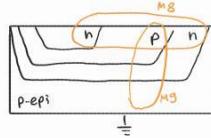
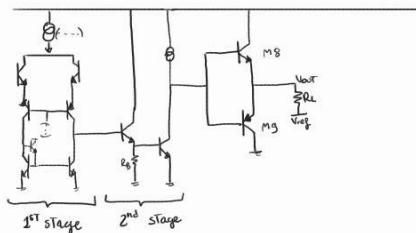
Let's start with the same idea of MOSFET:

CLASS A - Source Follower



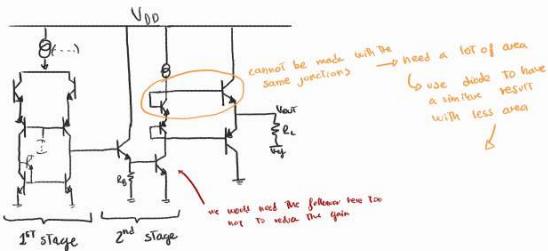
Being a Class A, we already saw that the power consumption is way too much, giving a low power efficiency. We adopt the second idea with push-pull

CLASS B - Push Pull

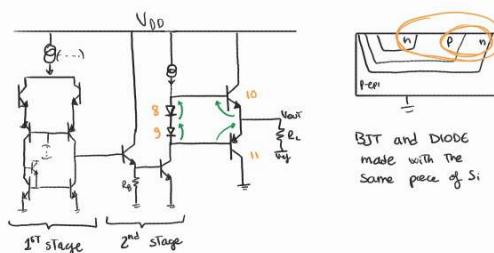


(we can add a follower not to have the 2nd harmonic)
 DISTORTION → 2nd Harmonic because $f_{ppm} \neq f_{pm}$ (That we didn't have with mosfet)
 → Main 3rd Harmonic → Need to reach $V_{BE} = V_{Bext}$
 ↳ CLASS AB

CLASS AB - Transdiode



CLASS AB - Diode



$$\begin{cases} V_{BS} + V_{OD} = V_{BE10} + V_{BE10} \\ I = I_S e^{\frac{qV_{BE}}{kT}} \Rightarrow V_{BE} = \frac{kT}{q} \ln \frac{I}{I_S} \end{cases}$$

$$\Rightarrow \frac{\ln \frac{I_2}{I_{S2}} + \ln \frac{I_2}{I_{S2}}}{I_{S2} I_{S2}} = \frac{\ln \frac{I_{10}}{I_{S10}} + \ln \frac{I_{10}}{I_{S10}}}{I_{S10} I_{S10}}$$

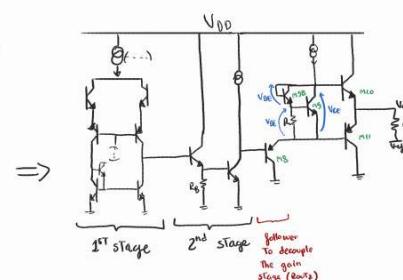
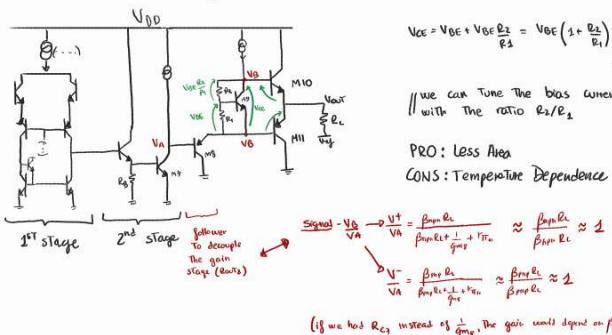
$$\Rightarrow \frac{\frac{I_2}{I_{S2}}}{I_{S2} I_{S2}} = \frac{\frac{I_{10}}{I_{S10}}}{I_{S10} I_{S10}} \Rightarrow \frac{I_{10}}{I_2} = \sqrt{\frac{I_{S10} I_{S10}}{I_{S2} I_{S2}}} \Rightarrow \frac{I_2}{I_8} = \sqrt{\frac{A_8 A_{10}}{A_8 A_8}}$$

We compensate Temperature shift! Good!

I_{10} and I_{S10} are already big To carry large signal.

If we want to reduce the bias current of Q_{10} or Q_{11} we would need a large diode → A lot of AREA (??)

CLASS AB - Vbe multiplier (to save area)

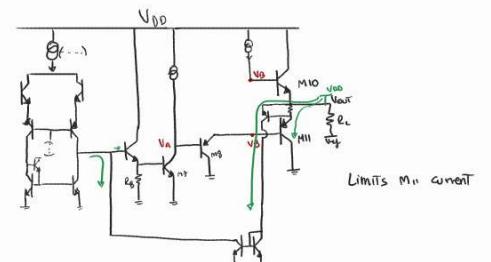
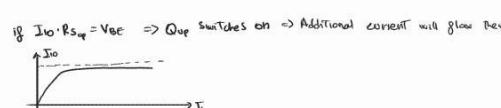
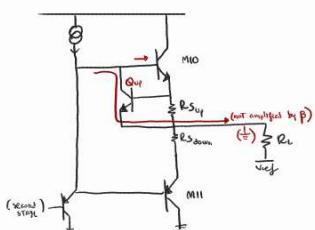


$V_{CE} \approx 2V_{BE}$
 ↳ Tuning R_2 , we can have $i_{B2} \ll i_B \Rightarrow V_{CE,20} < V_{CE,10}$

More strong against Temperature shift

CIRCUIT PROTECTION

Since the output node and the load is connected outside, we should consider some protection not to ruin Q_{10} and Q_{11}

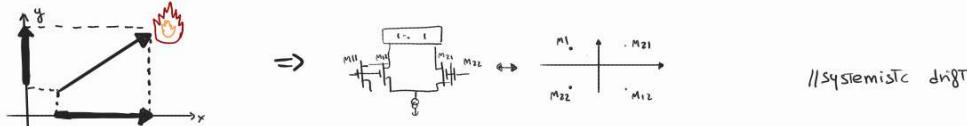


29. Variability and matching: Relative matching of threshold voltage values. Common centroid. Pelgrom's formula (L10_16)

In our circuits we have always taking in to account that pair of transistors (input, mirror) are identical. The truth is that there may be have some systematic errors and statistical errors.

Systematic error are caused by a gradient along a direction, for example, an hot spot of a circuit may cause a temperature gradient, a process production non uniformity may cause a gradien in tox,...

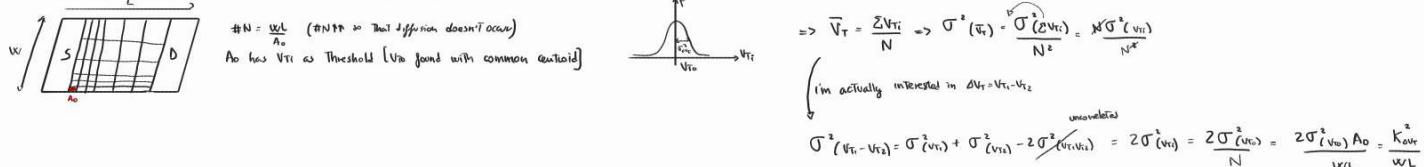
These systematic errors are solved with the common centroid technique: the gradient can be splitted in a gradient along x and a gradient along y. We can rearrange our devices in order to derive a mean value.



Statistical errors are caused by the fluctuation of some parameters in time and the fact that we cannot precisely calculate some parameters in each point, such as dopants. We have to use a statistical approach to study them and find its variance.

Taking a MOSFET, the statistical parameters that can fluctuate are the number of carriers (dopants) that cause a variation in the threshold and the mobility (and so k).

Let's study the statistical variation of the threshold first.



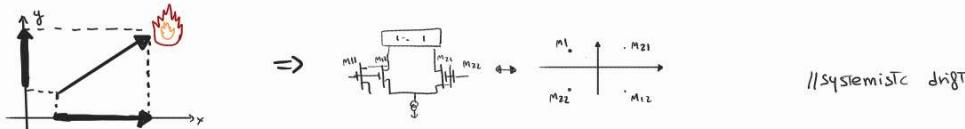
As we derived for V_t , the same calculation can be derived for k , finding an analog Pelgrom coefficient for it.

30. Variability and matching: Relative matching of resistors. Common centroid. Pelgrom's formula (L10_16)

In our circuits we have always taking in to account that pair of transistors (input, mirror) are identical. The truth is that there may be have some systematic errors and statistical errors.

Systematic error are caused by a gradient along a direction, for example, an hot spot of a circuit may cause a temperature gradient, a process production non uniformity may cause a gradien in tox,...

These systematic errors are solved with the common centroid technique: the gradient can be splitted in a gradient along x and a gradient along y. We can rearrange our devices in order to derive a mean value.



Statistical errors are caused by the fluctuation of some parameters in time and the fact that we cannot precisely calculate some parameters in each point, such as dopants. We have to use a statistical approach to study them and find its variance.

Let's now study the variability of a resistor affected by a fluctuation of temperature or dopants.

$$R = \frac{1}{\rho} \frac{L}{W} = \frac{1}{\rho_m \sigma_w} \frac{L}{W} = R_0 \frac{L}{w}$$

$$\delta R = dR_0 \frac{L}{w} + R_0 \frac{dL}{w} - R_0 \frac{L}{w} \delta w$$

$$\frac{dL}{L} = \frac{dR_0}{R_0} + \frac{dL}{L} - \frac{\delta w}{w}$$

$$R_{\text{tot}} = R_0 \frac{M}{N}$$

$$\left\{ \begin{array}{l} \sigma^2(\Delta R) = \sigma^2(2R_{\text{row}}) = M \sigma^2(\epsilon_{\text{row}}) \\ \sigma^2(\epsilon_{\text{row}}) = \frac{M \sigma^2(\epsilon_{\text{row}})}{(M R_{\text{row}})^2} = \frac{1}{M} \sigma^2(\epsilon_{\text{row}}) \end{array} \right. \quad \left\{ \begin{array}{l} \sigma^2(\epsilon_{\text{row}}) = \sigma^2(\epsilon_{\text{G}}) = N \sigma^2(\epsilon_0) \\ \sigma^2(\epsilon_{\text{G}}) = \frac{1}{N} \sigma^2(\epsilon_0) \end{array} \right.$$

$$\Rightarrow \left[\frac{\sigma^2(R_{\text{row}})}{R_{\text{row}}^2} = \frac{\sigma^2(\epsilon_{\text{row}})}{\epsilon_{\text{row}}^2} \right] \Rightarrow \frac{\sigma^2(\Delta R)}{R_{\text{tot}}^2} = \frac{1}{M} \cdot \frac{1}{N} \frac{\sigma^2(R_0)}{R_0^2} = \frac{R_0}{wL} \frac{\sigma^2(\epsilon_0)}{\epsilon_0^2}$$

(we are interested in $\Delta R = R_1 - R_2$)

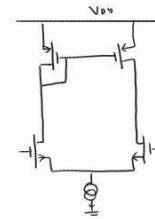
$$\frac{\sigma^2(\Delta R)}{R^2} = \left| \frac{2 \sigma^2(\epsilon_0)}{R^2} \right| = \frac{2 R_0 \sigma^2(\epsilon_0)}{wL R_0^2} = \frac{K_{\text{diff}}}{wL}$$

31. OTA: Offset. Deterministic and statistical contributions to input referred offset. Input referred offset in bipolar differential stages. Temperature effects. (L09B_19) 🎂

Let's analyse the differential input stage with MOSFET and derive how a mismatch of $V_{t,k}$ of input (mirror) pair of mosfet:

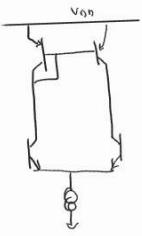
INPUT ΔV_T
$I_1 = k(V_{os} + \Delta V_T)^2 = kV_{os}^2 + k(\Delta V_T + 2\Delta V_T V_{os})$ $I_2 = k(V_{os})^2 = kV_{os}^2$ $\Delta I = I_1 - I_2 = k(\Delta V_T + 2\Delta V_T V_{os}) = 2kV_{os}\Delta V_T = g_m\Delta V_T$ $V_{os} = \frac{\Delta I}{g_m k}$ <i>if not balanced</i> $\sigma(V_{os}) = \sigma(\Delta V_T) = \frac{kV_{os}}{V_{os}}$

MIRROR ΔV_T
$I_3 = k(V_{os} + \Delta V_T)^2$ $I_A = kV_{os}^2$ $\Delta I = g_m\Delta V_T$ $V_{os} = \frac{\Delta I}{g_m k} = \frac{g_m}{g_m k} \Delta V_T = \frac{V_{os}}{V_{os}} \Delta V_T \Rightarrow \sigma(V_{os}) = \left(\frac{V_{os}}{V_{os}}\right) \sigma(\Delta V_T) = \frac{V_{os}}{V_{os}} \frac{K_{V_{os}}}{V_{os}}$



INPUT ΔK
$I_1 = (k + \Delta k)V_{os}^2$ $I_2 = kV_{os}^2$ $\Delta I = \Delta kV_{os}^2$ $V_{os} = \frac{\Delta I}{g_m k} = \frac{\Delta k V_{os}^2}{2k V_{os}^2} = \frac{\Delta k}{k} \frac{V_{os}^2}{2}$ $\sigma(V_{os}) = \frac{K_{\Delta k} k}{V_{os}^2} \frac{V_{os}}{2}$

MIRROR ΔK
$I_3 = (k + \Delta k)V_{os}^2$ $I_A = kV_{os}^2$ $\Delta I = \Delta kV_{os}^2$ $V_{os} = \frac{\Delta I}{g_m k} = \Delta k V_{os}^2 \cdot \frac{V_{os}}{2I_3} = \frac{\Delta k V_{os}^2 V_{os}}{2 \cdot k V_{os}^2} = \frac{\Delta k}{k} \frac{V_{os}}{2}$ $\sigma(V_{os}) = \frac{K_{\Delta k} k}{V_{os}^2} \frac{V_{os}}{2}$



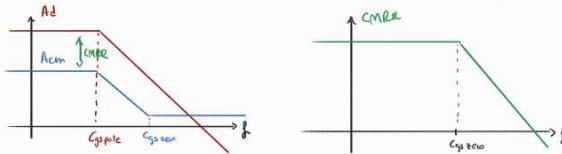
In BJT $I = I_s e^{\frac{qV_{BE}}{kT}}$ *statistic* $= q n_i^2 A_F e^{\frac{qV_{BE}}{kT}}$ \Rightarrow Temperature shift balanced with common centroid so the system work with the "same" temperature

INPUT
$I_1 = I_s e^{\frac{qV_{BE}}{kT}}$ $I_2 = I_s e^{\frac{qV_{BE}}{kT}}$ $\Delta I = I_1 - I_2 = I_s e^{\frac{qV_{BE}}{kT}} - I_s e^{\frac{qV_{BE}}{kT}} = I_s e^{\frac{qV_{BE}}{kT}} (1 - e^{-\frac{qV_{BE}}{kT}})$ $V_{os} = \frac{\Delta I}{g_m I_1} = \frac{I_s e^{\frac{qV_{BE}}{kT}}}{I_s} V_{th} = \frac{\Delta I_s}{I_s} V_{th}$

MIRROR
$I_3 = I_s e^{\frac{qV_{BE}}{kT}}$ $I_A = I_s$ $\Delta I = \Delta I_s e^{\frac{qV_{BE}}{kT}}$ $V_{os} = \frac{\Delta I_s}{I_s} V_{th}$

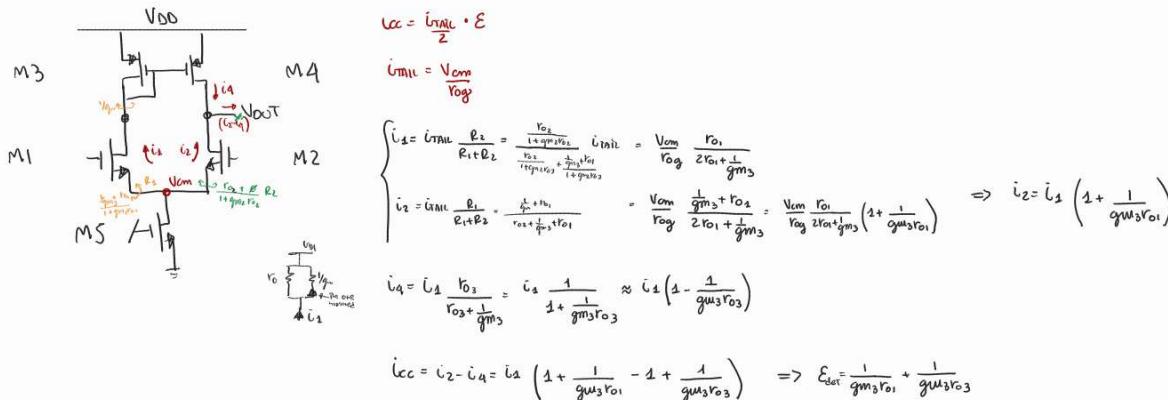
32. OTA: Common-mode rejection ratio. Deterministic and statistical limits to CMRR (L09B_19)

We have already derived (in DC) the value of an important parameter in our circuit: the CMRR. The Common Mode Rejection Ratio is the ratio between the differential and the common mode gain and it's important because an high CMRR means a good signal accuracy and a rejection of DC noise. Until now we have taken into account the DC value, but we should take into account that the common mode gain has a zero that the differential doesn't have, so at medium-high frequency, the CMRR drops down and may cause errors!

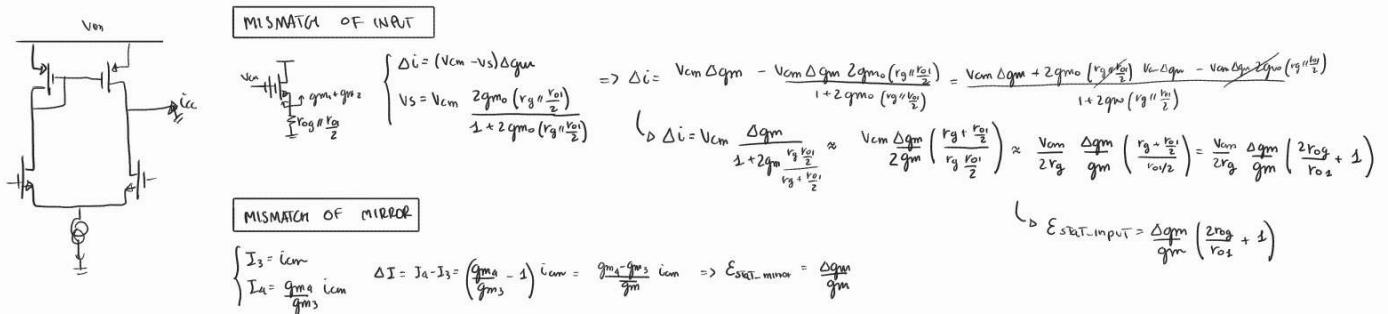


CMRR can be divided in the deterministic one and the statistical one.

The deterministic CMRR is due to the mirroring error and the difference of load seen by the input:



The statistical CMRR is due to the mismatch of mirrors and mismatch of inputs mosfet (gm):



Since the variation of gm is statistical, we should study its variance:

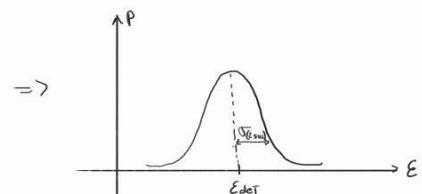
$$gm = 2k(V_{ds} - V_t)$$

$$\frac{\partial gm}{\partial V_t} = \frac{\partial gm}{\partial V_{ds}} \frac{\partial V_{ds}}{\partial V_t} + \frac{\partial gm}{\partial K} \Delta K = 2k \Delta V_t + 2V_{ds} \Delta K$$

$$\frac{\partial gm}{\partial K} = \frac{2k \Delta V_t}{2k V_{ds}} + \frac{2 \Delta K V_{ds}}{2k V_{ds}} = \frac{\Delta V_t}{V_{ds}} + \frac{\Delta K}{K}$$

$$\left(\sigma_{(gm/K)}^2 = \frac{\sigma_{(V_{ds})}^2}{V_{ds}^2} + \sigma_{(\Delta K)}^2 \right) \Rightarrow E_{stat} = \frac{\Delta gm}{gm} + \frac{\Delta gm}{gm_0} \left(\frac{2r_{og}}{r_{o1}} + 1 \right)$$

$$\sigma_{(E_{stat})}^2 = \underbrace{\sigma_{(\frac{gm}{gm_0})}^2}_{\text{mirror}} + \frac{\sigma_{(gm)}^2}{V_{ds}^2} + \left(\frac{2r_{og}}{r_{o1}} + 1 \right)^2 \left[\sigma_{(\frac{gm}{gm_0})}^2 + \frac{\sigma_{(gm)}^2}{V_{ds}^2} \right]$$



Thank God, that's all.