

# Lab 1

**Sara Frazer**

Oct 1, 2023

CDA3203 Computer Logic Design

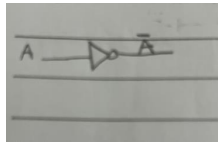
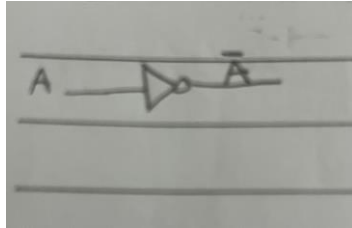
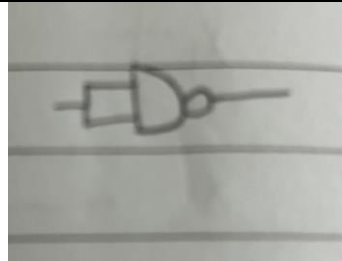
Fall 2023

Dr. Maria Petrie

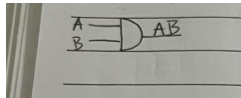
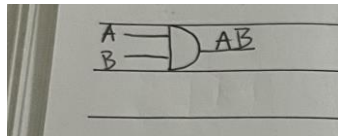
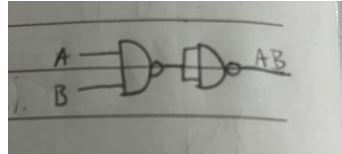
Florida Atlantic University

**Part 1:** Design 9 circuits by completing below: Draw the symbol for the gate, its Truth Table, its Simplest Sum of Products Expression, draw its NOT-AND-OR Equivalent Circuit, its all-NAND Equivalent Circuit.

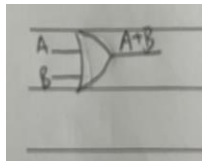
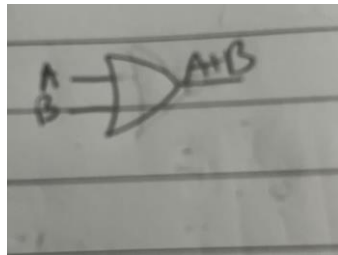
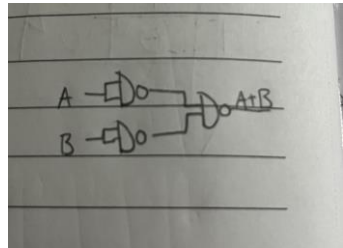
### 1.1 NOT gate.

Draw NOT gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit						
	<table><tr><th>A</th><th>NOT(A)</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table> <p>Y1=A'</p>	A	NOT(A)	0	1	1	0		
A	NOT(A)								
0	1								
1	0								

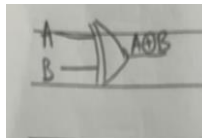
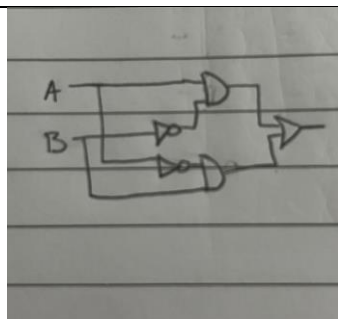
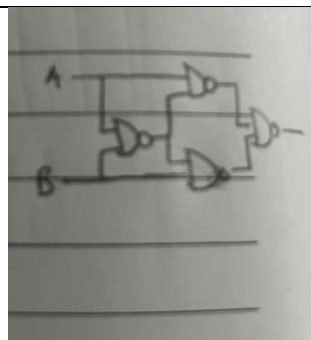
### 1.2- AND gate

Draw AND gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table border="1"><thead><tr><th>A</th><th>B</th><th>AND(A,B)</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table> <p>Y2=AB</p>	A	B	AND(A,B)	0	0	0	0	1	0	1	0	0	1	1	1		
A	B	AND(A,B)																
0	0	0																
0	1	0																
1	0	0																
1	1	1																

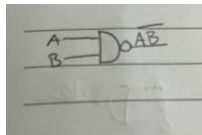
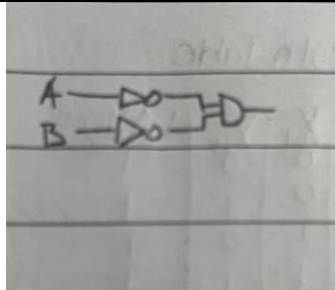
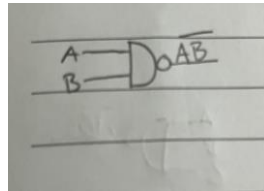
### 1.3- OR gate

Draw OR gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table><tr><th>A</th><th>B</th><th>OR</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table> <p>Y=A+B</p>	A	B	OR	0	0	0	0	1	1	1	0	1	1	1	1		
A	B	OR																
0	0	0																
0	1	1																
1	0	1																
1	1	1																

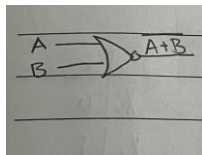
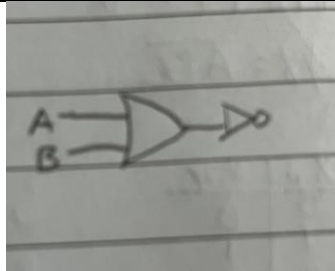
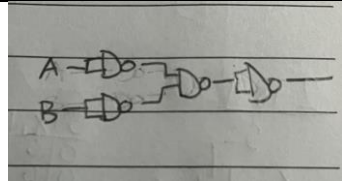
### 1.4- XOR gate

Draw XOR gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table border="1" data-bbox="431 1222 703 1409"><thead><tr><th>A</th><th>B</th><th>XOR(A,B)</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table> <p data-bbox="488 1444 626 1467"><math>Y4=AB'+A'B</math></p>	A	B	XOR(A,B)	0	0	0	0	1	1	1	0	1	1	1	0		
A	B	XOR(A,B)																
0	0	0																
0	1	1																
1	0	1																
1	1	0																

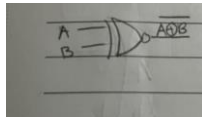
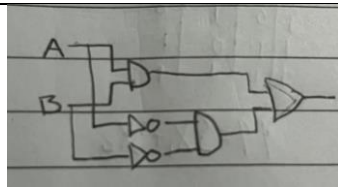
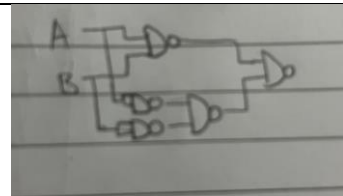
### 1.5- NAND gate

Draw NAND gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table><tr><th>A</th><th>B</th><th>NAND(A,B)</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <p>Y5=A'B'</p>	A	B	NAND(A,B)	0	0	1	0	1	1	1	0	1	1	1	0		
A	B	NAND(A,B)																
0	0	1																
0	1	1																
1	0	1																
1	1	0																

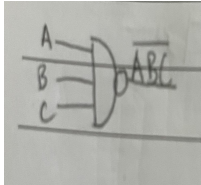
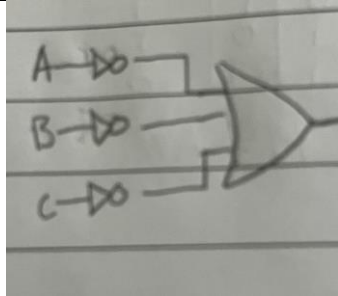
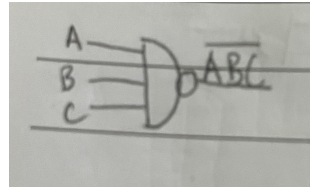
### 1.6- NOR gate

Draw NOR gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table border="1"><thead><tr><th>A</th><th>B</th><th>NOR(A,B)</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></tbody></table> <p><math>Y6=A'+B'</math></p>	A	B	NOR(A,B)	0	0	1	0	1	0	1	0	0	1	1	0		
A	B	NOR(A,B)																
0	0	1																
0	1	0																
1	0	0																
1	1	0																

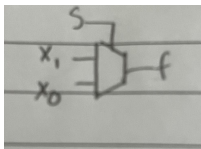
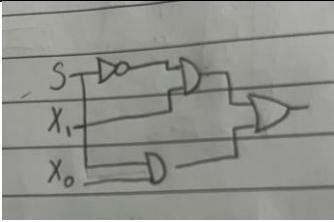
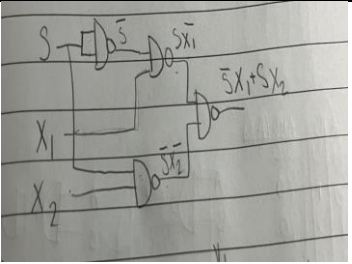
### 1.7- XNOR gate

Draw XNOR gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit															
	<table border="1"><thead><tr><th>A</th><th>B</th><th>XNOR(A,B)</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table> <p><math>Y7=(AB)+(A'B')</math></p>	A	B	XNOR(A,B)	0	0	1	0	1	0	1	0	0	1	1	1		
A	B	XNOR(A,B)																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

### 1.8 3-input NAND gate

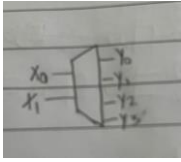
Draw 3-input NAND gate	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit																																				
	<table border="1"> <thead> <tr> <th>X2</th><th>X1</th><th>X0</th><th>NA ND 3</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> <p><math>Y8 = A'B'C'</math></p>	X2	X1	X0	NA ND 3	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0		
X2	X1	X0	NA ND 3																																				
0	0	0	1																																				
0	0	1	1																																				
0	1	0	1																																				
0	1	1	1																																				
1	0	0	1																																				
1	0	1	1																																				
1	1	0	1																																				
1	1	1	0																																				

### 1.9- 2 to 1 Encoder or Multiplexer (Mux)

Draw 2to1 Mux	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit																																				
	<table border="1"> <thead> <tr> <th>s</th><th>x1</th><th>x0</th><th>Mux</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p><math>Y8 = S'X1 + SX0</math></p>	s	x1	x0	Mux	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	1	1	1		
s	x1	x0	Mux																																				
0	0	0	0																																				
0	0	1	1																																				
0	1	0	0																																				
0	1	1	1																																				
1	0	0	0																																				
1	0	1	1																																				
1	1	0	0																																				
1	1	1	1																																				

### 1.10 - 2 to 4 decoder or Demultiplexer (DMux)

Draw 2to4 DMux	Truth Table and Simplest Sum of Products Equation	NOT-AND-OR Equivalent Circuit	all-NAND Equivalent Circuit
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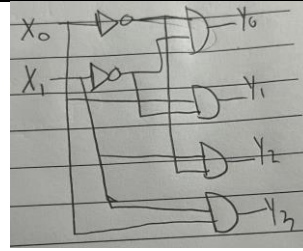
$X_1$	$X_0$	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$$Y_3 = X_1 X_0$$

$$Y_2 = X_1 X_0'$$

$$Y_1 = X_1' X_0$$

$$Y_0 = X_1' X_0'$$



### 3 Input NAND

#### Project wizard

New Project Wizard: Summary [page 5 of 5] ✕

When you click Finish, the project will be created with the following settings:

Project directory:  
Z:/LogicDesign/Lab1\_SaraFrazer/

Project name: NAND3\_SaraFrazer  
Top-level design entity: NAND3\_SaraFrazer  
Number of files added: 0  
Number of user libraries added: 0

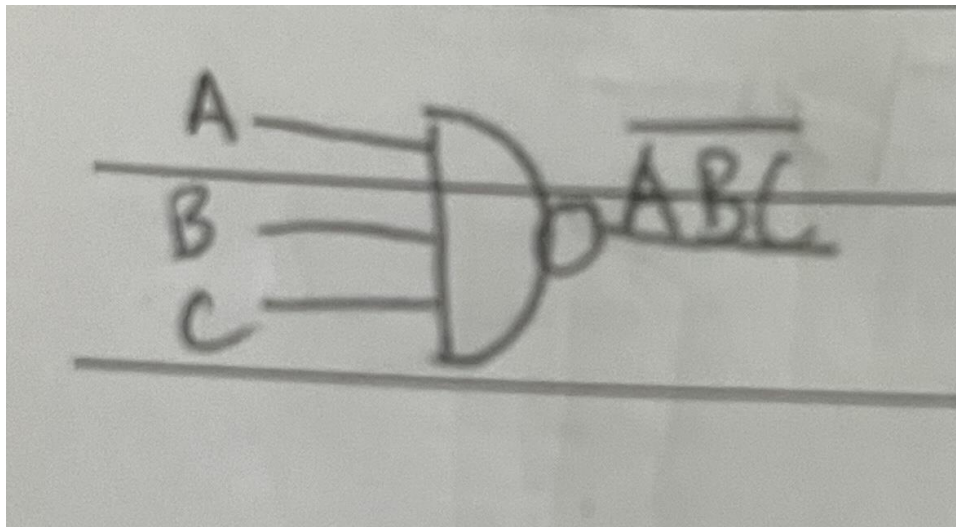
Device assignments:  
Family name: MAX3000A  
Device: EPM3064ALC44-10

EDA tools:  
Design entry/synthesis: <None>  
Simulation: <None>  
Timing analysis: <None>

Operating conditions:  
Core voltage: 3.3V  
Junction temperature range: 0-85 °C

< Back Next > Finish Cancel

#### Diagram



#### Truth Table

X2	X1	X0	NAND3
0	0	0	1
0	0	1	1
0	1	0	1



0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

## VHDL Code

```

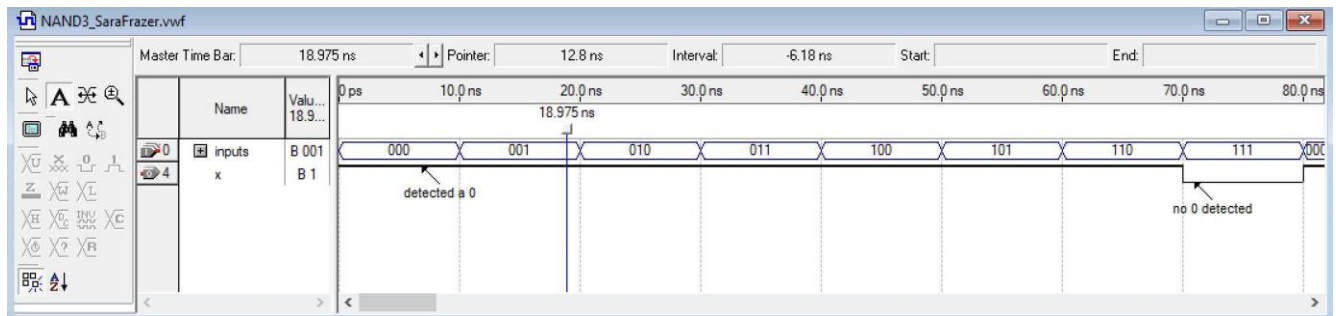
1  --3 input NAND
2  --Built from 2 input NAND
3  --by Sara Frazer
4
5  LIBRARY ieee;
6  USE ieee.std_logic_1164.all;
7
8  ENTITY NAND3_SaraFrazer IS
9      PORT(A,B,C : IN STD_LOGIC;
10         x : OUT STD_LOGIC);
11  END NAND3_SaraFrazer;
12  -- structural specification
13  ARCHITECTURE Structure OF NAND3_SaraFrazer IS
14      signal w1, w2 : STD_LOGIC;
15  BEGIN
16      w1<=A NAND B;
17      w2<=w1 NAND w1;
18      X<=w2 NAND C;
19  END Structure;

```

## Success Compilation

The screenshot displays the Quartus II IDE with the VHDL code from the previous block loaded in the editor. The 'Compiler Tool' window is open, showing the compilation progress. The 'Analysis & Synthesis' step is complete at 100% (00:00:04). The 'Filter' step is also complete at 100% (00:00:01). The 'Assembler' step is complete at 100% (00:00:02). The 'Classic Timing Analyzer' step is complete at 100% (00:00:01). The 'Full Compilation' progress bar is at 100% (00:00:08). A 'Quartus II' dialog box is open in the foreground, displaying the message: 'Full Compilation was successful (1 warning)'. The 'OK' button is visible. In the bottom right corner, there are links for 'View Quartus II Information' and 'Documentation'.

## Timing Diagram



## NAND 4

### Project Wizard

New Project Wizard: Summary [page 5 of 5] ✕

When you click Finish, the project will be created with the following settings:

Project directory:  
Z:/LogicDesign/Lab1\_SaraFrazer/

Project name: NAND4\_SaraFrazer

Top-level design entity: NAND4\_SaraFrazer

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3064ALC44-10

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

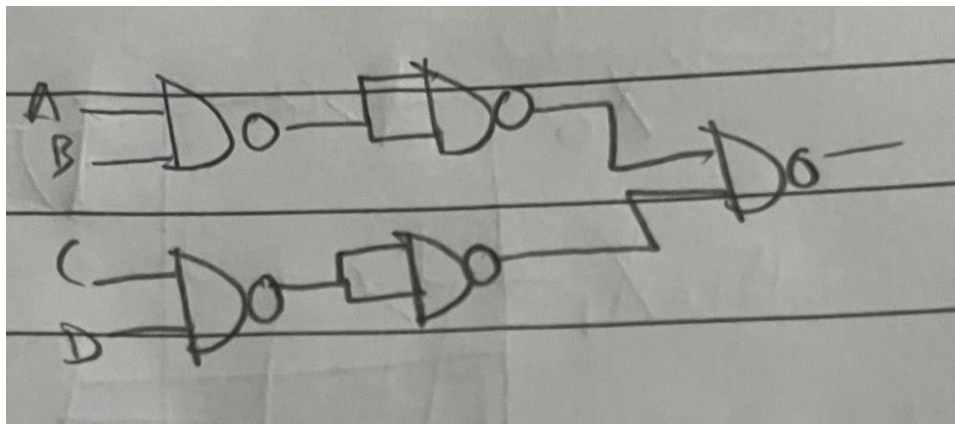
Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

< Back   Next >   Finish   Cancel

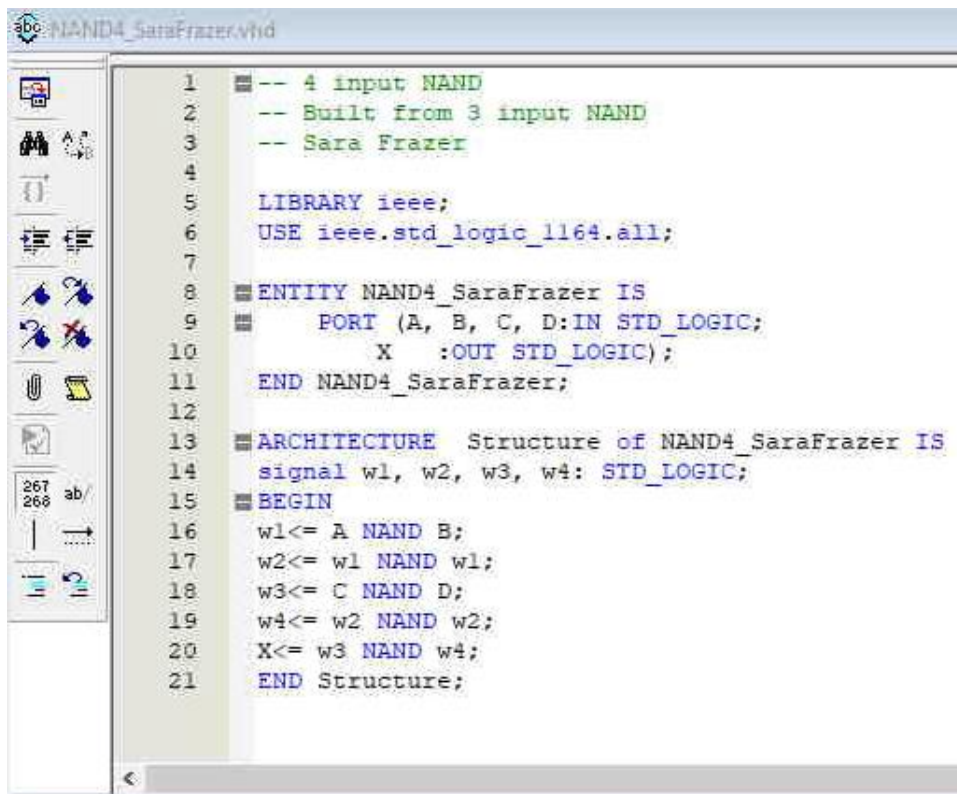
### Diagram



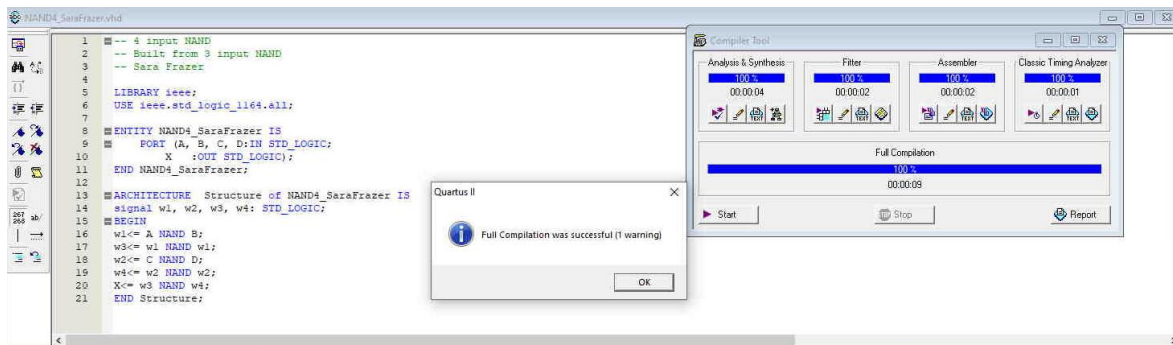
**Truth Table**

A	B	C	D	A'B'C'D'
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

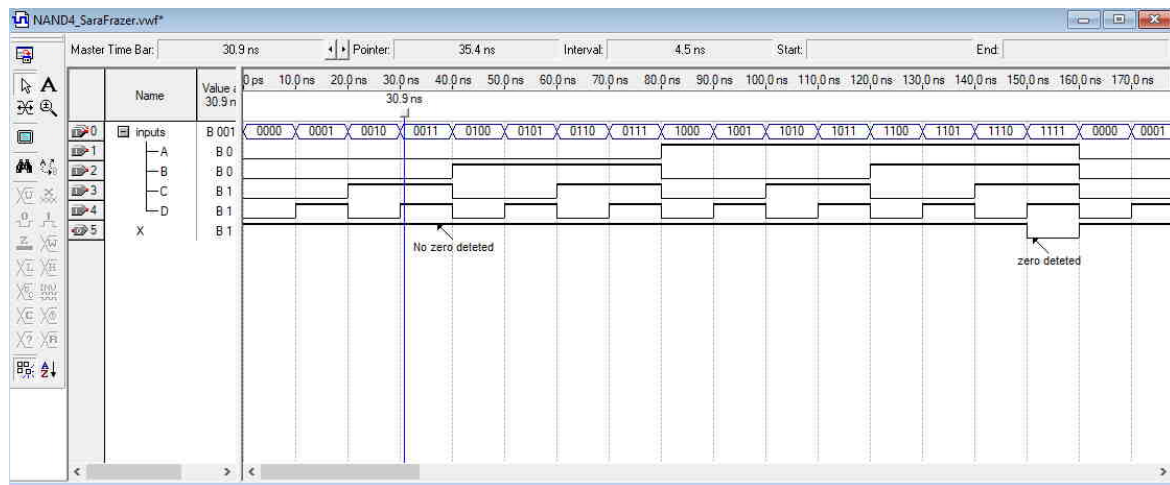
**VHDL Code**



## Success Compilation



## Timing Diagram



## 2 to 1 Mux

New Project Wizard: Summary [page 5 of 5] X

When you click Finish, the project will be created with the following settings:

Project directory:  
Z:/LogicDesign/Lab1\_SaraFrazer/

Project name: Mux2to1\_SaraFrazer

Top-level design entity: Mux2to1\_SaraFrazer

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3064ALC44-10

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

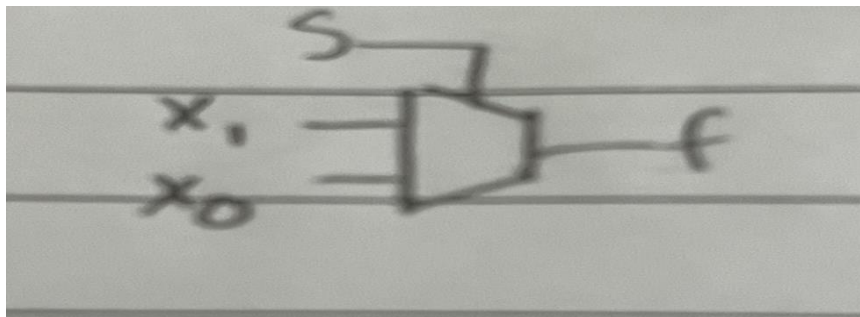
Core voltage: 3.3V

Junction temperature range: 0-85 °C

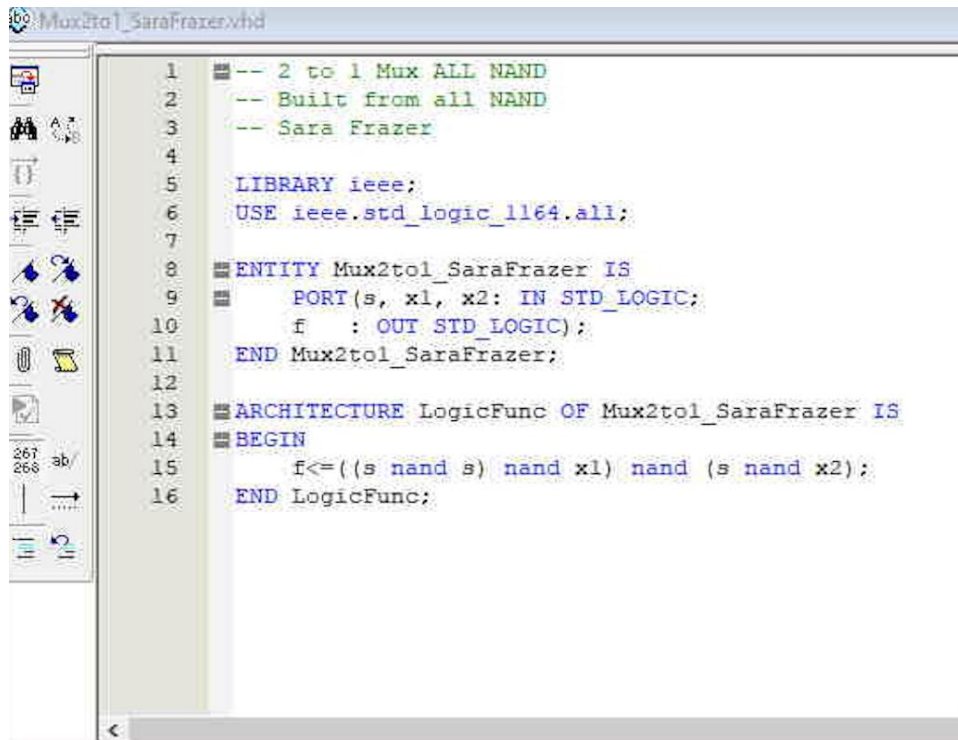
< Back Next > Finish Cancel

## Project Wizard

## Diagram

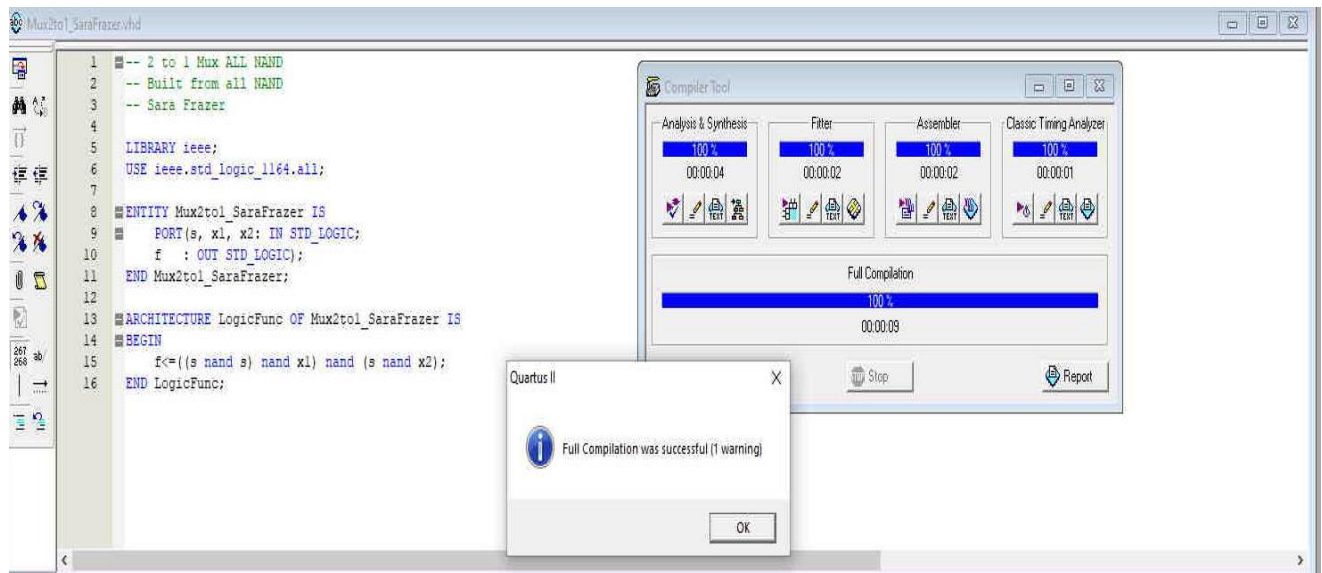


## VHDL Code



```
1  -- 2 to 1 Mux ALL NAND
2  -- Built from all NAND
3  -- Sara Frazer
4
5  LIBRARY ieee;
6  USE ieee.std_logic_1164.all;
7
8  ENTITY Mux2to1_SaraFrazer IS
9  PORT(s, x1, x2: IN STD_LOGIC;
10       f : OUT STD_LOGIC);
11  END Mux2to1_SaraFrazer;
12
13  ARCHITECTURE LogicFunc OF Mux2to1_SaraFrazer IS
14  BEGIN
15     f<=((s nand s) nand x1) nand (s nand x2);
16  END LogicFunc;
```

## Success Compilation



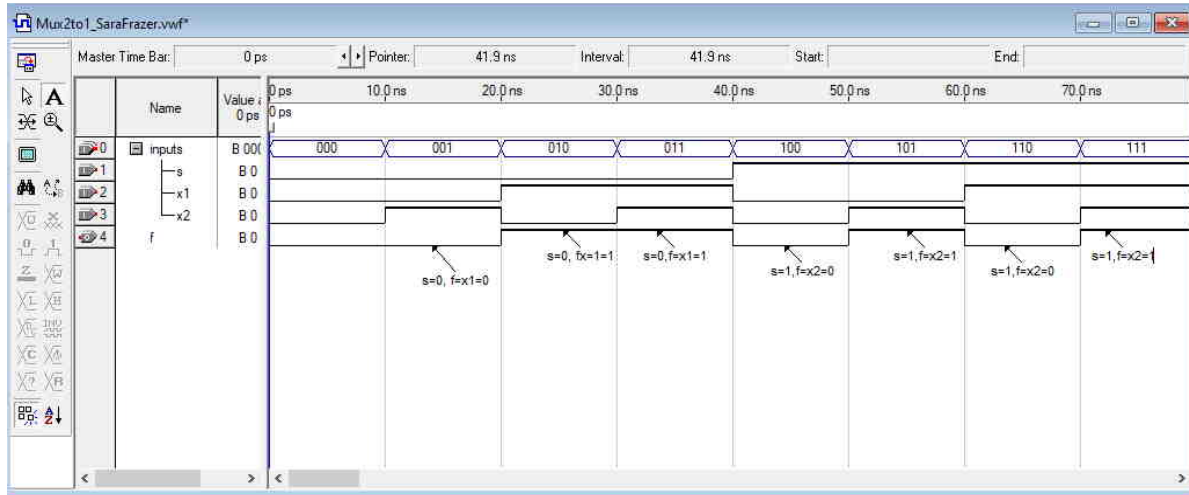
The screenshot shows the Quartus II IDE with the VHDL code from the previous block. The Compiler Tool window is open, showing the following progress:

Analysis & Synthesis	Filter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:04	00:00:02	00:00:02	00:00:01

Below these, the Full Compilation progress is shown as 100 % with a time of 00:00:09. A message box in the foreground states: "Full Compilation was successful (1 warning)".



## Timing Diagram



## 4 to 1 Mux

### Project Wizard

New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

Z:/LogicDesign/Lab1\_SaraFrazer/

Project name: Mux4to1\_SaraFrazer

Top-level design entity: Mux4to1\_SaraFrazer

Number of files added: 1

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3064ALC44-10

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

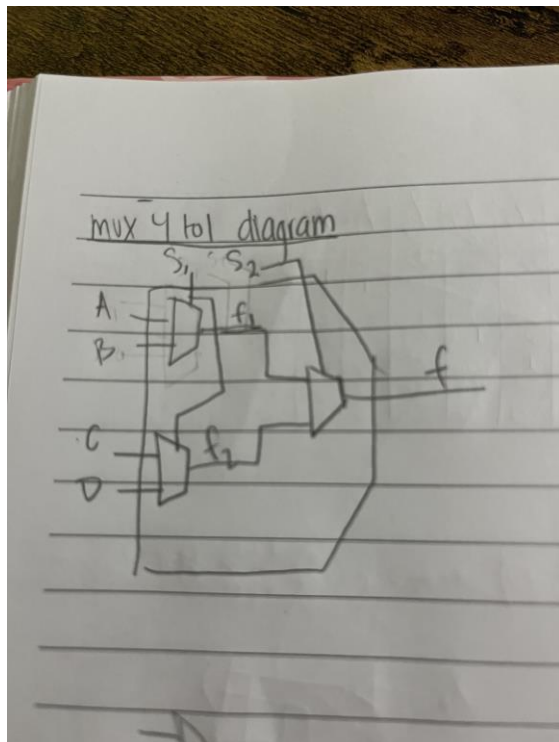
< Back

Next >

Finish

Cancel

### Diagram



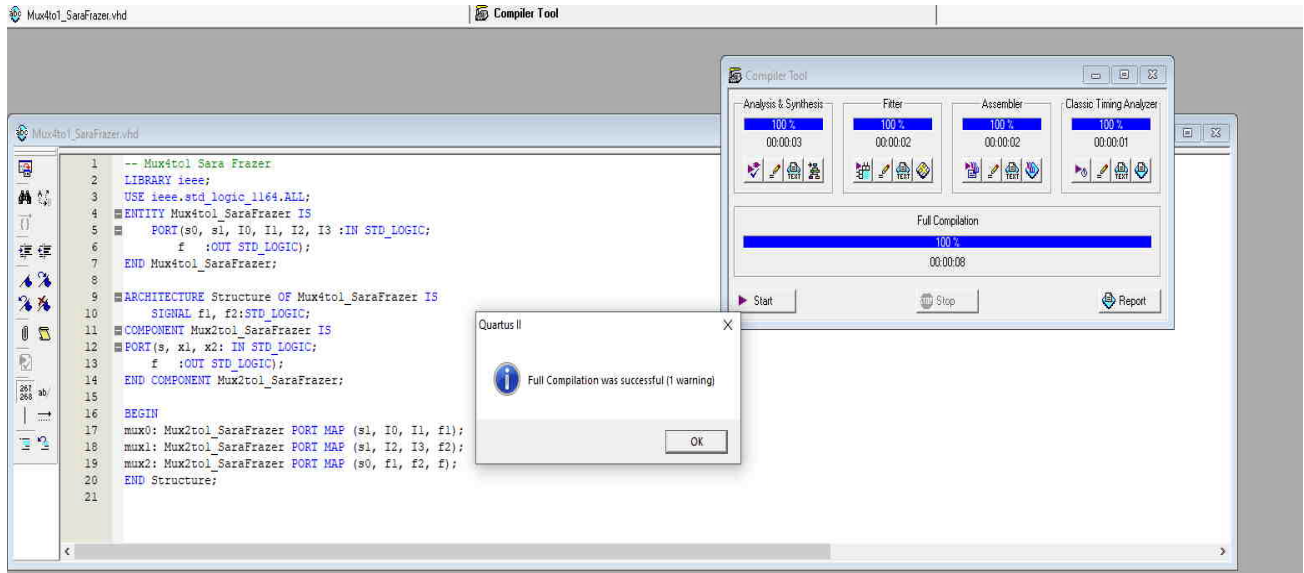
## Truth Table

$S_1$	$S_0$	$f$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

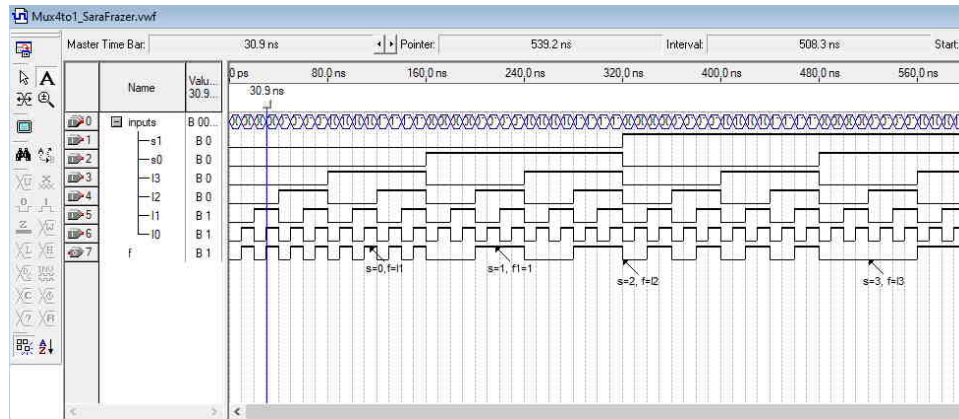
## VHDL Code

```
Mux4to1_SaraFrazer.vhd
1  -- Mux4to1 Sara Frazer
2  LIBRARY ieee;
3  USE ieee.std_logic_1164.ALL;
4  ENTITY Mux4to1_SaraFrazer IS
5  PORT(s0, s1, I0, I1, I2, I3 :IN STD_LOGIC;
6        f :OUT STD_LOGIC);
7  END Mux4to1_SaraFrazer;
8
9  ARCHITECTURE Structure OF Mux4to1_SaraFrazer IS
10     SIGNAL f1, f2:STD_LOGIC;
11     COMPONENT Mux2to1_SaraFrazer IS
12     PORT(s, x1, x2: IN STD_LOGIC;
13           f :OUT STD_LOGIC);
14     END COMPONENT Mux2to1_SaraFrazer;
15
16     BEGIN
17     mux0: Mux2to1_SaraFrazer PORT MAP (s1, I0, I1, f1);
18     mux1: Mux2to1_SaraFrazer PORT MAP (s1, I2, I3, f2);
19     mux2: Mux2to1_SaraFrazer PORT MAP (s0, f1, f2, f);
20     END Structure;
21
```

## Success Compilation



## Timing Diagram



## Mux 8to1

## Project Wizard

New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:  
Z:/LogicDesign/Lab1\_SaraFrazer/

Project name: Mux8to1\_SaraFrazer  
Top-level design entity: Mux8to1\_SaraFrazer  
Number of files added: 2  
Number of user libraries added: 0

Device assignments:  
Family name: MAX3000A  
Device: EPM3064ALC44-10

EDA tools:  
Design entry/synthesis: <None>  
Simulation: <None>  
Timing analysis: <None>

Operating conditions:  
Core voltage: 3.3V  
Junction temperature range: 0-85 °C

< Back Next > Finish Cancel

I added both mux 2 to and mux 4 to 1 files. Does not change the diagram if I only add mux 4to1.

## Drawing

