Lab 2

Sara Frazer

10/23/23

CDA 3203 Computer Logic Design

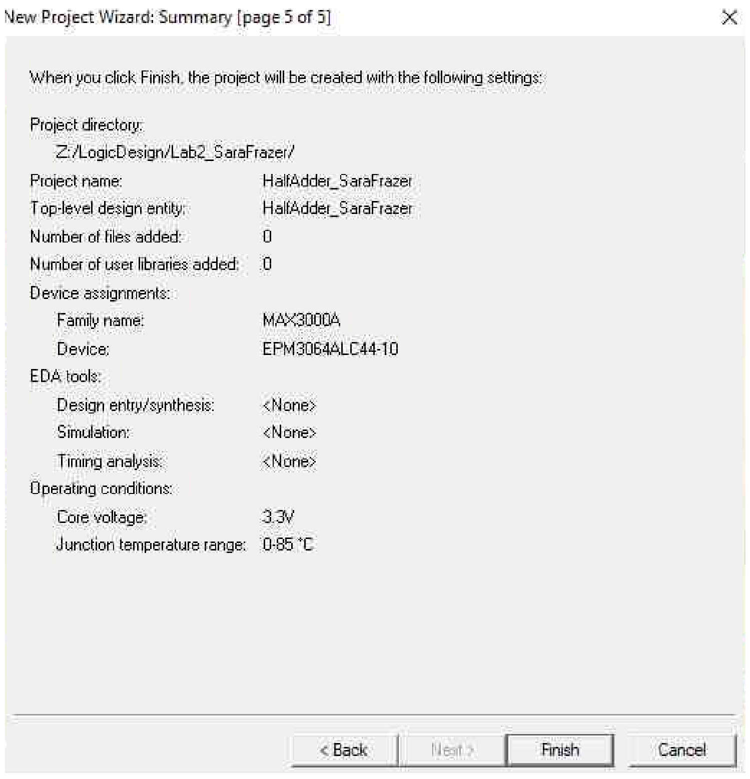
Fall 2023

Dr. Maria Petrie

Florida Atlantic University

Part 1: A 1-bit Half Adder to add 2 binary bits (A, B) and results in a 1-bit Sum and 1-bit Carry-out (Cout) with only NAND gates

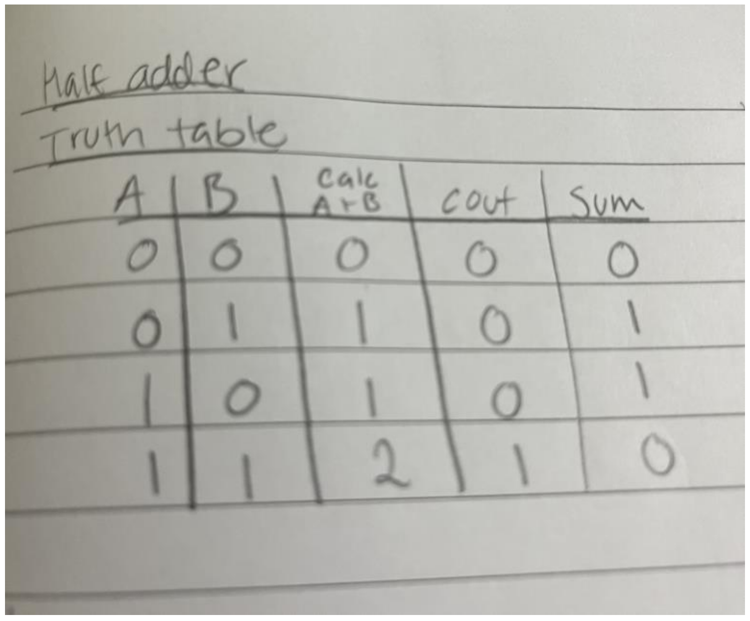
Project settings


New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

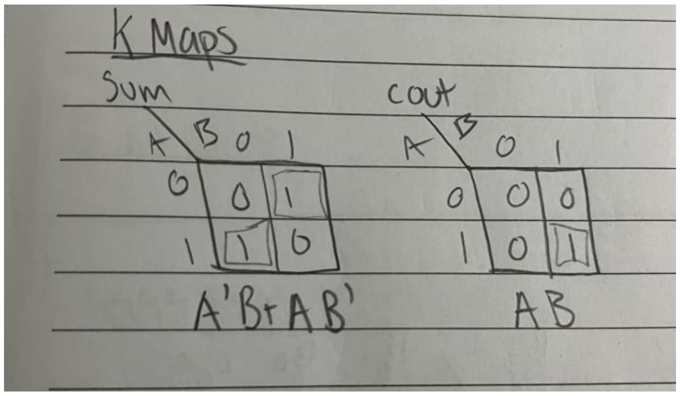
Project directory:	
Z:/LogicDesign/Lab2_SaraFrazer/	
Project name:	HalfAdder_SaraFrazer
Top-level design entity:	HalfAdder_SaraFrazer
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

Truth Table

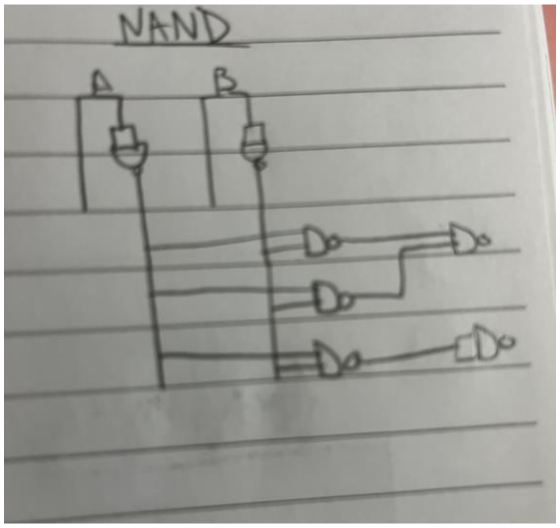

Half adder
Truth table

A	B	Calc A+B	Cout	Sum
0	0	0	0	0
0	1	1	0	1
1	0	1	0	1
1	1	2	1	0

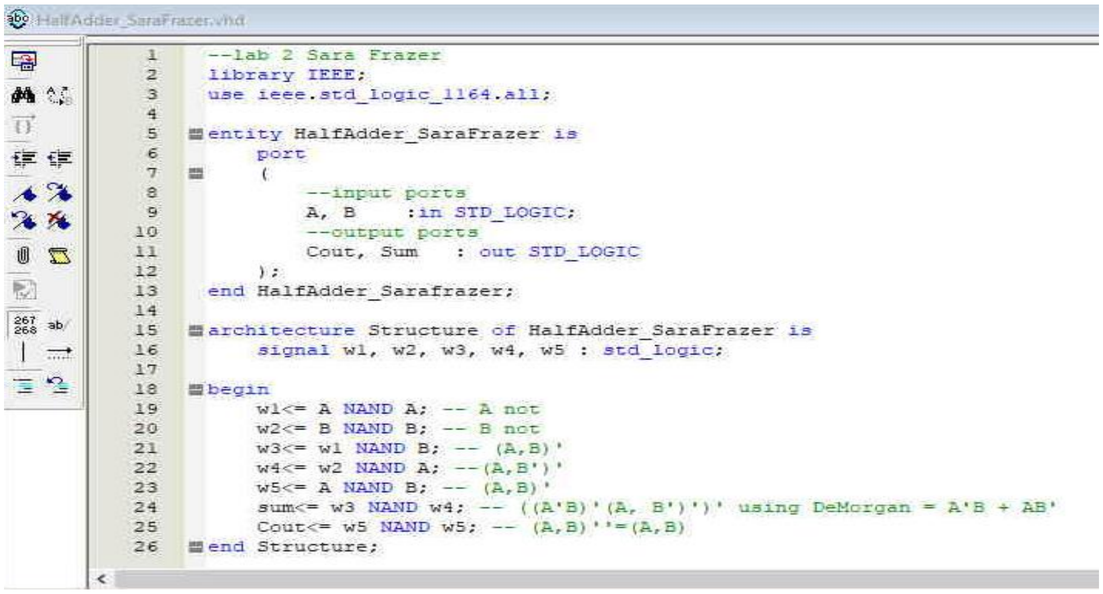
K Maps and Simplest Sum of Products



NAND Circuit

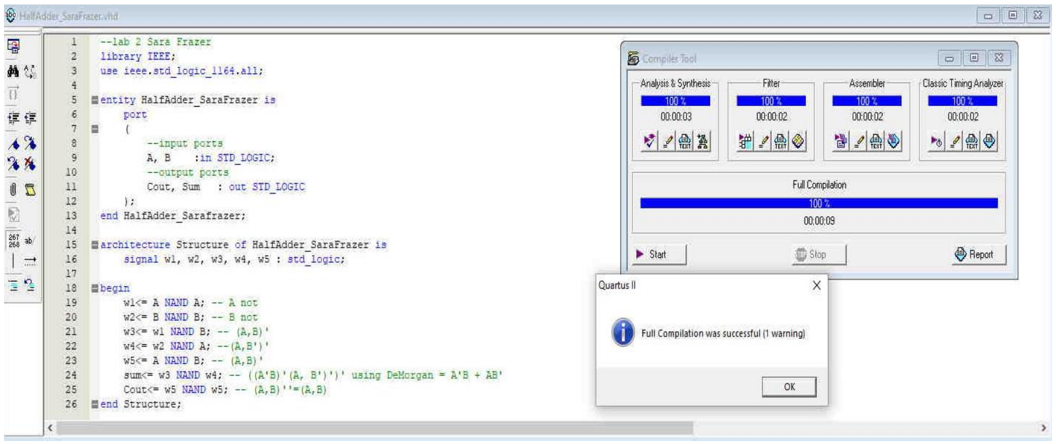


VHDL Code



```
--lab 2 Sara Frazer
library IEEE;
use ieee.std_logic_1164.all;

entity HalfAdder_SaraFrazer is
     port
     (
          --input ports
          A, B     :in STD_LOGIC;
          --output ports
          Cout, Sum    : out STD_LOGIC
     );
end HalfAdder_Sarafrazer;

architecture Structure of HalfAdder_SaraFrazer is
     signal w1, w2, w3, w4, w5 : std_logic;

begin
     w1<= A NAND A; -- A not
     w2<= B NAND B; -- B not
     w3<= w1 NAND B; -- (A,B)'
     w4<= w2 NAND A; --(A,B')'
     w5<= A NAND B; -- (A,B)'
     sum<= w3 NAND w4; -- ((A'B)'(A, B')')' using DeMorgan = A'B + AB'
     Cout<= w5 NAND w5; -- (A,B)''=(A,B)
end Structure;
```

Successful Compilation

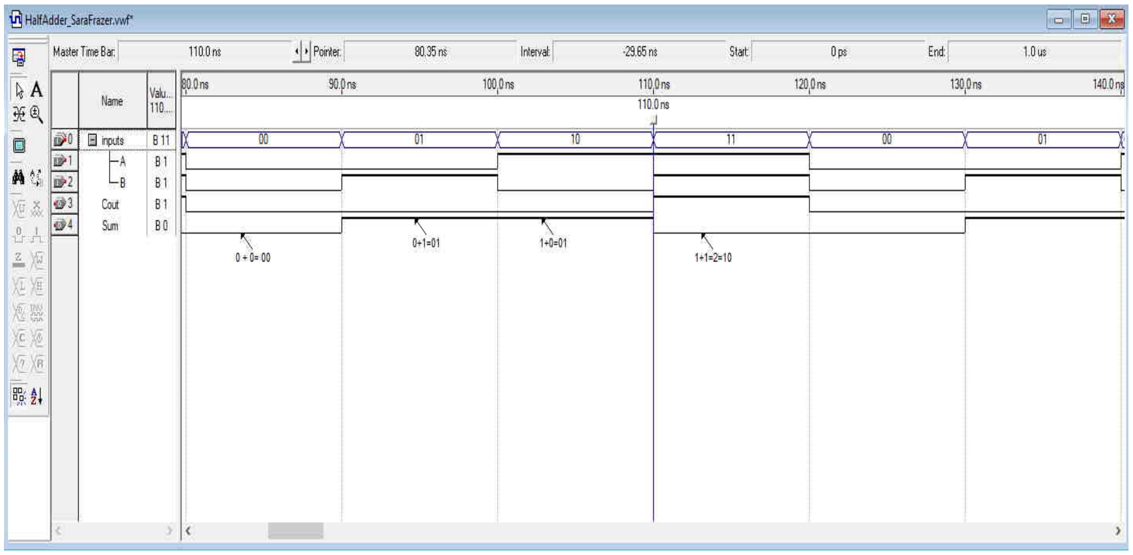


```vhdl
--lab 2 Sara Frazer
library IEEE;
use ieee.std_logic_1164.all;

entity HalfAdder_SaraFrazer is
    port
    (
        --input ports
        A, B    :in STD_LOGIC;
        --output ports
        Cout, Sum   : out STD_LOGIC
    );
end HalfAdder_Sarafrazer;

architecture Structure of HalfAdder_SaraFrazer is
    signal w1, w2, w3, w4, w5 : std_logic;

begin
    w1<= A NAND A; -- A not
    w2<= B NAND B; -- B not
    w3<= w1 NAND B; -- (A,B)'
    w4<= w2 NAND A; --(A,B')'
    w5<= A NAND B; -- (A,B)'
    sum<= w3 NAND w4; -- ((A'B)'(A, B')')' using DeMorgan = A'B + AB'
    Cout<= w5 NAND w5; -- (A,B)''=(A,B)
end Structure;
```

Quartus II

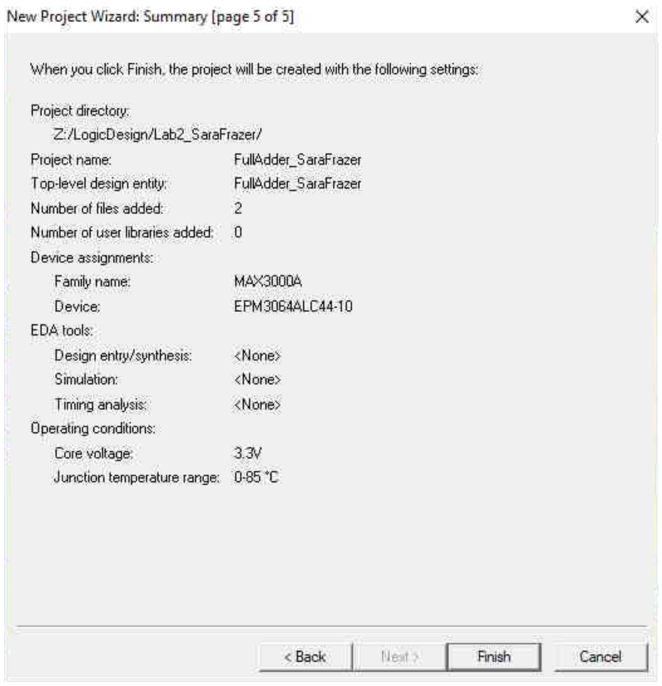
Full Compilation was successful (1 warning)

Timing Diagram



Part 2: A 1-bit Full Adder to add 2 binary bits (A, B) and a 1-bit Carry-in (Cin) and results in a 1-bit Sum and1-bit Carry-out (Cout) with only NAND gates.

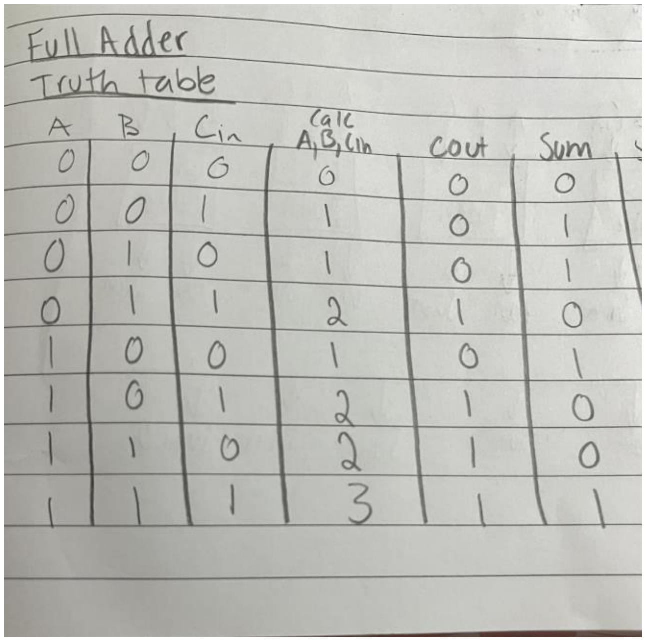
Project Settings



When you click Finish, the project will be created with the following settings:

Project directory:	
Z:/LogicDesign/Lab2_SaraFrazer/	
Project name:	FullAdder_SaraFrazer
Top-level design entity:	FullAdder_SaraFrazer
Number of files added:	2
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

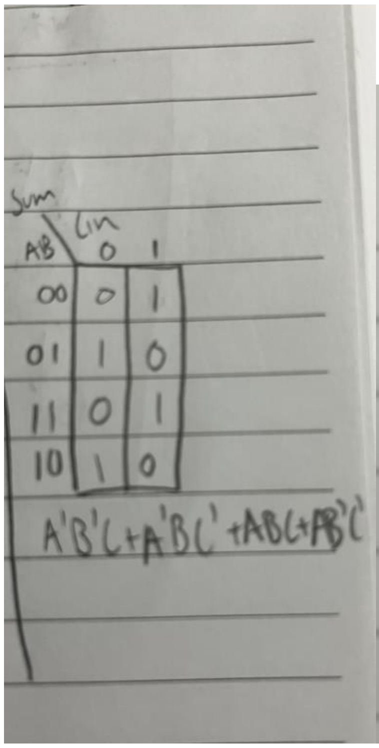
Truth Table



Full Adder
Truth table

A	B	Cin	Calc A,B,Cin	Cout	Sum
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	2	1	0
1	0	0	1	0	1
1	0	1	2	1	0
1	1	0	2	1	0
1	1	1	3	1	1

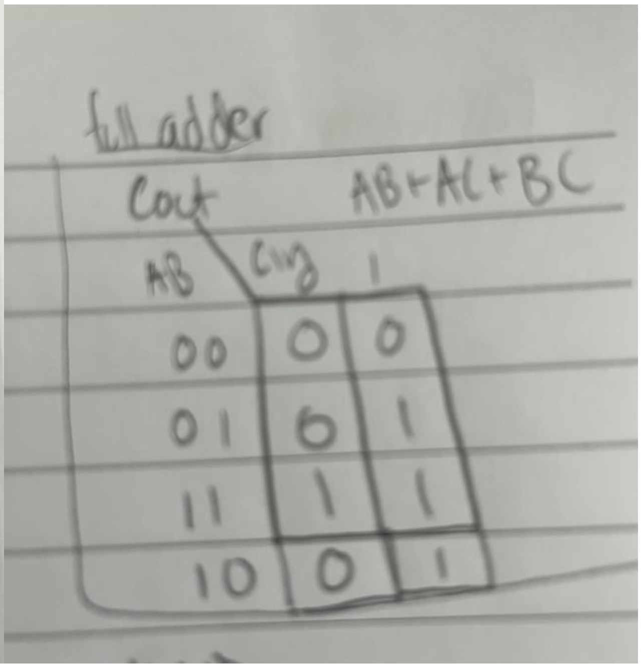
K Maps and Simplest Sum of Products



Sum

AB \ Cin	0	1
00	0	1
01	1	0
11	0	1
10	1	0

A'B'C+A'BC'+ABC+AB'C'

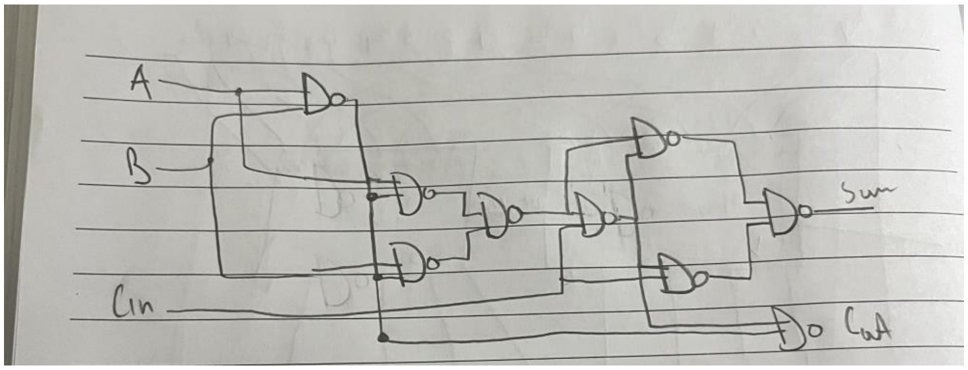


full adder

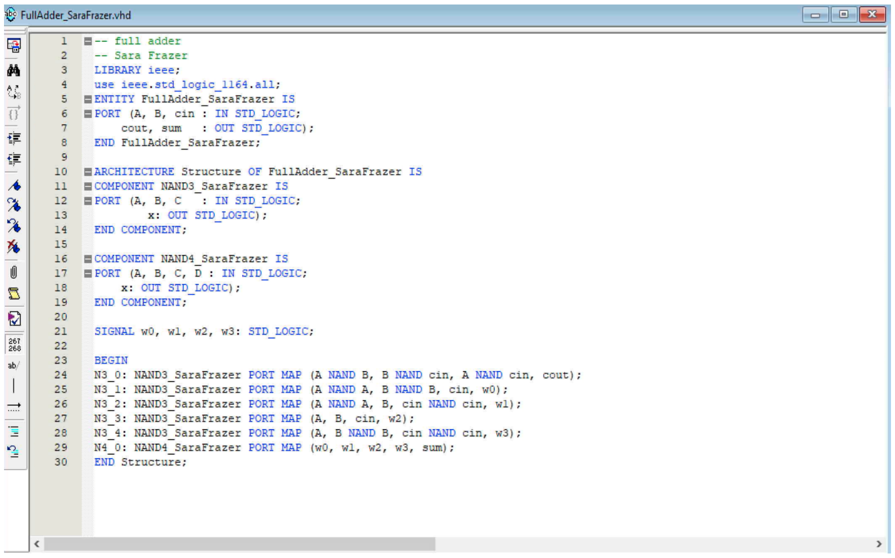
Cout AB+AC+BC

AB \ Cin		1
00	0	0
01	0	1
11	1	1
10	0	1

Simplest NAND Circuit

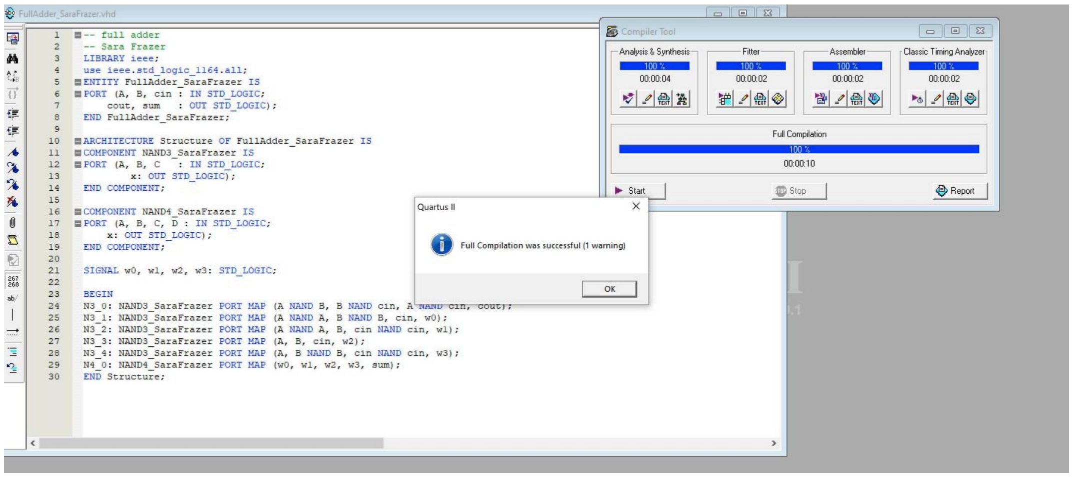


VHDL Code



```vhdl
-- full adder
-- Sara Frazer
LIBRARY ieee;
use ieee.std_logic_1164.all;
ENTITY FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum   : OUT STD_LOGIC);
END FullAdder_SaraFrazer;

ARCHITECTURE Structure OF FullAdder_SaraFrazer IS
COMPONENT NAND3_SaraFrazer IS
PORT (A, B, C   : IN STD_LOGIC;
        x: OUT STD_LOGIC);
END COMPONENT;

COMPONENT NAND4_SaraFrazer IS
PORT (A, B, C, D : IN STD_LOGIC;
    x: OUT STD_LOGIC);
END COMPONENT;

SIGNAL w0, w1, w2, w3: STD_LOGIC;

BEGIN
N3_0: NAND3_SaraFrazer PORT MAP (A NAND B, B NAND cin, A NAND cin, cout);
N3_1: NAND3_SaraFrazer PORT MAP (A NAND A, B NAND B, cin, w0);
N3_2: NAND3_SaraFrazer PORT MAP (A NAND A, B, cin NAND cin, w1);
N3_3: NAND3_SaraFrazer PORT MAP (A, B, cin, w2);
N3_4: NAND3_SaraFrazer PORT MAP (A, B NAND B, cin NAND cin, w3);
N4_0: NAND4_SaraFrazer PORT MAP (w0, w1, w2, w3, sum);
END Structure;
```

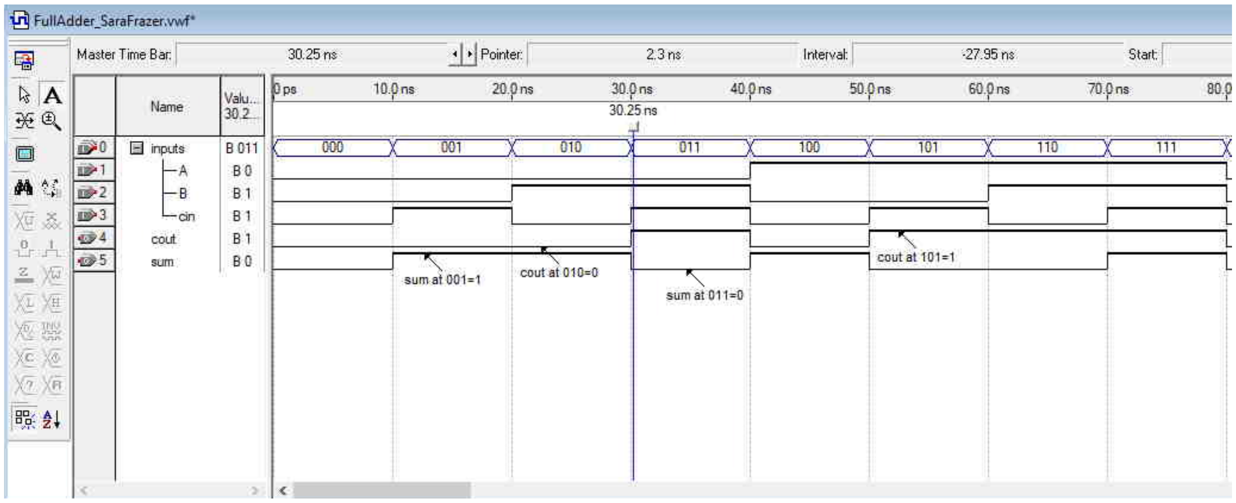
Successful Compilation



Full Compilation was successful (1 warning)

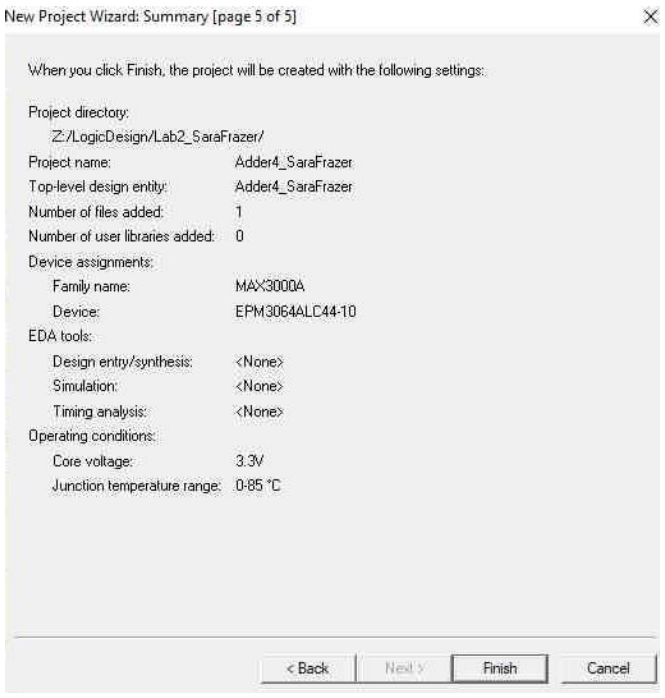
```vhdl
-- full adder
-- Sara Frazer
LIBRARY ieee;
use ieee.std_logic_1164.all;
ENTITY FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum   : OUT STD_LOGIC);
END FullAdder_SaraFrazer;

ARCHITECTURE Structure OF FullAdder_SaraFrazer IS
COMPONENT NAND3_SaraFrazer IS
PORT (A, B, C   : IN STD_LOGIC;
        x: OUT STD_LOGIC);
END COMPONENT;

COMPONENT NAND4_SaraFrazer IS
PORT (A, B, C, D : IN STD_LOGIC;
    x: OUT STD_LOGIC);
END COMPONENT;

SIGNAL w0, w1, w2, w3: STD_LOGIC;

BEGIN
N3_0: NAND3_SaraFrazer PORT MAP (A NAND B, B NAND cin, A NAND cin, cout);
N3_1: NAND3_SaraFrazer PORT MAP (A NAND A, B NAND B, cin, w0);
N3_2: NAND3_SaraFrazer PORT MAP (A NAND A, B, cin NAND cin, w1);
N3_3: NAND3_SaraFrazer PORT MAP (A, B, cin, w2);
N3_4: NAND3_SaraFrazer PORT MAP (A, B NAND B, cin NAND cin, w3);
N4_0: NAND4_SaraFrazer PORT MAP (w0, w1, w2, w3, sum);
END Structure;
```

Timing Diagram



Part 3: A 4-bit Adder to add 2 4 bit binary numbers (A3,A2,A1,A0 and B3,B2,B1,B0 with A0 and B0 being least significant bits) and a 1-bit Carry-in (Cin), and results in a 4-bit Sum (S3,S2,S1,S0) and 1-bit Carry-out (Cout) with the 1-bit Full Adder component you built

Project Settings

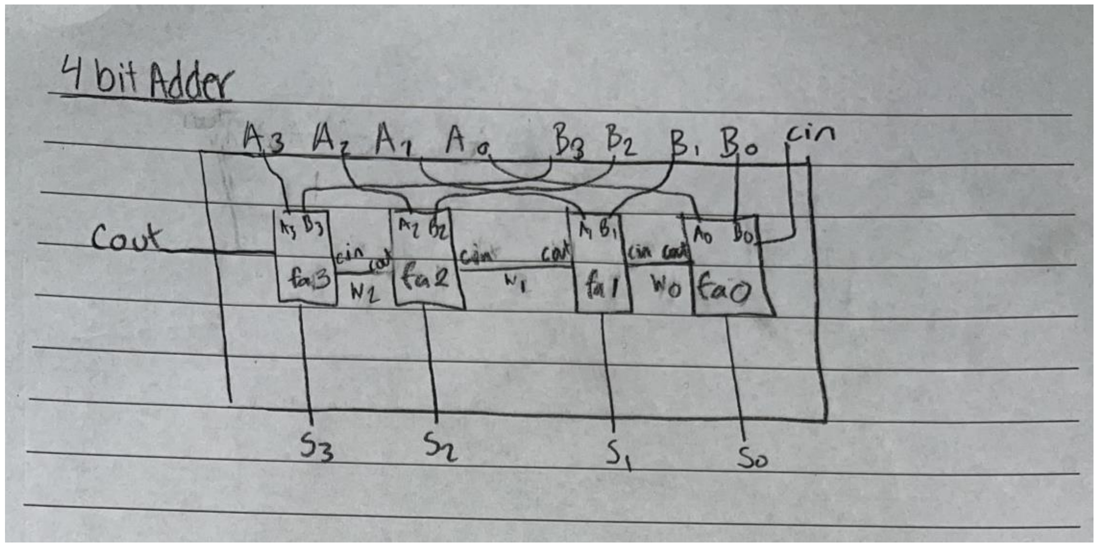


New Project Wizard: Summary [page 5 of 5]

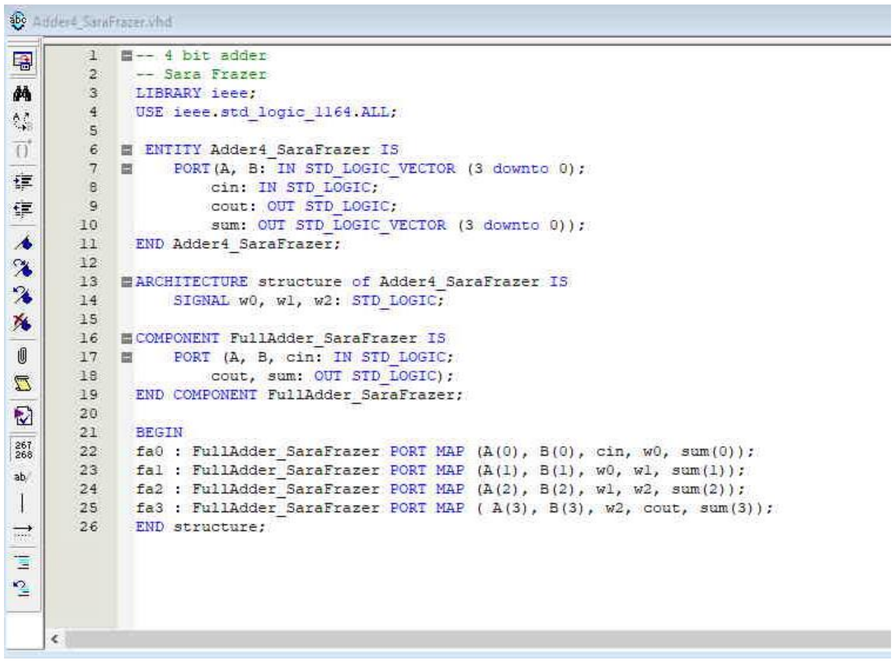
When you click Finish, the project will be created with the following settings:

Project directory:	
Z:/LogicDesign/Lab2_SaraFrazer/	
Project name:	Adder4_SaraFrazer
Top-level design entity:	Adder4_SaraFrazer
Number of files added:	1
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

Circuit Drawing



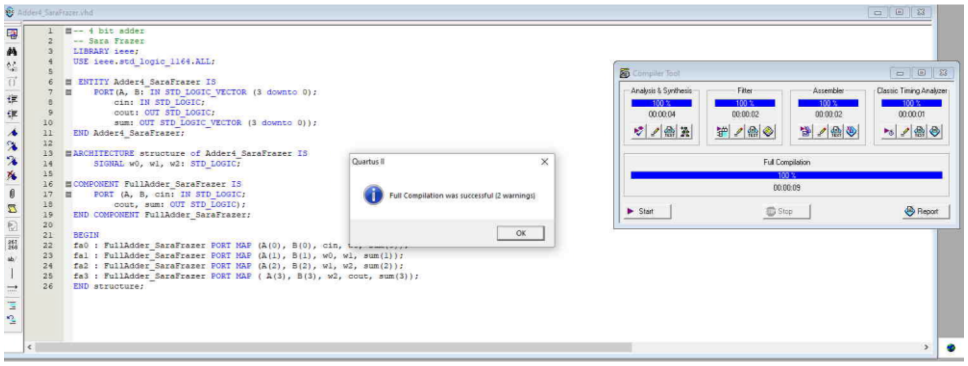
VHDL Code



Adder4_SaraFrazer.vhd

```
-- 4 bit adder
-- Sara Frazer
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

 ENTITY Adder4_SaraFrazer IS
    PORT(A, B: IN STD_LOGIC_VECTOR (3 downto 0);
         cin: IN STD_LOGIC;
         cout: OUT STD_LOGIC;
         sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END Adder4_SaraFrazer;

ARCHITECTURE structure of Adder4_SaraFrazer IS
    SIGNAL w0, w1, w2: STD_LOGIC;

COMPONENT FullAdder_SaraFrazer IS
    PORT (A, B, cin: IN STD_LOGIC;
         cout, sum: OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

BEGIN
fa0 : FullAdder_SaraFrazer PORT MAP (A(0), B(0), cin, w0, sum(0));
fa1 : FullAdder_SaraFrazer PORT MAP (A(1), B(1), w0, w1, sum(1));
fa2 : FullAdder_SaraFrazer PORT MAP (A(2), B(2), w1, w2, sum(2));
fa3 : FullAdder_SaraFrazer PORT MAP ( A(3), B(3), w2, cout, sum(3));
END structure;
```

Successful Compilation



```
-- 4 bit adder
-- Sara Frazer
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

 ENTITY Adder4_SaraFrazer IS
    PORT(A, B: IN STD_LOGIC_VECTOR (3 downto 0);
         cin: IN STD_LOGIC;
         cout: OUT STD_LOGIC;
         sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END Adder4_SaraFrazer;

ARCHITECTURE structure of Adder4_SaraFrazer IS
    SIGNAL w0, w1, w2: STD_LOGIC;

COMPONENT FullAdder_SaraFrazer IS
    PORT (A, B, cin: IN STD_LOGIC;
         cout, sum: OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

BEGIN
fa0 : FullAdder_SaraFrazer PORT MAP (A(0), B(0), cin,
fa1 : FullAdder_SaraFrazer PORT MAP (A(1), B(1), w0, w1, sum(1));
fa2 : FullAdder_SaraFrazer PORT MAP (A(2), B(2), w1, w2, sum(2));
fa3 : FullAdder_SaraFrazer PORT MAP ( A(3), B(3), w2, cout, sum(3));
END structure;
```

Quartus II

Full Compilation was successful (2 warnings)

OK

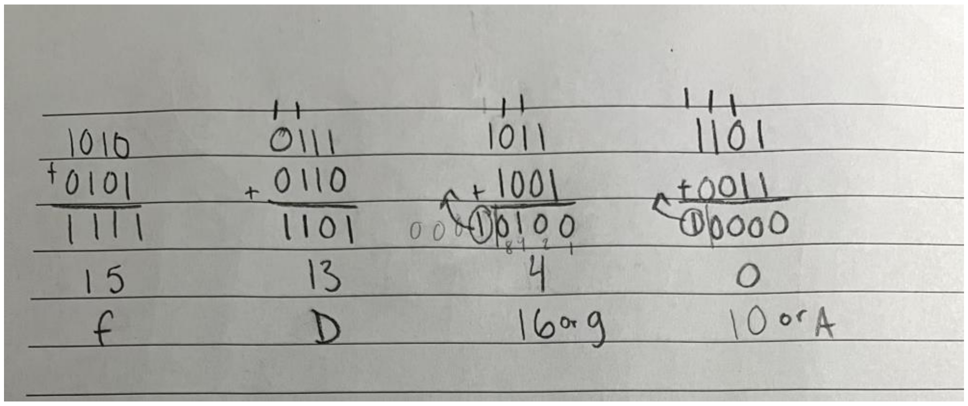
Compiler Tool

Analysis & Synthesis	Fitter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:04	00:00:02	00:00:02	00:00:01

Full Compilation 100 % 00:00:09

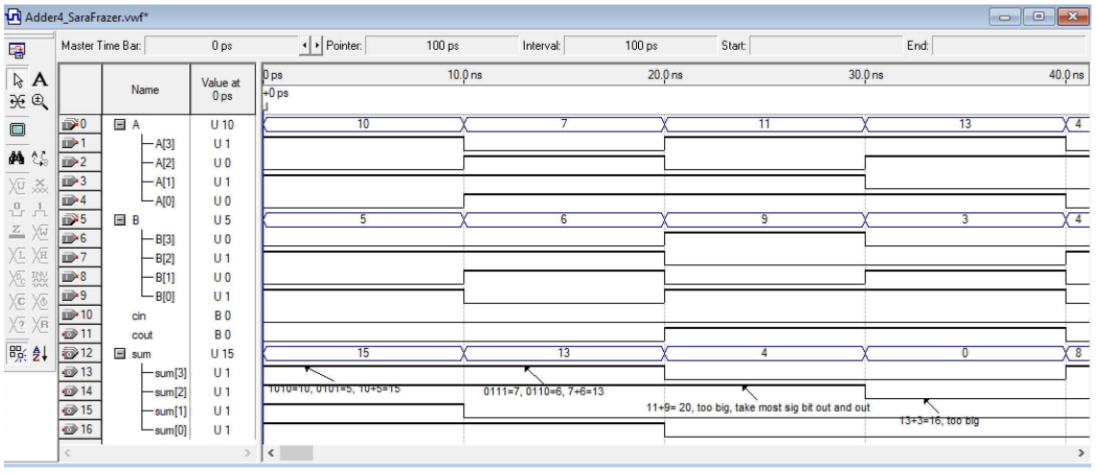
Start Stop Report

Use Cases



	11	111	111
1010	0111	1011	1101
+0101	+0110	+1001	+0011
1111	1101	00 ① 0100	① 0000
		8 4 2 1	
15	13	4	0
f	D	16 or g	10 or A

Timing Diagram



1010=10, 0101=5, 10+5=15

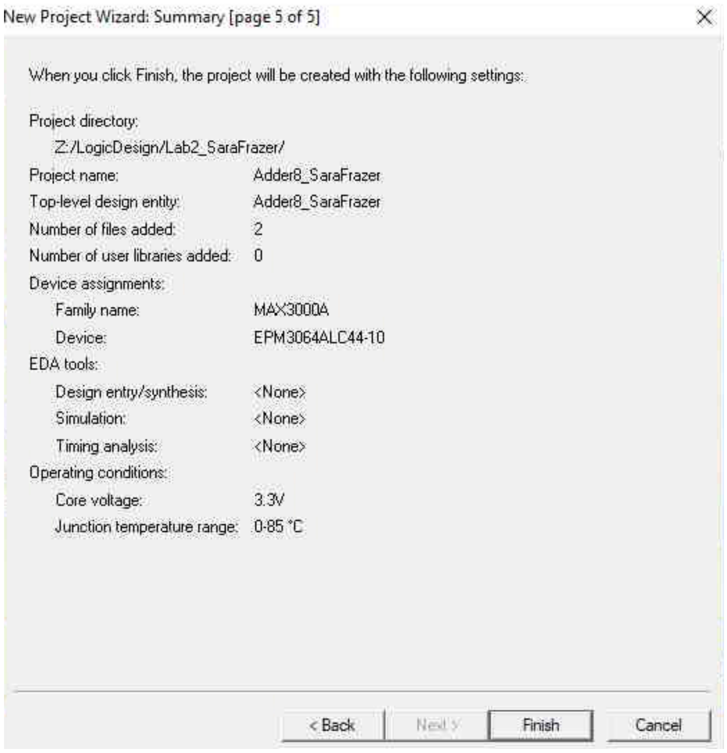
0111=7, 0110=6, 7+6=13

11+9= 20, too big, take most sig bit out and out

13+3=16, too big

Part 4: A 8-bit Adder to add 2 8-bit binary numbers (A7,A6,A5,A4,A3,A2,A1,A0 and B7,B6,B5,B4,B3,B2,B1,B0 with A0 and B0 being least significant bits) and a 1-bit Carry-in (Cin), and results in a 4-bit Sum (S7,S6,S5,S4,S3,S2,S1,S0) and 1-bit Carry-out (Cout) with the 1-bit Full Adder component you built.

Project Settings



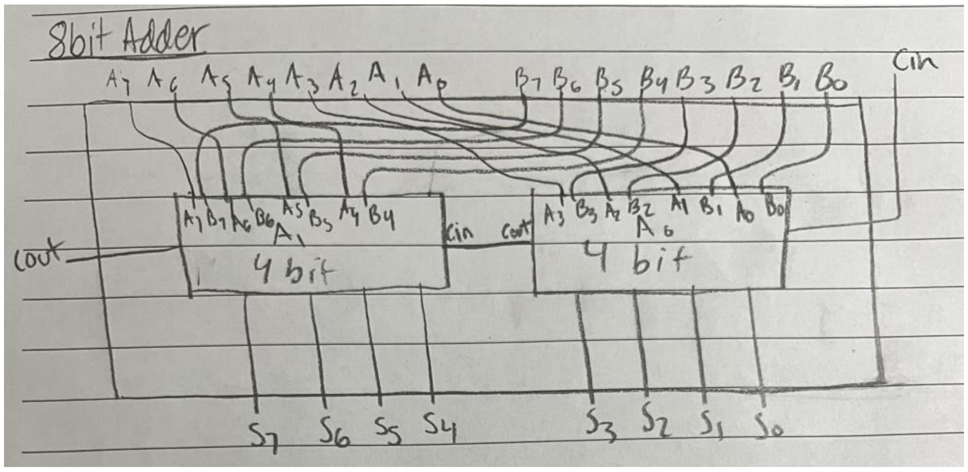
New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

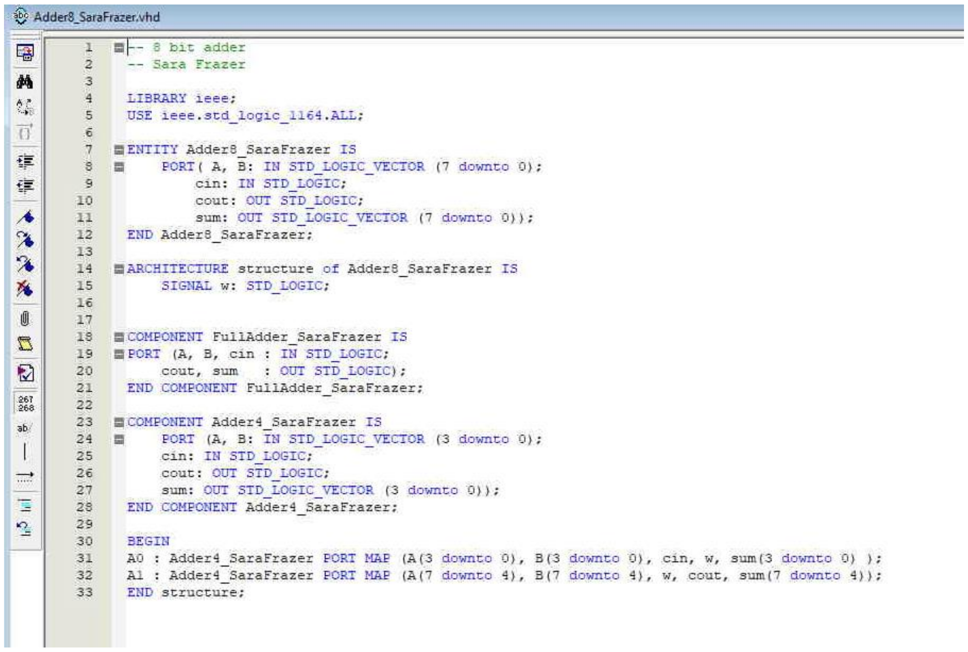
Project directory:
Z:/LogicDesign/Lab2_SaraFrazer/

Project name:	Adder8_SaraFrazer
Top-level design entity:	Adder8_SaraFrazer
Number of files added:	2
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

Circuit Drawing

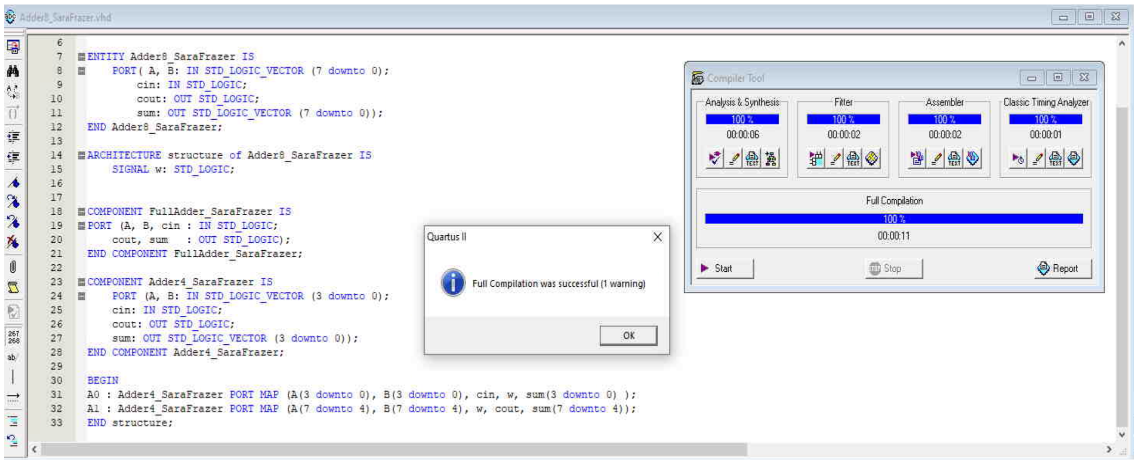


VHDL Code


Adder8_SaraFrazer.vhd

```vhdl
-- 8 bit adder
-- Sara Frazer

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Adder8_SaraFrazer IS
    PORT( A, B: IN STD_LOGIC_VECTOR (7 downto 0);
        cin: IN STD_LOGIC;
        cout: OUT STD_LOGIC;
        sum: OUT STD_LOGIC_VECTOR (7 downto 0));
END Adder8_SaraFrazer;

ARCHITECTURE structure of Adder8_SaraFrazer IS
    SIGNAL w: STD_LOGIC;


COMPONENT FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum   : OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

COMPONENT Adder4_SaraFrazer IS
    PORT (A, B: IN STD_LOGIC_VECTOR (3 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT Adder4_SaraFrazer;

BEGIN
A0 : Adder4_SaraFrazer PORT MAP (A(3 downto 0), B(3 downto 0), cin, w, sum(3 downto 0) );
A1 : Adder4_SaraFrazer PORT MAP (A(7 downto 4), B(7 downto 4), w, cout, sum(7 downto 4));
END structure;
```

Successful Compilation


Adder8_SaraFrazer.vhd

```vhdl

ENTITY Adder8_SaraFrazer IS
    PORT( A, B: IN STD_LOGIC_VECTOR (7 downto 0);
        cin: IN STD_LOGIC;
        cout: OUT STD_LOGIC;
        sum: OUT STD_LOGIC_VECTOR (7 downto 0));
END Adder8_SaraFrazer;

ARCHITECTURE structure of Adder8_SaraFrazer IS
    SIGNAL w: STD_LOGIC;


COMPONENT FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum   : OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

COMPONENT Adder4_SaraFrazer IS
    PORT (A, B: IN STD_LOGIC_VECTOR (3 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT Adder4_SaraFrazer;

BEGIN
A0 : Adder4_SaraFrazer PORT MAP (A(3 downto 0), B(3 downto 0), cin, w, sum(3 downto 0) );
A1 : Adder4_SaraFrazer PORT MAP (A(7 downto 4), B(7 downto 4), w, cout, sum(7 downto 4));
END structure;
```

Quartus II

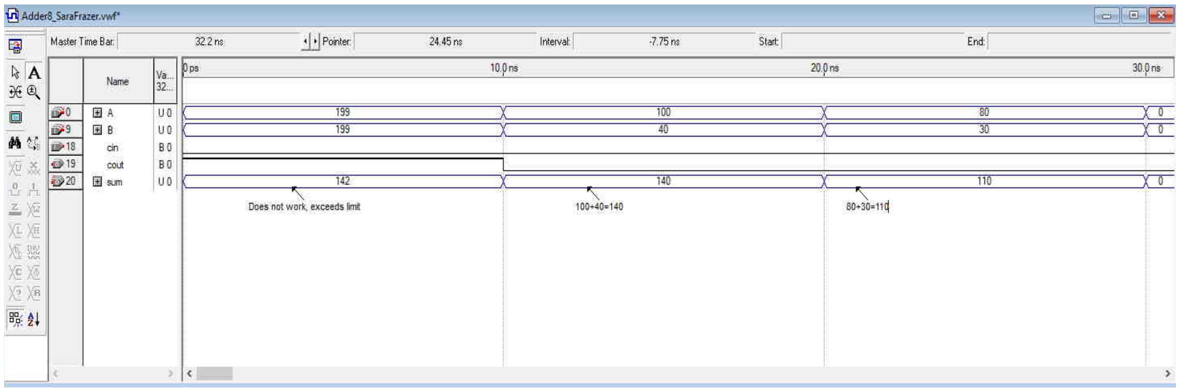
Full Compilation was successful (1 warning)

Compiler Tool

Analysis & Synthesis	Fitter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:06	00:00:02	00:00:02	00:00:01

Full Compilation 100 % 00:00:11

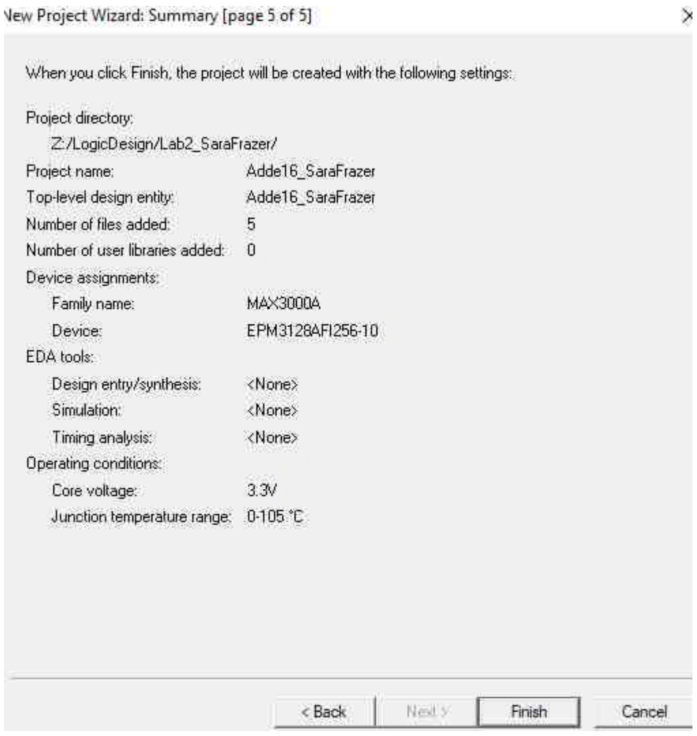
Timing Diagram


Adder8_SaraFrazer.vwf*

Master Time Bar: 32.2 ns   Pointer: 24.45 ns   Interval: -7.75 ns   Start: End:

Part 5: A 16-bit Adder to add 2 16-bit binary numbers (A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0 and B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0 with A0 and B0 being least significant bits) and a 1-bit Carry-in (Cin), and results in a 16-bit Sum(S15, S14, S13, S12, S11, S10, S9, S8, S7, S6, S5, S4, S3, S2, S1, S0) and 1-bit Carry-out (Cout) with component you built

Project Settings

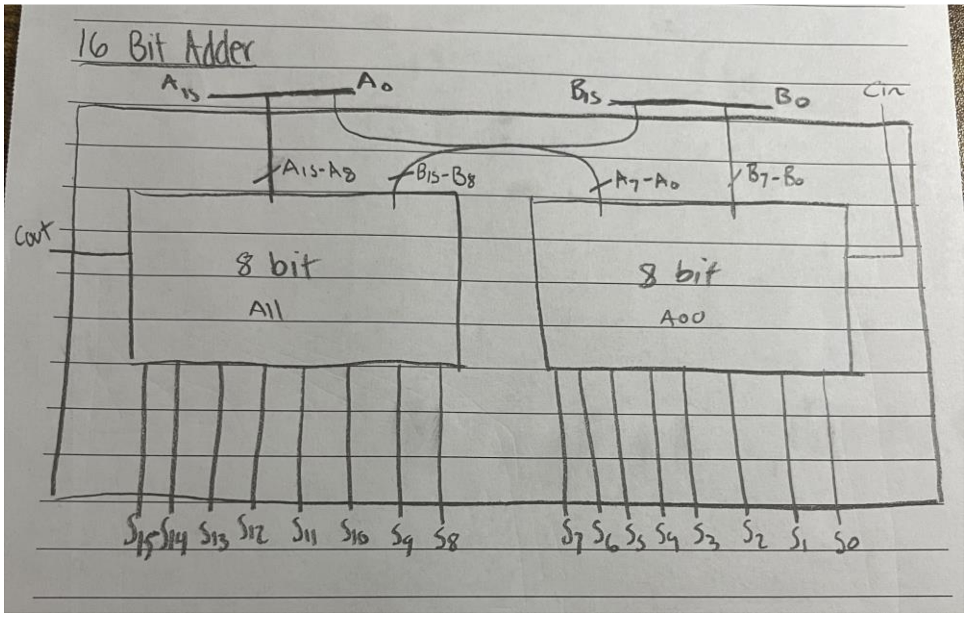


New Project Wizard: Summary [page 5 of 5]

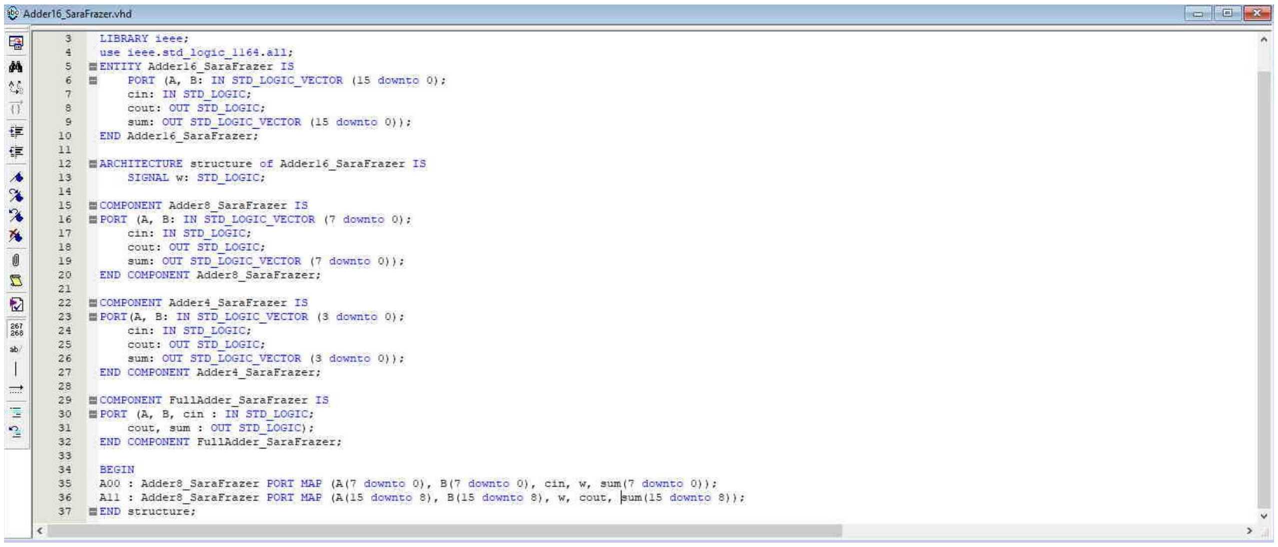
When you click Finish, the project will be created with the following settings:

Project directory:	
Z:/LogicDesign/Lab2_SaraFrazer/	
Project name:	Adde16_SaraFrazer
Top-level design entity:	Adde16_SaraFrazer
Number of files added:	5
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3128AFI256-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-105 °C

Circuit drawing



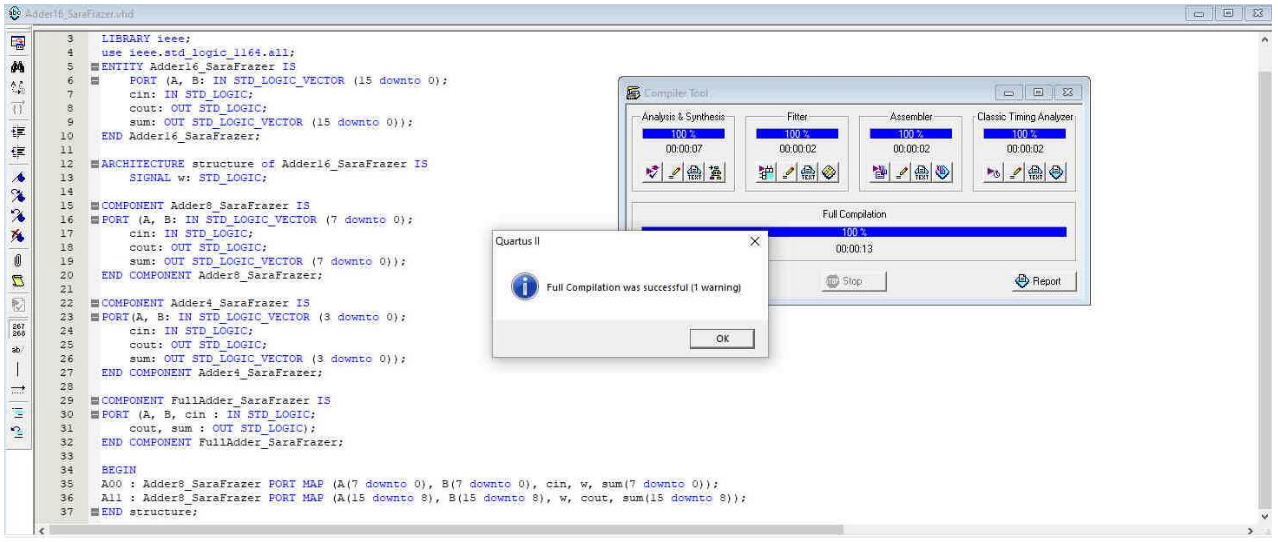
VHDL Code



Adder16_SaraFrazer.vhd

```
LIBRARY ieee;
use ieee.std_logic_1164.all;
ENTITY Adder16_SaraFrazer IS
    PORT (A, B: IN STD_LOGIC_VECTOR (15 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (15 downto 0));
END Adder16_SaraFrazer;

ARCHITECTURE structure of Adder16_SaraFrazer IS
    SIGNAL w: STD_LOGIC;

COMPONENT Adder8_SaraFrazer IS
PORT (A, B: IN STD_LOGIC_VECTOR (7 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (7 downto 0));
END COMPONENT Adder8_SaraFrazer;

COMPONENT Adder4_SaraFrazer IS
PORT(A, B: IN STD_LOGIC_VECTOR (3 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT Adder4_SaraFrazer;

COMPONENT FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum : OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

BEGIN
A00 : Adder8_SaraFrazer PORT MAP (A(7 downto 0), B(7 downto 0), cin, w, sum(7 downto 0));
A11 : Adder8_SaraFrazer PORT MAP (A(15 downto 8), B(15 downto 8), w, cout, sum(15 downto 8));
END structure;
```

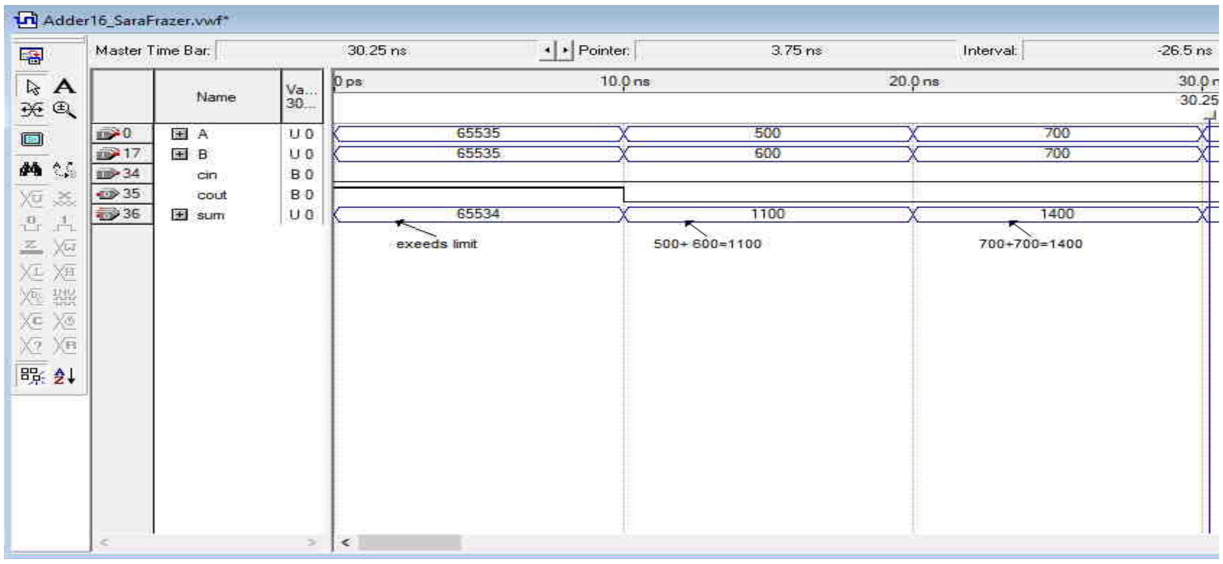
Successful Compilation



```
LIBRARY ieee;
use ieee.std_logic_1164.all;
ENTITY Adder16_SaraFrazer IS
    PORT (A, B: IN STD_LOGIC_VECTOR (15 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (15 downto 0));
END Adder16_SaraFrazer;

ARCHITECTURE structure of Adder16_SaraFrazer IS
    SIGNAL w: STD_LOGIC;

COMPONENT Adder8_SaraFrazer IS
PORT (A, B: IN STD_LOGIC_VECTOR (7 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (7 downto 0));
END COMPONENT Adder8_SaraFrazer;

COMPONENT Adder4_SaraFrazer IS
PORT(A, B: IN STD_LOGIC_VECTOR (3 downto 0);
    cin: IN STD_LOGIC;
    cout: OUT STD_LOGIC;
    sum: OUT STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT Adder4_SaraFrazer;

COMPONENT FullAdder_SaraFrazer IS
PORT (A, B, cin : IN STD_LOGIC;
    cout, sum : OUT STD_LOGIC);
END COMPONENT FullAdder_SaraFrazer;

BEGIN
A00 : Adder8_SaraFrazer PORT MAP (A(7 downto 0), B(7 downto 0), cin, w, sum(7 downto 0));
A11 : Adder8_SaraFrazer PORT MAP (A(15 downto 8), B(15 downto 8), w, cout, sum(15 downto 8));
END structure;
```

```
Compiler Tool
Analysis & Synthesis   100 %   00:00:07
Fitter                 100 %   00:00:02
Assembler              100 %   00:00:02
Classic Timing Analyzer 100 %  00:00:02
Full Compilation       100 %   00:00:13

Quartus II
Full Compilation was successful (1 warning)
```

Timing Diagram


Adder16_SaraFrazer.vwf*
Master Time Bar: 30.25 ns
Pointer: 3.75 ns
Interval: -26.5 ns
Name
Va... 30...
0 ps
10.0 ns
20.0 ns
30.0
30.25
0 A U 0
17 B U 0
34 cin B 0
35 cout B 0
36 sum U 0
65535
500
700
65535
600
700
65534
1100
1400
exeeds limit
500+ 600=1100
700+700=1400