

# Lab 3

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CDA 3203 Computer Logic Design

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Florida Atlantic University

## Hand Work

### 1.1 D Flip Flop

1.1 D Flip Flop

D	Q	Command	Q+
0	0	make Q=0	0
	1		0
1	0	make Q=1	1
	1		1



### 1.2 T Flip Flop

1.2 T Flip Flop

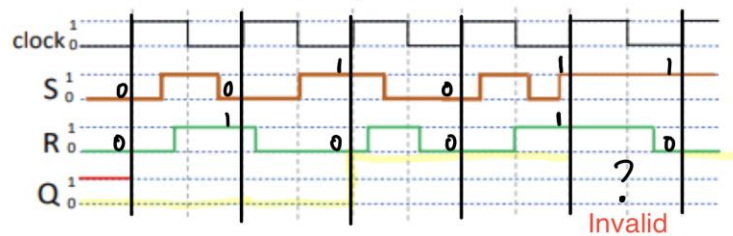
T	Q	Command	Q+
0	0	Hold	0
	1		0
1	0	Toggle	1
	1		0



### 1.3 S-R Flip Flop

1.3 S-R Flip Flop

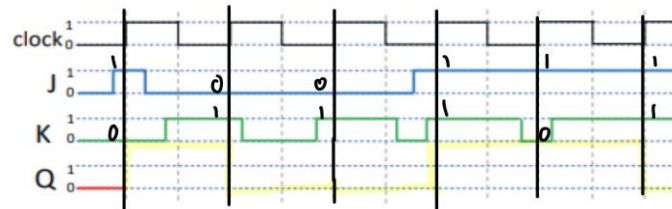
S	R	Q	Command	Q+
0	0	0	Hold	0
		1		1
0	1	0	Reset	0
		1		0
1	0	0	Set	1
		1		1
1	1	0	Invalid	?



### 1.4 J-K Flip Flop

1.4 J-K Flip Flop

J	K	Q	Command	Q+
0	0	0	Hold	0
		1		1
0	1	0	Reset	0
		1		0
1	0	0	Set	1
		1		1
1	1	0	Toggle	1



### 1.5 Excitation Tables

Q → Q <sup>+</sup>	Command	D
0 → 0	Q=0	0
0 → 1	Q=1	1
1 → 0	Q=0	0
1 → 1	Q=1	1

Q → Q <sup>+</sup>	Command	T
0 → 0	Hold	0
0 → 1	Toggle	1
1 → 0	Toggle	1
1 → 1	Hold	0

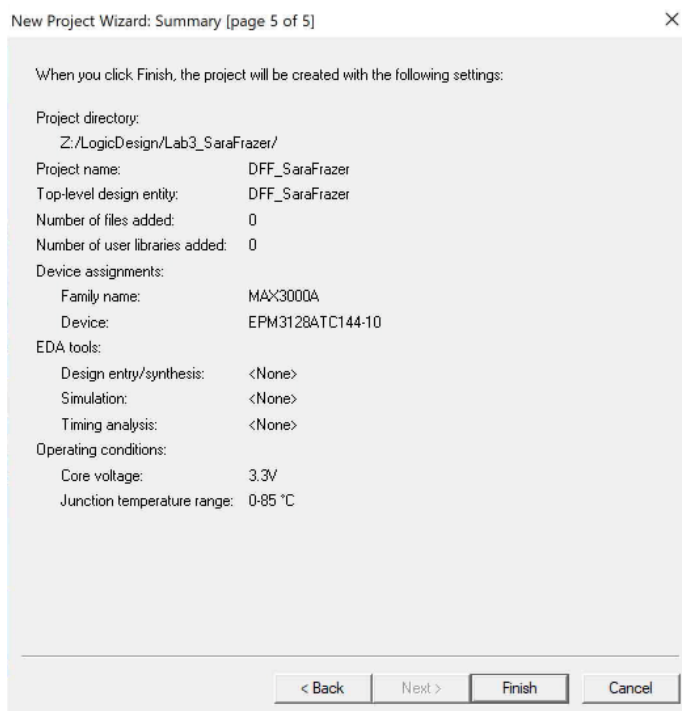
Q → Q <sup>+</sup>	Commands	S R
0 → 0	00	0x
0 → 1	01	10
1 → 0	10	01
1 → 1	11	x0

Q → Q <sup>+</sup>	Commands	J K
0 → 0	00	0x
0 → 1	01	1x
1 → 0	10	x1
1 → 1	11	x0

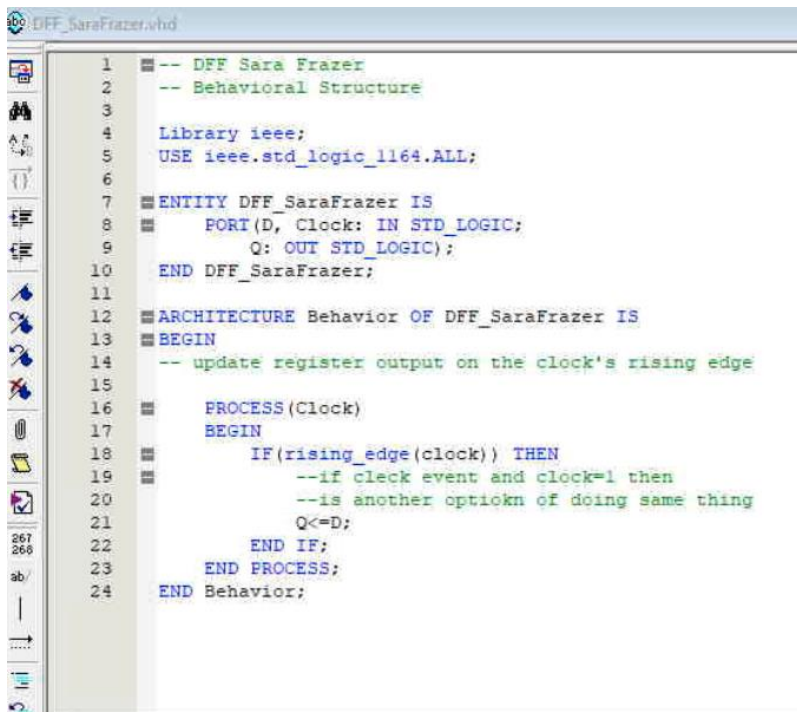
## 2.0 Design and Simulation of Sequential Components in Altera Quartus Using VHDL

### 2.1 Data Flip Flop (DFF)

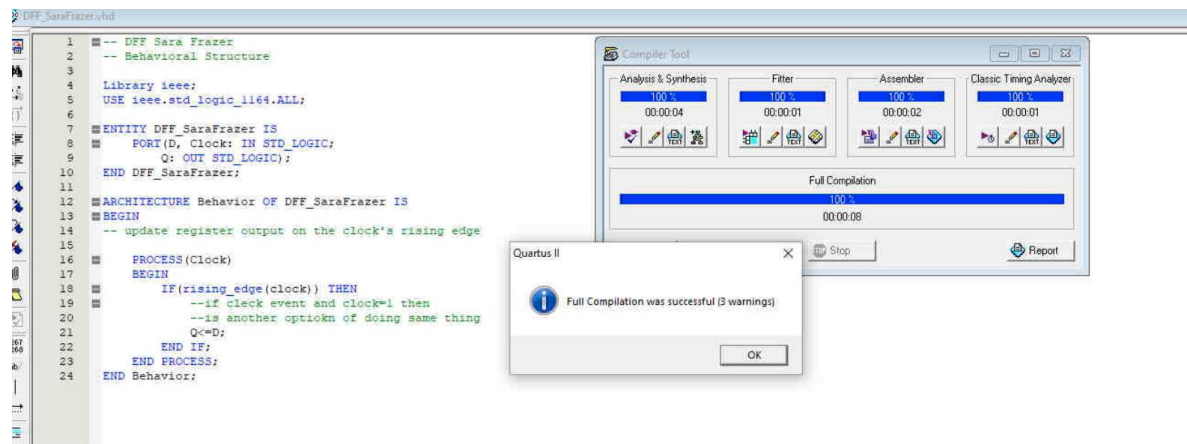
#### Project Wizard Settings



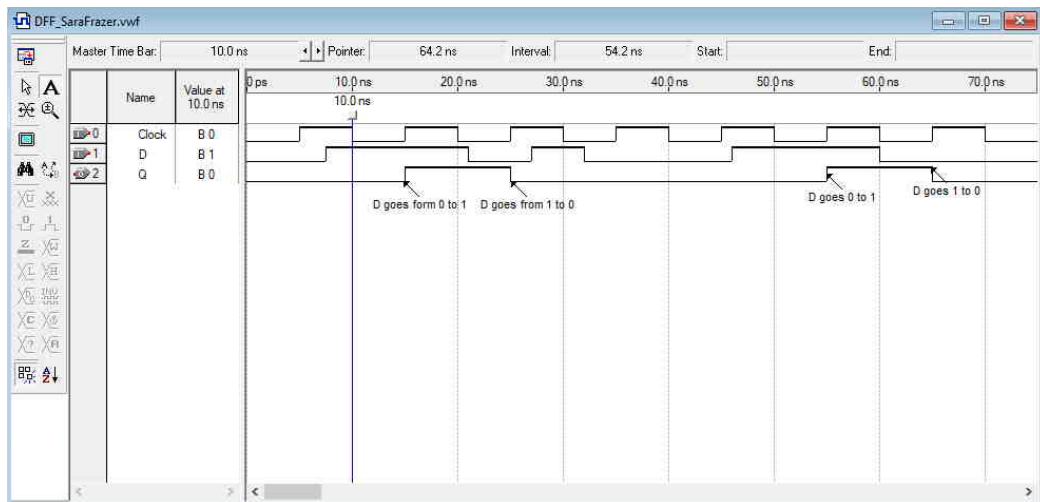
#### VHDL Code



## Successful Compilation



## Timing Diagram

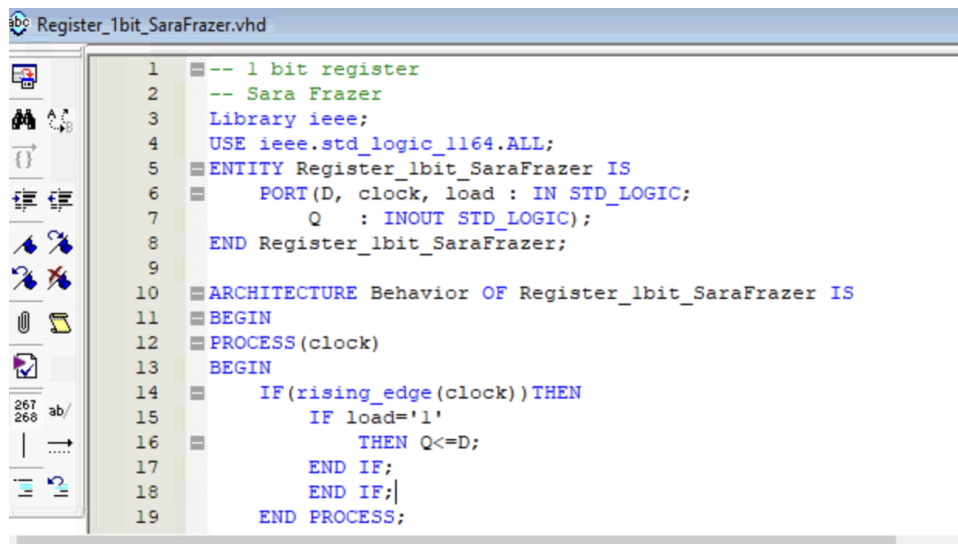


## 2.2-1 1-Bit Register

### Project Settings

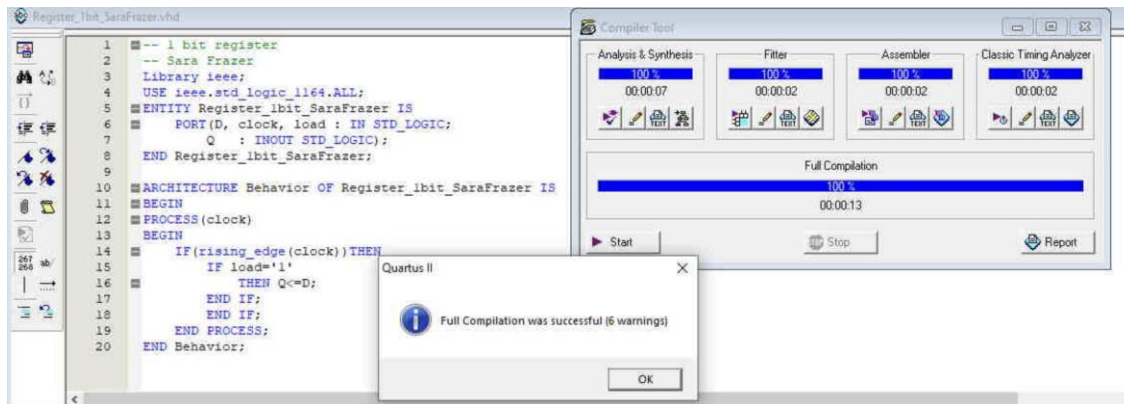


### VHDL Code

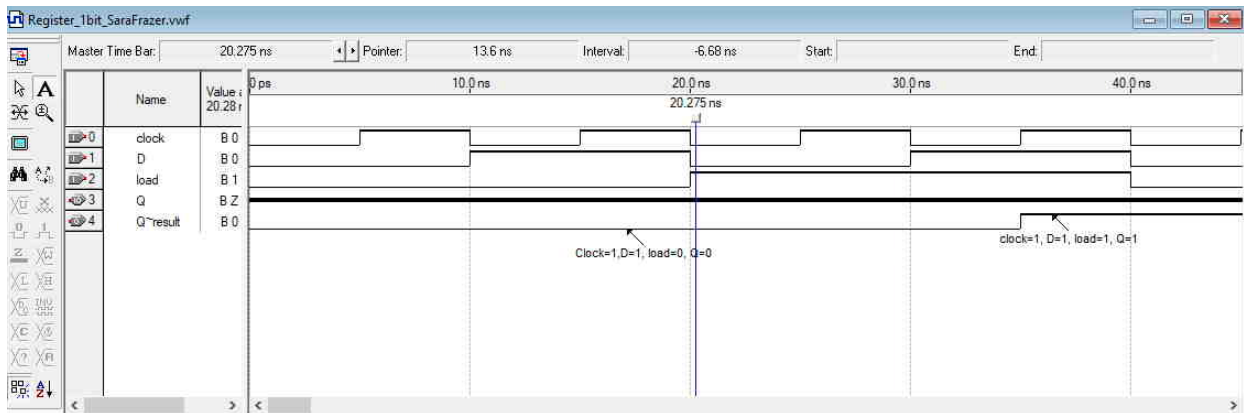


I accidentally cut off the “END Behavior;”

## Successful Compilation



## Timing Diagram



## 2.3 16-Bit Register

### Project Settings

New Project Wizard: Summary [page 5 of 5]



When you click Finish, the project will be created with the following settings:

Project directory:

Z:/LogicDesign/Lab3\_SaraFrazer/

Project name: Register\_16bit\_SaraFrazer

Top-level design entity: Register\_16bit\_SaraFrazer

Number of files added: 2

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3128ATC144-7

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

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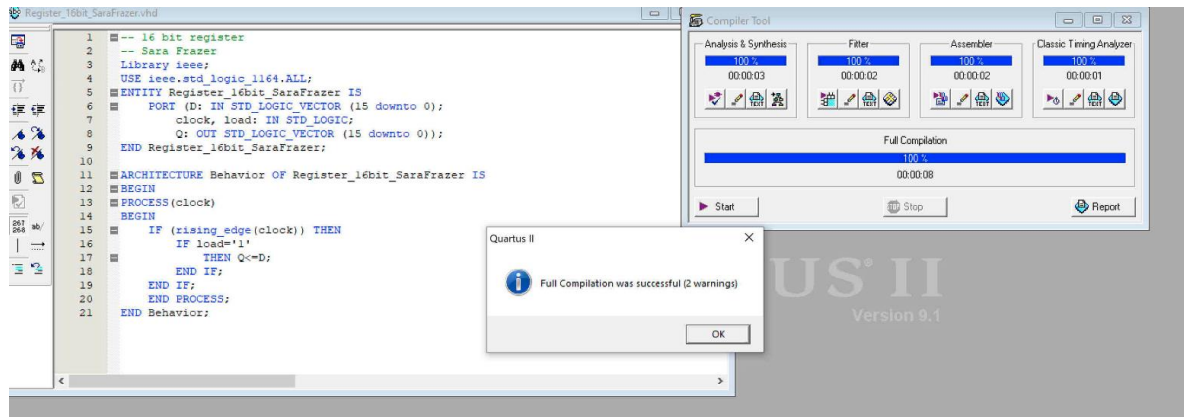
Finish

Cancel

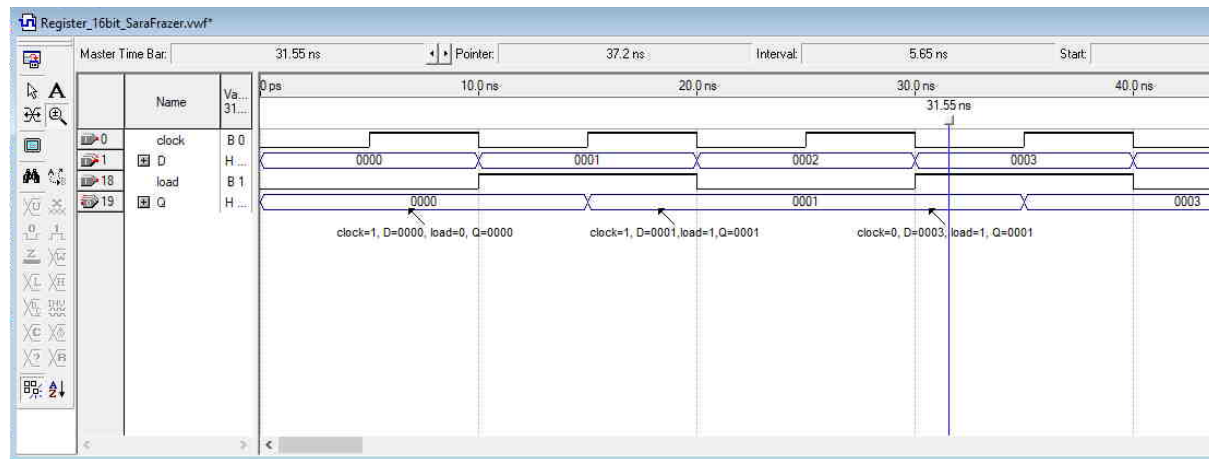
### VHDL

```
1  -- 16 bit register
2  -- Sara Frazer
3  Library ieee;
4  USE ieee.std_logic_1164.ALL;
5  ENTITY Register_16bit_SaraFrazer IS
6  PORT (D: IN STD_LOGIC_VECTOR (15 downto 0);
7        clock, load: IN STD_LOGIC;
8        Q: OUT STD_LOGIC_VECTOR (15 downto 0));
9  END Register_16bit_SaraFrazer;
10
11 ARCHITECTURE Behavior OF Register_16bit_SaraFrazer IS
12 BEGIN
13 PROCESS(clock)
14 BEGIN
15     IF (rising_edge(clock)) THEN
16         IF load='1'
17         THEN Q<=D;
18         END IF;
19     END IF;
20 END PROCESS;
21 END Behavior;
```

## Successful Compilation



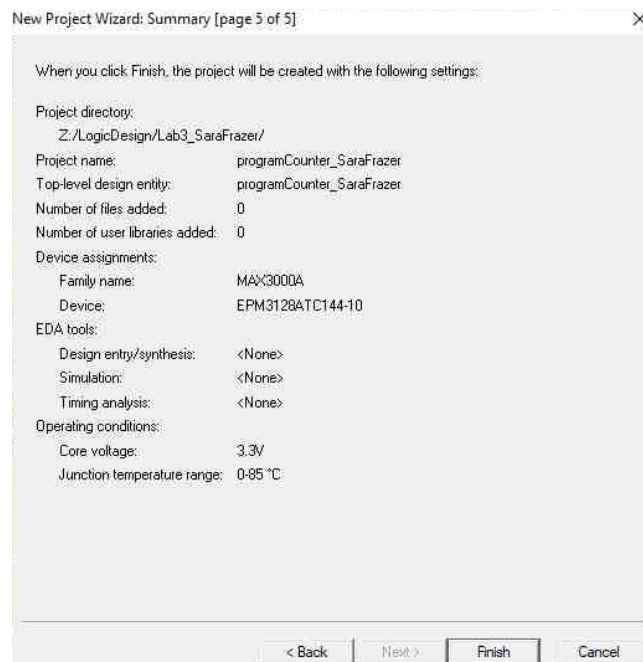
## Timing Diagram



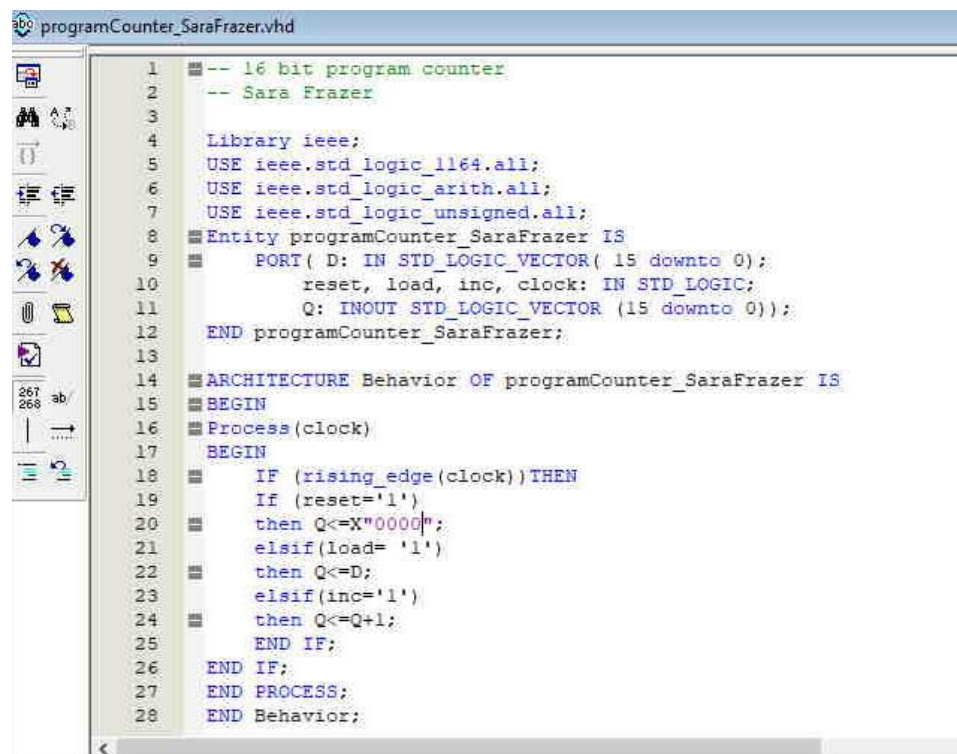


## 2.4 Program Counter Register

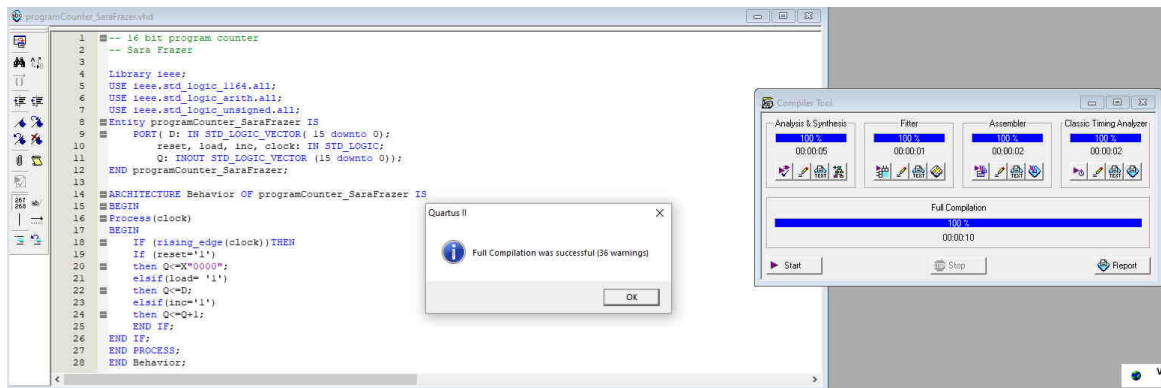
### Project Settings



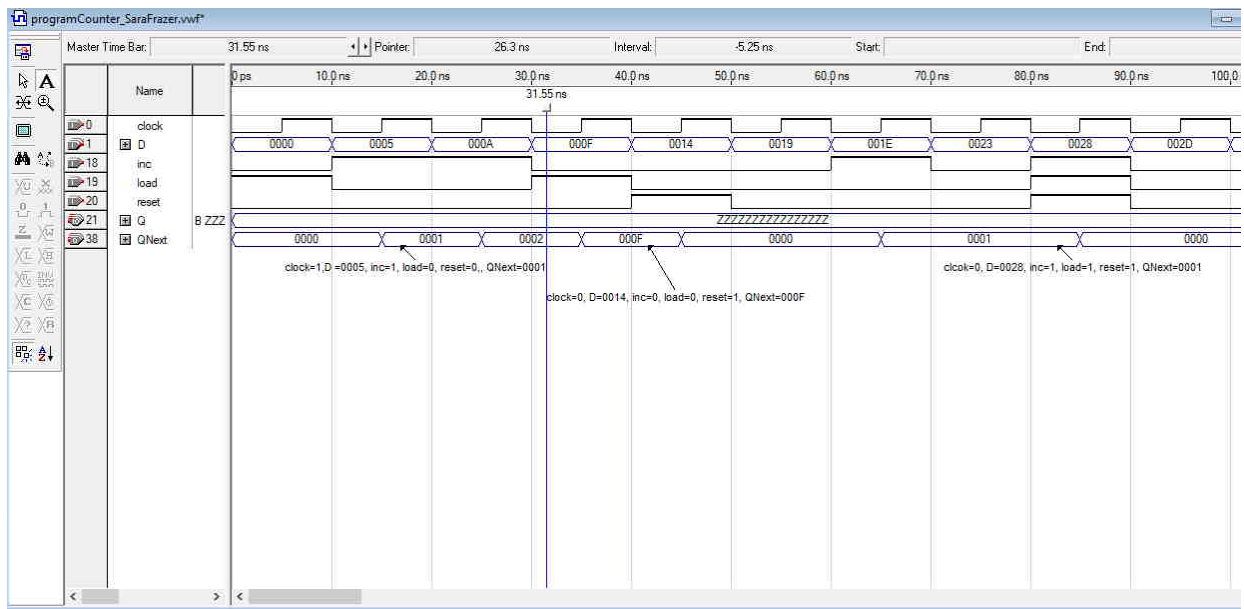
### VHDL Code



## Successful Compilation



## Timing Diagram



## 2.5 8 Register RAM

### Project Settings

New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

Z:/LogicDesign/Lab3\_SaraFrazer/

Project name: RAM\_8Register\_SaraFrazer

Top-level design entity: RAM\_8Register\_SaraFrazer

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: MAX3000A

Device: EPM3128ATC144-10

EDA tools:

Design entry/synthesis: <None>

Simulation: <None>

Timing analysis: <None>

Operating conditions:

Core voltage: 3.3V

Junction temperature range: 0-85 °C

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Finish

Cancel

### VHDL Code

```
1  -- 8 Register RAM Positive Edge Triggered
2  -- Sara Frazer
3  Library ieee;
4  USE ieee.std_logic_1164.ALL;
5  USE ieee.numeric_std.All;
6  ENTITY RAM_8Register_SaraFrazer IS
7  PORT ( D: IN STD_LOGIC_VECTOR(15 downto 0);
8        load, clock: IN STD_LOGIC;
9        address: IN STD_LOGIC_VECTOR(2 downto 0);
10       Q: OUT STD_LOGIC_VECTOR (15 downto 0));
11 END RAM_8Register_SaraFrazer;
12 ARCHITECTURE Behavior OF RAM_8Register_SaraFrazer IS
13     TYPE Array8x16 IS ARRAY (7 downto 0) OF STD_LOGIC_VECTOR (15 downto 0);
14     SIGNAL RAM: Array8x16;
15     SIGNAL index: INTEGER RANGE 0 to 7;
16 BEGIN
17     PROCESS(clock)
18     BEGIN
19         IF(rising_edge(clock)) THEN
20             IF(load='1') THEN
21                 FOR index in 0 to 7 LOOP
22                     RAM(index) <= D;
23                 END LOOP;
24             Q<=D;
25         ELSE
26             FOR index in 0 to 7 LOOP
27                 Q<=RAM(index);
28             END LOOP;
29         END IF;
30     END IF;
31 END process;
32 END behavior;
```

## Successful Compilation

The screenshot displays the Quartus II IDE with the VHDL source code for `RAM_SRegister_SaraFrazer.vhd` on the left. The code defines an 8-bit register with a positive edge-triggered clock and a 16-bit RAM array. The right pane shows the **Compiler Tool** window with the following progress bars:

- Analysis & Synthesis: 100% (00:00:04)
- Filter: 100% (00:00:02)
- Assembler: 100% (00:00:02)
- Classic Timing Analyzer: 100% (00:00:01)
- Full Compilation: 100% (00:00:09)

A **Quartus II** dialog box in the center confirms: "Full Compilation was successful (7 warnings)".

## Timing Diagram

