

# Mini Project

## Spartan6 DSP48A1

Name

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Group

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## Code

### 1. DSP48A1\_D\_BLOCK

```
module DSP48A1_D_BLOCK (D, rst, clk, En, out);
parameter WIDTH = 18;
parameter REG = 1;
parameter RSTTYPE = "SYNC";
input [WIDTH-1:0] D;
input clk, rst, En;
output [WIDTH-1:0] out;
reg [WIDTH-1:0] out_reg;
generate
    if (RSTTYPE == "SYNC") begin
        always @(posedge clk) begin
            if (rst)
                out_reg <= 0;
            else if (En)
                out_reg <= D;
        end
    end
    else if (RSTTYPE == "ASYNC") begin
        always @(posedge clk or posedge rst) begin
            if (rst)
                out_reg <= 0;
            else if (En)
                out_reg <= D;
        end
    end
endgenerate
assign out = (REG)? out_reg:D;
endmodule
```

## 2. DSP48A1

```
module DSP48A1 (
    A, B, D, C, Clk, Carryin, Opmode, Bcin, RstA, RstB, RstM, RstP, RstD, RstC, RstCarryin, RstOpmode,
    CEA, CEB, CEM, CEP, CEC, CED, CECarryin, CEOpmode, Pcin, Bcout, Pcout, P, M, Carryout, CarryoutF
);

// Parameter to configure the registers
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";

// Input ports
input [17:0] A, B, D, Bcin;
input [47:0] C, Pcin;
input [7:0] Opmode;
input Clk, Carryin, RstA, RstB, RstM, RstP, RstD, RstC, RstCarryin, RstOpmode,
    CEA, CEB, CEM, CEP, CEC, CED, CECarryin, CEOpmode;

// Output ports
output [17:0] Bcout;
output [47:0] Pcout, P;
output [35:0] M;
output Carryout, CarryoutF;

wire [17:0] A0_reg;
// Register pipeline for A input
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(A0REG), .RSTTYPE(RSTTYPE)) m1(.D(A), .rst(RstA), .clk(Clk), .En(CEA), .out(A0_reg));

wire [17:0] D_reg;
// Register pipeline for D input
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(DREG), .RSTTYPE(RSTTYPE)) m2(.D(D), .rst(RstD), .clk(Clk), .En(CED), .out(D_reg));

wire [47:0] C_reg;
// Register pipeline for C input
DSP48A1_D_BLOCK #(.WIDTH(48), .REG(CREG), .RSTTYPE(RSTTYPE)) m3(.D(C), .rst(RstC), .clk(Clk), .En(CEC), .out(C_reg));

wire [17:0] B0_reg;
// Conditional generation for B input
generate
    // Direct B input mode
    if (B_INPUT == "DIRECT")
        DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B0REG), .RSTTYPE(RSTTYPE)) m5(.D(B), .rst(RstB), .clk(Clk), .En(CEB), .out(B0_reg));
    // Cascade B input mode
    else if (B_INPUT == "CASCADE")
        DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B0REG), .RSTTYPE(RSTTYPE)) m6(.D(Bcin), .rst(RstB), .clk(Clk), .En(CEB), .out(B0_reg));
endgenerate

wire [17:0] A1_reg;
// Register pipeline for A1
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(A1REG), .RSTTYPE(RSTTYPE)) m7(.D(A0_reg), .rst(RstA), .clk(Clk), .En(CEA), .out(A1_reg));

wire [7:0] Opmode_reg;
// Register pipeline for Opmode
DSP48A1_D_BLOCK #(.WIDTH(8), .REG(OPMODEREG), .RSTTYPE(RSTTYPE)) m8(.D(Opmode), .rst(RstOpmode), .clk(Clk), .En(CEOpmode), .out(Opmode_reg));

wire [17:0] add_or_sub_reg;
// add or subtract logic based on Opmode
assign add_or_sub_reg = (Opmode_reg[6])? (D_reg - B0_reg):(D_reg + B0_reg);

wire [17:0] B_or_Preaddingsub;
// Select between B or Pre-add/Sub based on Opmode
assign B_or_Preaddingsub = (Opmode_reg[4])? add_or_sub_reg:B0_reg;

wire [17:0] B1_reg;
// Register pipeline for B1
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B1REG), .RSTTYPE(RSTTYPE)) m9(.D(B_or_Preaddingsub), .rst(RstB), .clk(Clk), .En(CEB), .out(B1_reg));
```

### 3. DSP48A1(Cont'd)

```
// Assign Bcout
assign Bcout = B1_reg;

wire [35:0] mul_reg;
// Multiplication logic
assign mul_reg = A1_reg * B1_reg;

wire [35:0] M_reg;
// Register pipeline for M
DSP48A1_D_BLOCK #(.WIDTH(36), .REG(MREG), .RSTTYPE(RSTTYPE)) m10(.D(mul_reg), .rst(RstM), .clk(Clk), .En(CEM), .out(M_reg));

generate
    genvar i;
    for(i=0; i<36; i=i+1)
        buf(M[i], M_reg[i]);
endgenerate

wire [47:0] conc_DAB;
// Concatenate inputs D, A, and B
assign conc_DAB = {D, A, B};

reg [47:0] X_out;
// X_out logic based on Opmode
always @(*) begin
    case (Opmode_reg[1:0])
        0: X_out = 0;
        1: X_out = mul_reg;
        2: X_out = P;
        3: X_out = conc_DAB;
    endcase
end

reg [47:0] Z_out;
// Z_out logic based on Opmode
always @(*) begin
    case (Opmode_reg[3:2])
        0: Z_out = 0;
        1: Z_out = Pcin;
        2: Z_out = P;
        3: Z_out = C_reg;
    endcase
end

endcase
end

wire Opmode_Carry;
// Opmode carry logic
assign Opmode_Carry = (CARRYINSEL == "CARRYIN")? Carryin:(CARRYINSEL == "OPMODES")? Opmode_reg[5]:0;

wire CIN;
// Register pipeline for carry-in
DSP48A1_D_BLOCK #(.WIDTH(1), .REG(CARRYINREG), .RSTTYPE(RSTTYPE)) m11(.D(Opmode_Carry), .rst(RstCarryin), .clk(Clk), .En(CECarryin), .out(CIN));

wire Carryout_reg;
wire [47:0] add_or_sub_outreg;
// Addition or subtraction based on Opmode
assign {Carryout_reg, add_or_sub_outreg} = (Opmode_reg[7])? (Z_out - (X_out + CIN)):(X_out + Z_out + CIN);

// Register pipeline for carry-out
DSP48A1_D_BLOCK #(.WIDTH(1), .REG(CARRYOUTREG), .RSTTYPE(RSTTYPE)) m12(.D(Carryout_reg), .rst(RstCarryin), .clk(Clk), .En(CECarryin), .out(Carryout));
assign CarryoutF = Carryout;

// Register pipeline for Pcout
DSP48A1_D_BLOCK #(.WIDTH(48), .REG(PREG), .RSTTYPE(RSTTYPE)) m13(.D(add_or_sub_outreg), .rst(RstP), .clk(Clk), .En(CEP), .out(P));
assign Pcout = P;

endmodule
```

## Test bench

```
module DSP48A1_tb ();
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";
reg [17:0] A_tb, B_tb, D_tb, Bcin_tb;
reg [47:0] C_tb, Pcin_tb;
reg [7:0] Opmode_tb;
reg Clk_tb, Carryin_tb, RstA_tb, RstB_tb, RstM_tb, RstP_tb, RstD_tb, RstC_tb, RstCarryin_tb, RstOpmode_tb,
CEA_tb, CEB_tb, CEM_tb, CEP_tb, CEC_tb, CED_tb, CECarryin_tb, CEOpmode_tb;
wire [17:0] Bcout_dut;
wire [47:0] Pcout_dut, P_dut;
wire [35:0] M_dut;
wire Carryout_dut, CarryoutF_dut;

DSP48A1 #(
    .A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG),
    .CREG(CREG), .DREG(DREG), .MREG(MREG), .PREG(PREG),
    .CARRYINREG(CARRYINREG), .CARRYOUTREG(CARRYOUTREG), .OPMODEREG(OPMODEREG),
    .CARRYINSEL(CARRYINSEL), .B_INPUT(B_INPUT), .RSTTYPE(RSTTYPE)
)
dut(
    .A(A_tb), .B(B_tb), .D(D_tb), .C(C_tb),
    .Clk(Clk_tb), .Carryin(Carryin_tb), .Opmode(Opmode_tb),
    .Bcin(Bcin_tb), .RstA(RstA_tb), .RstB(RstB_tb), .RstM(RstM_tb),
    .RstP(RstP_tb), .RstD(RstD_tb), .RstC(RstC_tb), .RstCarryin(RstCarryin_tb),
    .RstOpmode(RstOpmode_tb), .CEA(CEA_tb), .CEB(CEB_tb), .CEM(CEM_tb),
    .CEP(CEP_tb), .CEC(CEC_tb), .CED(CED_tb), .CECarryin(CECarryin_tb),
    .CEOpmode(CEOpmode_tb), .Pcin(Pcin_tb), .Bcout(Bcout_dut), .Pcout(Pcout_dut),
    .P(P_dut), .M(M_dut), .Carryout(Carryout_dut), .CarryoutF(CarryoutF_dut)
);

initial begin
    Clk_tb = 1;
    forever
        #1 Clk_tb = ~Clk_tb;
end

initial begin
    // Initialize all control signals
    A_tb = 0;
    B_tb = 0;
    C_tb = 0;
    D_tb = 0;
    Bcin_tb = 0;
    Pcin_tb = 0;
    Opmode_tb = 0;
    Carryin_tb = 0;
    RstA_tb = 0;
    RstB_tb = 0;
    RstM_tb = 0;
    RstP_tb = 0;
    RstD_tb = 0;
    RstC_tb = 0;
    RstCarryin_tb = 0;
    RstOpmode_tb = 0;
    CEA_tb = 0;
    CEB_tb = 0;
    CEM_tb = 0;
    CEP_tb = 0;
    CEC_tb = 0;
    CED_tb = 0;
    CECarryin_tb = 0;
    CEOpmode_tb = 0;

    // Test rest
    RstA_tb = 1;
    RstB_tb = 1;
    RstM_tb = 1;
    RstP_tb = 1;
    RstD_tb = 1;
    RstC_tb = 1;
    RstCarryin_tb = 1;
    RstOpmode_tb = 1;
    repeat(10) @(negedge Clk_tb);

    // Release reset and enable all stages
    RstA_tb = 0;
    RstB_tb = 0;
    RstM_tb = 0;
    RstP_tb = 0;
    RstD_tb = 0;
    RstC_tb = 0;
    RstCarryin_tb = 0;
    RstOpmode_tb = 0;
    CEA_tb = 1;
end
```

## Test bench (Cont'd)

```
CEB_tb = 1;
CEM_tb = 1;
CEP_tb = 1;
CEC_tb = 1;
CED_tb = 1;
CECarryin_tb = 1;
CEOpmode_tb = 1;
repeat(10) @(negedge Clk_tb);

// Test Case 1: Simple addition
A_tb = 15;
B_tb = 20;
C_tb = 10;
D_tb = 30;
Carryin_tb = 0;
Bcin_tb = 5;
Pcin_tb = 10;
Opmode_tb = 8'b01101111; // Set Opmode for addition
repeat(10) @(negedge Clk_tb);

// Test Case 2: Subtraction
A_tb = 60;
B_tb = 10;
C_tb = 35;
D_tb = 40;
Opmode_tb = 8'b01010100; // Set Opmode for subtraction
repeat(10) @(negedge Clk_tb);

// Test Case 3: Multiply with Carry-in
A_tb = 30;
B_tb = 10;
C_tb = 100;
D_tb = 30;
Opmode_tb = 8'b00101010; // Set Opmode for multiplication with carry-in
repeat(10) @(negedge Clk_tb);

// Test Case 4: Accumulation
A_tb = 35;
B_tb = 30;
C_tb = 100;
D_tb = 30;
Carryin_tb = 1;
Pcin_tb = 10;
Opmode_tb = 8'b10001101; // Set Opmode for accumulation
repeat(10) @(negedge Clk_tb);
```

```
// Test Case 5: chained operation
A_tb = 25;
B_tb = 40;
C_tb = 150;
D_tb = 30;
Carryin_tb = 0;
Opmode_tb = 8'b01111111; // Set Opmode for multiplication with carry-in
repeat(10) @(negedge Clk_tb);

// Test Case 6: Cascade B input
Bcin_tb = 15;
B_tb = 30;
C_tb = 250;
D_tb = 15;
Carryin_tb = 0;
Opmode_tb = 8'b11000010; // Set Opmode for using cascade input
repeat(10) @(negedge Clk_tb);

// Test Case 7: complex operation
A_tb = 20;
B_tb = 15;
C_tb = 200;
D_tb = 30;
Carryin_tb = 1;
Opmode_tb = 8'b10101010; // Set Opmode for pre-addition
repeat(10) @(negedge Clk_tb);

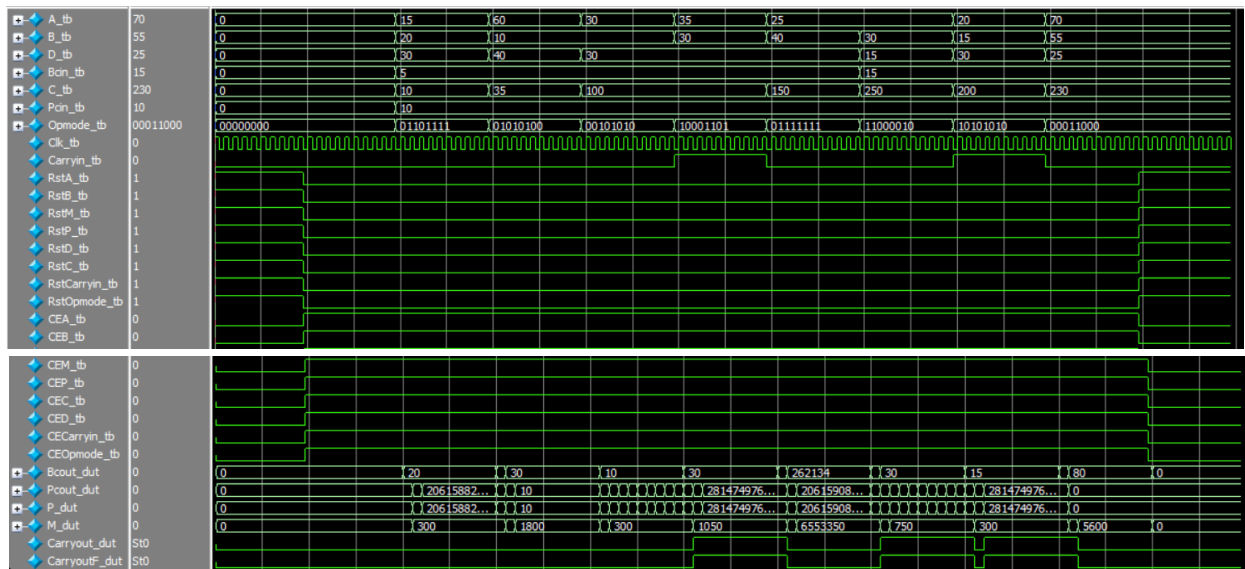
// Test Case 8: complex operation
A_tb = 70;
B_tb = 55;
C_tb = 230;
D_tb = 25;
Carryin_tb = 0;
Opmode_tb = 8'b00011000; // Set Opmode for pre-addition
repeat(10) @(negedge Clk_tb);

// reset and unenable all stages
RstA_tb = 1;
RstB_tb = 1;
RstM_tb = 1;
RstP_tb = 1;
RstD_tb = 1;
RstC_tb = 1;
RstCarryin_tb = 1;
RstOpmode_tb = 1;
CEA_tb = 0;
CEB_tb = 0;
CEM_tb = 0;
```

```
CEP_tb = 0;
CEC_tb = 0;
CED_tb = 0;
CECarryin_tb = 0;
CEOpmode_tb = 0;
repeat(10) @(negedge Clk_tb);
$stop;
end

initial begin
    $monitor("A = %d, B = %d, C = %d, D = %d, Carryin = %b, Bcin = %d, Pcin = %d, Opmode = %b, M = %d, P = %d, Carryout = %b, CarryoutF = %b",
        A_tb, B_tb, C_tb, D_tb, Carryin_tb, Bcin_tb, Pcin_tb, Opmode_tb, M_dut, P_dut, Carryout_dut, CarryoutF_dut);
end
endmodule
```

## Simulation



**Do file**

```
vlib work
vlog DSP48A1.v DSP48A1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -sim
```

## Constrain

```
# Clock signal
set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports Clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports Clk]
```

```

create_debug_port u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_CNT_1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property CLK_STOP_OPM false [get_debug_cores u_ila_0]
set_property C_INIT_FIVE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGGER_EN false [get_debug_cores u_ila_0]
set_property C_TRIGGER_IN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/cik]
connect_debug_port u_ila_0/cik [get_nets [list CLK_HUB_RNG]]
set_property PROBE_TYPE DATA and TRIGGER [get_debug_ports u_ila_0/probe]
set_property port_width 1 [get_debug_ports u_ila_0/probe]
create_debug_port u_ila_0/probe
set_property PROBE_TYPE DATA and TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 1 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list (D_0BUF[0]) (D_0BUF[1]) (D_0BUF[2]) (D_0BUF[3]) (D_0BUF[4]) (D_0BUF[5]) (D_0BUF[6]) (D_0BUF[7]) (D_0BUF[8]) (D_0BUF[9]) (D_0BUF[10]) (D_0BUF[11]) (D_0BUF[12]) (D_0BUF[13]) (D_0BUF[14]) (D_0BUF[15]) (D_0BUF[16]) (D_0BUF[17]) (D_0BUF[18]) (D_0BUF[19]) (D_0BUF[20]) (D_0BUF[21]) (D_0BUF[22]) (D_0BUF[23]) (D_0BUF[24]) (D_0BUF[25]) (D_0BUF[26]) (D_0BUF[27]) (D_0BUF[28]) (D_0BUF[29]) (D_0BUF[30]) (D_0BUF[31]) (D_0BUF[32]) (D_0BUF[33]) (D_0BUF[34]) (D_0BUF[35]) (D_0BUF[36]) (D_0BUF[37]) (D_0BUF[38]) (D_0BUF[39]) (D_0BUF[40]) (D_0BUF[41]) (D_0BUF[42]) (D_0BUF[43]) (D_0BUF[44]) (D_0BUF[45]) (D_0BUF[46]) (D_0BUF[47]) (D_0BUF[48]) (D_0BUF[49]) (D_0BUF[50]) (D_0BUF[51]) (D_0BUF[52]) (D_0BUF[53]) (D_0BUF[54]) (D_0BUF[55]) (D_0BUF[56]) (D_0BUF[57]) (D_0BUF[58]) (D_0BUF[59]) (D_0BUF[60]) (D_0BUF[61]) (D_0BUF[62]) (D_0BUF[63]) (D_0BUF[64]) (D_0BUF[65]) (D_0BUF[66]) (D_0BUF[67]) (D_0BUF[68]) (D_0BUF[69]) (D_0BUF[70]) (D_0BUF[71]) (D_0BUF[72]) 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(D_0BUF[146]) (D_0BUF[147]) (D_0BUF[148]) (D_0BUF[149]) (D_0BUF[150]) (D_0BUF[151]) (D_0BUF[152]) (D_0BUF[153]) (D_0BUF[154]) (D_0BUF[155]) (D_0BUF[156]) (D_0BUF[157]) (D_0BUF[158]) (D_0BUF[159]) (D_0BUF[160]) (D_0BUF[161]) (D_0BUF[162]) (D_0BUF[163]) (D_0BUF[164]) (D_0BUF[165]) (D_0BUF[166]) (D_0BUF[167]) (D_0BUF[168]) (D_0BUF[169]) (D_0BUF[170]) (D_0BUF[171]) (D_0BUF[172]) (D_0BUF[173]) (D_0BUF[174]) (D_0BUF[175]) (D_0BUF[176]) (D_0BUF[177]) (D_0BUF[178]) (D_0BUF[179]) (D_0BUF[180]) (D_0BUF[181]) (D_0BUF[182]) (D_0BUF[183]) (D_0BUF[184]) (D_0BUF[185]) (D_0BUF[186]) (D_0BUF[187]) (D_0BUF[188]) (D_0BUF[189]) (D_0BUF[190]) (D_0BUF[191]) (D_0BUF[192]) (D_0BUF[193]) (D_0BUF[194]) (D_0BUF[195]) (D_0BUF[196]) (D_0BUF[197]) (D_0BUF[198]) (D_0BUF[199]) (D_0BUF[200]) (D_0BUF[201]) (D_0BUF[202]) (D_0BUF[203]) (D_0BUF[204]) (D_0BUF[205]) (D_0BUF[206]) (D_0BUF[207]) (D_0BUF[208]) (D_0BUF[209]) (D_0BUF[210]) (D_0BUF[211]) (D_0BUF[212]) (D_0BUF[213]) (D_0BUF[214]) (D_0BUF[215]) (D_0BUF[216]) (D_0BUF[217]) (D_0BUF[218]) (D_0BUF[219]) (D_0BUF[220]) (D_0BUF[221]) (D_0BUF[222]) (D_0BUF[223]) (D_0BUF[224]) (D_0BUF[225]) (D_0BUF[226]) (D_0BUF[227]) (D_0BUF[228]) (D_0BUF[229]) (D_0BUF[230]) (D_0BUF[231]) (D_0BUF[232]) (D_0BUF[233]) (D_0BUF[234]) (D_0BUF[235]) (D_0BUF[236]) (D_0BUF[237]) (D_0BUF[238]) (D_0BUF[239]) (D_0BUF[240]) (D_0BUF[241]) (D_0BUF[242]) (D_0BUF[243]) (D_0BUF[244]) (D_0BUF[245]) (D_0BUF[246]) (D_0BUF[247]) (D_0BUF[248]) (D_0BUF[249]) (D_0BUF[250]) (D_0BUF[251]) (D_0BUF[252]) (D_0BUF[253]) (D_0BUF[254]) (D_0BUF[255]) (D_0BUF[256]) (D_0BUF[257]) (D_0BUF[258]) (D_0BUF[259]) (D_0BUF[260]) (D_0BUF[261]) (D_0BUF[262]) (D_0BUF[263]) (D_0BUF[264]) (D_0BUF[265]) (D_0BUF[266]) (D_0BUF[267]) (D_0BUF[268]) (D_0BUF[269]) (D_0BUF[270]) (D_0BUF[271]) (D_0BUF[272]) (D_0BUF[273]) (D_0BUF[274]) (D_0BUF[275]) (D_0BUF[276]) (D_0BUF[277]) (D_0BUF[278]) (D_0BUF[279]) (D_0BUF[280]) (D_0BUF[281]) (D_0BUF[282]) (D_0BUF[283]) (D_0BUF[284]) (D_0BUF[285]) (D_0BUF[286]) (D_0BUF[287]) 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```

## Constrain (cont'd)

```

create_debug_port u_ila_0 probe1
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 1 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe2
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 1 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe3
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 1 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list CECarryin_IBUF]]
create_debug_port u_ila_0 probe4
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 1 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe5
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 1 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe6
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 1 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list CE0pmode_IBUF]]
create_debug_port u_ila_0 probe7
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 1 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe8
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 1 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list CLK_IBUF]]
create_debug_port u_ila_0 probe9
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list RStA_IBUF]]
create_debug_port u_ila_0 probe20
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RStB_IBUF]]
create_debug_port u_ila_0 probe21
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RStC_IBUF]]
create_debug_port u_ila_0 probe22
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RStCarryin_IBUF]]
create_debug_port u_ila_0 probe23
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RStD_IBUF]]
create_debug_port u_ila_0 probe24
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RStM_IBUF]]
create_debug_port u_ila_0 probe25
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RSt0pmode_IBUF]]
create_debug_port u_ila_0 probe26
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RStP_IBUF]]
set_property CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property CLK_DIV_FACTOR 100 [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets CLK_IBUF]

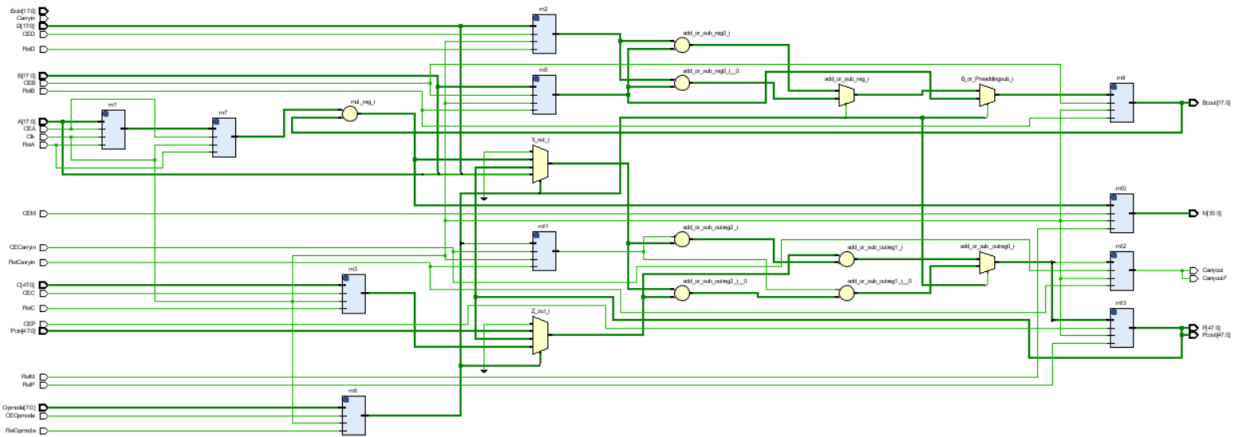
```

## Monitor

#	A	0	B	=	70	C	=	0	D	=	0	, CarryIn =	0	, Bein	=	0	, Pcin	=	0	, Opande	=	00000000, M	=	0	, P	P	=	0	, Carryout	=	0	, CarryoutF	=	0
#	A	=	15	, B	=	20	, C	=	10	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01101111, M	=	300	, P	=	2061898234270	, Carryout	=	0	, CarryoutF	=	0
#	A	=	15	, B	=	20	, C	=	30	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01101111, M	=	300	, P	=	2061898234270	, Carryout	=	0	, CarryoutF	=	0
#	A	=	60	, B	=	10	, C	=	35	, D	=	40	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	2061898234270	, Carryout	=	0	, CarryoutF	=	0
#	A	=	60	, B	=	10	, C	=	35	, D	=	40	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	274877476101	, Carryout	=	0	, CarryoutF	=	0
#	A	=	60	, B	=	10	, C	=	35	, D	=	40	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	274877476101	, Carryout	=	0	, CarryoutF	=	0
#	A	=	60	, B	=	10	, C	=	35	, D	=	40	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	1800	, P	=	10	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	1000	, P	=	10	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	1000	, P	=	20	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	41	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	83	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	100	, P	=	10	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	335	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	671	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	134	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	2487	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	01010100, M	=	300	, P	=	5375	, Carryout	=	0	, CarryoutF	=	0
#	A	=	30	, B	=	10	, C	=	100	, D	=	30	, CarryIn =	0	, Bein	=	5	, Pcin	=	10	, Opande	=	00001101, M	=	300	, P	=	837						



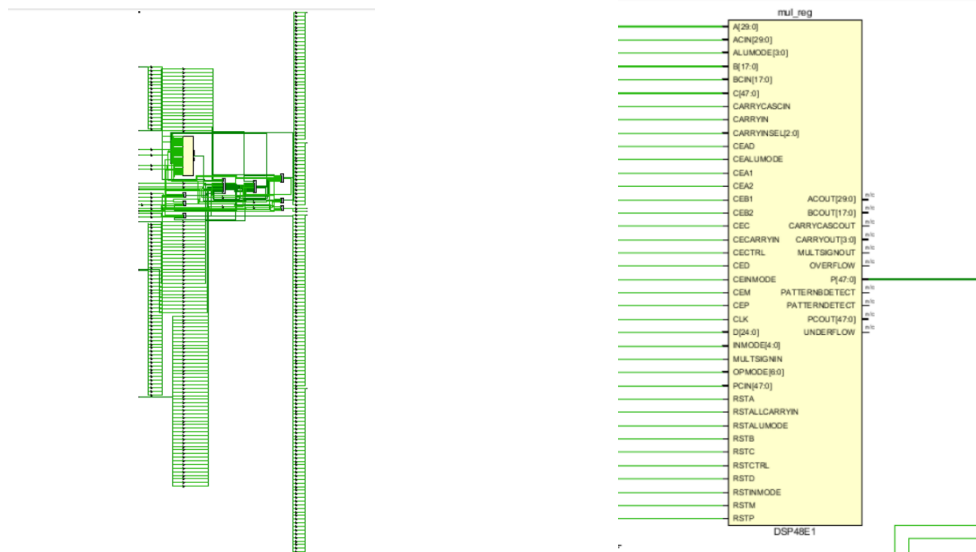
## Elaboration schematic



## RTL message

- Vivado Commands (3 infos)
  - General Messages (3 infos)
      - [IP\_Flow 19-234] Refreshing IP repositories
      - [IP\_Flow 19-1704] No user IP repositories specified
      - [IP\_Flow 19-2313] Loaded Vivado IP repository 'G:\Vivado3\Vivado\2018.2\data\ip'.
  - Elaborated Design (18 infos)
    - General Messages (18 infos)
      - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)
      - [Synth 8-6155] done synthesizing module 'DSP48A1\_D\_BLOCK' (1#1) [DSP48A1\_D\_BLOCK.v:1] (6 more like this)
      - [Device 21-403] Loading part xc7a200tfg1156-3
      - [Project 1-570] Preparing netlist for logic optimization
      - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
      - [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.

## Synthesis schematic

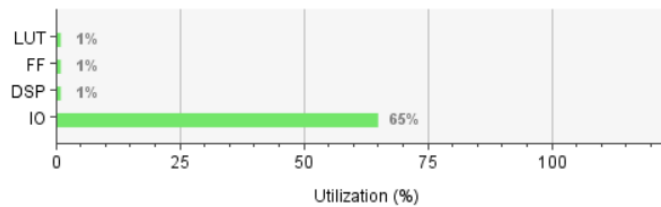


## Synthesis message

- ▼ Synthesis (29 Infos)
  - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
  - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v.1] (6 more like this)
  - [Synth 8-6155] done synthesizing module 'DSP48A1\_D\_BLOCK' (1#1) [DSP48A1\_D\_BLOCK.v.1] (6 more like this)
  - [Device 21-403] Loading part xc7a200t#g1156-3
  - [Synth 8-5818] HDL\_ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1.v.68] (1 more like this)
  - [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP48A1\_D\_BLOCK.v.13]
  - [Project 1-571] Translating synthesized netlist
  - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-570] Preparing netlist for logic optimization
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.
  - [Common 17-83] Releasing license: Synthesis
  - [Common 17-1381] The checkpoint 'G:/Sarah/Digital\_Course/digital\_course\_models/mini\_proj/project\_MINI/project\_MINI.runs/synth\_1/DSP48A1.dcp' has been generated.
  - [runtcl-4] Executing : report\_utilization -file DSP48A1\_utilization\_synth.rpt -pb DSP48A1\_utilization\_synth.pb
  - [Common 17-206] Exiting Vivado at Tue Jul 30 00:39:56 2024...
- ▼ Synthesized Design (6 Infos)
  - ▼ General Messages (6 Infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.

## Synthesis Utilization

Resource	Utilization	Available	Utilization %
LUT	231	134600	0.17
FF	178	269200	0.07
DSP	1	740	0.14
IO	327	500	65.40

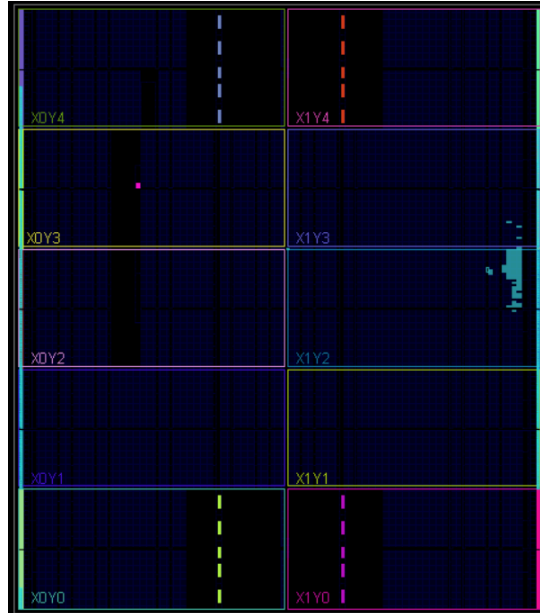


## Synthesis Timing

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA
Total Number of Endpoints: 741	Total Number of Endpoints: 741	Total Number of Endpoints: NA

There are no user specified timing constraints.

## Implementation Schematic

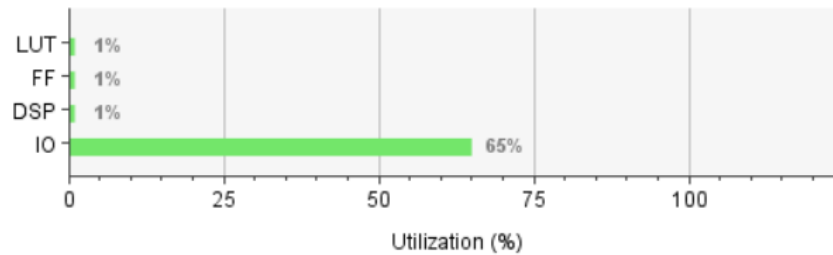


## Implementation message

```
Implementation (75 info)
  Design Initiation (7 info)
    [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    [Netlist 29-26] Unisim Transformation completed in 1 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Device 21-403] Loading part xc7a200tfg1156-3
    [Project 1-570] Preparing netlist for logic optimization
    [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    [Project 1-694] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  Opt Design (23 info)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    [Project 1-461] DRC finished with 0 Errors
    [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    [Timing 38-35] Done setting XDC timing constraints.
    [Opt 31-148] Retargeted 0 cells.
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pins. (1 more like this)
    [Opt 31-369] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    [Opt 31-652] Phase BUF optimization created 0 cells of which 0 are BUFs and removed 0 cells.
    [Pwprot 34-132] Skipping clock gating for clocks with a period > 2.00 ns.
    [Common 17-43] Releasing license: Implementation
    [Common 17-138] The checkpoint 'G:\Sarah\Digital_Course\digital_course_modelsimmini_proj\project_MH\project_MH\nrunsimpt_1\DSP48A1_opt.dcp' has been generated.
    [Junit4-4] Executing: report_drc -file DSP48A1_drc_opted.rpt -ps DSP48A1_drc_opted.rpt -rpt DSP48A1_drc_opted.rpt
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'G:\Vivado\2018.2\ipdata\'.
    [DRC 23-27] Running DRC with 2 threads (1 more like this)
    [Corebit 2-168] The results of DRC are in file DSP48A1_drc_opted.rpt
  Place Design (16 info)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    [DRC 23-27] Running DRC with 2 threads (1 more like this)
    [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
    [Place 38-511] Multithreading enabled for place_design using a maximum of 2 CPUs
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pins. (1 more like this)
    [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
    [Common 17-43] Releasing license: Implementation
    [Common 17-138] The checkpoint 'G:\Sarah\Digital_Course\digital_course_modelsimmini_proj\project_MH\project_MH\nrunsimpt_1\DSP48A1_placed.dcp' has been generated.
    [Junit4-4] Executing: report_drc -file DSP48A1_placed.rpt (2 more like this)
  Route Design (23 info)
    [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    [Vivado_Tcl 4-198] DRC finished with 0 Errors
    [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
    [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
    [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.
    [Route 35-16] Router Completed Successfully
    [Common 17-43] Releasing license: Implementation
    [Common 17-138] The checkpoint 'G:\Sarah\Digital_Course\digital_course_modelsimmini_proj\project_MH\project_MH\nrunsimpt_1\DSP48A1_routed.dcp' has been generated.
    [DRC 23-27] Running DRC with 2 threads (1 more like this)
    [Corebit 2-168] The results of DRC are in file DSP48A1_drc_routed.rpt
    [Junit4-4] Executing: report_drc -file DSP48A1_drc_routed.rpt -ps DSP48A1_drc_routed.rpt -rpt DSP48A1_drc_routed.rpt (7 more like this)
    [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
    [DRC 23-133] Running Methodology with 2 threads
    [Corebit 2-1526] The results of Report Methodology are in file DSP48A1_methodology_drc_routed.rpt
    [Vivado_Tcl 4-445] No incremental route to report, no incremental placement and routing data was found.
    [Timing 38-915] UpdateTimingParams: Speed grade -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
    [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
  Implemented Design (5 info)
    General Messages (5 info)
      [Netlist 29-17] Analyzing 207 Unisim elements for replacement
      [Netlist 29-26] Unisim Transformation completed in 0 CPU seconds
      [Project 1-479] Netlist was created with Vivado 2018.2
      [Project 1-570] Preparing netlist for logic optimization
      [Project 1-111] Unisim Transformation Summary:
        No Unisim elements were transformed.
```

## Implementation Utilization

Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	179	269200	0.07
DSP	1	740	0.14
IO	327	500	65.40



## Implementation Timing

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA
Total Number of Endpoints: 744	Total Number of Endpoints: 744	Total Number of Endpoints: NA

There are no user specified timing constraints.

## NO ERRORS Checks