Mini Project
Spartan6 DSP48A1

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Code

1. DSP48A1_D_BLOCK

```
module DSP48A1_D_BLOCK (D, rst, clk, En, out);
parameter WIDTH = 18;
parameter REG = 1;
parameter RSTTYPE = "SYNC";
input [WIDTH-1:0] D;
input clk, rst, En;
output [WIDTH-1:0] out;
reg [WIDTH-1:0] out_reg;
generate
    if (RSTTYPE == "SYNC") begin
        always @(posedge clk) begin
            if (rst)
                out_reg <= 0;
            else if (En)
                out_reg <= D;
        end
    end
    else if (RSTTYPE == "ASYNC") begin
        always @(posedge clk or posedge rst) begin
            if (rst)
                out_reg <= 0;
            else if (En)
                out_reg <= D;
        end
    end
endgenerate
assign out = (REG)? out_reg:D;

endmodule
```

2. DSP48A1

```
module DSP48A1 (
    A, B, D, C, Clk, Carryin, Opmode, Bcin, RstA, RstB, RstM, RstP, RstD, RstC, RstCarryin, RstOpmode,
    CEA, CEB, CEM, CEP, CEC, CED, CECarryin, CEOpmode, Pcin, Bcout, Pcout, P, M, Carryout, CarryoutF
);

// Parameter to configure the registers
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";

// Input ports
input [17:0] A, B, D, Bcin;
input [47:0] C, Pcin;
input [7:0] Opmode;
input Clk, Carryin, RstA, RstB, RstM, RstP, RstD, RstC, RstCarryin, RstOpmode,
CEA, CEB, CEM, CEP, CEC, CED, CECarryin, CEOpmode;

// Output ports
output [17:0] Bcout;
output [47:0] Pcout, P;
output [35:0] M;
output Carryout, CarryoutF;

wire [17:0] A0_reg;
// Register pipeline for A input
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(A0REG), .RSTTYPE(RSTTYPE)) m1(.D(A), .rst(RstA), .clk(Clk), .En(CEA), .out(A0_reg));
```

```
wire [17:0] D_reg;
// Register pipeline for D input
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(DREG), .RSTTYPE(RSTTYPE)) m2(.D(D), .rst(RstD), .clk(Clk), .En(CED), .out(D_reg));

wire [47:0] C_reg;
// Register pipeline for C input
DSP48A1_D_BLOCK #(.WIDTH(48), .REG(CREG), .RSTTYPE(RSTTYPE)) m3(.D(C), .rst(RstC), .clk(Clk), .En(CEC), .out(C_reg));

wire [17:0] B0_reg;
// Conditional generation for B input
generate
    // Direct B input mode
    if (B_INPUT == "DIRECT")
        DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B0REG), .RSTTYPE(RSTTYPE)) m5(.D(B), .rst(RstB), .clk(Clk), .En(CEB), .out(B0_reg));
    // Cascade B input mode
    else if (B_INPUT == "CASCADE")
        DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B0REG), .RSTTYPE(RSTTYPE)) m6(.D(Bcin), .rst(RstB), .clk(Clk), .En(CEB), .out(B0_reg));
endgenerate

wire [17:0] A1_reg;
// Register pipeline for A1
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(A1REG), .RSTTYPE(RSTTYPE)) m7(.D(A0_reg), .rst(RstA), .clk(Clk), .En(CEA), .out(A1_reg));

wire [7:0] Opmode_reg;
// Register pipeline for Opmode
DSP48A1_D_BLOCK #(.WIDTH(8), .REG(OPMODEREG), .RSTTYPE(RSTTYPE)) m8(.D(Opmode), .rst(RstOpmode), .clk(Clk), .En(CEOpmode), .out(Opmode_reg));

wire [17:0] add_or_sub_reg;
// add or subtract logic based on Opmode
assign add_or_sub_reg = (Opmode_reg[6])? (D_reg - B0_reg):(D_reg + B0_reg);

wire [17:0] B_or_Preaddingsub;
// Select between B or Pre-add/Sub based on Opmode
assign B_or_Preaddingsub = (Opmode_reg[4])? add_or_sub_reg:B0_reg;

wire [17:0] B1_reg;
// Register pipeline for B1
DSP48A1_D_BLOCK #(.WIDTH(18), .REG(B1REG), .RSTTYPE(RSTTYPE)) m9(.D(B_or_Preaddingsub), .rst(RstB), .clk(Clk), .En(CEB), .out(B1_reg));
```

3. DSP48A1(Cont'd)

```
// Assign Bcout
assign Bcout = B1_reg;

wire [35:0] mul_reg;
// Multiplication logic
assign mul_reg = A1_reg * B1_reg;

wire [35:0] M_reg;
// Register pipeline for M
DSP48A1_D_BLOCK #(.WIDTH(36), .REG(MREG), .RSTTYPE(RSTTYPE)) m10(.D(mul_reg), .rst(RstM), .clk(Clk), .En(CEM), .out(M_reg));

generate
    genvar i;
    for(i=0; i<36; i=i+1)
        buf(M[i], M_reg[i]);
endgenerate

wire [47:0] conc_DAB;
// Concatenate inputs D, A, and B
assign conc_DAB = {D, A, B};

reg [47:0] X_out;
// X_out logic based on Opmode
always @(*) begin
    case (Opmode_reg[1:0])
        0: X_out = 0;
        1: X_out = mul_reg;
        2: X_out = P;
        3: X_out = conc_DAB;
    endcase
end

reg [47:0] Z_out;
// Z_out logic based on Opmode
always @(*) begin
    case (Opmode_reg[3:2])
        0: Z_out = 0;
        1: Z_out = Pcin;
        2: Z_out = P;
        3: Z_out = C_reg;
    endcase
end

wire Opmode_Carry;
// Opmode carry logic
assign Opmode_Carry = (CARRYINSEL == "CARRYIN")? Carryin:(CARRYINSEL == "OPMODE5")? Opmode_reg[5]:0;

wire CIN;
// Register pipeline for carry-in
DSP48A1_D_BLOCK #(.WIDTH(1), .REG(CARRYINREG), .RSTTYPE(RSTTYPE)) m11(.D(Opmode_Carry), .rst(RstCarryin), .clk(Clk), .En(CECarryin), .out(CIN));

wire Carryout_reg;
wire [47:0] add_or_sub_outreg;
// Addition or subtraction based on Opmode
assign {Carryout_reg, add_or_sub_outreg} = (Opmode_reg[7])? (Z_out - (X_out + CIN)):(X_out + Z_out + CIN);

// Register pipeline for carry-out
DSP48A1_D_BLOCK #(.WIDTH(1), .REG(CARRYOUTREG), .RSTTYPE(RSTTYPE)) m12(.D(Carryout_reg), .rst(RstCarryin), .clk(Clk), .En(CECarryin), .out(Carryout));
assign CarryoutF = Carryout;

// Register pipeline for Pcout
DSP48A1_D_BLOCK #(.WIDTH(48), .REG(PREG), .RSTTYPE(RSTTYPE)) m13(.D(add_or_sub_outreg), .rst(RstP), .clk(Clk), .En(CEP), .out(P));
assign Pcout = P;

endmodule
```

Test bench

```
module DSP48A1_tb ();
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";
reg [17:0] A_tb, B_tb, D_tb, Bcin_tb;
reg [47:0] C_tb, Pcin_tb;
reg [7:0] Opmode_tb;
reg Clk_tb, Carryin_tb, RstA_tb, RstB_tb, RstM_tb, RstP_tb, RstD_tb, RstC_tb, RstCarryin_tb, RstOpmode_tb,
CEA_tb, CEB_tb, CEM_tb, CEP_tb, CEC_tb, CED_tb, CECarryin_tb, CEOpmode_tb;
wire [17:0] Bcout_dut;
wire [47:0] Pcout_dut, P_dut;
wire [35:0] M_dut;
wire Carryout_dut, CarryoutF_dut;

DSP48A1 #(
.A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG),
.CREG(CREG), .DREG(DREG), .MREG(MREG), .PREG(PREG),
.CARRYINREG(CARRYINREG),.CARRYOUTREG(CARRYOUTREG), .OPMODEREG(OPMODEREG),
.CARRYINSEL(CARRYINSEL), .B_INPUT(B_INPUT), .RSTTYPE(RSTTYPE)
)
dut(
    .A(A_tb), .B(B_tb), .D(D_tb), .C(C_tb),
    .Clk(Clk_tb), .Carryin(Carryin_tb), .Opmode(Opmode_tb),
    .Bcin(Bcin_tb), .RstA(RstA_tb), .RstB(RstB_tb), .RstM(RstM_tb),
    .RstP(RstP_tb), .RstD(RstD_tb), .RstC(RstC_tb), .RstCarryin(RstCarryin_tb),
    .RstOpmode(RstOpmode_tb), .CEA(CEA_tb), .CEB(CEB_tb), .CEM(CEM_tb),
    .CEP(CEP_tb), .CEC(CEC_tb), .CED(CED_tb), .CECarryin(CECarryin_tb),
    .CEOpmode(CEOpmode_tb), .Pcin(Pcin_tb), .Bcout(Bcout_dut), .Pcout(Pcout_dut),
    .P(P_dut), .M(M_dut), .Carryout(Carryout_dut), .CarryoutF(CarryoutF_dut)
);

initial begin
    Clk_tb = 1;
    forever
        #1 Clk_tb = ~Clk_tb;
end
```

```
initial begin
    // Initialize all control signals
    A_tb = 0;
    B_tb = 0;
    C_tb = 0;
    D_tb = 0;
    Bcin_tb = 0;
    Pcin_tb = 0;
    Opmode_tb = 0;
    Carryin_tb = 0;
    RstA_tb = 0;
    RstB_tb = 0;
    RstM_tb = 0;
    RstP_tb = 0;
    RstD_tb = 0;
    RstC_tb = 0;
    RstCarryin_tb = 0;
    RstOpmode_tb = 0;
    CEA_tb = 0;
    CEB_tb = 0;
    CEM_tb = 0;
    CEP_tb = 0;
    CEC_tb = 0;
    CED_tb = 0;
    CECarryin_tb = 0;
    CEOpmode_tb = 0;

    // Test rest
    RstA_tb = 1;
    RstB_tb = 1;
    RstM_tb = 1;
    RstP_tb = 1;
    RstD_tb = 1;
    RstC_tb = 1;
    RstCarryin_tb = 1;
    RstOpmode_tb = 1;
    repeat(10) @(negedge Clk_tb);

    // Release reset and enable all stages
    RstA_tb = 0;
    RstB_tb = 0;
    RstM_tb = 0;
    RstP_tb = 0;
    RstD_tb = 0;
    RstC_tb = 0;
    RstCarryin_tb = 0;
    RstOpmode_tb = 0;
    CEA_tb = 1;
```

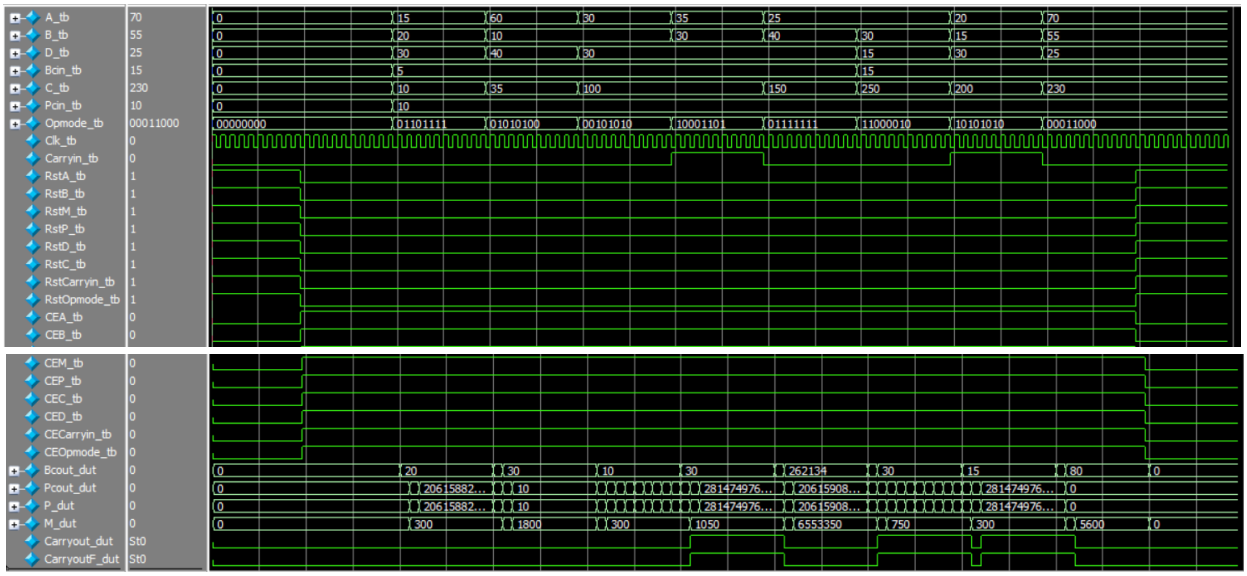
Test bench (Cont'd)

```
CEB_tb = 1;
CEM_tb = 1;
CEP_tb = 1;
CEC_tb = 1;
CED_tb = 1;
CECarryin_tb = 1;
CEOpmode_tb = 1;
repeat(10) @(negedge Clk_tb);

// Test Case 1: Simple addition
A_tb = 15;
B_tb = 20;
C_tb = 10;
D_tb = 30;
Carryin_tb = 0;
Bcin_tb = 5;
Pcin_tb = 10;
Opmode_tb = 8'b01101111; // Set Opmode for addition
repeat(10) @(negedge Clk_tb);

// Test Case 2: Subtraction
A_tb = 60;
B_tb = 10;
C_tb = 35;
D_tb = 40;
Opmode_tb = 8'b01010100; // Set Opmode for subtraction
repeat(10) @(negedge Clk_tb);

// Test Case 3: Multiply with Carry-in
A_tb = 30;
B_tb = 10;
C_tb = 100;
D_tb = 30;
Opmode_tb = 8'b00101010; // Set Opmode for multiplication with carry-in
repeat(10) @(negedge Clk_tb);

// Test Case 4: Accumulation
A_tb = 35;
B_tb = 30;
C_tb = 100;
D_tb = 30;
Carryin_tb = 1;
Pcin_tb = 10;
Opmode_tb = 8'b10001101; // Set Opmode for accumulation
repeat(10) @(negedge Clk_tb);
```

```
// Test Case 5: chained operation
A_tb = 25;
B_tb = 40;
C_tb = 150;
D_tb = 30;
Carryin_tb = 0;
Opmode_tb = 8'b01111111; // Set Opmode for multiplication with carry-in
repeat(10) @(negedge Clk_tb);

// Test Case 6: Cascade B input
Bcin_tb = 15;
B_tb = 30;
C_tb = 250;
D_tb = 15;
Carryin_tb = 0;
Opmode_tb = 8'b11000010; // Set Opmode for using cascade input
repeat(10) @(negedge Clk_tb);

// Test Case 7: complex operation
A_tb = 20;
B_tb = 15;
C_tb = 200;
D_tb = 30;
Carryin_tb = 1;
Opmode_tb = 8'b10101010; // Set Opmode for pre-addition
repeat(10) @(negedge Clk_tb);

// Test Case 8: complex operation
A_tb = 70;
B_tb = 55;
C_tb = 230;
D_tb = 25;
Carryin_tb = 0;
Opmode_tb = 8'b00011000; // Set Opmode for pre-addition
repeat(10) @(negedge Clk_tb);

// reset and unenable all stages
RstA_tb = 1;
RstB_tb = 1;
RstM_tb = 1;
RstP_tb = 1;
RstD_tb = 1;
RstC_tb = 1;
RstCarryin_tb = 1;
RstOpmode_tb = 1;
CEA_tb = 0;
CEB_tb = 0;
CEM_tb = 0;
```

```
    CEP_tb = 0;
    CEC_tb = 0;
    CED_tb = 0;
    CECarryin_tb = 0;
    CEOpmode_tb = 0;
    repeat(10) @(negedge Clk_tb);
    $stop;
end

initial begin
    $monitor("A = %d, B = %d, C = %d, D = %d, Carryin = %b,  Bcin  = %d, Pcin = %d, Opmode = %b, M = %d, P = %d, Carryout = %b, CarryoutF = %b",
    A_tb, B_tb, C_tb, D_tb, Carryin_tb, Bcin_tb, Pcin_tb, Opmode_tb, M_dut, P_dut, Carryout_dut, CarryoutF_dut);
end
endmodule
```

Simulation

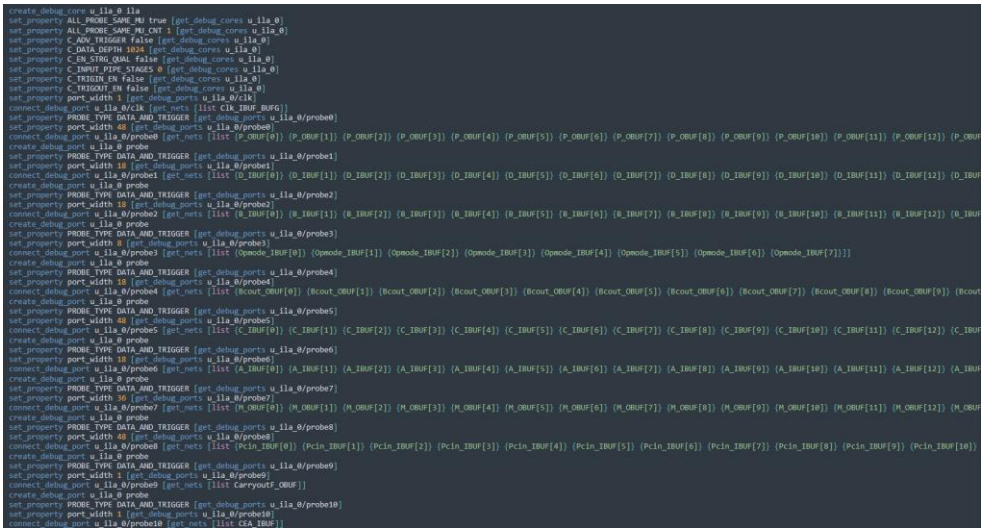


Do file

```
vlib work
vlog DSP48A1.v DSP48A1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -sim
```

Constrain

```
# Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports Clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports Clk]
```



Constrain (cont'd)

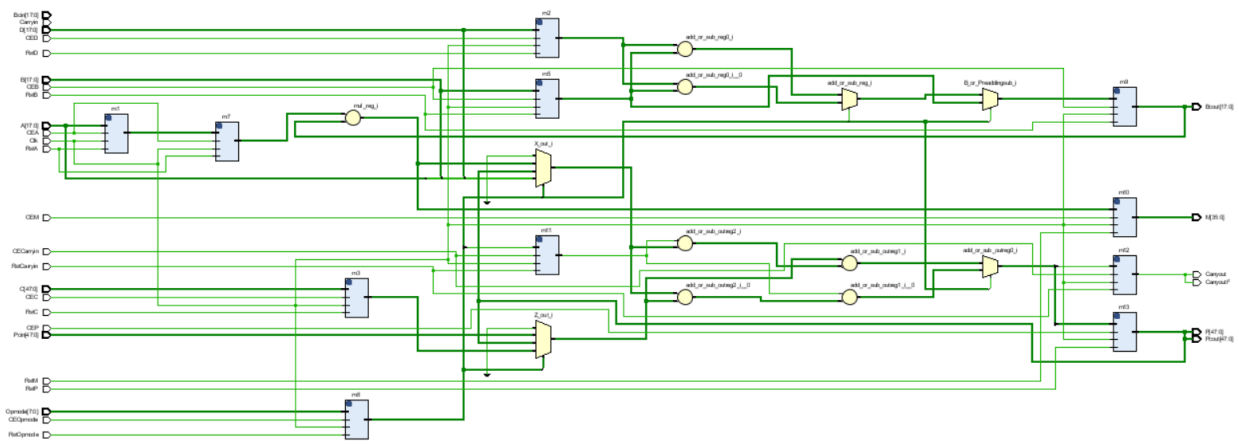
```
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECarryin_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEOpmode_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list Clk_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RstA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RstB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RstC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RstCarryin_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RstD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
```

```
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RstM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RstOpmode_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RstP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets Clk_IBUF_BUFG]
```

Monitor

```
# A =  0, B =  0, C =   0, D =  0, Carryin = 0, Bcin =  0, Pcin =  0, Opmode = 00000000, M =       0, P =               0, Carryout = 0, CarryoutF = 0
# A = 15, B = 20, C =  10, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01101111, M =       0, P =               0, Carryout = 0, CarryoutF = 0
# A = 15, B = 20, C =  10, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01101111, M =     300, P =   2061588234270, Carryout = 0, CarryoutF = 0
# A = 15, B = 20, C =  10, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01101111, M =     300, P =   2061588234271, Carryout = 0, CarryoutF = 0
# A = 60, B = 10, C =  35, D = 40, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01010100, M =     300, P =   2061588234271, Carryout = 0, CarryoutF = 0
# A = 60, B = 10, C =  35, D = 40, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01010100, M =     300, P =   2748794798101, Carryout = 0, CarryoutF = 0
# A = 60, B = 10, C =  35, D = 40, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01010100, M =     600, P =              11, Carryout = 0, CarryoutF = 0
# A = 60, B = 10, C =  35, D = 40, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01010100, M =    1800, P =              10, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =    1800, P =              10, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     900, P =              20, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =              41, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =              83, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =             167, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =             335, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =             671, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =            1343, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =            2687, Carryout = 0, CarryoutF = 0
# A = 30, B = 10, C = 100, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 00101010, M =     300, P =            5375, Carryout = 0, CarryoutF = 0
# A = 35, B = 30, C = 100, D = 30, Carryin = 1, Bcin =  5, Pcin = 10, Opmode = 10001101, M =     300, P =            5375, Carryout = 0, CarryoutF = 0
# A = 35, B = 30, C = 100, D = 30, Carryin = 1, Bcin =  5, Pcin = 10, Opmode = 10001101, M =     300, P =           10751, Carryout = 0, CarryoutF = 0
# A = 35, B = 30, C = 100, D = 30, Carryin = 1, Bcin =  5, Pcin = 10, Opmode = 10001101, M =    1050, P = 281474976709705, Carryout = 1, CarryoutF = 1
# A = 35, B = 30, C = 100, D = 30, Carryin = 1, Bcin =  5, Pcin = 10, Opmode = 10001101, M =    1050, P = 281474976709706, Carryout = 1, CarryoutF = 1
# A = 25, B = 40, C = 150, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01111111, M =    1050, P = 281474976709706, Carryout = 1, CarryoutF = 1
# A = 25, B = 40, C = 150, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01111111, M =    1000, P =   2061590855870, Carryout = 0, CarryoutF = 0
# A = 25, B = 40, C = 150, D = 30, Carryin = 0, Bcin =  5, Pcin = 10, Opmode = 01111111, M = 6553350, P =   2061590855871, Carryout = 0, CarryoutF = 0
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M = 6553350, P =   2061590855871, Carryout = 0, CarryoutF = 0
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M = 6553350, P =   1030798704821, Carryout = 0, CarryoutF = 0
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =       0, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P =   1030798704822, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P =   1030798704822, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P =   1030798704822, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P =   1030798704822, Carryout = 1, CarryoutF = 1
# A = 25, B = 30, C = 250, D = 15, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 11000010, M =     750, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 20, B = 15, C = 200, D = 30, Carryin = 1, Bcin = 15, Pcin = 10, Opmode = 10101010, M =     750, P = 280444178005834, Carryout = 1, CarryoutF = 1
# A = 20, B = 15, C = 200, D = 30, Carryin = 1, Bcin = 15, Pcin = 10, Opmode = 10101010, M =     750, P =   1030798704822, Carryout = 1, CarryoutF = 1

# A = 20, B = 15, C = 200, D = 30, Carryin = 1, Bcin = 15, Pcin = 10, Opmode = 10101010, M =     300, P =               0, Carryout = 0, CarryoutF = 0
# A = 20, B = 15, C = 200, D = 30, Carryin = 1, Bcin = 15, Pcin = 10, Opmode = 10101010, M =     300, P = 281474976710655, Carryout = 1, CarryoutF = 1
# A = 70, B = 55, C = 230, D = 25, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 00011000, M =     300, P = 281474976710655, Carryout = 1, CarryoutF = 1
# A = 70, B = 55, C = 230, D = 25, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 00011000, M =    3850, P =               0, Carryout = 1, CarryoutF = 1
# A = 70, B = 55, C = 230, D = 25, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 00011000, M =    5600, P =               0, Carryout = 0, CarryoutF = 0
# A = 70, B = 55, C = 230, D = 25, Carryin = 0, Bcin = 15, Pcin = 10, Opmode = 00011000, M =       0, P =               0, Carryout = 0, CarryoutF = 0
```

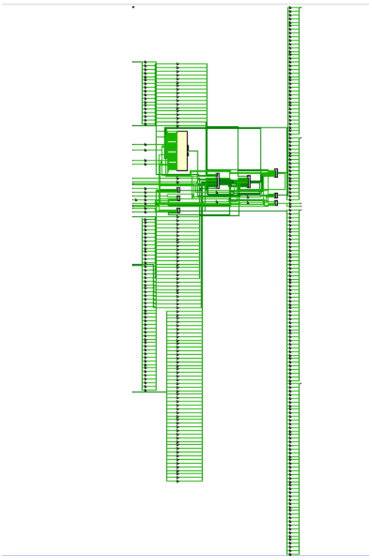
Elaboration schematic

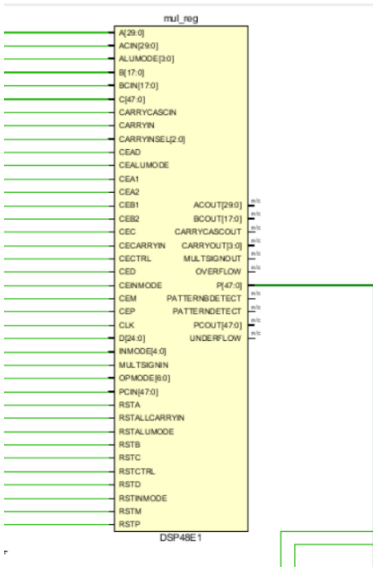


RTL message

- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'G:/vivado3/Vivado/Vivado/2018.2/data/ip'.
- Elaborated Design (18 infos)
  - General Messages (18 infos)
    - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)
    - [Synth 8-6155] done synthesizing module 'DSP48A1_D_BLOCK' (1#1) [DSP48A1_D_BLOCK.v:1] (6 more like this)
    - [Device 21-403] Loading part xc7a200tffg1156-3
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

Synthesis schematic





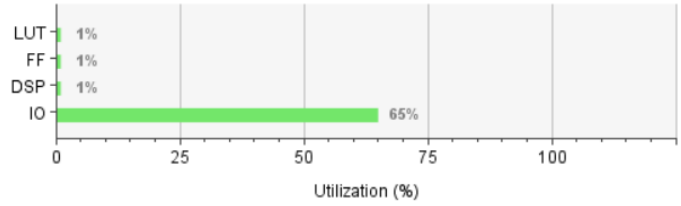
Synthesis message

Synthesis (29 infos)
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)
- [Synth 8-6155] done synthesizing module 'DSP48A1_D_BLOCK' (1#1) [DSP48A1_D_BLOCK.v:1] (6 more like this)
- [Device 21-403] Loading part xc7a200tffg1156-3
- [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1.v:68] (1 more like this)
- [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP48A1_D_BLOCK.v:13]
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.
- [Common 17-83] Releasing license: Synthesis
- [Common 17-1381] The checkpoint 'G:/Sarah/Digital_Course/digital_course_modelsim/mini_proj/project_MINI/project_MINI.runs/synth_1/DSP48A1.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file DSP48A1_utilization_synth.rpt -pb DSP48A1_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Tue Jul 30 00:39:56 2024...

Synthesized Design (6 infos)
- General Messages (6 infos)
  - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-479] Netlist was created with Vivado 2018.2
  - [Project 1-570] Preparing netlist for logic optimization
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.

Synthesis Utilization

Resource	Utilization	Available	Utilization %
LUT	231	134600	0.17
FF	178	269200	0.07
DSP	1	740	0.14
IO	327	500	65.40

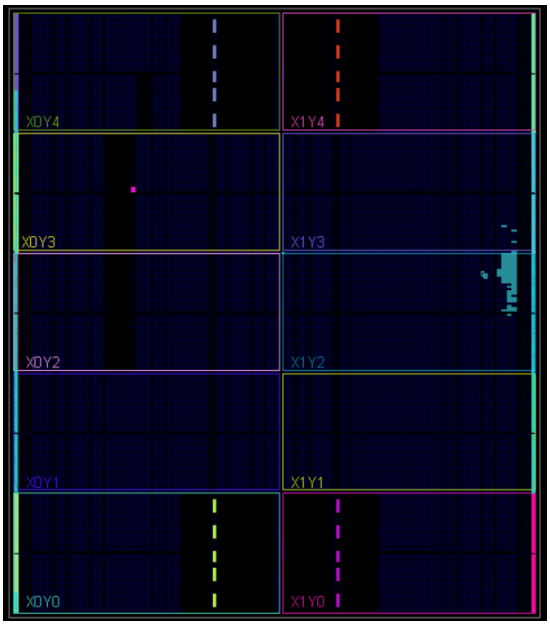


Synthesis Timing

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	741	Total Number of Endpoints:	741	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Implementation Schematic

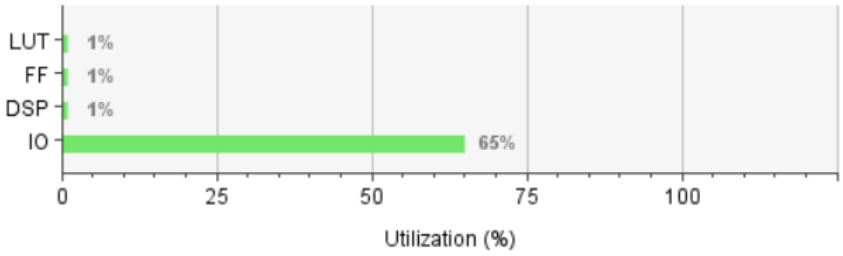


Implementation message

- Implementation (75 infos)
  - Design Initialization (7 infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a200tffg1156-3
    - [Project 1-570] Preparing netlist for logic optimization
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - Opt Design (23 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [Timing 38-35] Done setting XDC timing constraints.
    - [Opt 31-40] Retargeted 0 cell(s).
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
    - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    - [Common 17-83] Releasing license: Implementation
    - [Common 17-1381] The checkpoint 'G:/Sarah/Digital_Course/digital_course_modelsim/mini_proj/project_MINI/project_MINI.runs/impl_1/DSP48A1_opt.dcp' has been generated.
    - [runtcl-4] Executing : report_drc -file DSP48A1_drc_opted.rpt -pb DSP48A1_drc_opted.pb -rpx DSP48A1_drc_opted.rpx
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'G:/Vivado3/Vivado/2018.2/data/ip'.
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Coretcl 2-168] The results of DRC are in file DSP48A1_drc_opted.rpt.
  - Place Design (16 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
    - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
    - [Common 17-83] Releasing license: Implementation
    - [Common 17-1381] The checkpoint 'G:/Sarah/Digital_Course/digital_course_modelsim/mini_proj/project_MINI/project_MINI.runs/impl_1/DSP48A1_placed.dcp' has been generated.
    - [runtcl-4] Executing : report_io -file DSP48A1_io_placed.rpt (2 more like this)
  - Route Design (29 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [Vivado_Tcl 4-198] DRC finished with 0 Errors
    - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
    - [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
    - [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.
    - [Route 35-16] Router Completed Successfully
    - [Common 17-83] Releasing license: Implementation
    - [Common 17-1381] The checkpoint 'G:/Sarah/Digital_Course/digital_course_modelsim/mini_proj/project_MINI/project_MINI.runs/impl_1/DSP48A1_routed.dcp' has been generated.
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Coretcl 2-168] The results of DRC are in file DSP48A1_drc_routed.rpt.
    - [runtcl-4] Executing : report_drc -file DSP48A1_drc_routed.rpt -pb DSP48A1_drc_routed.pb -rpx DSP48A1_drc_routed.rpx (7 more like this)
    - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
    - [DRC 23-133] Running Methodology with 2 threads
    - [Coretcl 2-1520] The results of Report Methodology are in file DSP48A1_methodology_drc_routed.rpt.
    - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
    - [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
    - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
- Implemented Design (5 infos)
  - General Messages (5 infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

Implementation Utilization

Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	179	269200	0.07
DSP	1	740	0.14
IO	327	500	65.40



Implementation Timing

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	744	Total Number of Endpoints:	744	Total Number of Endpoints:	NA

There are no user specified timing constraints.

NO ERRORS Checks