Reg. No. : | | | | | | | | | | | | |

**Question Paper Code : S1356**

M.C.A. DEGREE EXAMINATION, FEBRUARY/MARCH 2016.

First Semester

DMC 7105 — COMPUTER ORGANIZATION AND DESIGN

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the 1's and 2's complement of 7?

2. Define AND gate.

3. Define Associative and Commutative Laws.

4. Write a note on Latches.

5. What is an Up-down counters?

6. What is a pipeline?

7. What is meant by addressing?

8. Define Virtual memory.

9. Write any two functions of Bus-interface.

10. What is Buffer chaining?

PART B — (5 × 16 = 80 marks)

11. (a) For the Truth table given below, transfer the outputs to the K-map, then write the Boolean expression for the result. (16)

| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Or

(b) Illustrate the implementation of NAND and NOR gates. (16)

12. (a) How do you design an ALU? Describe, in detailed, through an example. (16)

Or

(b) Discuss the JK Flip-flop with a neat diagram and draw a truth table for its functions. (16)

13. (a) Illustrate the working principles of the Von-Neumann architecture with a neat diagram. (16)

Or

(b) Describe the execution style of a fetch-execute cycle with a neat diagram. (16)

14. (a) (i) Explain the address translation. (8)

(ii) Discuss the structure of the physical memory. (8)

Or

(b) Discuss the functions of the Cache memory and its mapping. (16)

15. (a) (i) What is meant by data transfer? Illustrate. (4)

(ii) Distinguish between the serial data transfer and parallel data transfer. (8)

(iii) Illustrate the operation chaining. (4)

Or

(b) Illustrate the working principles of Full-duplex and Half-duplex. (16)

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Reg. No. : | | | | | | | | | | | | |

**Question Paper Code : 80356**

M.C.A. DEGREE EXAMINATION, AUGUST 2015.

First Semester

DMC 7105 — COMPUTER ORGANIZATION AND DESIGN

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Perform subtraction of the following unsigned binary numbers by using 1's and 2's complement method 1000–11000.

2. Simplify the expression $(BC' + A'D)(AB' + CD')$ using Boolean algebra.

3. Differentiate between combinational and sequential circuits.

4. Draw the logic diagram of a 2-to-4 decoder with only NOR gates.

5. What are the advantages and disadvantages of Von-Neumann architecture?

6. Define clock rate and instruction rate.

7. What is virtual memory?

8. What is cache memory?

9. Differentiate between parallel and serial data transfer.

10. What are the advantages of interrupt-initiated data transfer over transfer under program control without an interrupt?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify the Boolean function $F(A, B, C, D) = \sum(3, 7, 11, 13, 14, 15)$ using four-variable maps. (10)

(ii) What are universal gates? Construct AND gate, OR gate using NOR gate only. (6)

Or

(b) (i) Simplify the following Boolean function in product-of-sums form by means of four-variable map. Draw the logic diagram with OR-AND gates and NOR gates.

$F(A, B, C, D) = \sum (0, 2, 8, 9, 10, 11, 14, 15)$ (10)

(ii) Define Boolean algebra and state the basic identities of Boolean algebra. (6)

12. (a) Design and explain a 4-bit binary counter with parallel load and synchronous clear. (16)

Or

(b) (i) Construct a 16 × 1 line multiplexer with two 8-to-1 multiplexers and one 2-to-1 line multiplexer. Use block diagram for the three multiplexer. (10)

(ii) Explain JK flip-flop with graphic symbol and characteristic table. (6)

13. (a) (i) What is a multicore-processor? Explain the architecture of a typical multi-core processor with the help of block diagram. (10)

(ii) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks. (6)

Or

(b) (i) Explain various phages of the instruction cycle in detail. (8)

(ii) Explain Von-Neumann architecture with the help of block diagram. (8)

14. (a) (i) Explain how the logical address is converted in to real address in a paged memory system. (8)

(ii) Explain direct and associative mapping with reference to cache memory. (8)

Or

(b) (i) Explain any two page replacement algorithms in detail. (8)

(ii) Discuss about the significance of L1, L2 and L3 cache memory in detail. (8)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (8)

(ii) Explain why DMA have priority over CPU when both request a memory transfer. (8)

Or

(b) (i) Explain the typical parallel I/O transfer interface with the help of block diagram. (8)

(ii) Describe data transfer using programmed-I/O with the help of flow chart. (8)

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**Question Paper Code : 22358**

M.C.A. DEGREE EXAMINATION, FEBRUARY/MARCH 2015.

First Semester

DMC 7105 — COMPUTER ORGANIZATION AND DESIGN

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a K-map?
2. Convert $(2686)_{10}$ to a binary number.
3. What is an encoder?
4. What is the 2s complement of 5?
5. Define pipeline.
6. What are multicore processors?
7. What is paging?
8. What is significance of levels of cache?
9. Define Bus interface.
10. Write a note on buffer chaining.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Implement the Boolean expression $Y = AB'C'D + B'CD + A'D' + BCD$ using NAND gates only. (8)

(ii) Simplify $Y = A'BCD + BC'D + A'B + B'CD$ using k-map. (8)

Or

(b) Simplify the following Boolean functions by means of the tabulation method :

(i) $P(A,B,C) = \Sigma(0,2,4,5,6)$. (6)

(ii) $P(A,B,C,D,E,F) = \Sigma(6,9,13,19,18,25,27,29,41,45,57,61)$. (10)

12. (a) Design a 4 bit up counter and draw the logic diagram. (16)

Or

(b) Discuss the functions of all the Flip-Flops with a neat diagram. (16)

13. (a) Illustrate the Von-Neumann architecture with a neat diagram. (16)

Or

(b) Discuss the various types of instruction formats with examples. (16)

14. (a) (i) Write a note on Cache mapping. (10)

(ii) Discuss the LRU replacement with an example. (6)

Or

(b) What is the need for virtual memory? Describe how address translation is done in a paged memory system.

15. (a) Describe the DMA operation with neat diagram. (16)

Or

(b) Explain the asynchronous data transfer with an example. (16)

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