North South University

CSE 332L : Semester Final Project

Project: 20-bit single cycle MIPS CPU with R-type, I-type, and J-type instructions

Faculty: TnF

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Section: 2

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Types of Instructions and their Format:

opcode: Operation Code
rs: Source Register
rt: Temporary Register
rd: Destination Register
shamt: Shift Amount

R-type: opcode(3bits) rs(4bits) rt(4bits) rd(4bits) shamt(2bits) function(3bits)

MSB LSB

opcode(3)	rs(4)	rt(4)	rd(4)	shamt(2)	function(3)

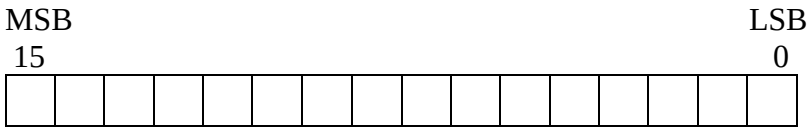
I-type: opcode(3bits) rs(4bits) rt(4bits) Immediate(9bits)

opcode(3)	rs(4)	rt(4)	Immediate(9)

J-type: opcode(3bits) address(17bits)

opcode(3)	Address(17)

Data bits: 16 bits throughout the project.



Opcodes and Functions:

R Type:

AND: 000 xxxx xxxx xxxx xx 000

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0

OR: 000 xxxx xxxx xxxx xx 001

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1

NOR: 000 xxxx xxxx xxxx xx 010

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0

SLT: 000 xxxx xxxx xxxx xx 011

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1

SRL: 000 xxxx xxxx xxxx xx 100

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0

SLL: 000 xxxx xxxx xxxx xx 101

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1

ADD: 000 xxxx xxxx xxxx xx 110

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0

SUB: 000 xxxx xxxx xxxx xx 111

0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1

I Type:

BEQ: 001 xxxx xxxx xxxxxxxxx

0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

BNE: 010 xxxx xxxx xxxxxxxxx

0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

LW: 011 xxxx xxxx xxxxxxxxx

0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

SW: 100 xxxx xxxx xxxxxxxxx

1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

J Type:

J: 101 xxxxxxxxxxxxxxxxx

1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Tables:

Control Signals Table:

Instruction	Reg Dst	ALU Op1	ALU Op0	ALU Src	Branch Equal	BranchNot Equal	MemRead	Mem Write	Reg Write	MemTo Reg	Jump
R-Type	1	1	0	0	0	0	0	0	1	0	0
lw	0	0	0	1	0	0	1	0	1	1	0
sw	0	0	0	1	0	0	0	1	0	0	0
beq	0	0	1	0	1	0	0	0	0	0	0
bne	0	0	1	0	0	1	0	0	0	0	0
j	0	0	0	0	0	0	0	0	0	0	1

ALU Control Signals Table (detailed):

Instruction OpCode	ALUOp1	ALUOp0	Instruction Operation	Function Code	Desired ALU Action	ALU Control Input
Lw	0	0	load word	xxx	add	110
Sw	0	0	store word	xxx	add	110
Beq	0	1	branch equal	xxx	subtract	111
Ben	0	1	branch not equal	xxx	subtract	111
R-type	1	0	and	000	AND	000
R-type	1	0	or	001	OR	001
R-type	1	0	nor	010	NOR	010
R-type	1	0	slt	011	set if less than	011
R-type	1	0	srl	100	shift right logical	100
R-type	1	0	sll	101	shift left logical	101
R-type	1	0	add	110	add	110
R-type	1	0	sub	111	subtract	111

ALU Control Signals Table (minimized**):**

ALUOp1	ALUOp0	Function2	Function1	Function0	O2	O1	O0
0	0	x	x	x	1	1	0
0	1	x	x	x	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	1	0
1	0	1	1	1	1	1	1

Equations:

Equations for ALU Operations (O_2, O_1, O_0):

O_0 = $(\sim A_1\ A_0\ \sim F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ F_1\ F_0) + (A_1\ \sim A_0\ \sim F_2\ F_0\ F_1) + (A_1\ \sim A_0\ F_2\ F_0\ \sim F_1) + (A_1\ \sim A_0\ F_2\ F_1\ F_0)$

O_1 = $(\sim A_1\ \sim A_0\ \sim F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ \sim F_1\ F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ F_1\ F_0) + (\sim A_1\ \sim A_0\ F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ F_2\ \sim F_1\ F_0) + (\sim A_1\ \sim A_0\ F_2\ F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ F_2\ F_1\ F_0) + (\sim A_1\ A_0\ \sim F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ F_1\ F_0) + (A_1\ \sim A_0\ \sim F_2\ F_1\ F_0) + (A_1\ \sim A_0\ \sim F_2\ F_1\ \sim F_0) + (A_1\ \sim A_0\ F_2\ F_1\ \sim F_0) + (A_1\ \sim A_0\ F_2\ F_1\ F_0)$

O_2 = $(\sim A_1\ \sim A_0\ \sim F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ \sim F_1\ F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ \sim F_2\ F_1\ F_0) + (\sim A_1\ \sim A_0\ F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ F_2\ \sim F_1\ F_0) + (\sim A_1\ \sim A_0\ F_2\ F_1\ \sim F_0) + (\sim A_1\ \sim A_0\ F_2\ F_1\ F_0) + (\sim A_1\ A_0\ \sim F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ \sim F_2\ F_1\ F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ \sim F_1\ F_0) + (\sim A_1\ A_0\ F_2\ F_1\ \sim F_0) + (\sim A_1\ A_0\ F_2\ F_1\ F_0) + (A_1\ \sim A_0\ F_2\ \sim F_1\ \sim F_0) + (A_1\ \sim A_0\ F_2\ \sim F_1\ F_0) + (A_1\ \sim A_0\ F_2\ F_1\ \sim F_0) + (A_1\ \sim A_0\ F_2\ F_1\ F_0)$

Sample Test Case (loop from 0 until 6):

r0 = 6
r2 = 1
beq r0 r1 6
add r1 r2 r1
jump 0

00100000001000000110 = 20206(Hex)
00000010010000100110 = 02426(Hex)
10100000000000000000 = A0000(Hex)