A Report

on

Project entitled

"Performance comparison of ONOFIC and LECTOR based approaches for Leakage Power Reduction"

Submitted By

SARITA GAJANAN BIAWE

ID - (H20211230208H)

Under The Guidance Of

Dr. Surya Shankar Dan

For the Fulfillment of Academic Requirement

Of The Course

ADVANCED VLSI DESIGN (MEL G623)

`

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE PILANI,

HYDERABAD CAMPUS

INTRODUCTION

High-performance, low power integrated circuits (ICs) are the most essential requirement of present VLSI industry. small size and fast response conditions for the electronic systems are achieved with the help of ICs. The Very large scale integration is possible only when the dimensions of devices to be integrate are scaled-down as small as possible without much affecting their functionality. The power supply and the threshold voltage of the devices must be scaled-down for the lower technology nodes. But, leakage current is inversely proportional to the threshold voltage. Scaling-down of the threshold voltage produces large leakage current which increases the leakage power and changes the characteristics of the electronic systems and disturbs the reliability of IC. Hence, the increasing power dissipation is the major concern for low power VLSI design engineers.

CMOS is most widely used in ICs because of numerous advantages compared to other logics such as high noise immunity, low leakage power, easy fabrication, high device density, full rail to rail output etc. CMOS logic comprises two power dissipation components: dynamic and static power dissipation. The current flows during the logic transitions is identified as dynamic current which is responsible for dynamic power dissipation. Static current flows during the static logic levels and accumulates the static power dissipation.

Dynamic power dessipation is the major part of the total power dessipation when technology nodes are generally above 100 nm. But, present electronic industry is working for the lower technology nodes (below 100 nm) and static or leakage power dissipation is the main component of the total power dissipation in lower (below 100nm) technology nodes. To reduce the leakage power two techniques i.e. ONOFIC and LECTOR are studied and implemented in this project and their performance is compared based on power, delay and power-delay product.

ONOFIC TECHNIQUE

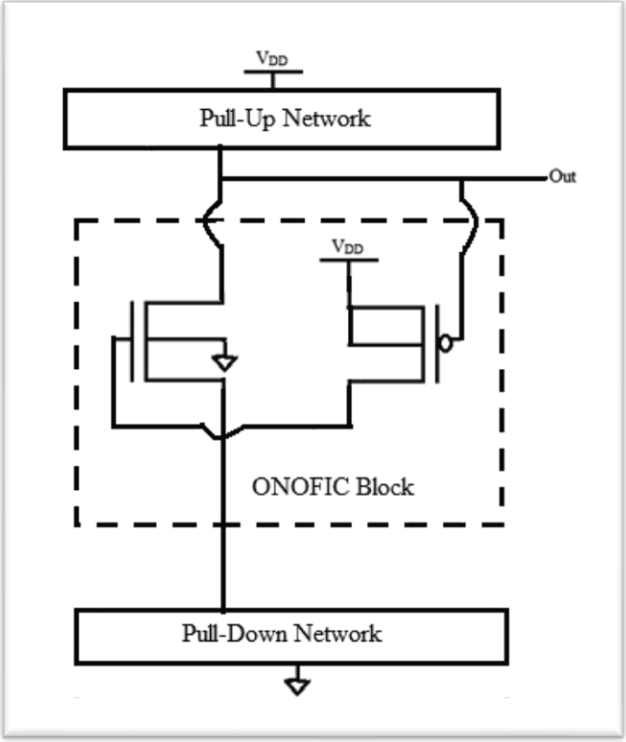


Figure 1.1

In onofic circuits two NMOS stacking transistors are connected in pull down to control the leakage current. The gate of this leakage control transistors is controlled by a PMOS transistor which takes input from the output and provide feedback to the leakage control transistors. For example, when the pull-down network is on the output becomes one and the feedback PMOS goes into off condition and following that the leakage control transistors also goes into sub threshold region and the leakage current becomes very low almost negligible. And when pull down network is on output is zero, so the controlling PMOS is on and that turns on the leakage control transistor which provides an additional resistance for leakage and short circuit current flow.

LECTOR TECHNIQUE

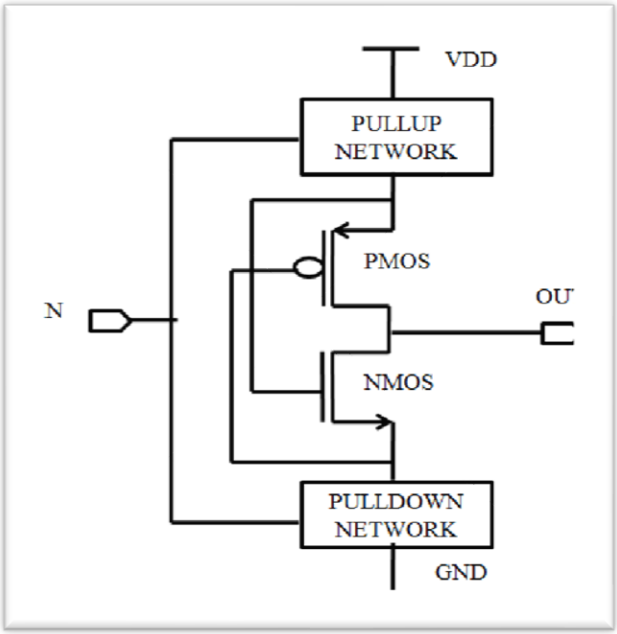
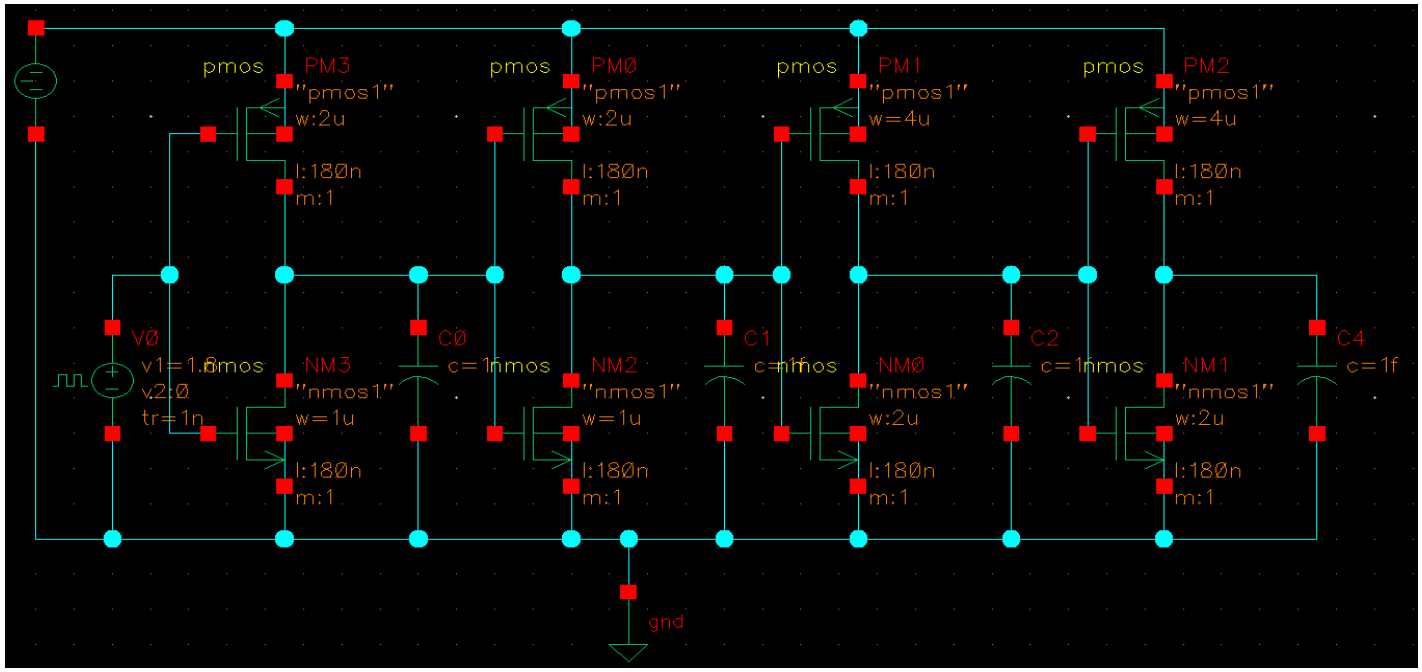


Figure 1.2

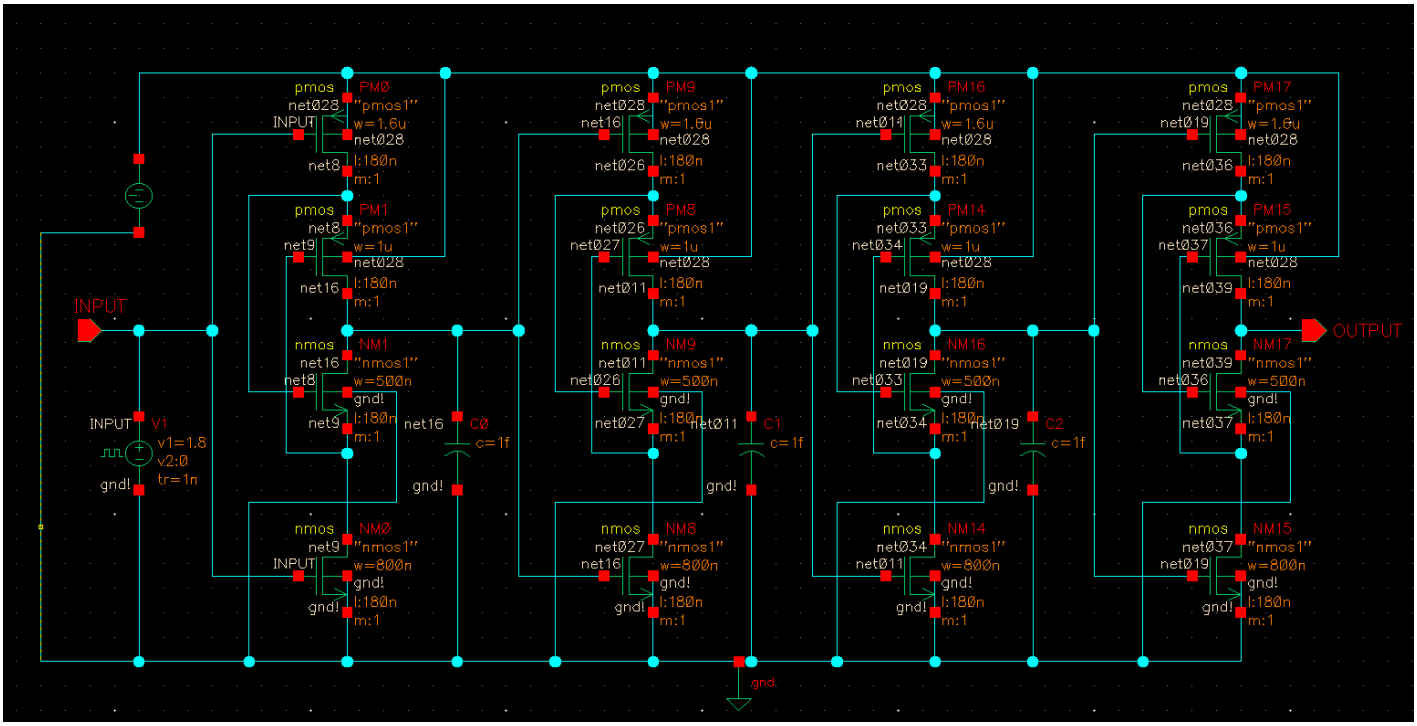
The basic idea behind the LECTOR method is insertion of the two additional transistors in between PUN and PDN of the CMOS logic. These extra transistors are connected in a specific arrangement in CMOS logic. LECTOR has single type threshold voltage devices throughout the logic design. Additional transistors are termed as leakage control transistors (LCTs). LCTs are responsible for the leakage reduction. The logical diagram of the LECTOR method is given in Figure 1.2. The input terminals of the LCTs are joined with the source terminals of each other. One LCT always closes to the cut-off state which helps to minimize the leakage current. The configuration of this method generates the distorted output because of the connections of the LCTs. It means noise margin is degraded in LECTOR method

CIRCUIT SCHEMATIC

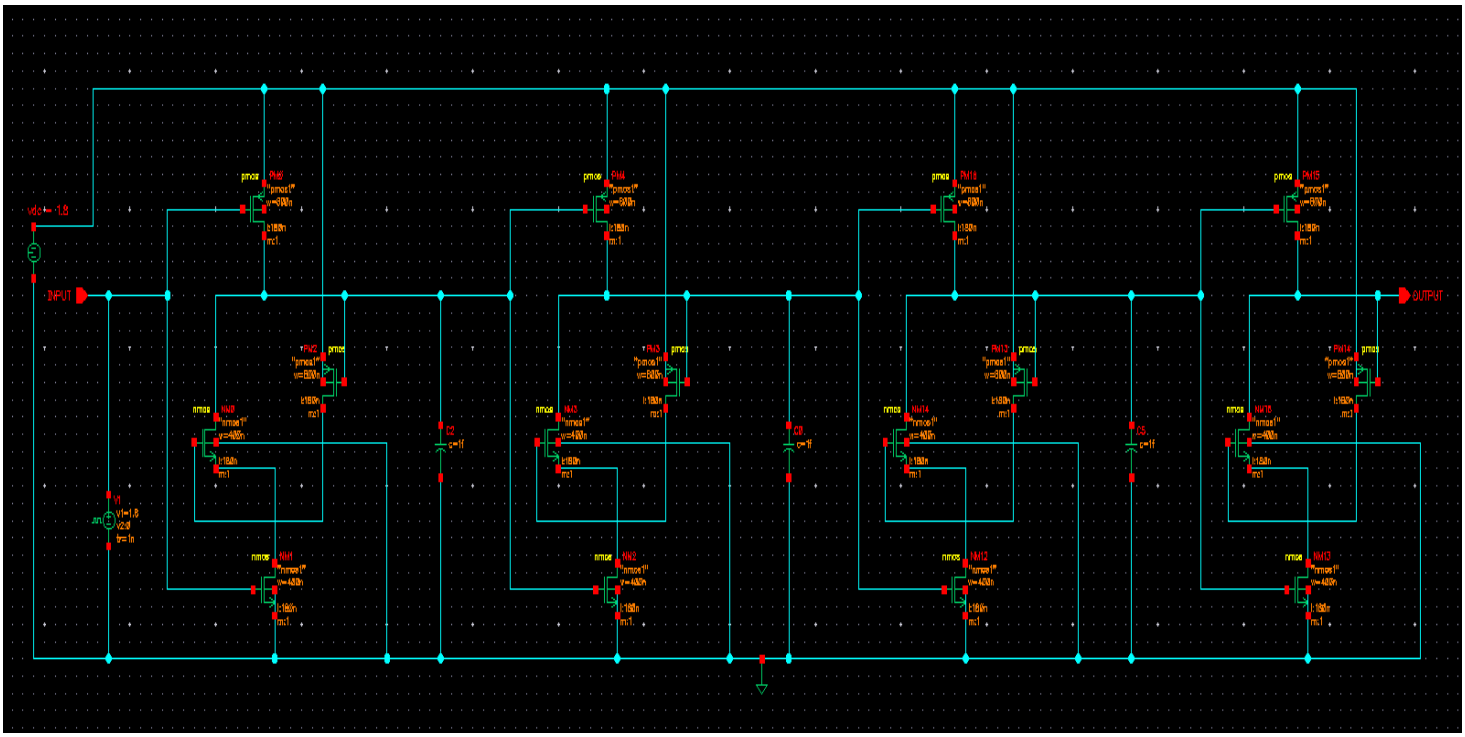
1.CONVENTIONAL 2-STAGE BUFFER



2.LECTOR 2-STAGE BUFFER

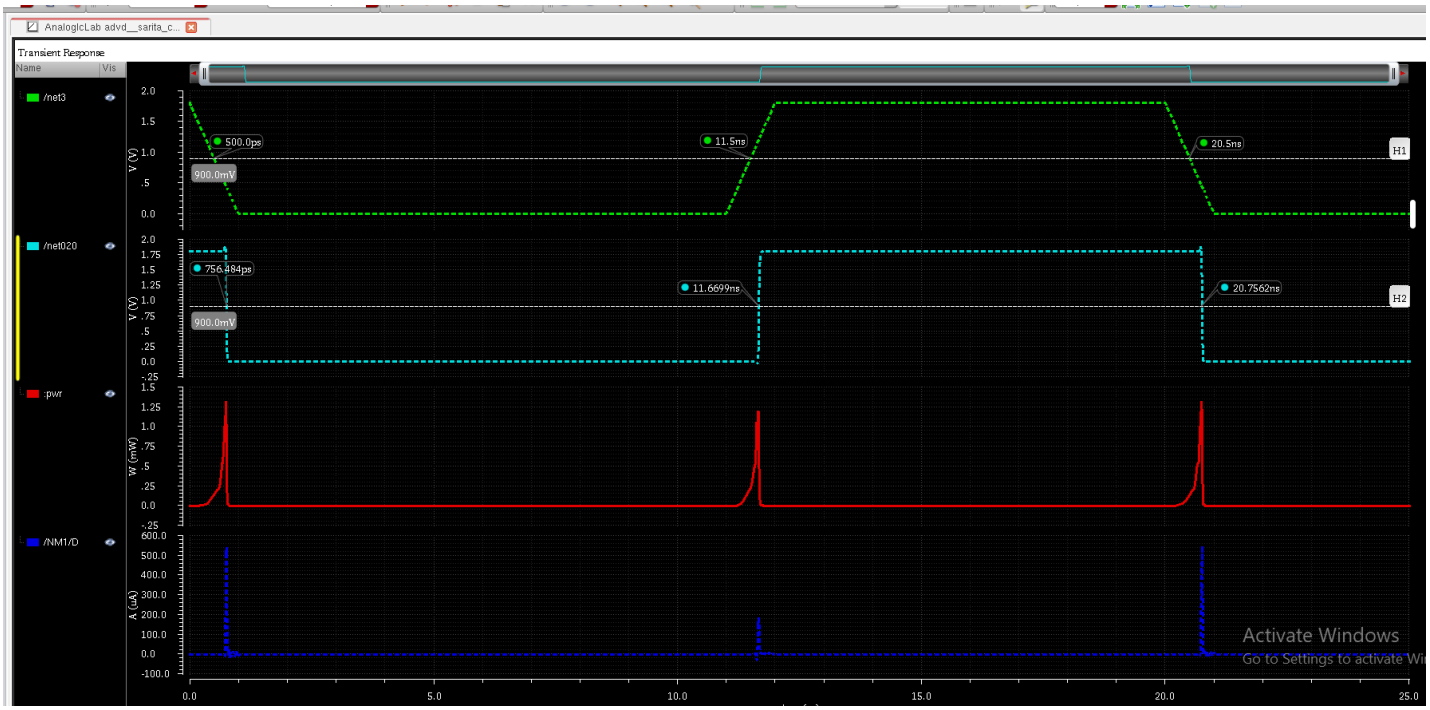


3.ONOFIC 2-STAGE BUFFER



SIMULATION RESULTS IN 180nm TECHNOLOGY NODE

CONVENTIONAL 2-STAGE BUFFER

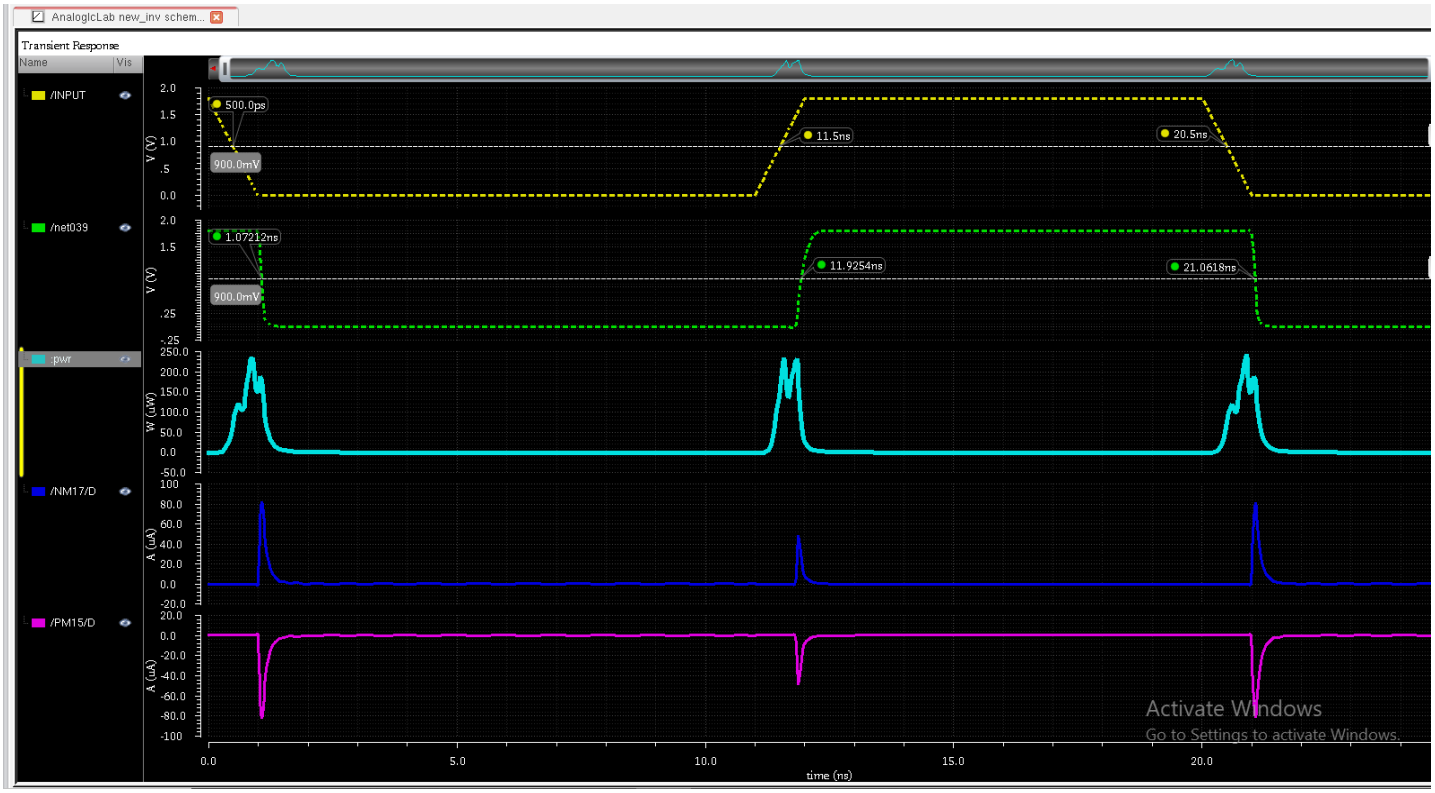


TIMING DIAGRAM

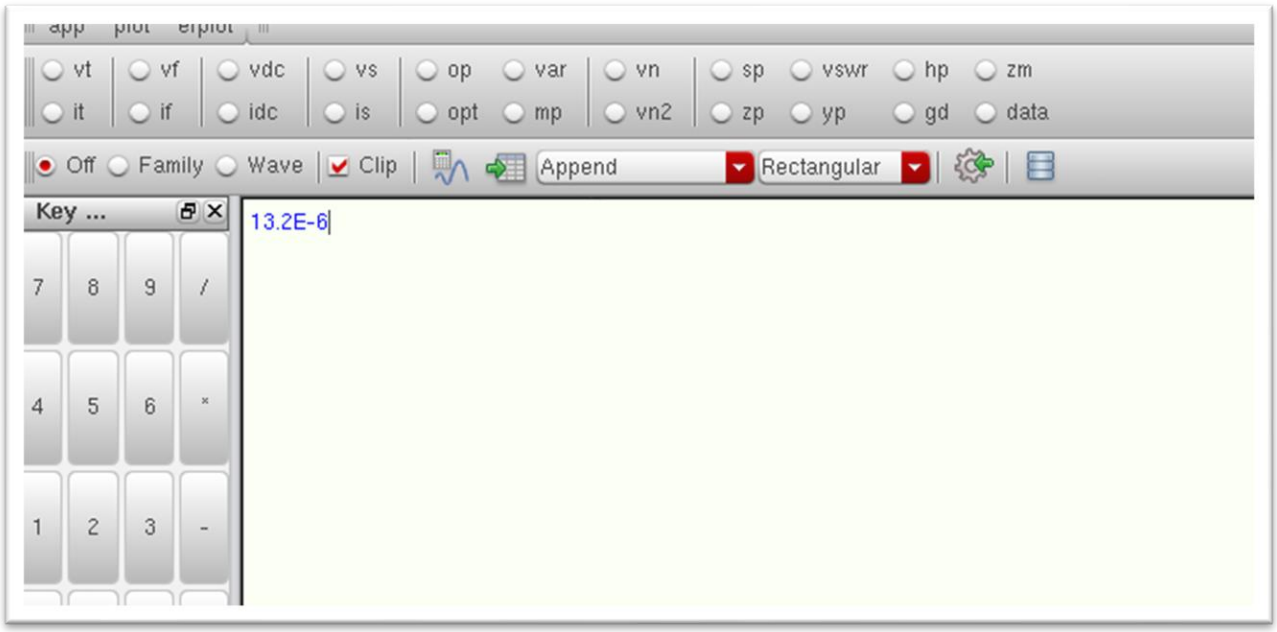
AVERAGE POWER CONSUMPTION

VOLTAGE, CURRENT AND POWER WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

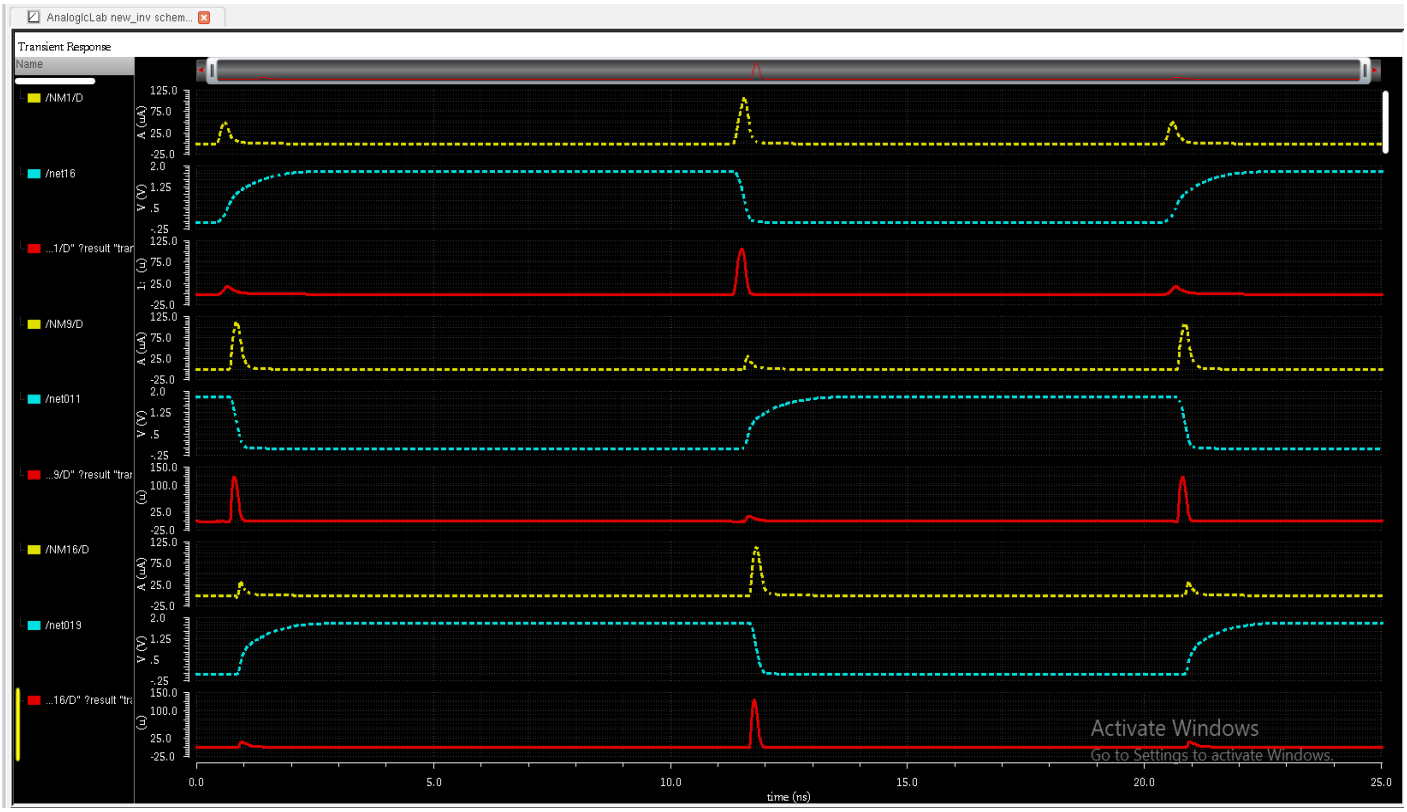
LECTOR 2-STAGE BUFFER



TIMING DIAGRAM

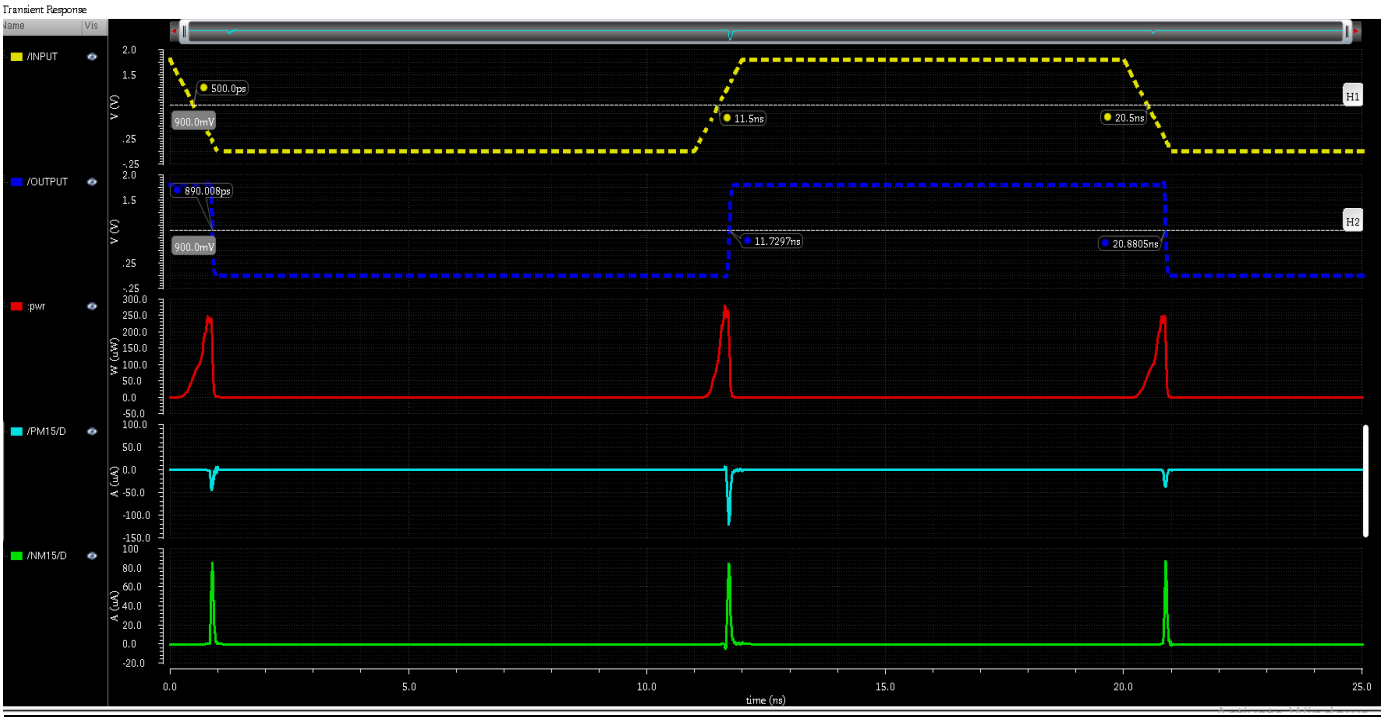


AVERAGE POWER CONSUMPTION

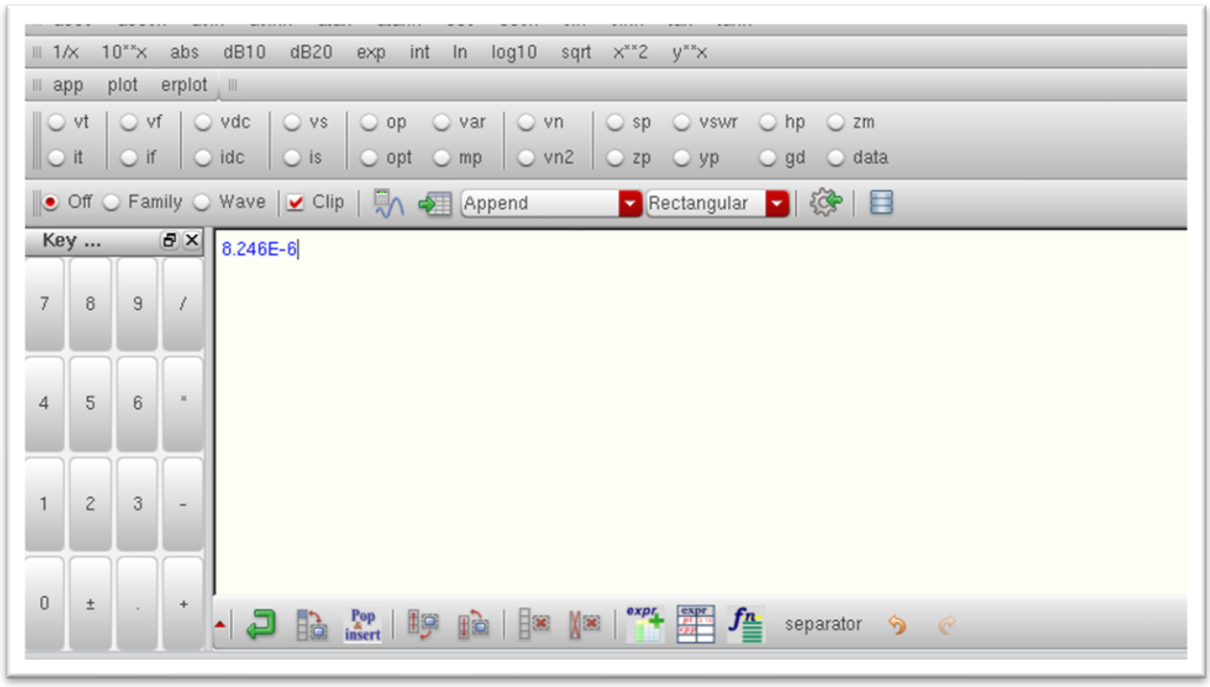


VOLTAGE, CURRENT AND POWER WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

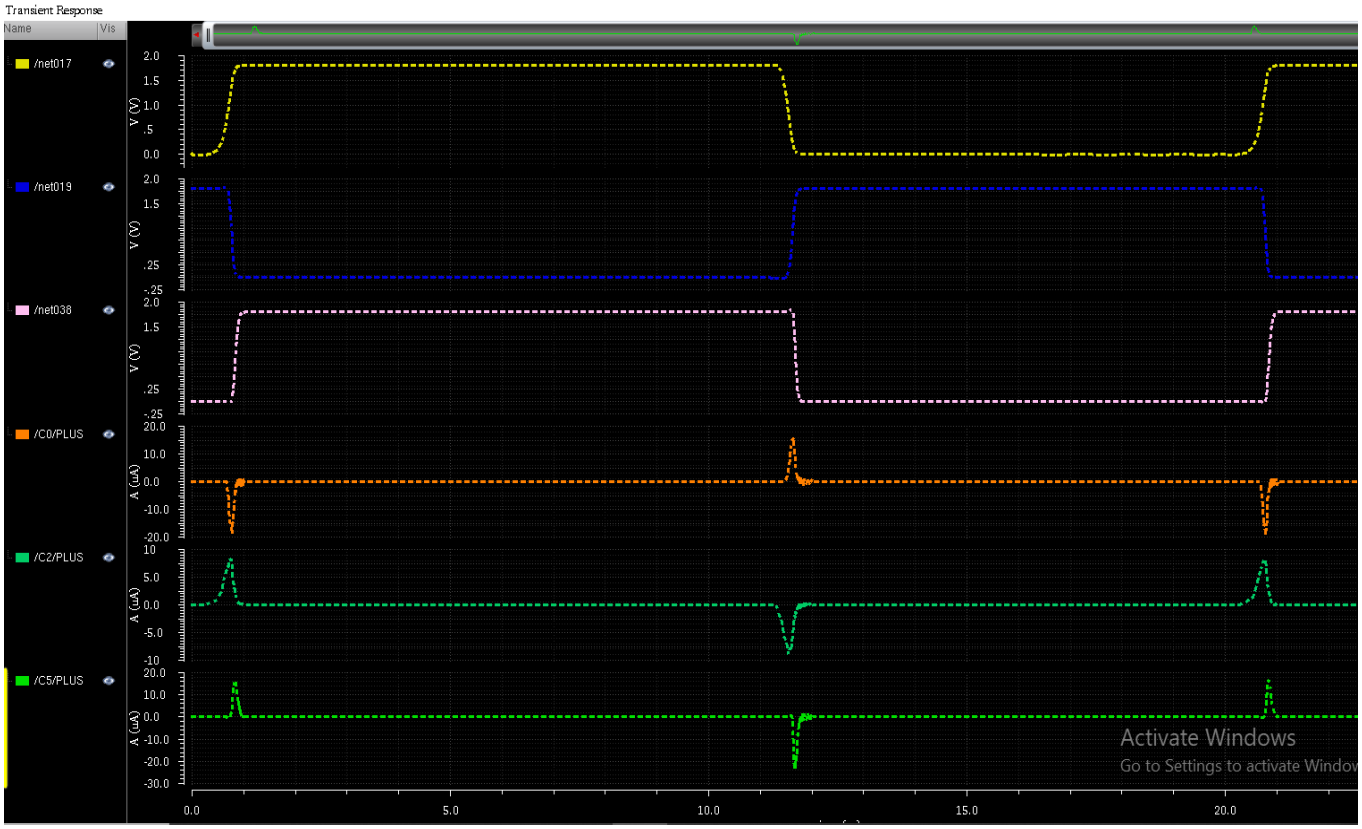
ONOFIC 2-STAGE BUFFER



TIMING DIAGRAM



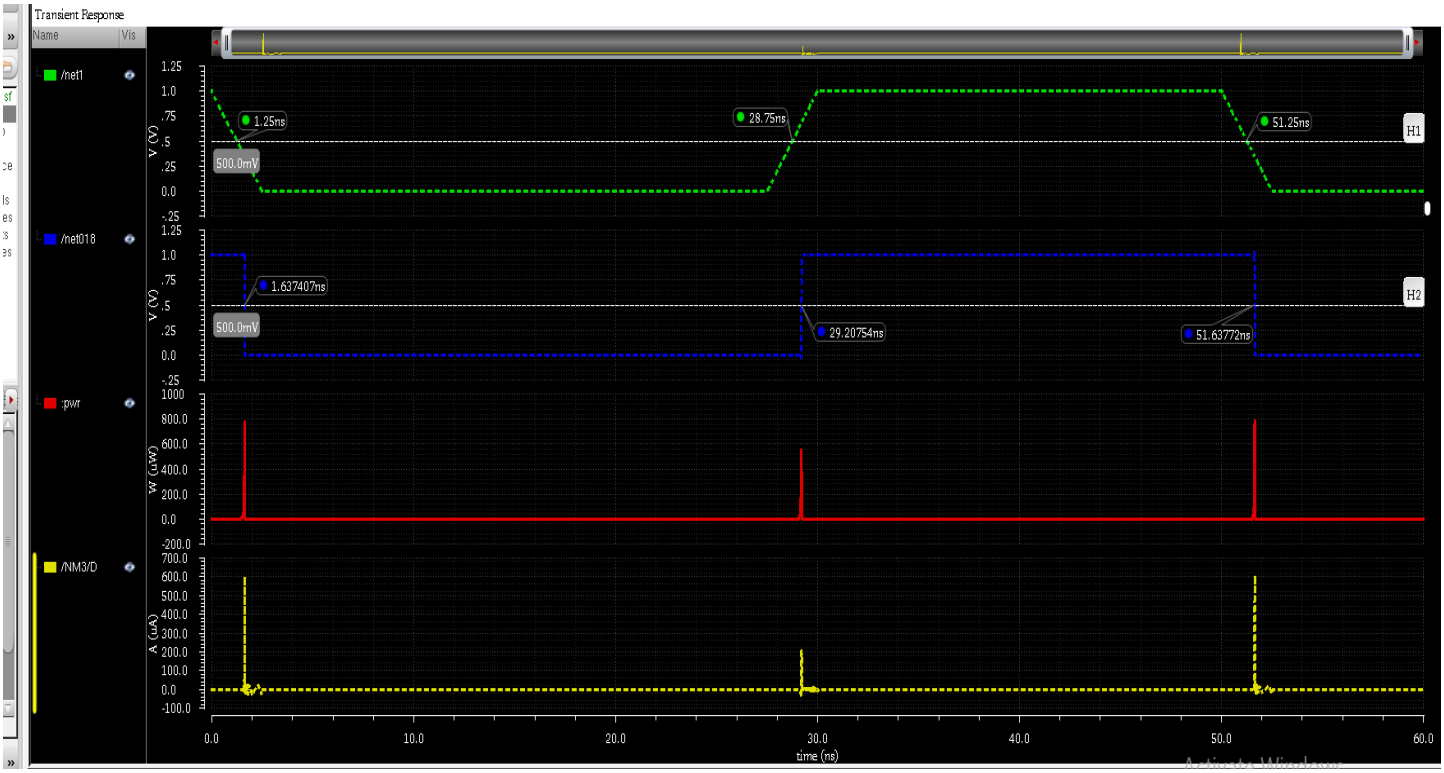
AVERAGE POWER CONSUMPTION



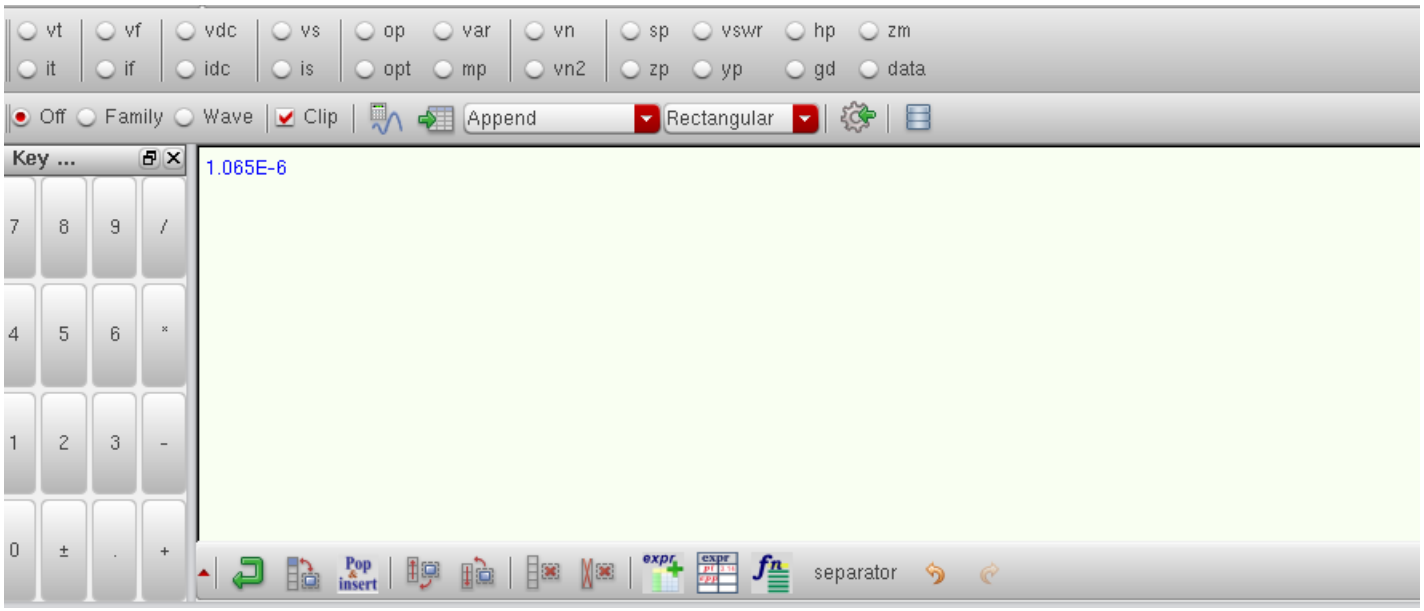
VOLTAGE AND CURRENT WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

SIMULATION RESULTS IN 45nm TECHNOLOGY NODE

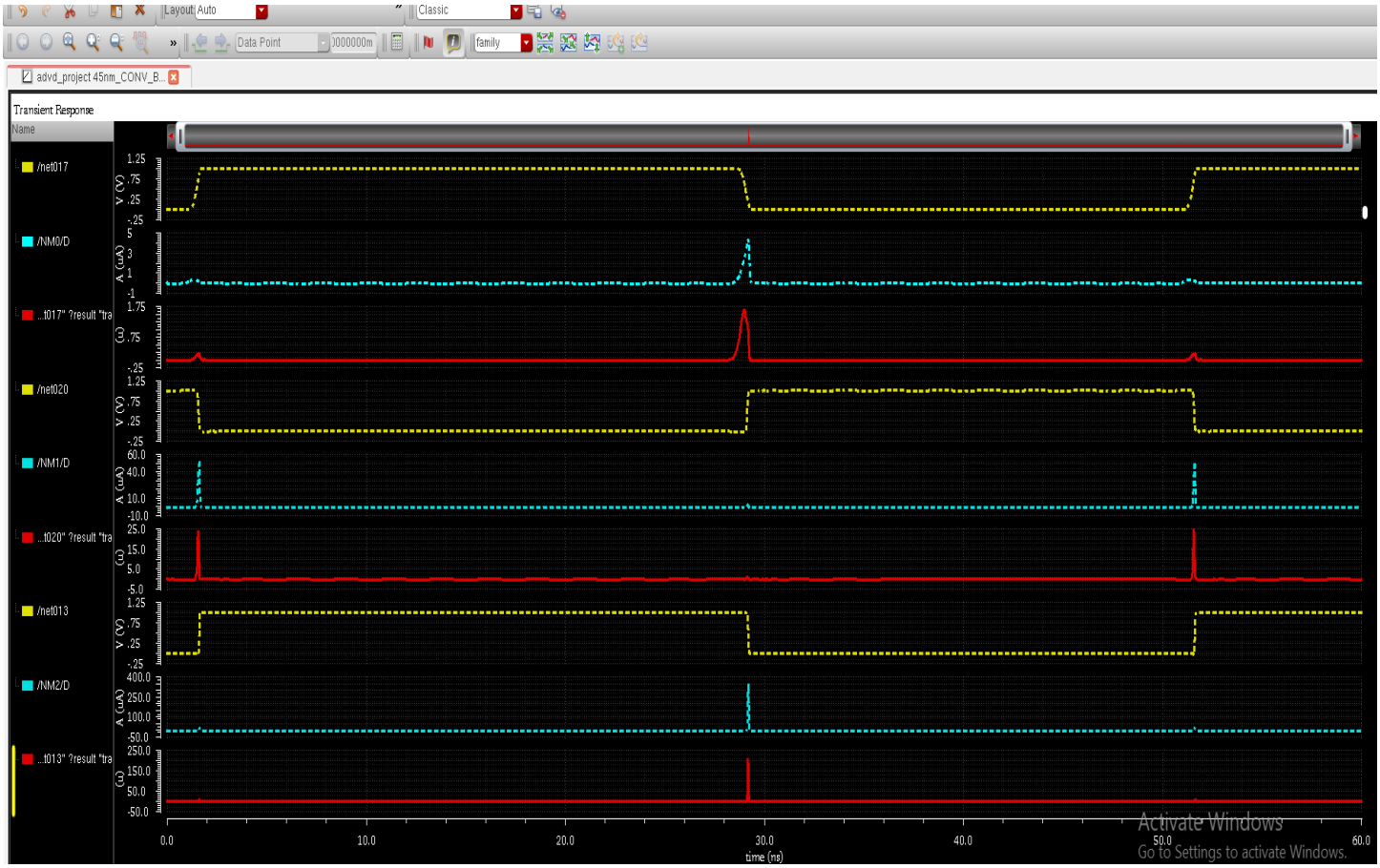
CONVENTIONAL 2-STAGE BUFFER



TIMING DIAGRAM

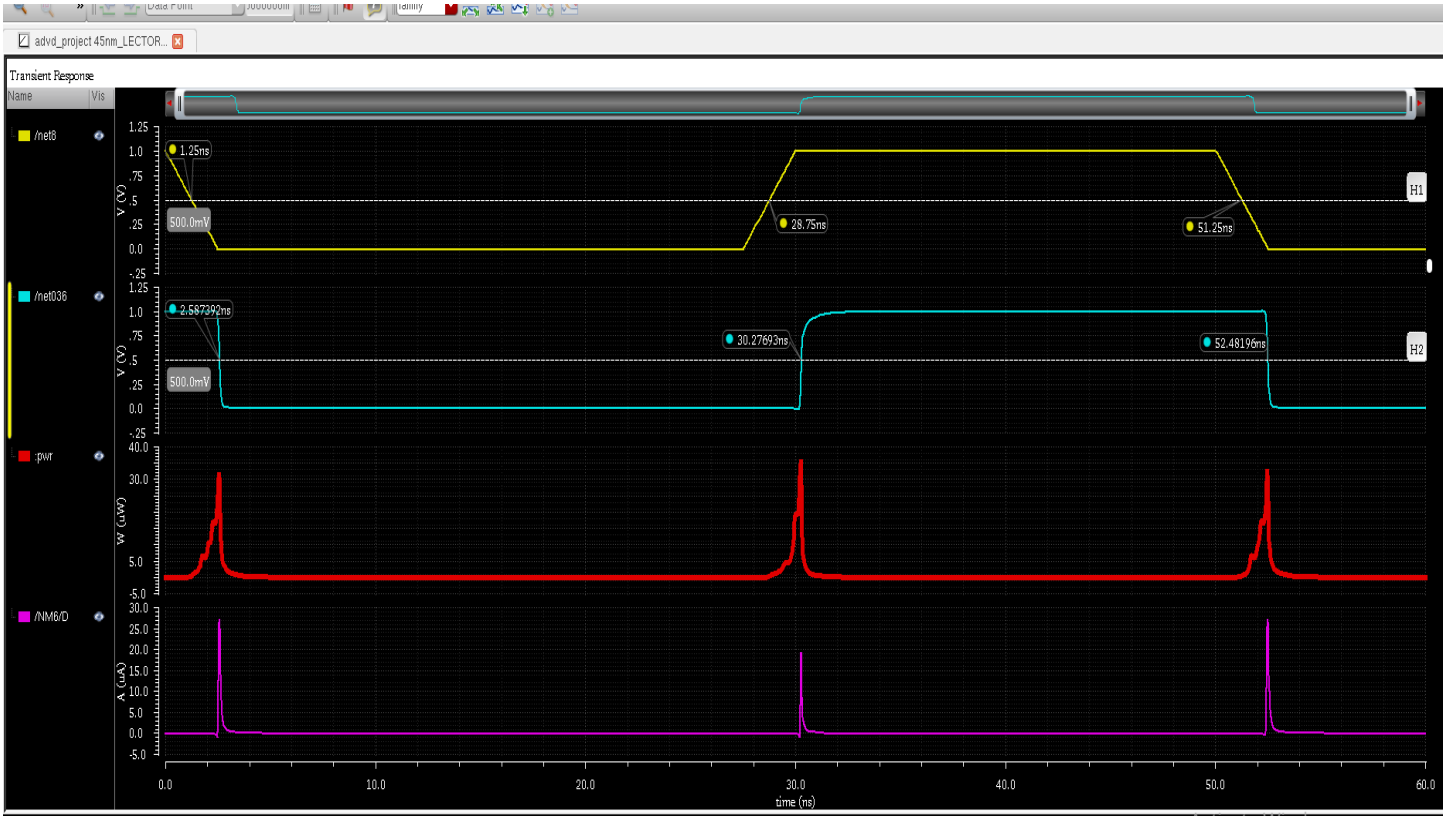


AVERAGE POWER CONSUMPTION

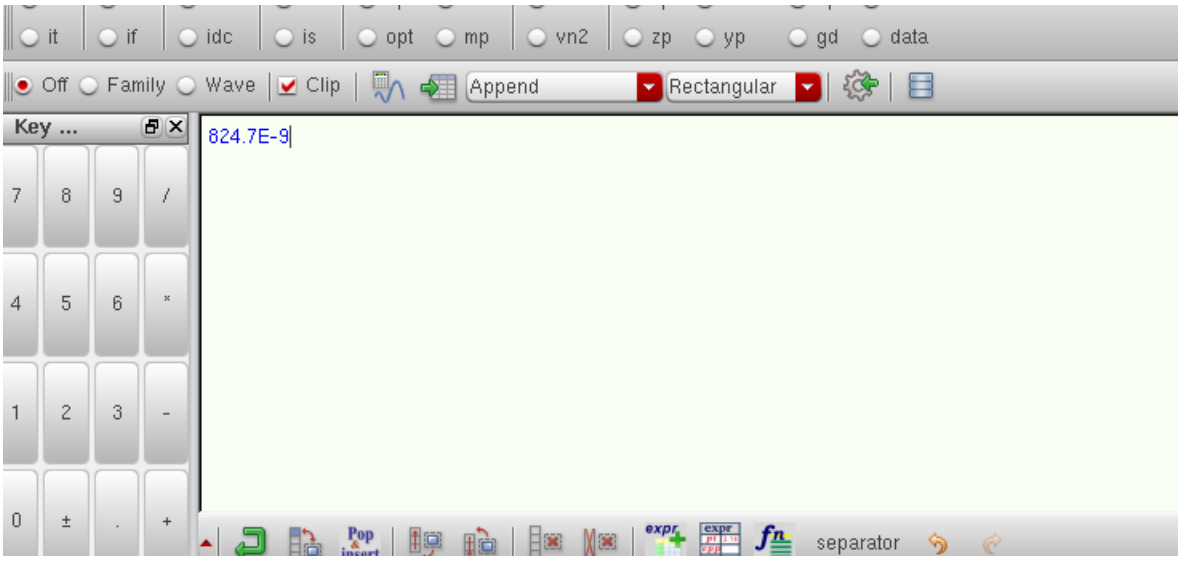


VOLTAGE AND CURRENT WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

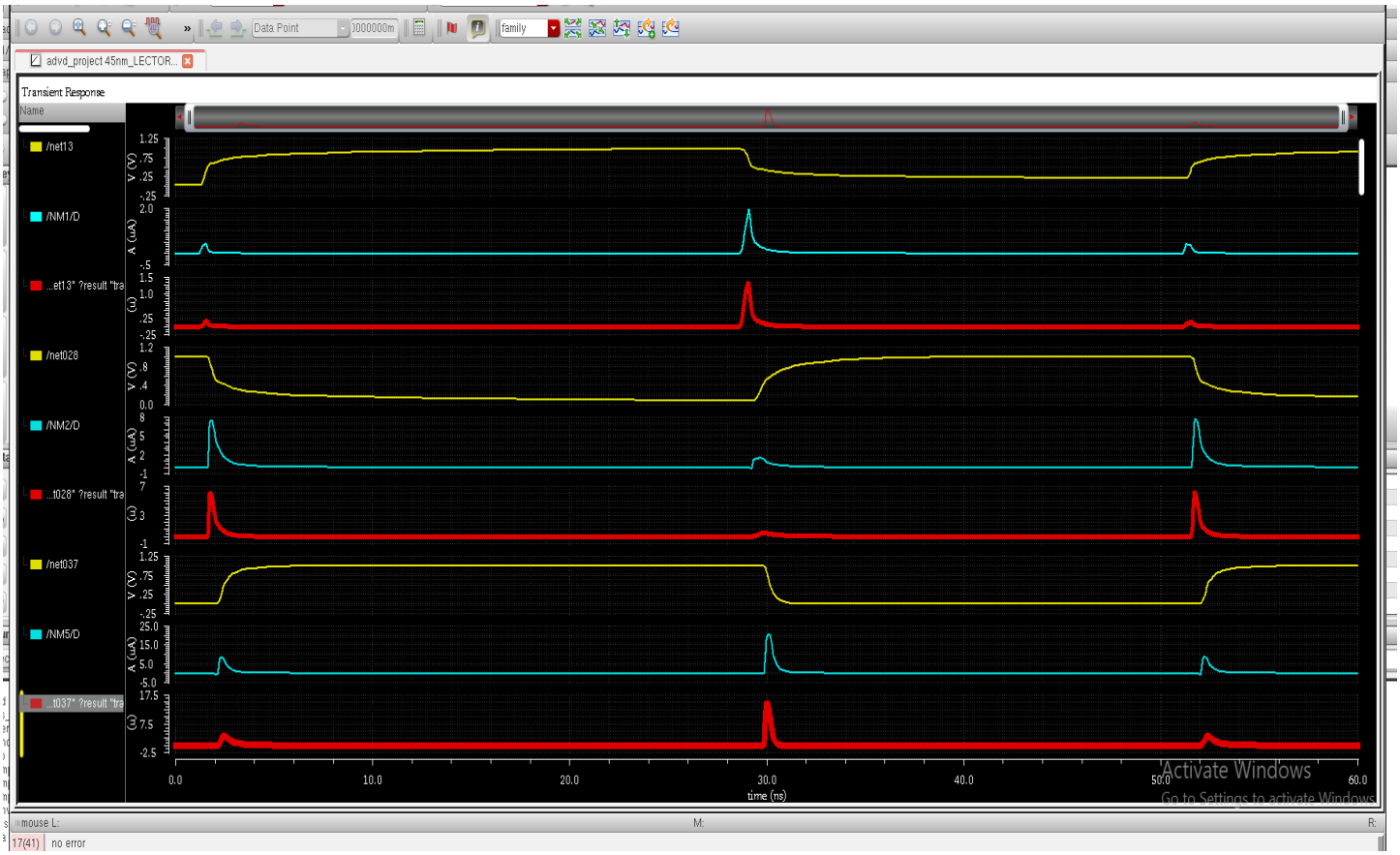
LECTOR 2-STAGE BUFFER



TIMING DIAGRAM



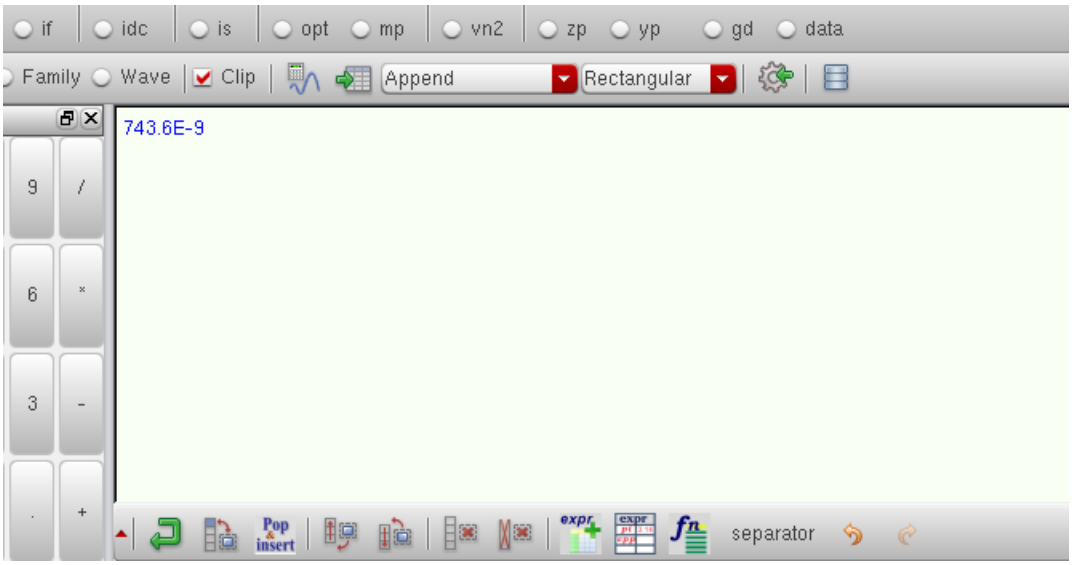
AVERAGE POWER CONSUMPTION



VOLTAGE AND CURRENT WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

ONOFIC 2-STAGE BUFFER

TIMING DIAGRAM

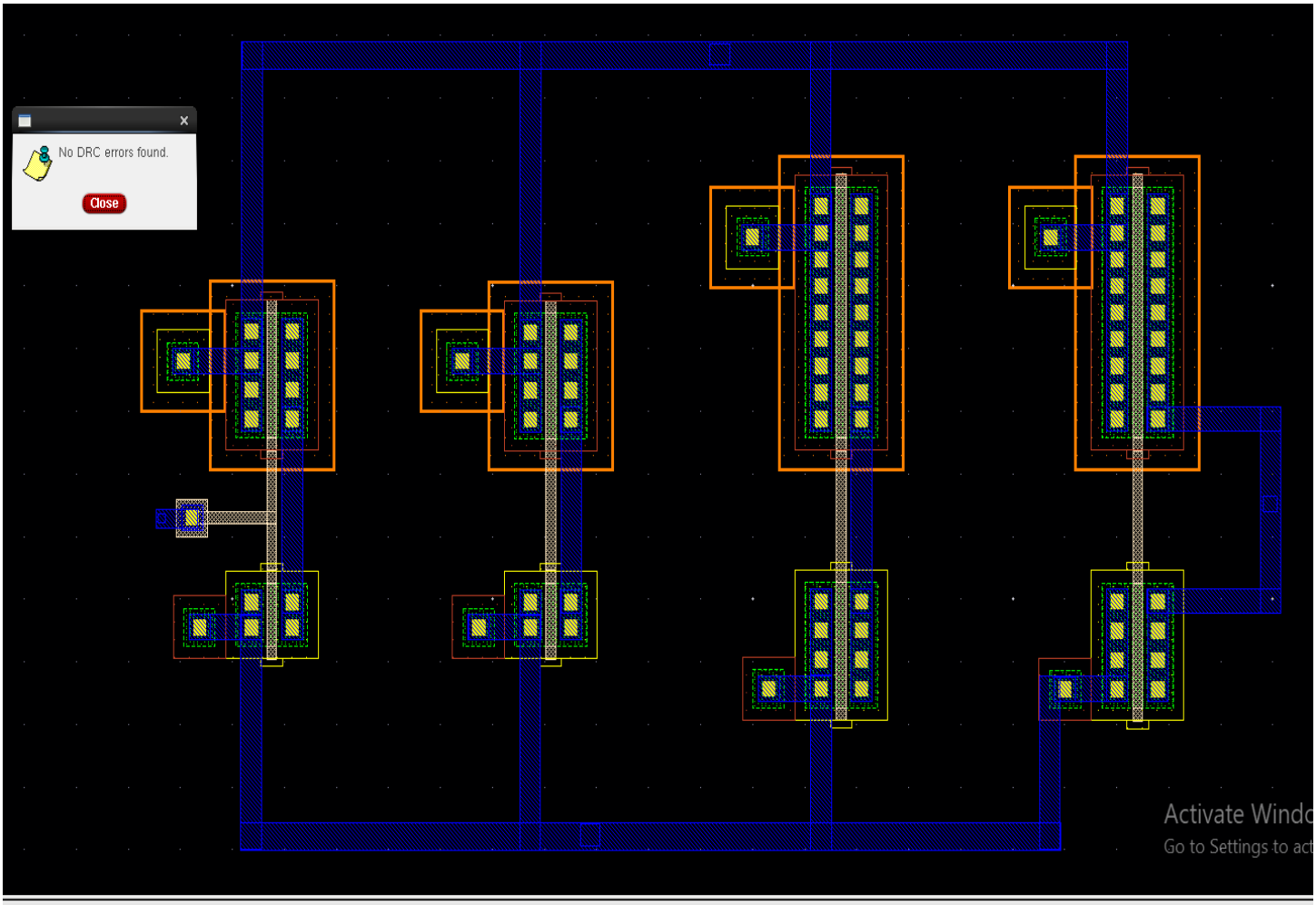


AVERAGE POWER CONSUMPTION

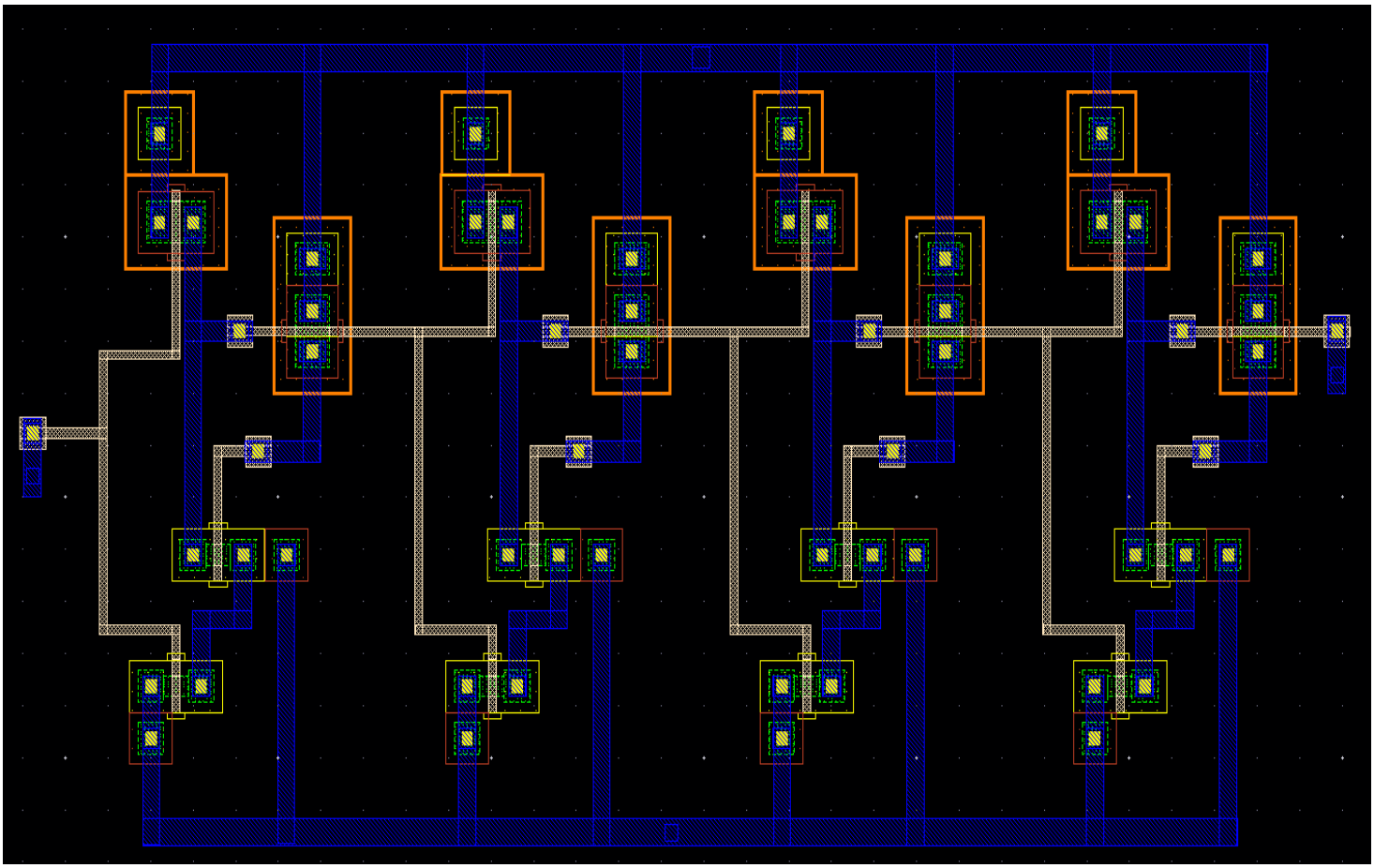
VOLTAGE AND CURRENT WAVEFORMS AT OUTPUT OF EACH INVERTER STAGE

LAYOUT

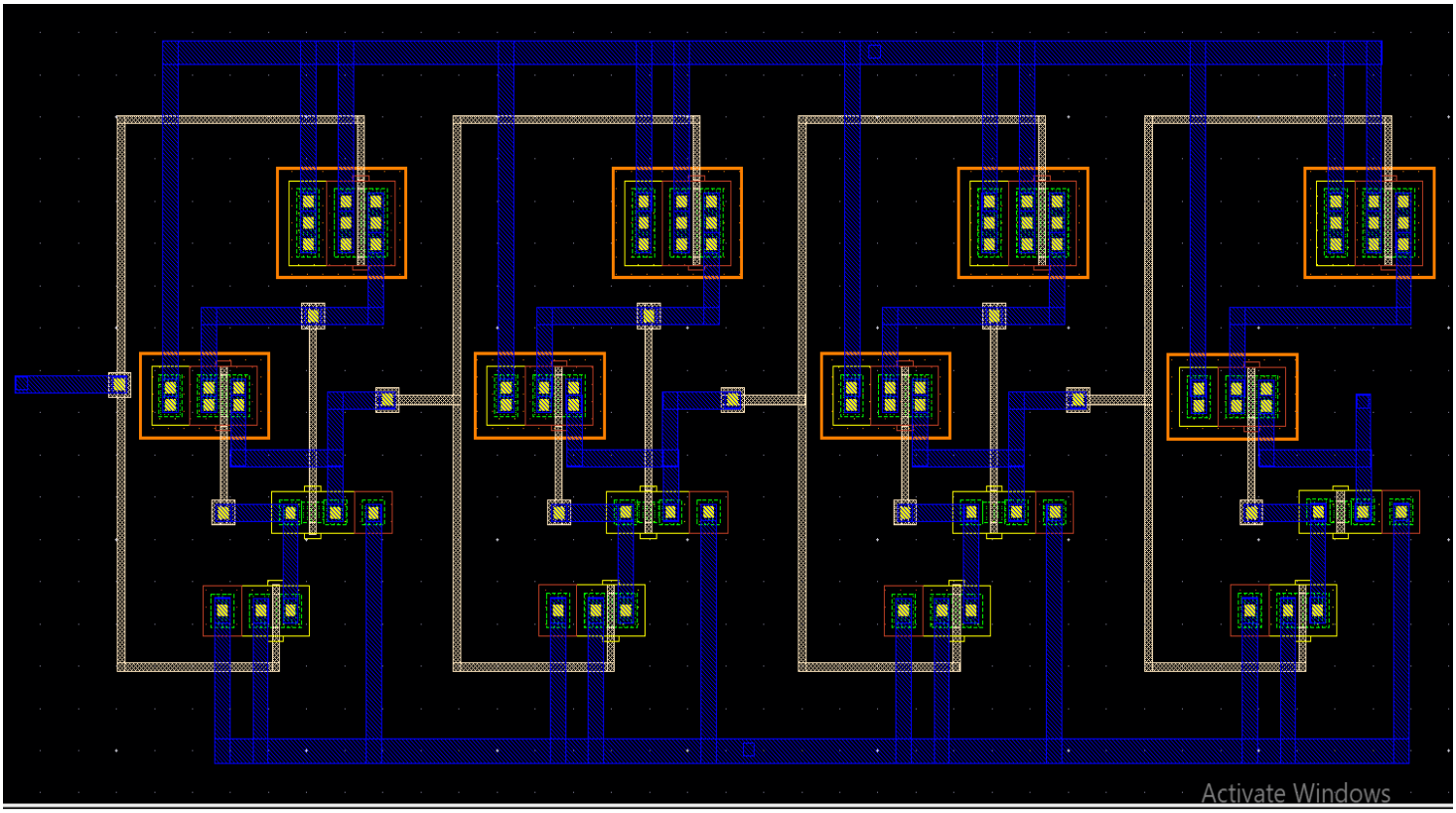
1. CONVENTIONAL 2-STAGE BUFFER



2. ONOFIC 2-STAGE BUFFER



3. LECTOR 2-STAGE BUFFER



RESULTS

For 180nm Technology

Sr. No.	Logic circuit	Power (µW)	Delay (psec)	PDP (x 10^{-18} W-sec)
1	Conventional 2-stage buffer	**16.93**	**205**	**3470.65**
2	ONOFIC 2-stage buffer	**8.24**	**300**	**2472**
3	LECTOR 2-stage buffer	**13.2**	**490**	**6468**

For 45nm Technology

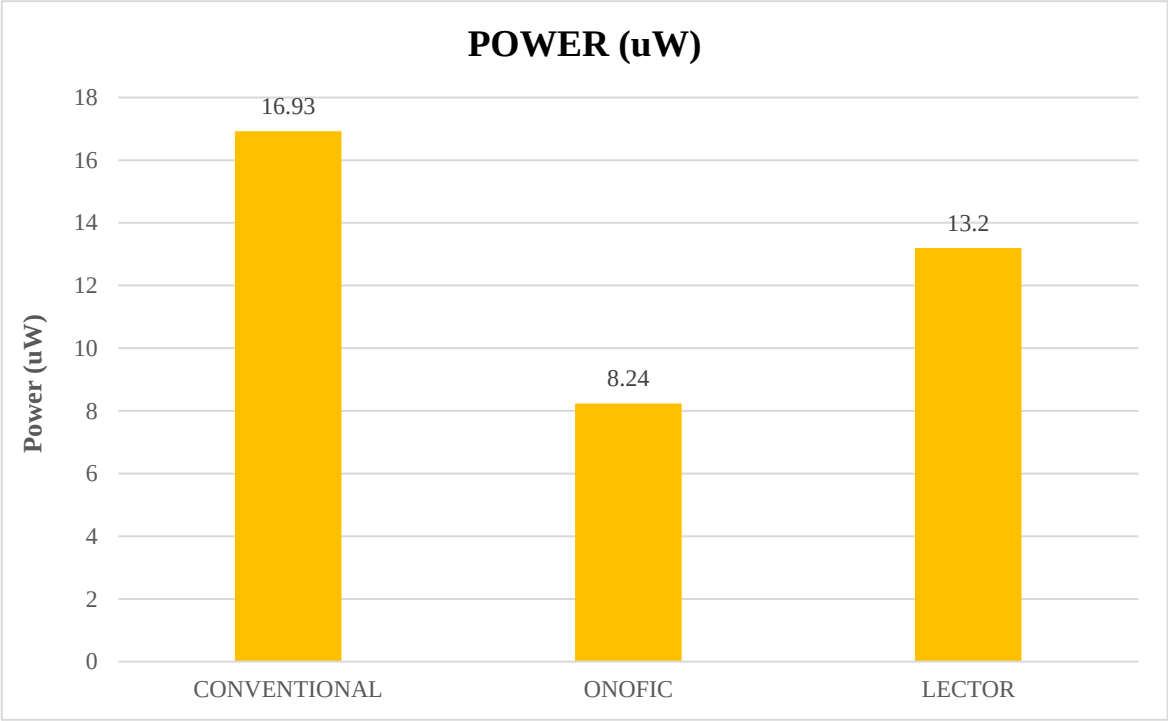
Sr. No.	Logic circuit	Power (µW)	Delay (psec)	PDP (x 10^{-18} W-sec)
1	Conventional 2-stage buffer	**1.06**	**415**	**439.9**
2	ONOFIC 2-stage buffer	**0.74**	**475**	**351.5**
3	LECTOR 2-stage buffer	**0.82**	**1375**	**1127.5**

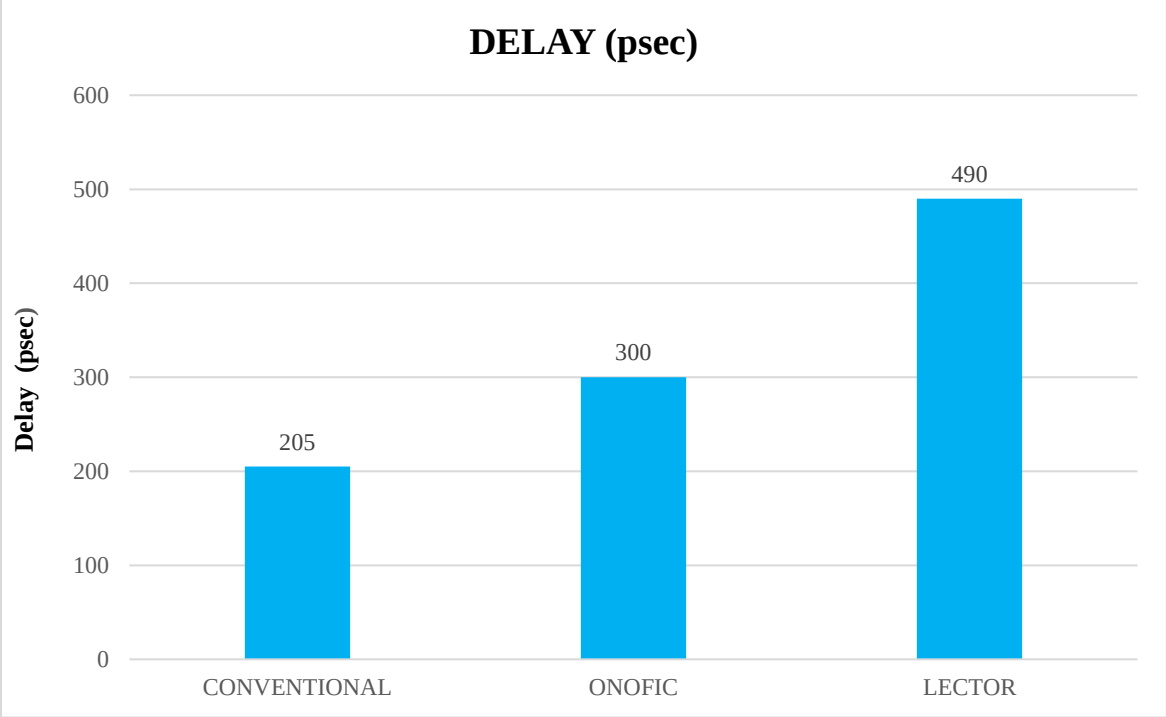
For 90nm Technology

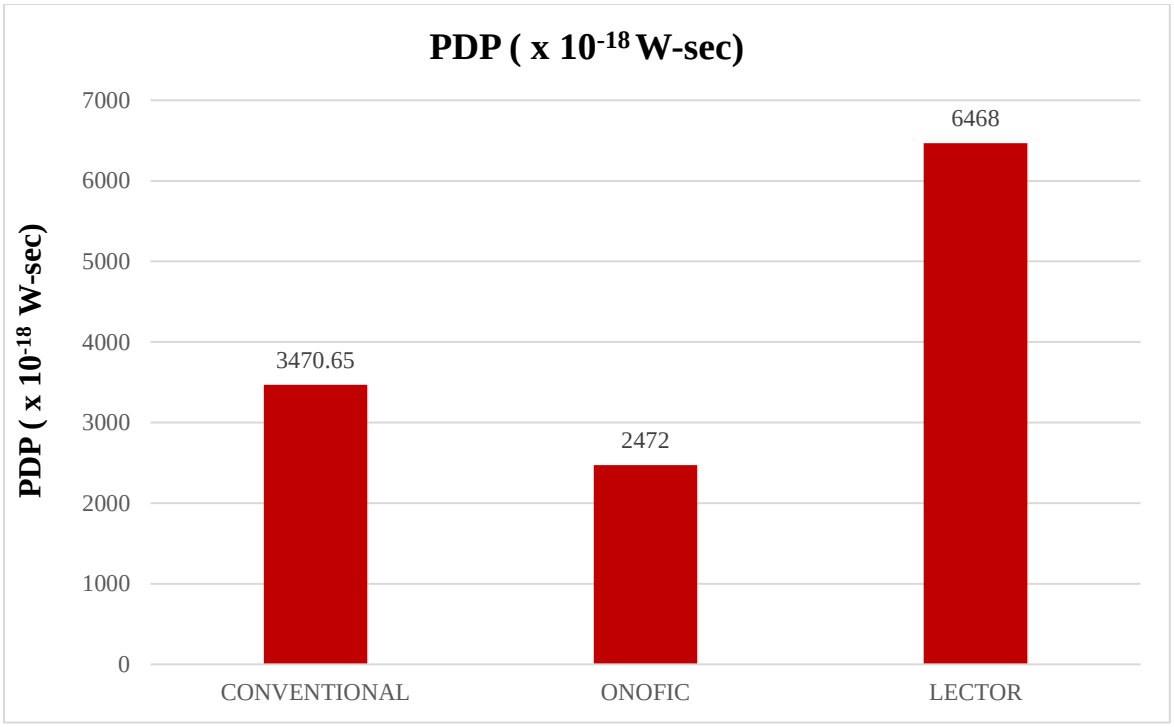
Sr. No.	Logic circuit	Power (µW)	Delay (psec)	PDP (x 10^{-18} W-sec)
1	Conventional 2-stage buffer	**5.20**	**292**	**1518.4**
2	ONOFIC 2-stage buffer	**2.09**	**367**	**767.03**
3	LECTOR 2-stage buffer	**3.83**	**880**	**3370.4**

PERFORMANCE COMPARISON

For 180nm Technology

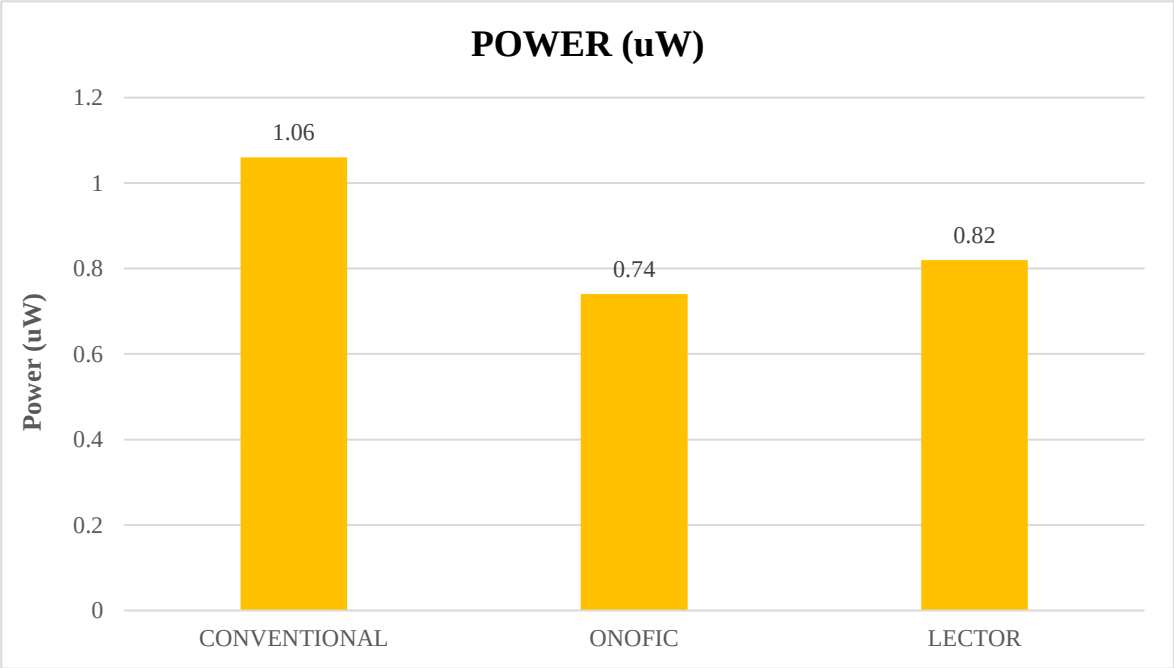


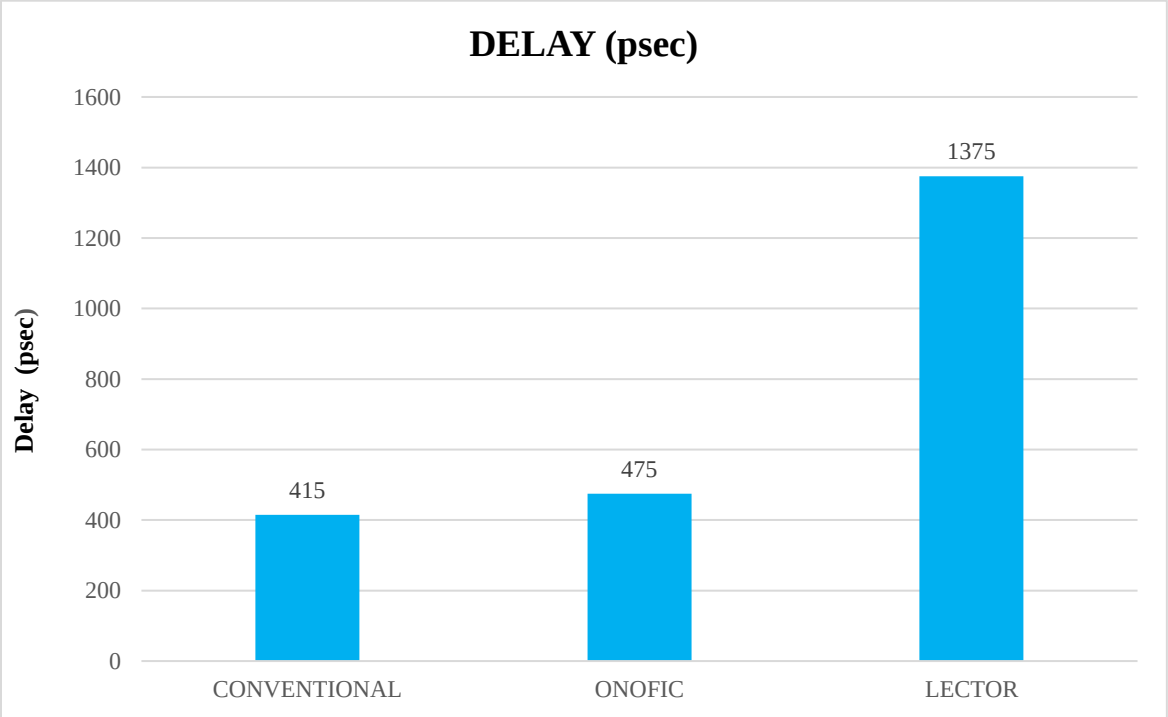


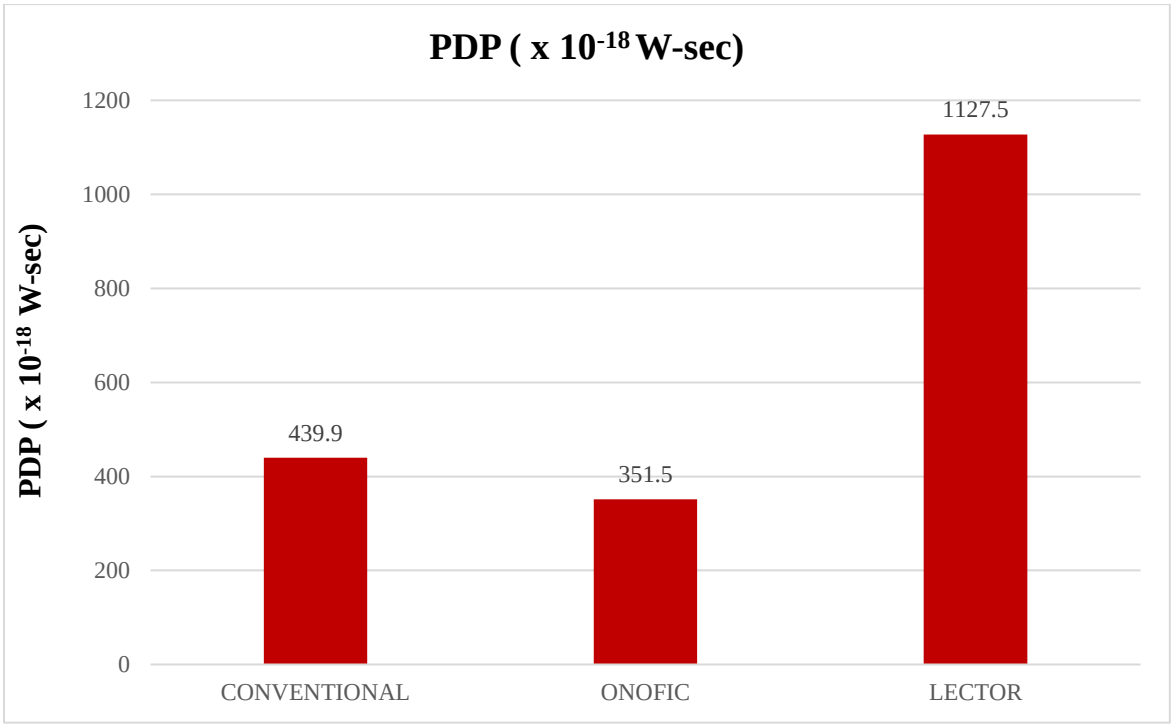

PDP (x 10-18 W-sec)
PDP (x 10-18 W-sec)
7000
6000
5000
4000
3000
2000
1000
0
3470.65
2472
6468
CONVENTIONAL
ONOFIC
LECTOR

PERFORMANCE COMPARISON

For 45nm Technology

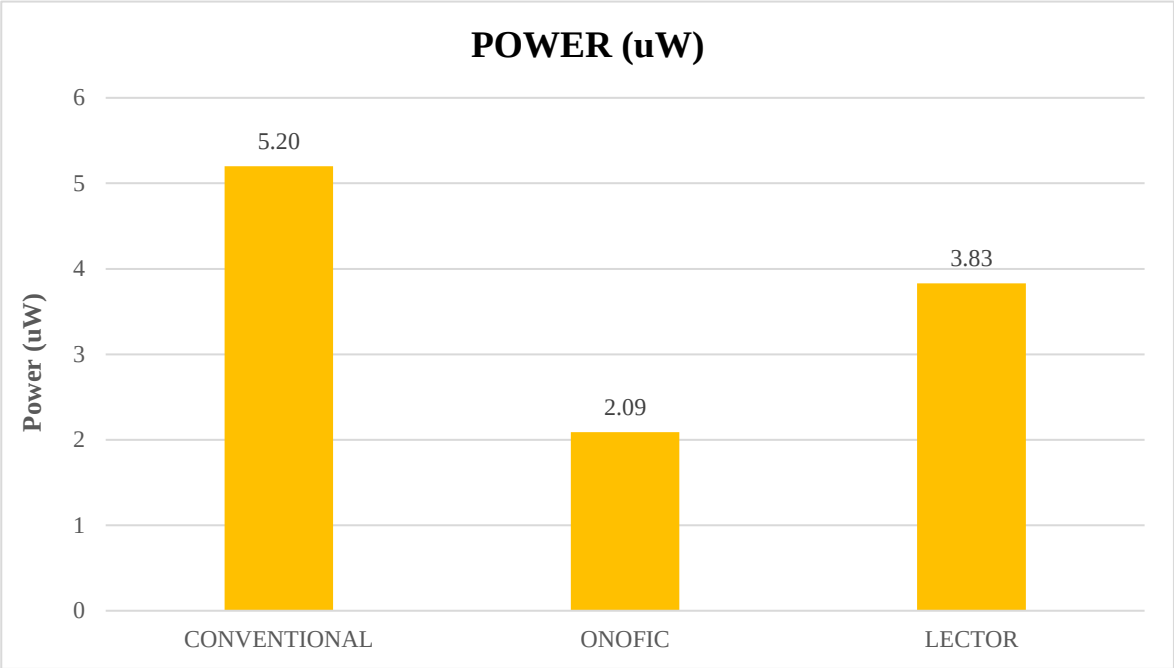


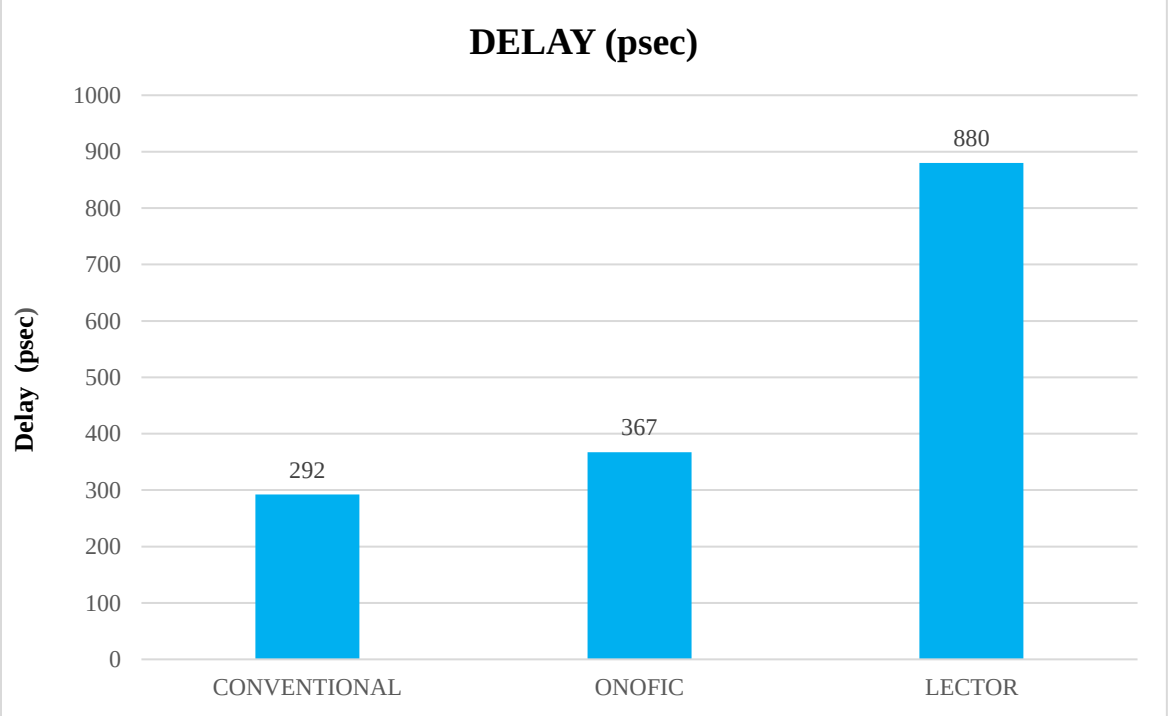


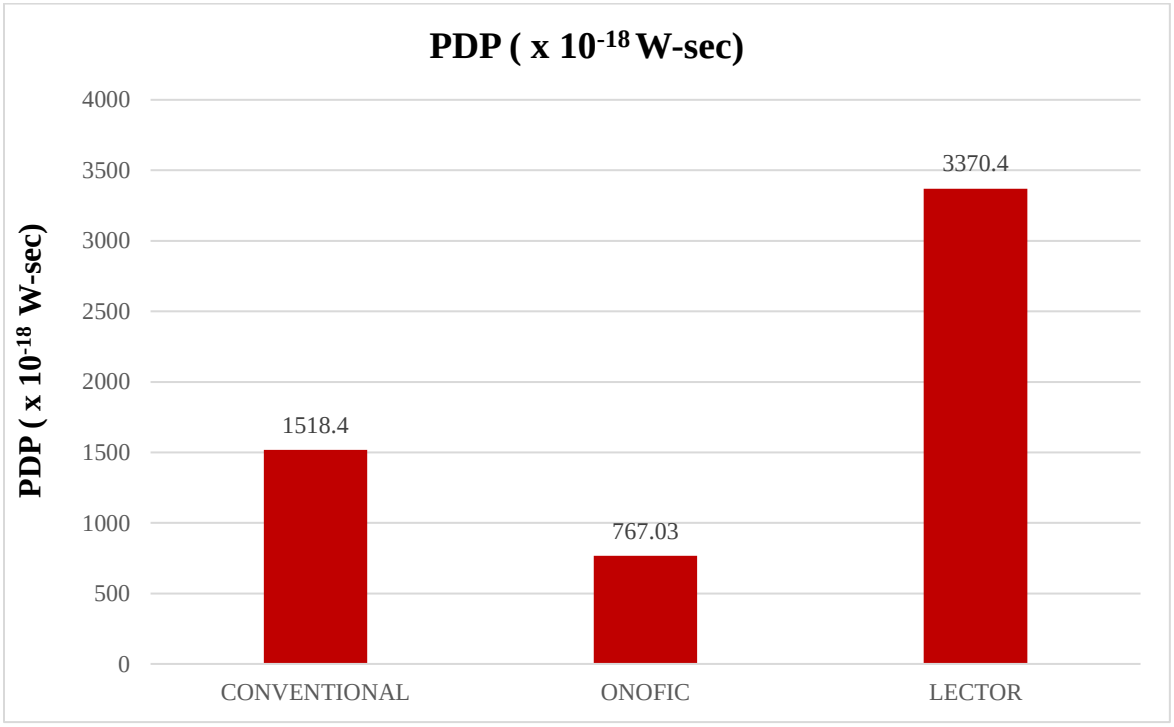

PDP (x 10-18 W-sec)
PDP (x 10-18 W-sec)
1200
1000
800
600
400
200
0
439.9
351.5
1127.5
CONVENTIONAL
ONOFIC
LECTOR

PERFORMANCE COMPARISON

For 90nm Technology






PDP (x 10-18 W-sec)
PDP (x 10-18 W-sec)
4000
3500
3000
2500
2000
1500
1000
500
0
1518.4
767.03
3370.4
CONVENTIONAL
ONOFIC
LECTOR

CONCLUSION

- In Lector technique the leakage power as well as short circuit power consumed by the gates reduces.
- In Lector technique due to stacking effect the delay of the circuit increases. in ONOFIC technique the power consumed is even less due to the feedback control PMOS connected to the output.
- In case of ONOFIC circuits as the gate capacitors of the stacking transistors are not directly connected to the charging and discharging path, the net capacitance of the charging and discharging path are less.
- So, delay in case of ONOFIC circuit is less compared to LECTOR.
- As the technology node reduces the overall power consumed reduces as the supply voltage reduces.
- As the different types of leakage are more in lower technology node the overall result of the circuits takes a hit.