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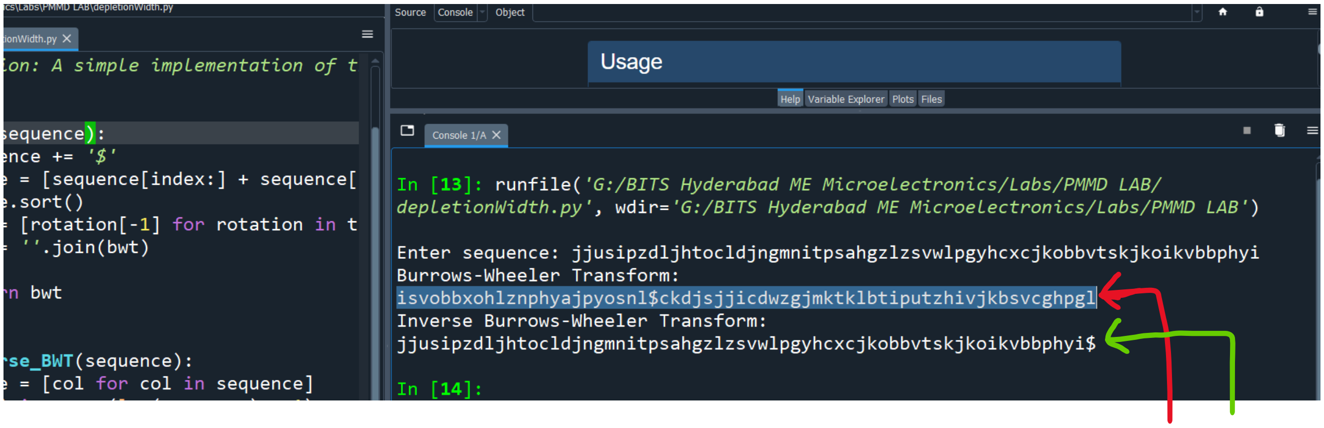
- **Random String generated:**

jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi

- **BWT computed using Python Code:**

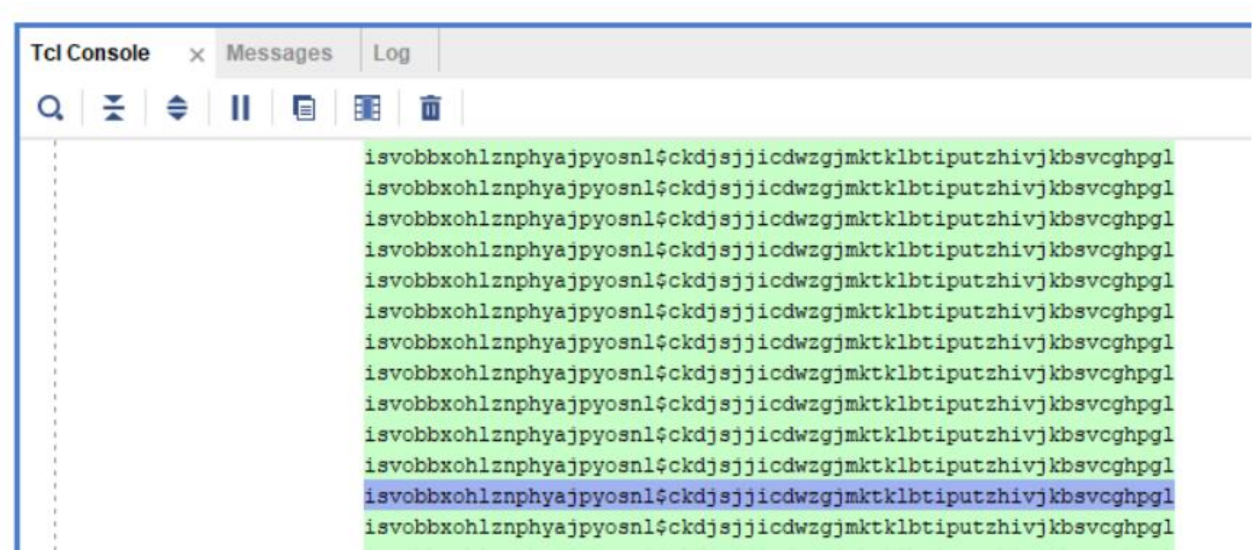
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl



```
ion: A simple implementation of t


sequence):
ence += '$'
e = [sequence[index:] + sequence[
e.sort()
= [rotation[-1] for rotation in t
= ''.join(bwt)

rn bwt


rse_BWT(sequence):
e = [col for col in sequence]
```

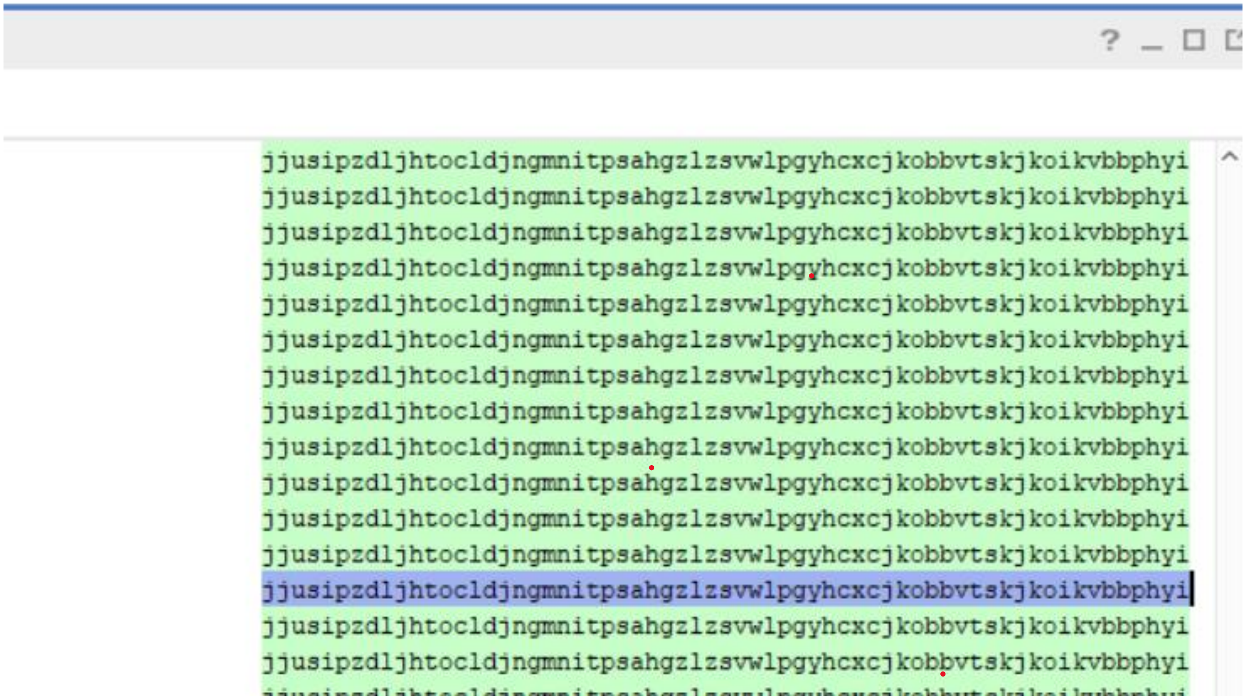
```
In [13]: runfile('G:/BITS Hyderabad ME Microelectronics/Labs/PMMD LAB/
depletionWidth.py', wdir='G:/BITS Hyderabad ME Microelectronics/Labs/PMMD LAB')

Enter sequence: jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
Burrows-Wheeler Transform:
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
Inverse Burrows-Wheeler Transform:
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi$

In [14]:
```

- **BWT computed using Verilog code:**



```
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
isvobbxohlznphyajpyosnl$ckdjsjjicdwzgjmktklbtiputzhivjkbsvcghpgl
```

- **IBWT computed using Verilog code:**



```
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
jjusipzdljhtocldjngmnitpsahgzlzsvwlpgyhcxcjkobbvtskjkoikvbbphyi
```

From the above results, it is verified that the Verilog code for BWT and IBWT is working correctly.

The output from Verilog code and python code matched exactly.

So the Verilog module is verified.