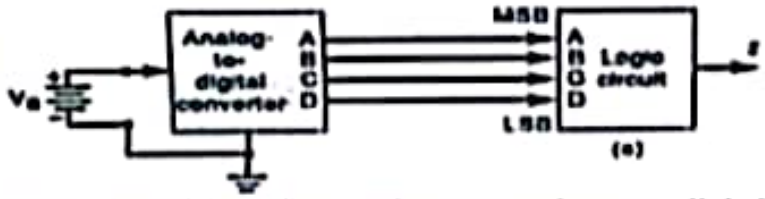
QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR 2022 OF 20 BATCH B.E (CS)

SUBJECT: DIGITAL LOGIC DESIGN

Dated: 30.05.2022 | Maximum Marks: 60 | Time Allowed: 3 Hour

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No		QUESTIONS	CLO	Taxonomy Level	PLO	Marks
01	(a)	Implement the logic circuit for the following expression 1. $x = [D + (\overline{A + B})C] \cdot E$ 2. $y = AC + B\bar{C} + \bar{A}BC$	CLO_2	C_3	PLO_2	06
	(b)	Simplify the following logic expressions using Boolean algebra/theorems. Also, Implement the simplified expressions using fundamental gates. 1. $z = \overline{(\bar{A} + C)} + \overline{(B + \bar{D})}$ 2. $\omega = \overline{(A + BC) \cdot (D + EF)}$	CLO_2	C_3	PLO_2	06
02		Describe the NAND and NOR gates in detail. Also, explain why these gates are called universal gates. Draw all fundamental gates using NAND/NOR gates and also prove them using the expressions.	CLO_1	C_2	PLO_1	12
03		 (a) Refer to the above Figure, where an analogue-to-digital converter is monitoring the dc voltage of a 12-V storage battery on an orbiting spaceship. The converter's output is a four-bit binary number, ABCD, corresponding to the battery voltage in steps of 1 V, with A as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is greater than and equal to $0110_2 = 6_{10}$; that is, the battery voltage is greater than and equal to 6 V. Design this logic circuit. Use K-map for simplifying the expression.	CLO_2	C_3	PLO_2	12
04	(a)	What are a Multiplexer and a De-multiplexer? Analyze the operation of 4-to-1 Multiplexer and 1-to-4 De-multiplexer with its logic diagrams, logic circuits, and truth table.	CLO_3	C_4	PLO_4	06
	(b)	Design a full adder logic circuit.	CLO_3	C_4	PLO_4	06
05	(a)	Analyze the operation of the NAND latch to verify its truth table. Describe the concept of setup and hold times using a proper timing diagram.	CLO_3	C_4	PLO_4	06
	(b)	What are a counter and its types? Design and analyze the operation of 3-bit asynchronous counter in detail.	CLO_3	C_4	PLO_4	06

Best of Luck!

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR 2022 OF 20-BATCH B.E (ES)

SUBJECT: DIFFERENTIAL EQUATIONS & FOURIER SERIES

Dated: 26.05.2022 **Maximum Marks: 60** **Time Allowed: 3 Hours**

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.		QUESTION	CLOs	Ma
Q. 01	(a)	i. Define PDE and give at least two examples of your choice. ii. Mention the names of methods used for forming PDEs.	C2	
	(b)	Use Method of Separation of Variables to solve the PDE $$\frac{\partial^2 V}{\partial x^2} = \frac{\partial V}{\partial t}$$	C2	
Q. 02	(a)	Find the Fourier series for the Periodic function $$f(x) = \begin{cases} 0, & -\pi < x < 0 \\ x, & 0 < x < \pi \end{cases}$$ $$f(x + 2\pi) = f(x)$$	C2	
	(b)	Define Even and Odd functions with Examples. Explain definite integral property of Even and Odd functions in your own words.	C2	
Q. 03	(a)	Find the Fourier Transform of 1. $f(x) = \begin{cases} 1 & for\ \|x\| < a \\ 0 & for\ \|x\| > a \end{cases}$	C3	
	(b)	State the Convolution theorem on Fourier transform	C3	
Q. 04		If $F_1(s)$ and $F_2(s)$ are Fourier transforms of $f_1(x)$ and $f_2(x)$ respectively, then prove the following (i) $F[af_1(x) + bf_2(x)] = aF_1(s) + bF_2(s)$ (ii) $F[f_1(x-a)] = e^{ias}F_1(s)$	C3	
Q. 05		Discuss and write some applications of differential equations in i. RLC Circuits ii. Electrical\ Mechanical Vibrations	C3	

The End

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR, 2022 OF 20 BATCH, B.E (ES)

SUBJECT: INSTRUMENTATION & MEASUREMENTS

Dated: 23.05.2022 Maximum Marks: 60 Time Allowed: 3 Hour

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No	QUESTIONS	CLO	Taxon. Level	PLO	Marks
Q.01 (a)	Explain the construction and working principle of a strain gauge as a force sensor.	2	C_2	02	[06]
(b)	Define the following phenomenon i. See back effect ii. Photoelectric effect iii. Stress and strain	1	C_1	01	[06]
Q.02 (a)	Demonstrate how RTD sensors work and how temperature is measured using RTD sensors in any application and sketch the output characteristics of the RTD transducer.	3	C_3	04	[08]
(b)	A platinum RTD with α =0.00392Ω/ Ω/C° has a normal resistance of 100 Ω at 0C°. (a) Compute the resistance at 450 C°. (b) Calculate, at what temp the resistance of the RTD is 170 Ω.	3	C_3	04	[04]
Q.03	Explain the working principle of the thermocouple transducer. Also compare the performance with other temperature transducers on the basis of temperature range, cost, and characteristics.	2	C_2	02	[12]
Q.04 (a)	A capacitive transducer used two quartz diaphragm of an area of 750mm separated by a distance of 7mm. A pressure of 900 KN/m² was applied to the top of the diaphragm producing a deflection of 1.2mm. The capacitor is 446 pF when pressure is applied. Calculate the value of capacitance when no pressure was applied.	3	C_3	04	[06]
(b)	A resistance strain gauge with a Gauge Factor of 5 is cemented to a steal chamber which is subjected to $1x10^{-4}$ strain. If the original resistance value of the gauge is 120 Ω then, calculate the impact of strain on resistance.	3	C_3	04	[06]
Q.05 (a)	Discuss how capacitive sensors work and which parameters of the capacitor can be used for the purpose of sensing.	2	C_2	02	[06]
(b)	Explain the working principle of Hall effect sensors.	2	C_2	02	[06]

The End

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR, 2022 OF 20-BATCH, B.E (ES)

SUBJECT: PAKISTAN STUDIES

Dated: 02.06.2022 Maximum Marks: 30 Time Allowed: 02 Hours

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.		QUESTION	CLOs	Taxonomy Level	PLOs	Marks
Q. 01		Discuss the problems faced by Pakistan at the time of its creation.	1	C1	6	10
Q. 02		Constitution is the supreme law of land. Discuss the salient features of Constitution of 1973.	2	C2	12	10
Q. 03		Discuss the causes hampered the Indo-Pak relations.	2	C2	12	10

The End

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

MID-SEMESTER EXAMINATION OF FIRST SEMESTER – SECOND YEAR (3RD SEMESTER) 2022, 20 BATCH, B.E (ES/CH)

SUBJECT: DIFFERENTIAL EQUATIONS & FOURIER SERIES

Dated: 15.02.2022 **Maximum Marks: 20** **Time Allowed: 01 Hour.**

NOTE: ATTEMPT ANY TWO (02) QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No		CLO	Taxonomy Level	Marks
01(a)	Differentiate between Initial and Boundary conditions; Is it $\frac{d^2y}{dx^2}+y=0,\quad y(0)=1, y(\frac{\pi}{2})=-1$ Initial condition value problem?	1	C1	06
01(b)	Form the differential equation from the given relation $y=(x^3+k)e^{-3x}$	5	C5	04
02(a)	Find the general solution of the following: i $\frac{dy}{dx}=1+x+y^2+xy^2$ ii $\frac{dy}{dx}=\frac{x^3+y^3}{x^3y+xy^3}$	4	C4	06
02(b)	Define Exact and Non-exact differential equations; hence check whether it is Exact or Non-exact. $(3x^2y+2)dx+(x+y)dy=0$	1	C1	04
03	A cup of a coffee was initially boiling at $80^{\circ}C$, it was placed in air at $40^{\circ}C$ after 20 minutes the temperature was $60^{\circ}C$, what will be the temperature of coffee after 40 minutes?	3	C3	10

---Good Luck---

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

MID-SEMESTER EXAMINATION OF FIRST SEMESTER – SECOND YEAR (2nd SEMESTER) 2022, 20 BATCH, B.E (ES)

SUBJECT: INSTRUMENTATION & MEASUREMENTS

Dated: 14.02.2022 Maximum Marks: 20 Time Allowed: 01 Hour.

NOTE: ATTEMPT ANY TWO (02) QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No	QUESTIONS	CLO	Taxonomy Level	PLO	Marks
Q.01 (a)	Define the following types of instruments: (I) Absolute and Secondary instrument (II) Indicating and recording instrument	01	C_1	01	[05]
Q.01 (b)	Define the following terms. I) Accuracy & Precision II) Reproducibility III) Drift iv) Dead zone v) Signal to Noise Ratio	01	C_1	01	[05]
Q.02(a)	Discuss the elements of generalized Measurement system with the help of block diagram.	02	C_2	02	[06]
Q.02(b)	An amplifier whose Bandwidth is 150 KHz has some noise power spectrum density 6×10^{-21} J. If the input resistance is 50 KΩ and Amplifier gain is 100. Calculate noise input voltage.	02	C_2	02	[04]
Q.03(a)	Explain the working principle of PMMC Instruments.	02	C_2	02	[06]
Q.03(b)	An amplifier has a signal voltage level of 5μV at the input and noise voltage level of 1μV. (I) Calculate the SNR at the input. (II) If the voltage gain of an amplifier is 10, calculate the SNR at the output.	02	C_2	02	[04]

"Best Courage"