QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

MID-SEMESTER EXAMINATION OF FIRST SEMESTER – SECOND YEAR (3rd SEMESTER) 2022, 20 BATCH, B.E (TC)

SUBJECT: CIRCUIT ANALYSIS

Dated: 17.02.2022 Maximum Marks: 20 Time Allowed: 01 Hour.

NOTE: ATTEMPT ANY TWO (02) QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.			CLO	Taxonomy Level	Marks
Q. 01	(a)	With the help of figures explain the applications of ohm's law. Also derive an expression for the current divider rule when two resistors are connected in parallel.	1	C_1	05
	(b)	Calculate the effective resistance of the following combination of resistances shown in Figure (a) and voltage drop across each resistance when a p.d of 60V is applied across the terminals A and B.	3	C_3	05
Q. 02	(a)	State Kirchhoff's laws as applied to electrical circuits. Enlist its applications. Also write-down the steps used for solving a circuit using nodal analysis method.	1	C_1	05
	(b)	A network is shown in Figure (b), determine the line currents I_a,I_b and I_c. Also show that the sum of currents at reference node is zero.	3	C_3	05
Q. 03	(a)	What do you mean by analyzing an electric circuit? Also define the following terms, a) Linear and non-linear electric circuits b) Unilateral and bilateral elements c) Ideal and practical sources d) Node and its types	1	C_1	05
	(b)	A network is shown in Figure (c). Using Δ-Y or Y-Δ transformation compute the resistance between terminals AB, BC and CA.	3	C_3	05

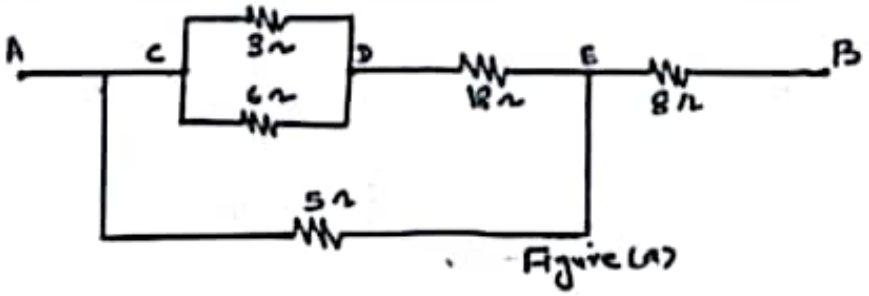

Figure (a)

16

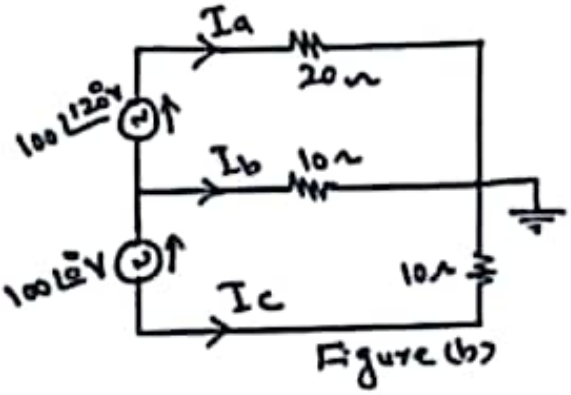

Figure (b)

Figure (c)

Good Luck

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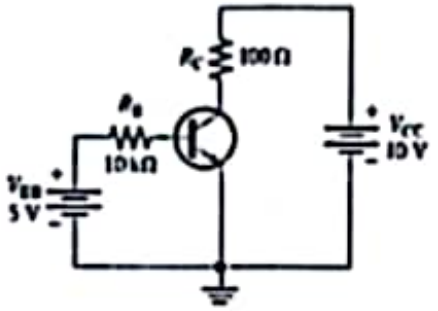
MID-SEMESTER EXAMINATION OF FIRST SEMESTER – SECOND YEAR (3rd SEMESTER) 2022, 20 BATCH, B.E (TC)

SUBJECT: AMPLIFIER & OSCILLATORS

Dated: 18.02.2022 Maximum Marks: 20 Time Allowed: 01 Hour.

NOTE: ATTEMPT ANY TWO (02) QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.		Question	CLO	Taxonomy Level	Marks
Q. 01	(a)	Draw the circuit of a practical single stage transistor amplifier. Explain the function of each component.	1	C2	05
	(b)	Determine I_B, I_C, I_E, V_{BE}, V_{CE} and V_{CB} in the circuit given below. The transistor has a $\beta_{ac} = 150$. 	1	C3	05
Q. 02	(a)	Explain transistor RC coupled amplifier with special reference to frequency response, advantages, disadvantages and applications.	1	C2	07
	(b)	A single stage amplifier has a voltage gain of 60. The collector load $R_c = 500\Omega$ and input impedance is 1KΩ. Calculate the overall gain when two stages are cascaded through R-C coupling. Comment on the result.	1	C3	03
Q. 03		Write note on any two of the following: i. Common collector amplifier ii. Hybrid parameters of a transistor iii. Transformer coupled transistor amplifier	1	C4	10

Good Luck

$V_T =$

300

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

MID-SEMESTER EXAMINATION OF FIRST SEMESTER – SECOND YEAR (3rd SEMESTER) 2022, 20 BATCH, B.E (TC)

SUBJECT: DIGITAL LOGIC DESIGN

Dated: 16.02.2022 Maximum Marks: 20 Time Allowed: 01 Hour.

NOTE: ATTEMPT ANY TWO (02) QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.		Question	CLO	Taxonomy Level	Marks
Q. 01	(a)	Do as directed: 1. $C8_{16} - 3A_{16}$ = _____ 16. 2. 1011100.10101_2 = _____ 10. 3. $11110011_2 + 1001_2$ = _____ 2.	1	C1	06
	(b)	Draw the NAND and NOR gate equivalent of AND, OR and Inverter.	2	C2	04
Q. 02	(a)	Reduce $f(ABCD) = \Sigma(1,3,4,5,7,10,11,12,14,15)$ by using K-Map. Also find the minimized expression.	1	C1	04
	(b)	Draw the K-Map table and expression for each of the following inputs: 1. $f = \Sigma(0,2,4,6,8,10,12,14)$ 2. $f = \Sigma(4,5,6,7)$ 3. $f = \Sigma(4,5)$	2	C2	06
Q. 03		Simplify the following Boolean expression: $\bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$ Also draw the circuit diagram of the simplified expression by using NOR universal gate.	3	C3	10

Good Luck

ID. No/Seat No.

QUAID-E-AWAM UNIVERSITY OF ENGINEERING SCIENCE AND TECHNOLOGY, NAWABSHAH

MID-SEMESTER EXAMINATION 2022 OF FIRST SEMESTER – SECOND YEAR (3rd SEMESTER) 20-BATCH B.E (CC)

(TELECOMMUNICATION ENGINEERING)

TECHNICAL REPORT WRITING AND PRESENTATION SKILLS

Dated: 14-02-2022 **Time Allowed: 45 MINUTES** **Max. Marks:**

NOTE: ATTEMPT ANY TWO QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No		CLO	Taxonomy Level	Marks
01	"The most important thing in communication is hearing what is not said". Describe the proverb by relating with the values of non-verbal communication according to your own perception.	01	C2	05
02	What is the importance of technical writing report in professional life? Describe its types, examples and definitions.	01	C2	05
03	Discuss the purpose of oral presentation.	01	C2	05

Name of Subject Teacher: Hijab-e-zahra

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR 2022 OF 20 BATCH, B.E (TC)

SUBJECT: TECHNICAL REPORT WRITING & PRESENTATION SKILLS

Dated: 06.06.2022 Maximum Marks: 30 Time Allowed: 02 Hours

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.	QUESTION	CLOs	Taxonomy Level	PLOs	Marks
Q. 01	Describe the Format Guidelines for technical report writing.	2	C2	2	10
Q. 02	Discuss characteristics of technical writing report by giving related examples.	2	C2	2	10
Q. 03	Explain how can we improve our presentation skills in the class?	3	C2	3	10

The End

QUAID-E-AWAM UNIVERSITY OF ENGINEERING, SCIENCE & TECHNOLOGY, NAWABSHAH

FINAL SEMESTER REGULAR EXAMINATION OF FIRST SEMESTER – SECOND YEAR 2022 OF 20 BATCH, B.E (TC)

SUBJECT: DIGITAL LOGIC DESIGN

Dated: 30.05.2022 Maximum Marks: 60 Time Allowed: 3 Hour

NOTE: ATTEMPT ALL QUESTIONS. ALL QUESTIONS CARRY EQUAL MARKS.

Q. No.		QUESTION	CLOs	Taxonomy Level	Mar
Q. 01	(a)	A staircase light is controlled by two switches one at the top of the stairs and another at the bottom of the stairs: 1. Make the truth table for this system 2. Write the logic equation in SOP form 3. Realize the circuit using AND-OR gates	1	C2	0
	(b)	Convert -98_{10} to two's complement and verify the result.	1	C3	0
Q. 02	(a)	Draw the truth table, equations, circuit and block symbol of half adder and full adder.	2	C4	0
	(b)	Draw the truth table and logic diagram of decimal to BCD encoder.	2	C2	0
Q. 03	(a)	Define display devices and discuss different types of display devices.	3	C3	0
	(b)	Define shift register discuss the basic forms of data movement in shift registers.	3	C4	0
Q. 04	(a)	By using 4-bit adder perform the following addition, when A=1011 and B=1110. Draw neat and clean diagram also. Write down the C_{out} and Sum output of each stage.	1	C2	0
	(b)	Draw neat and clean diagram of 1 to 4 line MUX.	2	C3	0
Q. 05		Write short notes on the following: 1. Latch and its types 2. Flip Flop and its types	3	C4	

The End