Lab2 Stage 1

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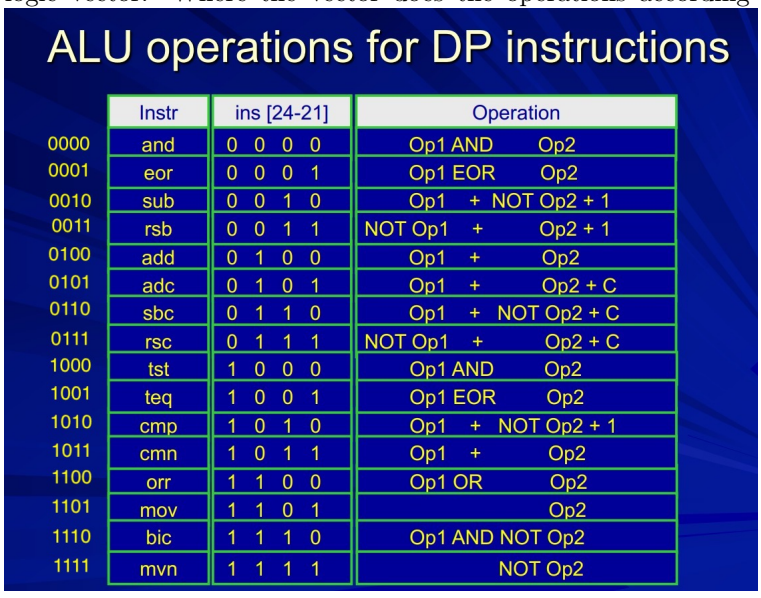
1 Introduction

Designing and Testing of basic Modules like ALU, Register File, Program Memory and Data Memory.

2 ALU

It is a Combinational Circuit taking 2 operands($op1$ and $op2$) which are 32 bit standard logic vectors. It outputs $result$ which is also a standard 32 bit standard logic vector. The operation to be done(op) is modelled as 4 bit standard logic vector. Where the vector does the operations according to the figure:



	Instr	ins [24-21]	Operation
0000	and	0 0 0 0	Op1 AND Op2
0001	eor	0 0 0 1	Op1 EOR Op2
0010	sub	0 0 1 0	Op1 + NOT Op2 + 1
0011	rsb	0 0 1 1	NOT Op1 + Op2 + 1
0100	add	0 1 0 0	Op1 + Op2
0101	adc	0 1 0 1	Op1 + Op2 + C
0110	sbc	0 1 1 0	Op1 + NOT Op2 + C
0111	rsc	0 1 1 1	NOT Op1 + Op2 + C
1000	tst	1 0 0 0	Op1 AND Op2
1001	teq	1 0 0 1	Op1 EOR Op2
1010	cmp	1 0 1 0	Op1 + NOT Op2 + 1
1011	cmn	1 0 1 1	Op1 + Op2
1100	orr	1 1 0 0	Op1 OR Op2
1101	mov	1 1 0 1	Op2
1110	bic	1 1 1 0	Op1 AND NOT Op2
1111	mvn	1 1 1 1	NOT Op2

Here the ins is precisely the vector op.
We also take input carryin(a bit) and output carryout(a bit) for performing the operations like addc. For finding this carryout, we create a signal of 33 bits and after operation, the last bit would represent the carry while the rest 32 bits

would represent the add or subtract value.

```
# Info: Device Utilization for 7A100TCSG324
# Info: ***********************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------------------
# Info: IOs                               102     210      48.57%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              196     63400     0.31%
# Info: CLB Slices                        49      15850     0.31%
# Info: Dffs or Latches                   34      126800    0.03%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------------------
# Info: ************************************************
# Info: Library: work    Cell: ALU    View: BEV
# Info: ************************************************
# Info:  Number of ports :                          102
# Info:  Number of nets :                           532
# Info:  Number of instances :                      463
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                 34
# Info:  Number of LUTs :                           196
# Info:  Number of Primitive LUTs :                 197
# Info:  Number of LUTs with LUTNM/HLUTNM :           2
# Info:  Number of MUX CARRYs :                      63
# Info:  Number of accumulated instances :          463
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
```

3 Register File

3.1 Inputs

- Read Addresses x2(4 bit standard logic vector)
- Write Address x1(4 bit standard logic vector)
- Data Input x1(32 bit standard logic vector)
- Write Enable x1(1 to enable write and 0 to disable it)

- Clock x1

Contains Array of 16 standard logic vector of 32 bits each (Named MEMORY). If Write enable is 1, then at rising clock edge, the Input Data gets written into the Memory at the Write Address.

3.2 Outputs

- Data Outputs x2(32 bit standard logic vectors): Contents of Memory selected by Read Addresses are outputted

```
# Info: Device Utilization for 7A100TCSG324
# Info: ***********************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------------------
# Info: IOs                               110     210      52.38%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              48      63400     0.08%
# Info: CLB Slices                        12      15850     0.08%
# Info: Dffs or Latches                   4       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: Distributed RAMs
# Info:    RAM32M                         10
# Info:    RAM64M                         2
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------------------
# Info: ***************************************************************
# Info: Library: work    Cell: RegisterFiles    View: BEV
# Info: ***************************************************************
# Info:  Number of ports :                          110
# Info:  Number of nets :                           225
# Info:  Number of instances :                      116
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                  4
# Info:  Number of LUTs :                            48
# Info:  Number of Primitive LUTs :                  48
# Info:    Number of LUTs as Distributed RAM :       48
# Info:  Number of accumulated instances :          128
# Info: ****************************
```

4 Program Memory

4.1 Inputs

- Address x1(6 bit standard Logic Vector denoting the address of memory to be read)

It's memory cannot be changed once initialized. It only reads the Memory present at the Input Address and outputs it to Read Data Port.

4.2 Outputs

- ReadData x1(32 bit standard logic vector)

```
# Info: ********************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ********************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: --------------------------------------------------------------------
# Info: IOs                               38      210      18.10%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              32      63400     0.05%
# Info: CLB Slices                        8       15850     0.05%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: --------------------------------------------------------------------
# Info: ********************************************************************
# Info: Library: work    Cell: ProgramMemory    View: BEV
# Info: ********************************************************************
# Info:  Number of ports :                          38
# Info:  Number of nets :                           76
# Info:  Number of instances :                      70
# Info:  Number of references to this view :         0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           32
# Info:  Number of Primitive LUTs :                 32
# Info:  Number of gates :                          32
# Info:  Number of accumulated instances :          70
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
# Info: Design: work.ProgramMemory.BEV
```

5 Data Memory

5.1 Inputs

- Address x1(6 bit standard logic vector)
- Write Data x1(32 bit standard Logic Vector)
- Write Enable x1(4 bit standard Logic Vector)
- Clock x1

At the rising edge of the clock, it writes the bytes of Write Data specified by the Write Enable to the Address of the Memory.

5.2 Outputs

- ReadData x1(32 bit standard Logic Vector): It outputs the data present at the Address of the Memory.

```
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                              Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                                   75      210      35.71%
# Info: Global Buffers                        1       32        3.12%
# Info: LUTs                                  32      63400     0.05%
# Info: CLB Slices                            8       15850     0.05%
# Info: Dffs or Latches                       0       126800    0.00%
# Info: Block RAMs                            0       135       0.00%
# Info: Distributed RAMs
# Info:    RAM64M                             8
# Info: DSP48E1s                              0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: DataMemory    View: BEV
# Info: ************************************************************
# Info:  Number of ports :                            75
# Info:  Number of nets :                            150
# Info:  Number of instances :                        79
# Info:  Number of references to this view :           0
# Info: Total accumulated area :
# Info:  Number of LUTs :                             32
# Info:  Number of Primitive LUTs :                   32
# Info:    Number of LUTs as Distributed RAM :        32
# Info:  Number of accumulated instances :            83
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
# Info: Design: work.DataMemory.BEV
```