Lab2 Stage 2

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1 Introduction

Single Cycle Multi Component Processor Design in VHDL. Created Components such as Program Counter, Flags and Condition Checker for this stage.

2 Program Counter

The Program Counter is updated by an increment of 4 in every rising edge of the clock cycle. But if we have an offset and a branch instruction then the Program counter is updated by the respective offset + 8.

2.1 Inputs

- PCin x1(32 Bit standard Logic Vector)
- Clk x1(1 bit standard logic clock)
- Predicate x1(1 bit standard logic)
- Offset x1(24 bit standard logic vector)

2.2 Output

- PCout (32 Bit Standard Logic Vector)

3 Flags

The Flags are conditionally updated on every clock cycle.

3.1 Inputs

- carryout: The carry output from ALU
- op1: The first input for ALU
- op2: The second input for ALU

- result: The result of operation from ALU
- S: Standard Logic Selector

3.2 Outputs

- Z: Zero Flag, 0 when result not equal to 0, 1 when result equals 0.
- N: Negative Flag, 1 when result is negative(32nd bit is 1) else 0.
- V: Overflow Flag = op1(31) xor op2(31) xor result(31) xor carryoutput.
- C: Carry Flag = 33nd bit of result

How DP instructions affect Flags C, V, Z, N

<table>
<tr><td rowspan="2">Instructions</td><td colspan="3">Effect on Flags</td></tr>
<tr><td>if S-bit = 0</td><td>if S-bit = 1 and
no shift/rotate</td><td>if S-bit = 1 and
shift/rotate is there</td></tr>
<tr><td>add, sub, rsb,
adc, sbc, rsc</td><td>No flags are affected</td><td colspan="2">All 4 flags are affected, ALU carry is used</td></tr>
<tr><td>cmp, cmn</td><td colspan="3">All 4 flags are affected, ALU carry is used</td></tr>
<tr><td>and, orr, xor, bic,
mov, mvn</td><td>No flags are affected</td><td>Only Z and N are
affected</td><td rowspan="2">C, Z and N are affected
shift/rotate carry is used</td></tr>
<tr><td>tst, teq</td><td colspan="2">Only Z and N are affected</td></tr>
</table>

4 Condition Checker

It checks the Cond and outputs the Predicate based on the values of Z flag.

4.1 Inputs

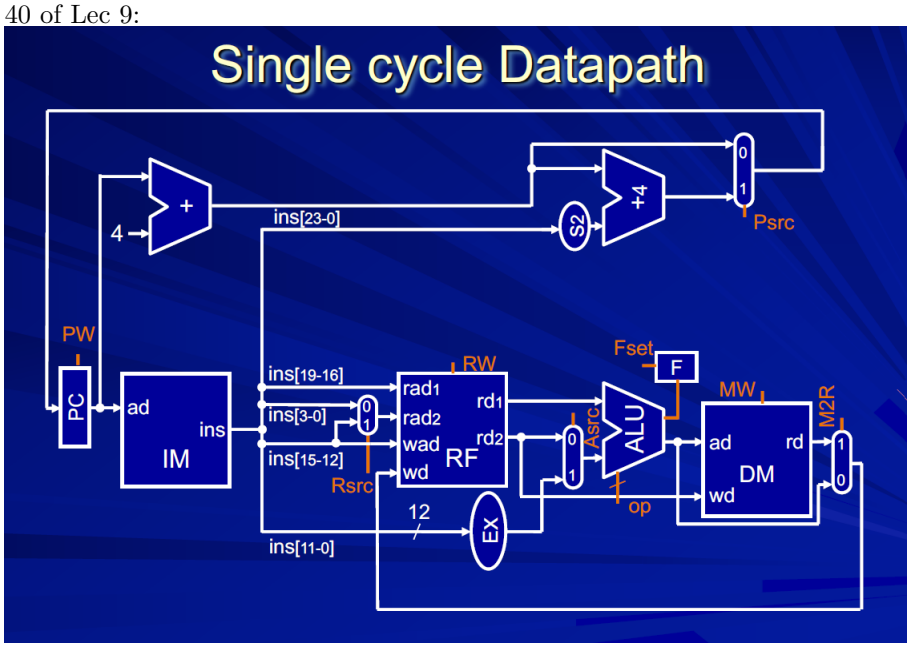
- Cond: 28th and 29th bits of the Instruction
- Z Flag

4.2 Outputs

- Predicate: Standard Logic which implies branch when 1 and not branch when 0.

5 Gluing Circuit

The fundamental Logic for the Gluing Circuit came from the Diagram in page 40 of Lec 9:



5.1 Inputs

- Clk: Standard Logic Synchronized Clock
- Reset: Standard Logic, Program counter goes to 0 when reset = 1

The individual components i.e. ALU, DataMemory, ProgramMemory, RegisterFiles, ProgramCounter, Flags and ConditionChecker are glued using the port maps of signals and "If" & "else" statements are used to imitate the multiplexers according to DP/DT/Branch instructions.
The period of the clock is 10 ns and hence a runtime of around 100 ns is expected to be inputted in the Playground.