EE 340: Communications Laboratory
Autumn 2015

# Lab 8: Clock Synchronization for Data Recovery in Communication Links using PLLs

# Legends

Question/Observation: Show it to the TA and explain (carries marks)


Recall/think about something

Caution

Additional information - weblink

# Aim of the experiment

To study clock synchronization for recovering data.

- To study understand the concept of clock synchronization in communication systems
- To get familiar with a phase detector (and the principle on which it is based) that can be used for clock recovery and timing synchronization in a serial communication link
- To understand the working of a PLL

# Component list

- *D Flip-Flops: 7474*
- *X-OR gates: 7486*
- *Inverters: 7404*
- *Mosfets: 4007*
- *VCO (part of a PLL IC): 4046*

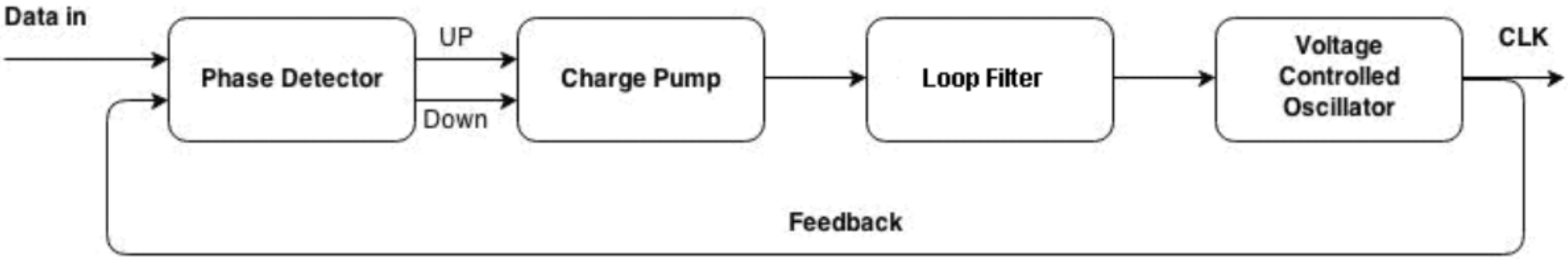



FIGURE 1. A PHASE LOCKED LOOP FOR CLOCK RECOVERY AND SYNCRONIZATON

# PART1: Design Hogge PD

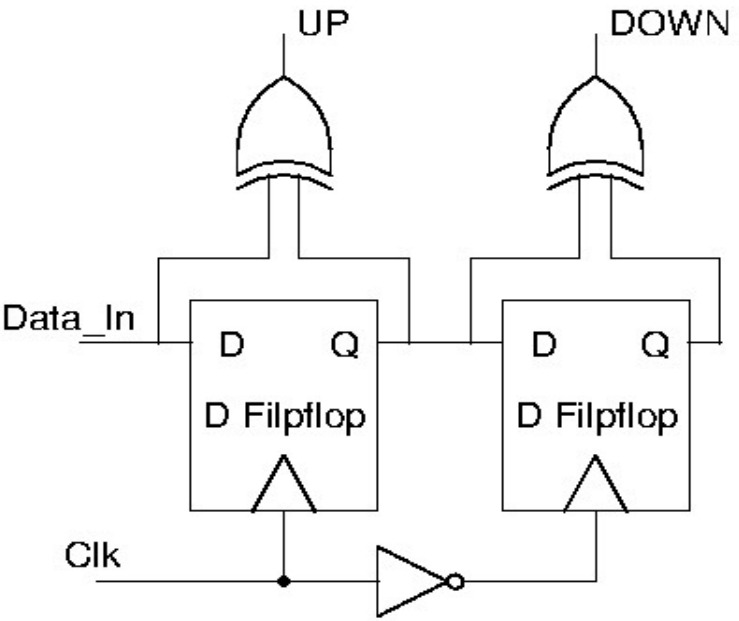
- Design the Hogge Phase detector with a 5V supply shown in adjacent fig.

⚠ Make sure that you are not leaving set/reset pins of the flip-flops floating (disable them by connecting the to VDD).

- Apply a 11kHz clock and 11kbps ’010101...’ data to the Phase detector input and observe that UP and DOWN pulses are as expected when you adjust the phase of the clock with respect to the data input.
- Make sure that you are keeping the outputs of the AFG in ”High impedance“ mode ⚠

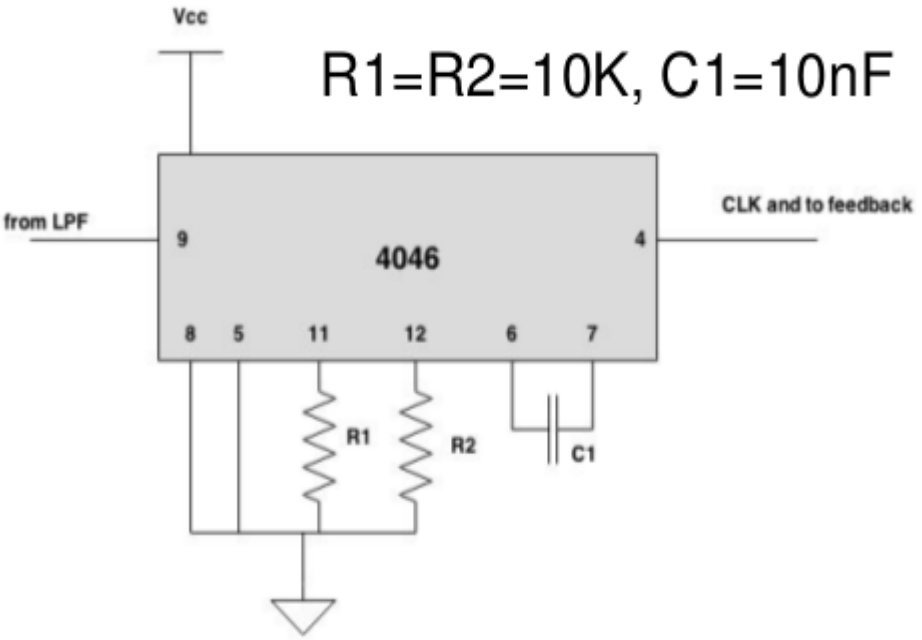
✓ Also observe the rising edges of the clock with respect to data periods -- it should be in the center of the data periods-- when the UP and DOWN pulses are equal in width.

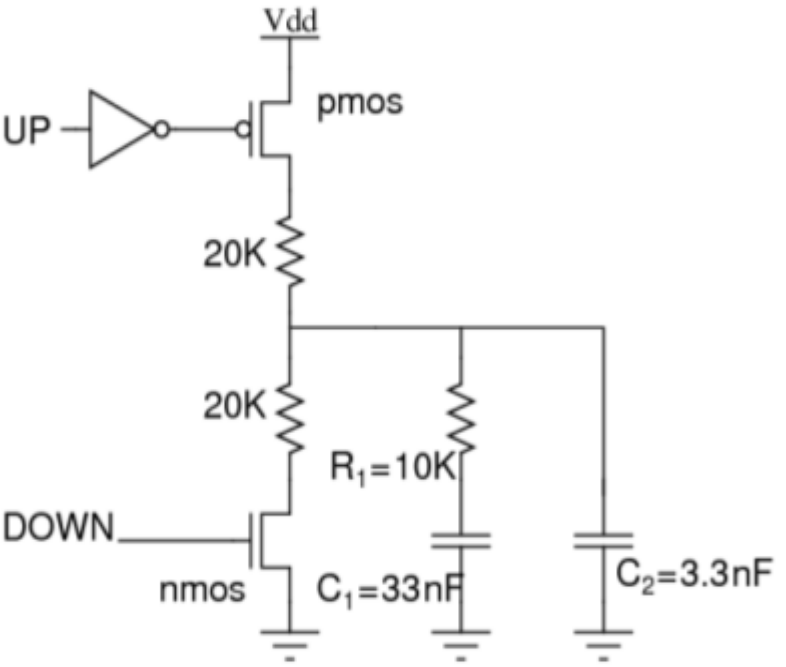
✓ Why does duty cycle of 'DOWN' pulse remains constant. Explain?



# PART2: VCO/CP Characterization

- Characterize your 4046 VCO by varying the control voltage and observing the frequency change.
- ✓ Find the center frequency (when control voltage is 2.5V) and the VCO gain in Hz/V and (rad/s)/V at around 2.5V control voltage.
- Make the Charge Pump and Loop Filter shown in the figure below.
- ✓ It is a very poor quality charge-pump (give the reason to your TA).



# PART3: PLL Characterization

- Connect all the blocks to complete the PLL
- Characterize the PLL for the ’1010101010..’ data in terms of its locking range and acquisition range


- ☑ Perform the same thing for the random bit sequence provided to you on your function generator.
- ☑ Show that clock rising edges are at the center of random data periods (when the loop filter voltage is about 2.5V).
- ☑ Why it is not always in the center (i.e. when loop filter voltage is not around 2.5V)?

# PART4: Summary of Lab

- Follow the subsequent steps for the following two cases:
  - Deterministic data ’101010101010’ data and
  - Random data (transition density=50%).`

| | $K_{PD}$ | $I_{CP}$ | $Z_{LF}$ | $K_{VCO}$ | Open Loop Gain |
|---|---|---|---|---|---|
| Random | | | | | |
| Deterministic Data | | | | | |

- Use the utility on weblink for bode plot and find gain and phase margin.