Core Instruction Formats

31 27	26 25	24 20	19 15	14 12	11 7	6 0	
funct7		rs2	rs1	funct3	rd	opcode	R-type
imm[11:0]			rs1	funct3	rd	opcode	I-type
imm[11:5]		rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12|10:5]		rs2	rs1	funct3	imm[4:1|11]	opcode	B-type

INSTRUCTION DECODE SHEET

Instruction	Opcode(Op)	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUOp
lw	0000011	1	00	1	0	1	0	00
sw	0100011	0	01	1	1	x	0	00
R-type	0110011	1	xx	0	0	0	0	10
B-type	1100011	0	10	0	0	x	1	01
I-type	0010011	1	00	1	0	0	0	11

ALUOp	Meaning
00	add
11	subtract
10	Look at funct3 fields and $\{opcode_5, funct7_5\}$ 5th bit
11	Look funct3 field

ALUOp	funct3	{Op_5,$funct7_5$}	ALUControl	Instruction
00	x	x	000	lw,sw
01	000	x	100	beq
	001	x	101	bne
	100	x	110	blt
	101	x	111	bgt
10	000	00,01,10	000	add
	000	11	001	sub
	110	x	011	or
	111	x	010	and
11	000	x	000	add
	110	x	011	or
	111	x	010	and

ALUControl	Instruction
000	add
001	sub
010	and
011	or
100	==
101	!=
110	<
111	>