

CMOS Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)

With Decoded 7-Segment Display Outputs and:

Display Enable – CD4026B

Ripple Blanking – CD4033B

■ CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven

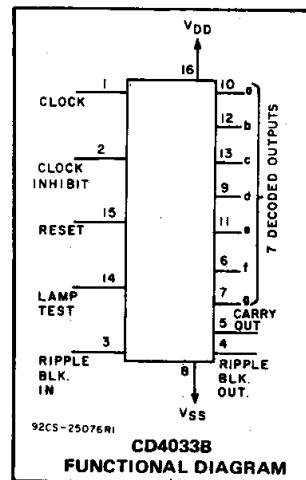
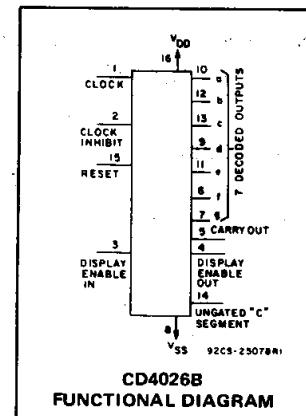
Features:

- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 6 MHz (typ.) at $V_{DD}=10$ V
- Ideal for low-power displays
- Display enable output (CD4026B)
- "Ripple blanking" and lamp test (CD4033B)
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Schmitt-triggered clock inputs
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

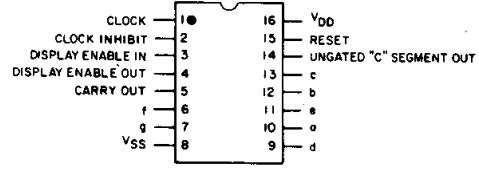
- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers (e.g. $\div 60$, $\div 60$, $\div 12$ counter/display)
- Counter/display driver for meter applications

segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

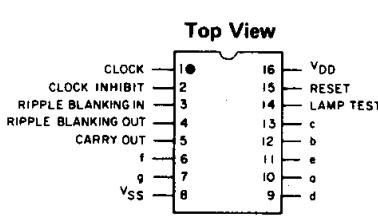


TERMINAL DIAGRAMS

Top View



Top View



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$, Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max +265 $^\circ\text{C}$

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max +265 $^\circ\text{C}$

CD4026B, CD4033B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS	
		MIN.	MAX.		
Supply-Voltage Range (For T _A = Full Package Temperature Range)		3	18	V	
Clock Input Frequency, f _{CL}	5	—	2.5	MHz	
	10	—	5.5		
	15	—	8		
Clock Pulse Width, t _{WCL}	5	220	—	ns	
	10	100	—		
	15	80	—		
Clock Rise and Fall Time, t _{CL} -t _{fCL}	5	—	Unlimited		
	10	—			
	15	—			
Clock Inhibit Set Up Time, t _{SU}	5	200	—		
	10	50	—		
	15	30	—		
Reset Pulse Width, t _R	5	200	—		
	10	100	—		
	15	50	—		
Reset Removal Time	5	30	—		
	10	15	—		
	15	10	—		

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25								
				-55	-40	+85	+125	Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA	
	—	0,10	10	10	10	300	300	—	0.04	10		
	—	0,15	15	20	20	600	600	—	0.04	20		
	—	0,20	20	100	100	3000	3000	—	0.08	100		
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA	
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—		
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—		
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA	
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—		
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—		
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05				—	0	0,05	V	
	—	0,10	10	0,05				—	0	0,05		
	—	0,15	15	0,05				—	0	0,05		
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95				4,95	5	—	V	
	—	0,10	10	9,95				9,95	10	—		
	—	0,15	15	14,95				14,95	15	—		
Input Low Voltage, V _{IL} Max.	0,5, 4,5	—	5	1,5				—	—	1,5	V	
	1,9	—	10	3				—	—	3		
	1,5, 13,5	—	15	4				—	—	4		
Input High Voltage, V _{IH} Min.	0,5, 4,5	—	5	3,5				3,5	—	—	V	
	1,9	—	10	7				7	—	—		
	1,5, 13,5	—	15	11				11	—	—		
Input Current I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA	

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

CD4026B, CD4033B Types

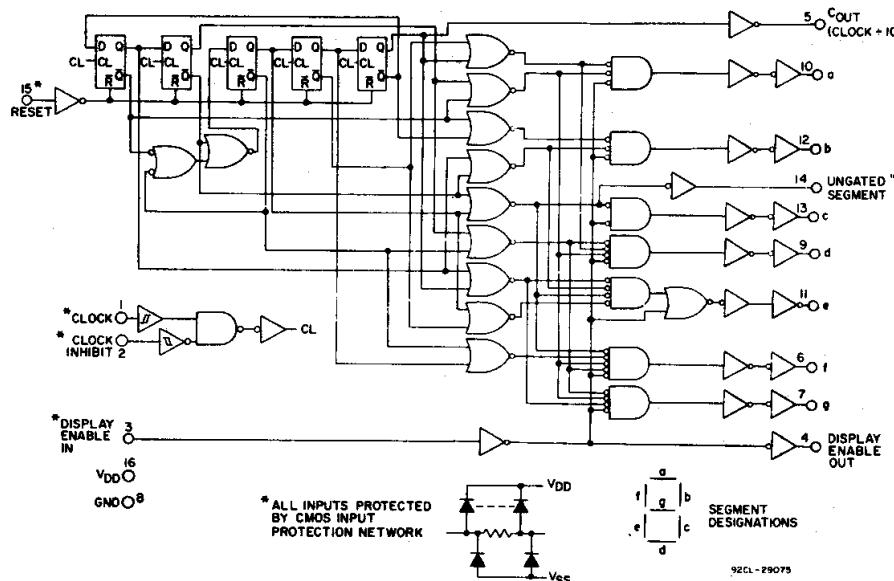


Fig. 1 – CD4026B logic diagram.

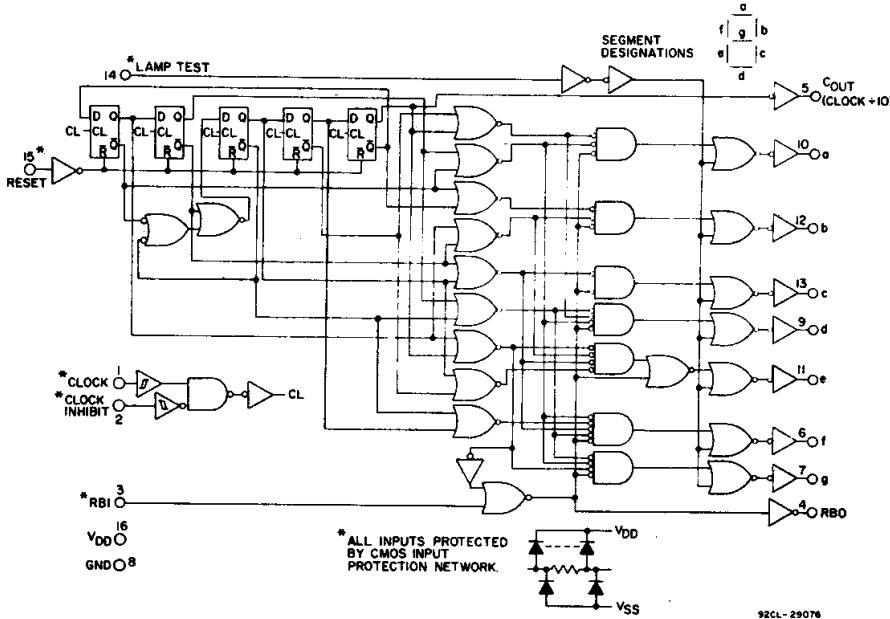


Fig. 2 – CD4033B logic diagram.

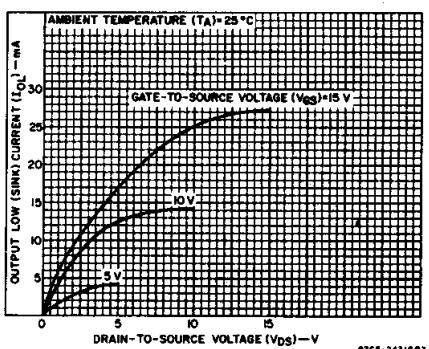


Fig. 6 – Typical n-channel output low (sink) current characteristics.

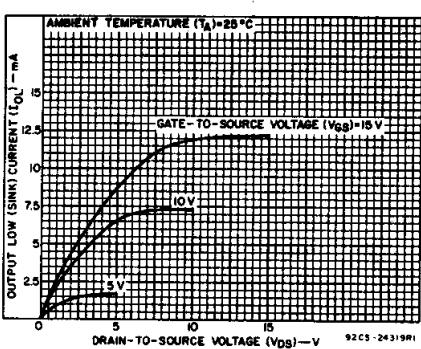


Fig. 7 – Minimum n-channel output low (sink) current characteristics.

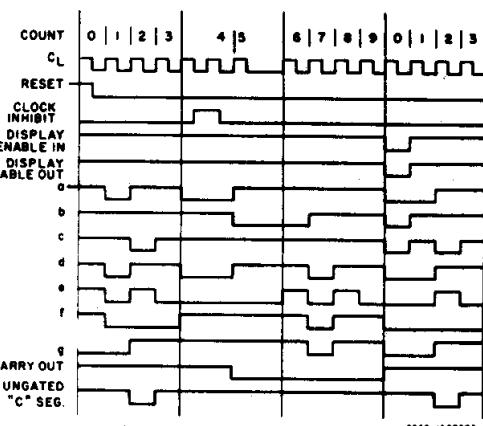


Fig. 3 – CD4026B timing diagram.

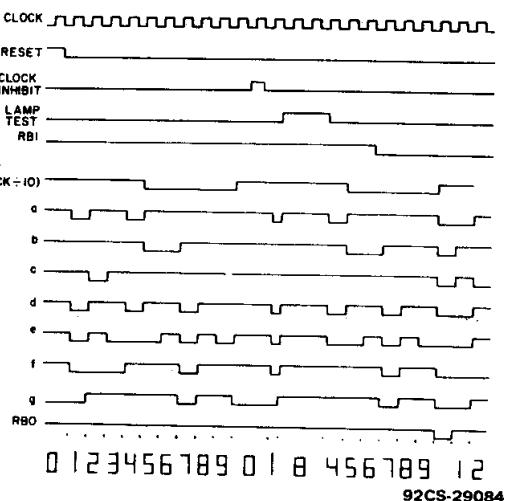


Fig. 4 – CD4033B timing diagram.

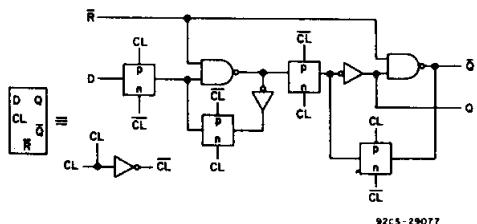


Fig. 5 – Detail of typical flip-flop stage for both types.

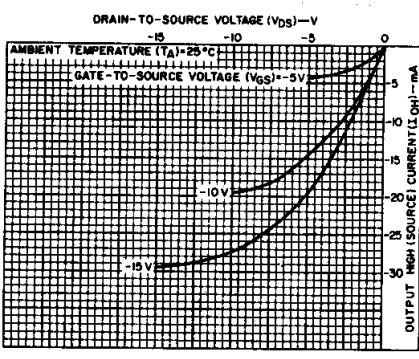


Fig. 8 – Typical p-channel output high (source) current characteristics.

CD4026B, CD4033B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}, R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS $V_{DD} (\text{V})$	LIMITS			UNITS
		Min.	Typ.	Max.	
CLOCKED OPERATION					
Propagation Delay Time; t_{PLH}, t_{PHL} Carry-Out Line	5	—	250	500	ns
	10	—	100	200	
	15	—	75	150	
Decode Outlines	5	—	350	700	
	10	—	125	250	
	15	—	90	180	
Transition Time; t_{THL}, t_{TLH} Carry-Out Line	5	—	100	200	
	10	—	50	100	
	15	—	25	50	
Maximum Clock Input Frequency, f_{CL}^Δ	5	2.5	5	—	MHz
	10	5.5	11	—	
	15	8	16	—	
Min. Clock Pulse Width, t_W	5	—	110	220	
	10	—	50	100	
	15	—	40	80	
Clock and Clock Inhibit Rise or Fall Time; t_{rCL}, t_{fCL}	5	—	Unlimited		ns
	10	—			
	15	—			
Average Input Capacitance, C_{IN}	Any Input	—	5	7	pF
RESET OPERATION					
Propagation Delay Time; To Carry-Out Line, t_{PLH}	5	—	275	550	
	10	—	120	240	
	15	—	80	160	
To Decode Out Lines, t_{PHL}, t_{PLH}	5	—	300	600	
	10	—	125	250	
	15	—	90	180	
Min. Reset Pulse Width, t_W	5	—	100	120	
	10	—	50	100	
	15	—	25	50	
Min. Reset Removal Time	5	—	0	30	
	10	—	0	15	
	15	—	0	10	

^Δ Measured with respect to carry-out line.

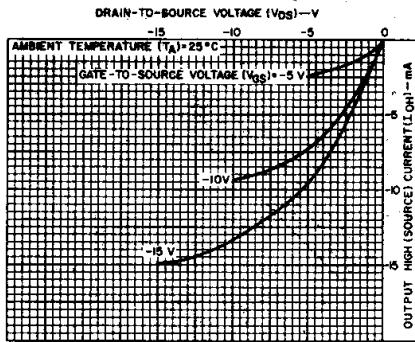


Fig. 9 – Minimum p-channel output high (source) current characteristics.

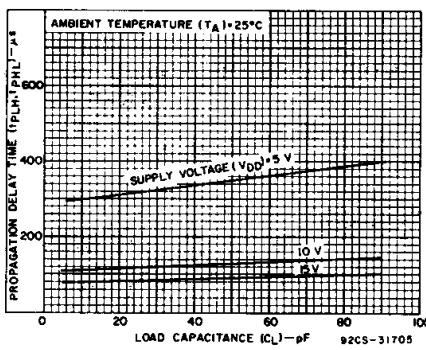


Fig. 10 – Typical propagation delay time as a function of load capacitance for decoded outputs.

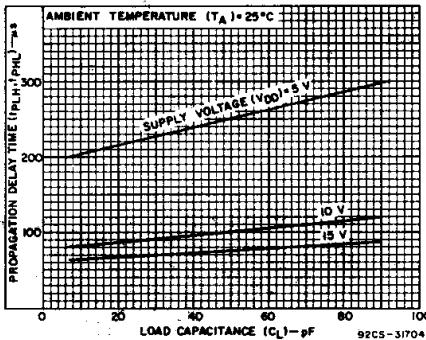


Fig. 11 – Typical propagation delay time as a function of load capacitance for carry-out outputs.

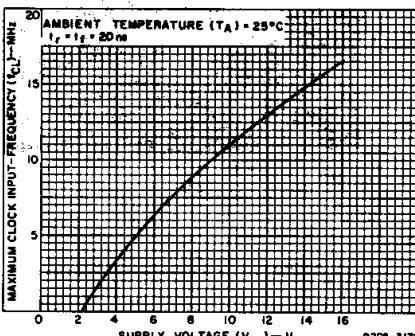


Fig. 12 – Typical maximum clock input-frequency as a function of supply voltage.

CD4026B, CD4033B Types

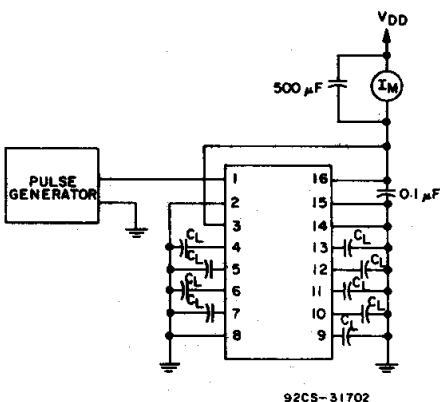
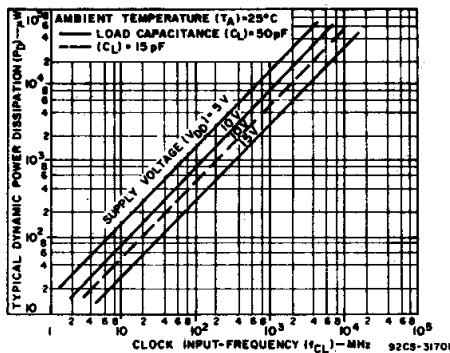


Fig. 14 – Dynamic power dissipation test circuit for CD4033B.

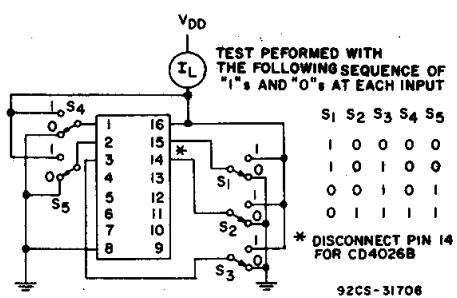


Fig. 15 – Quiescent device current.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS

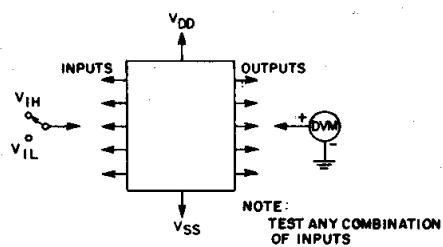
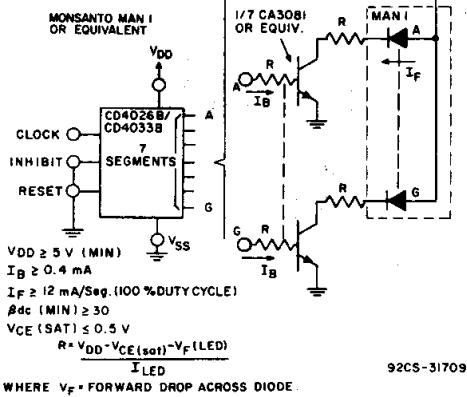
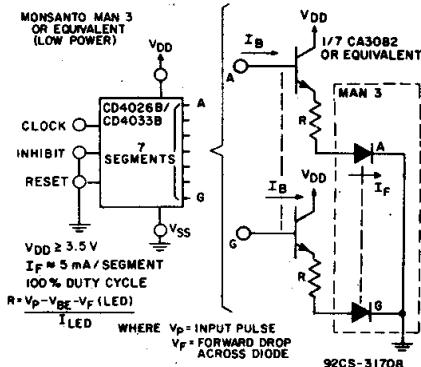


Fig. 16 – Input voltage.

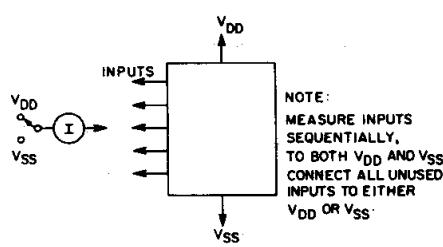
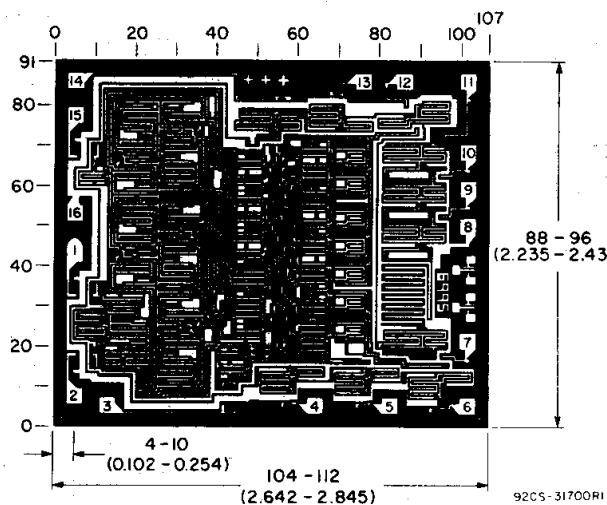
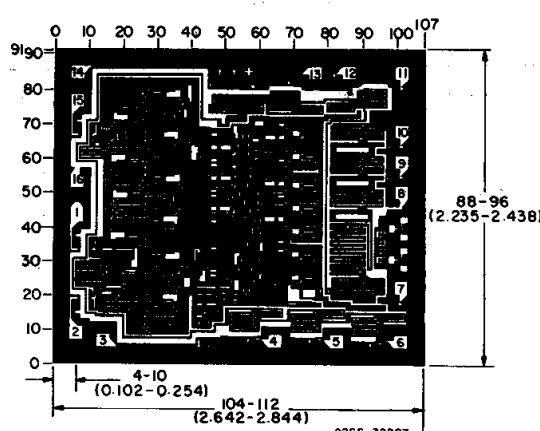


Fig. 17 – Input current.

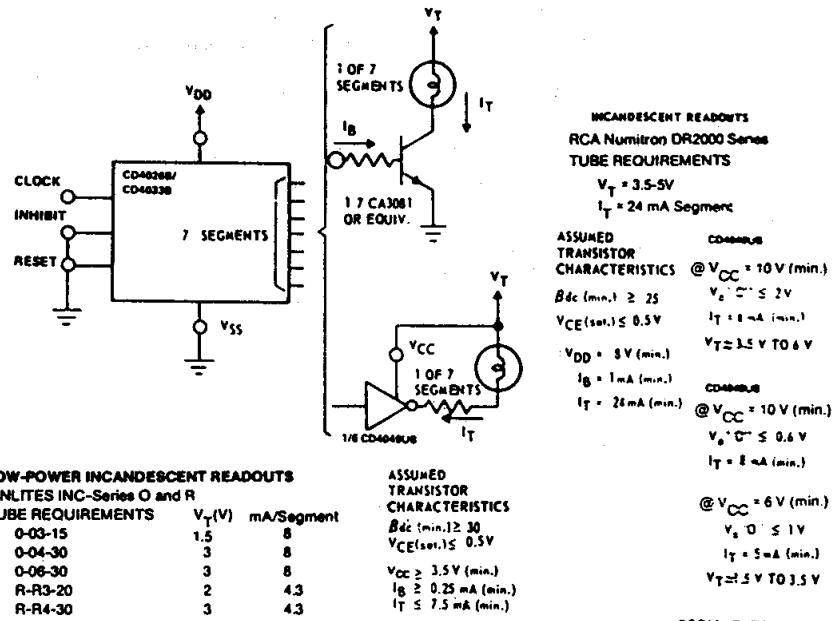


Chip dimensions and pad layout for CD4026B

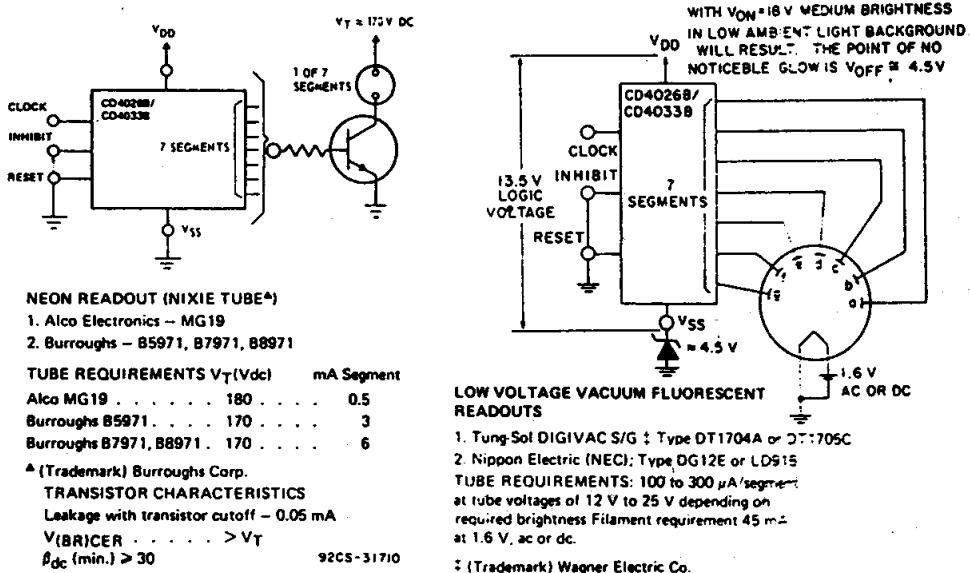
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Chip dimensions and pad layout for CD4033B

CD4026B, CD4033B Types**INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES***

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4026BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4026BE
CD4026BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4026BE
CD4026BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4026BE
CD4026BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4026B
CD4026BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4026B
CD4026BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM026B
CD4026BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM026B
CD4026BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM026B
CD4033BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4033BE
CD4033BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4033BE
CD4033BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM033B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

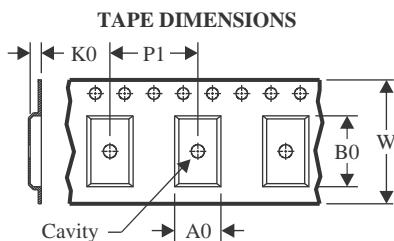
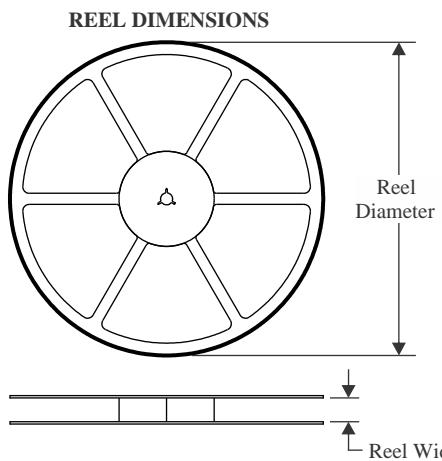
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

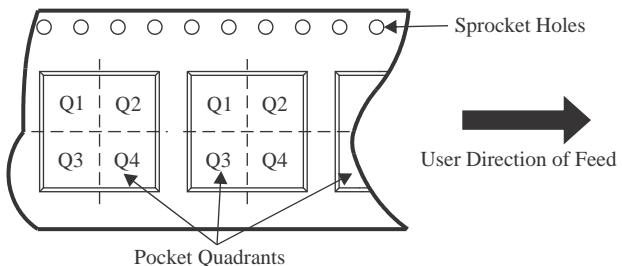
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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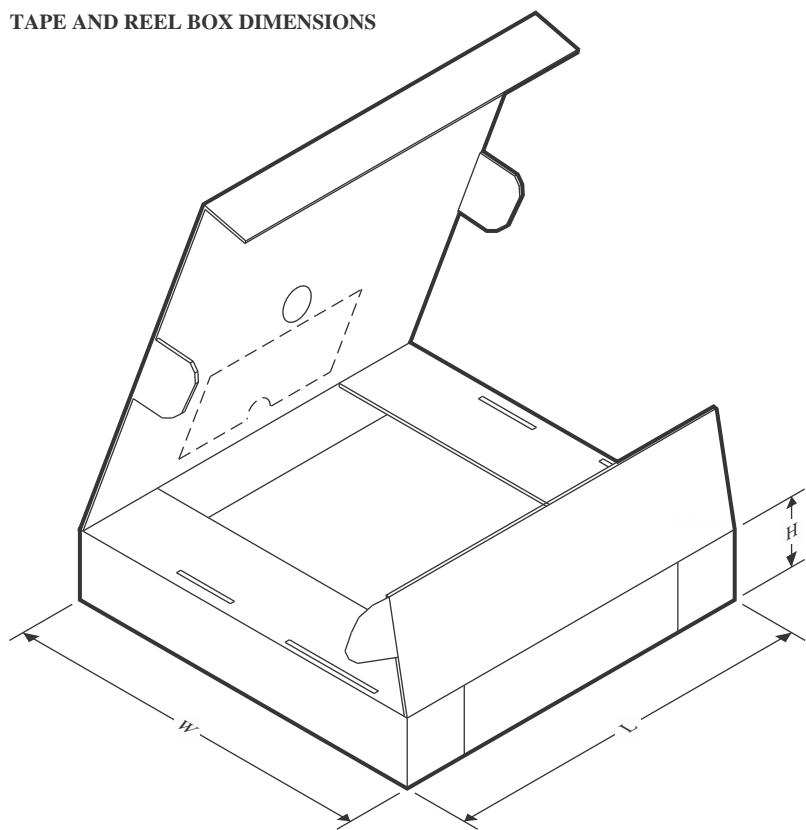
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


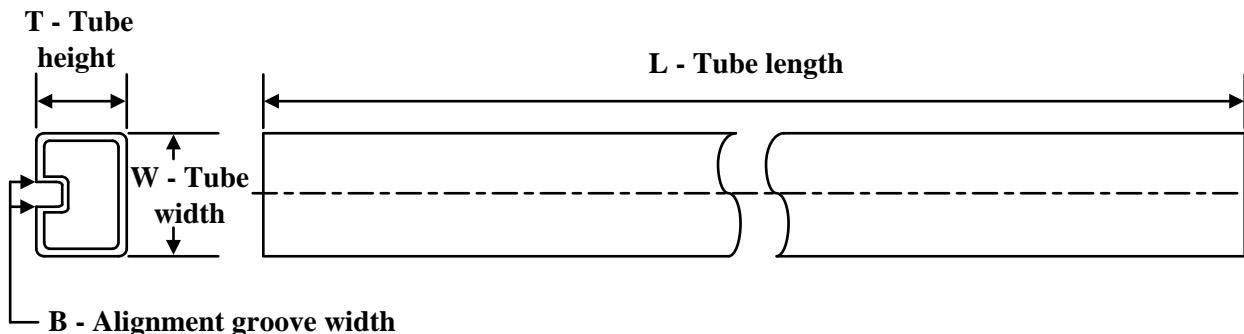
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4026BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4026BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4026BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4026BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD4026BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4026BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4026BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4026BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4026BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4026BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4033BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4033BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4033BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4033BE.A	N	PDIP	16	25	506	13.97	11230	4.32

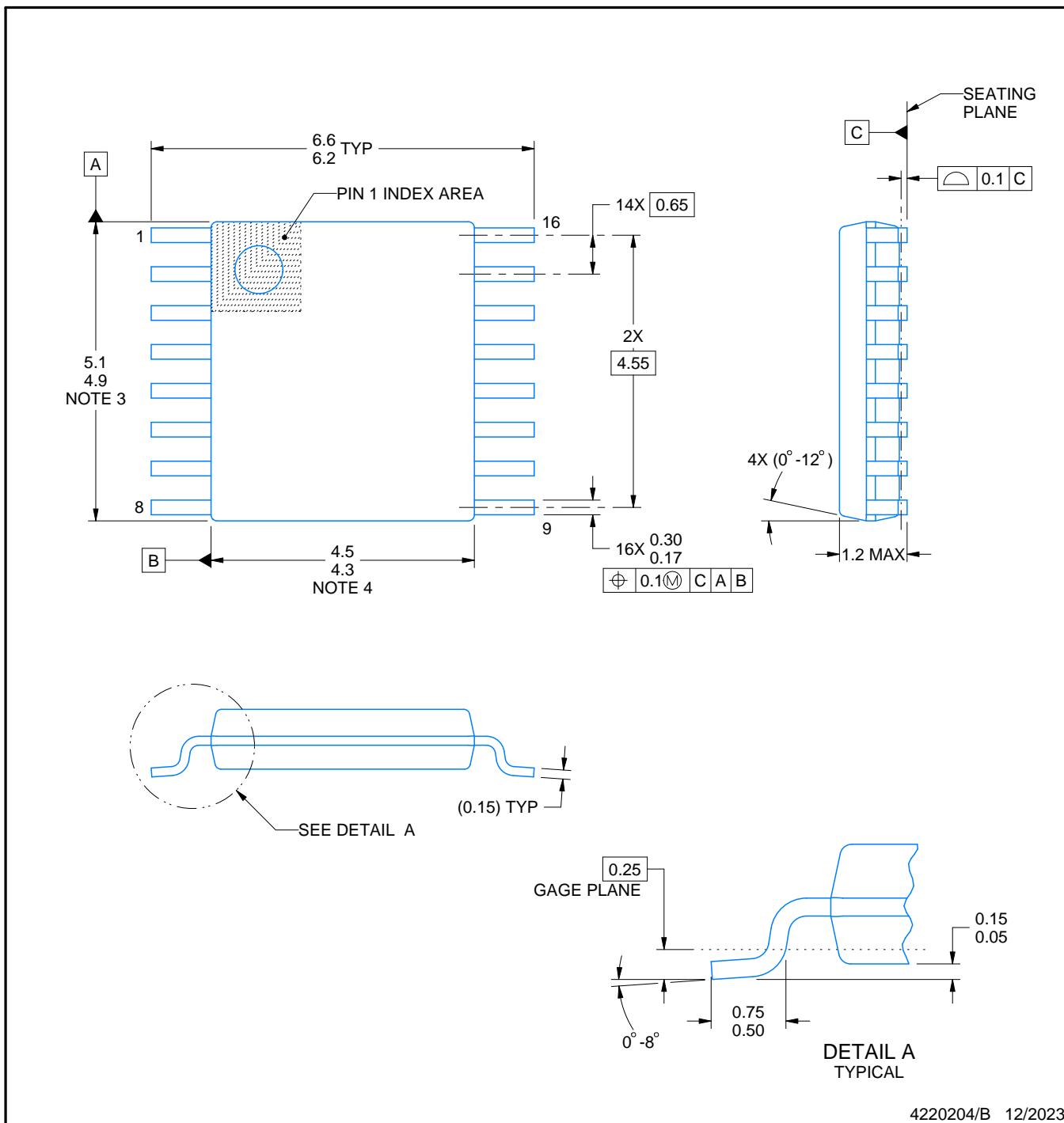
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

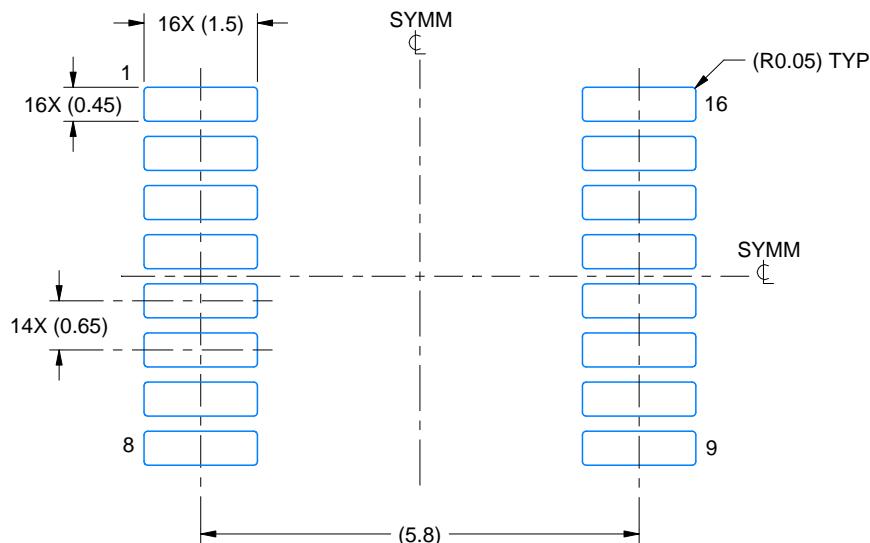
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

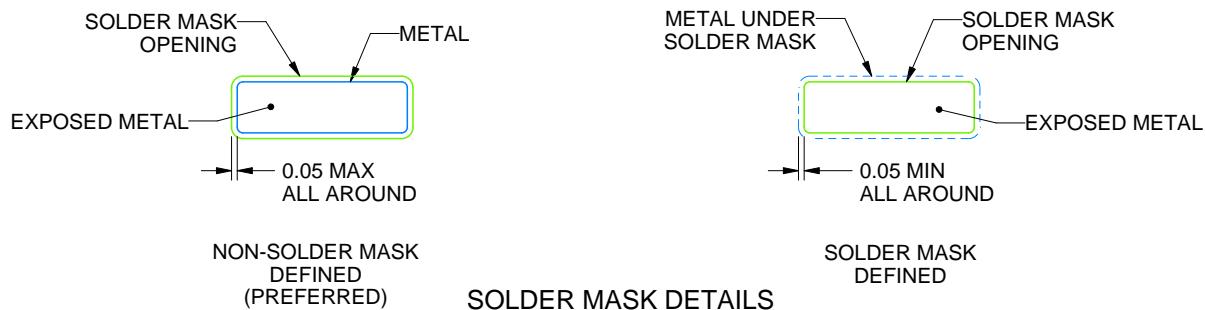
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

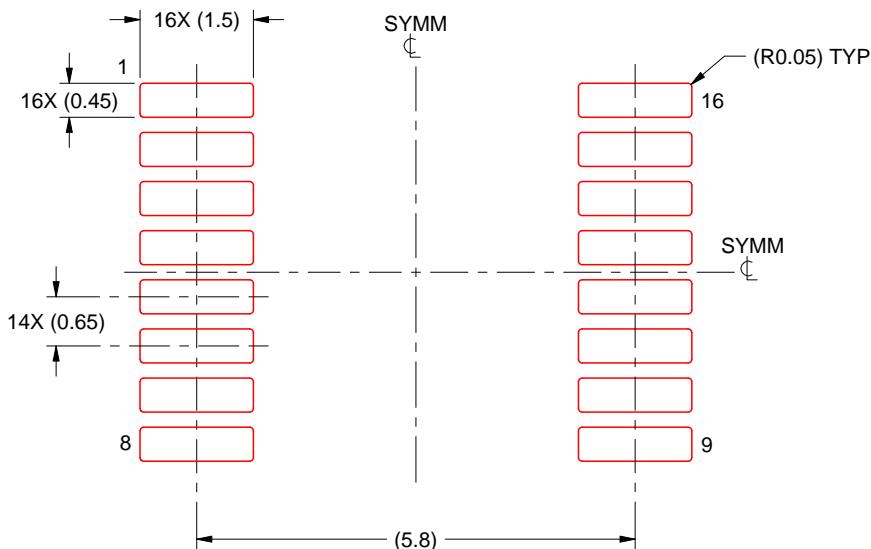
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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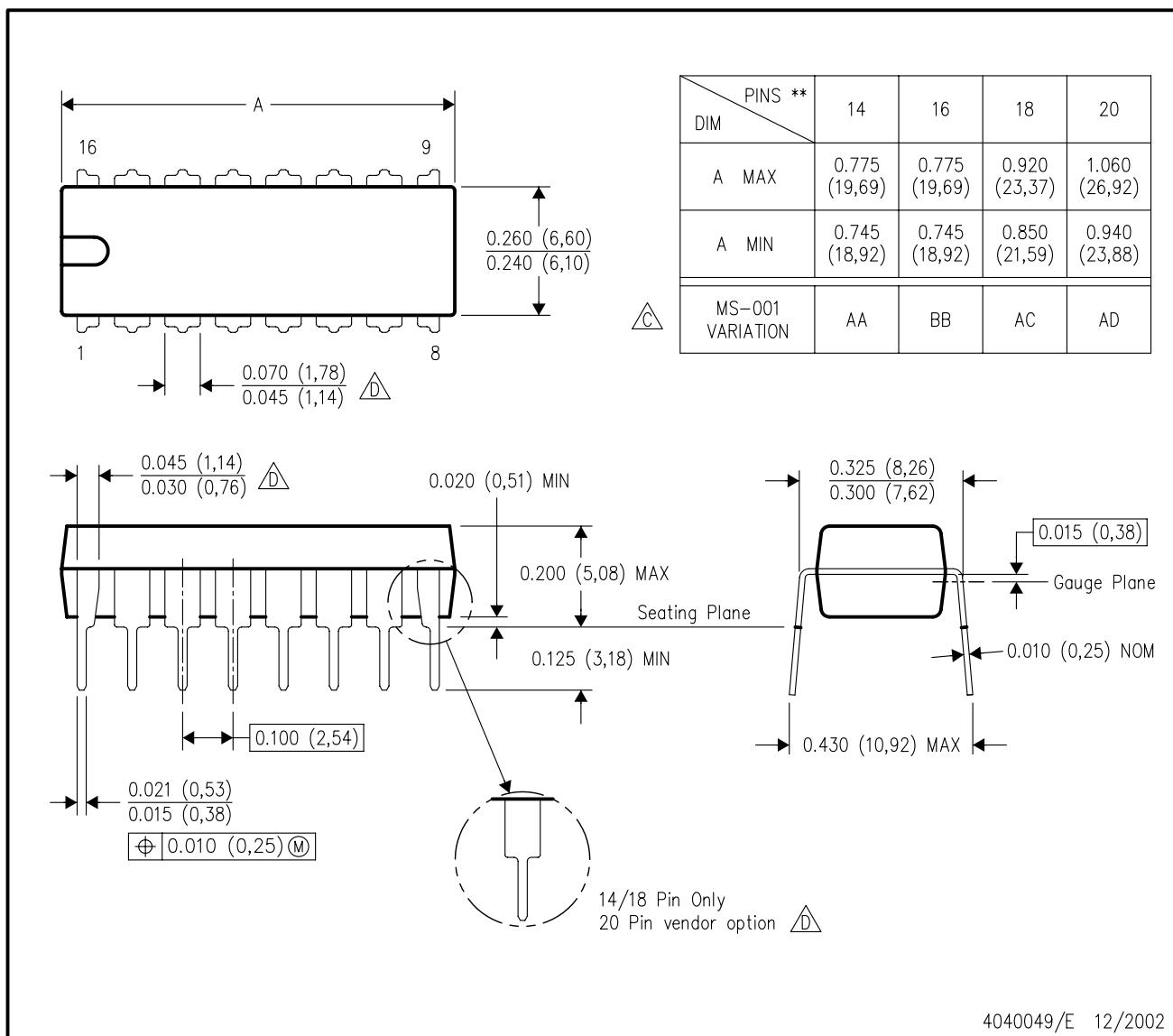
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

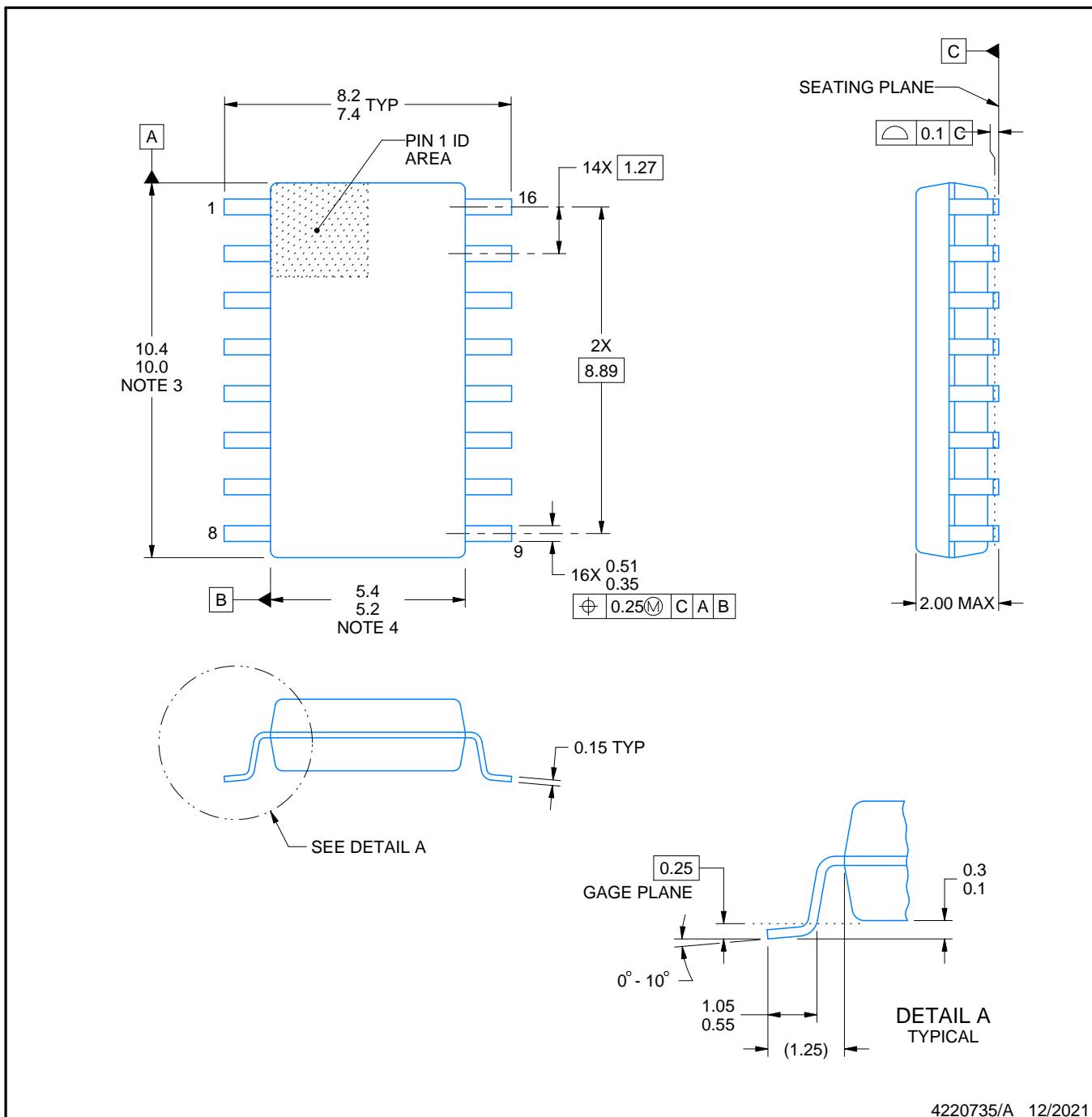
NS0016A



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



NOTES:

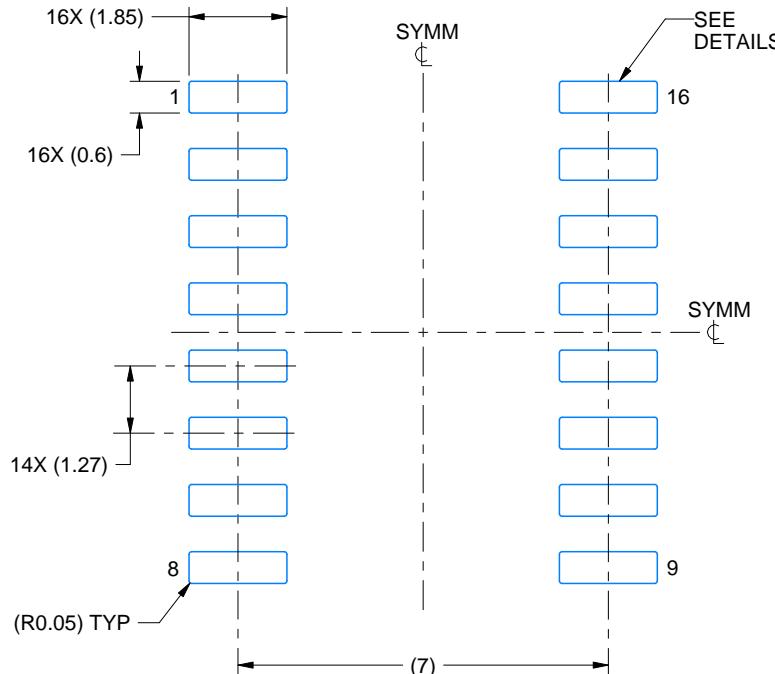
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

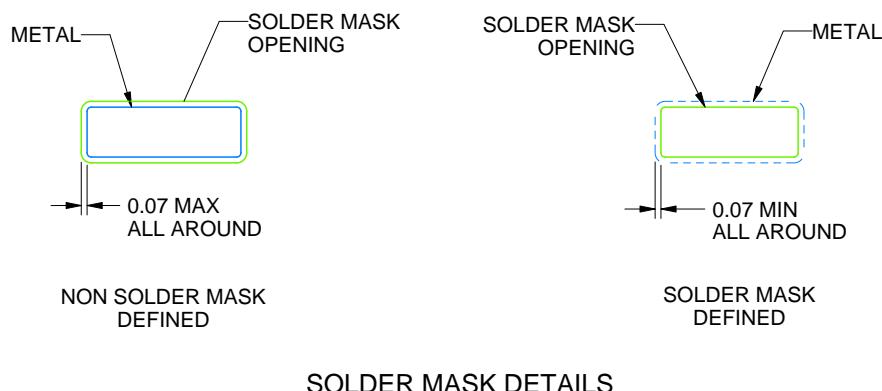
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

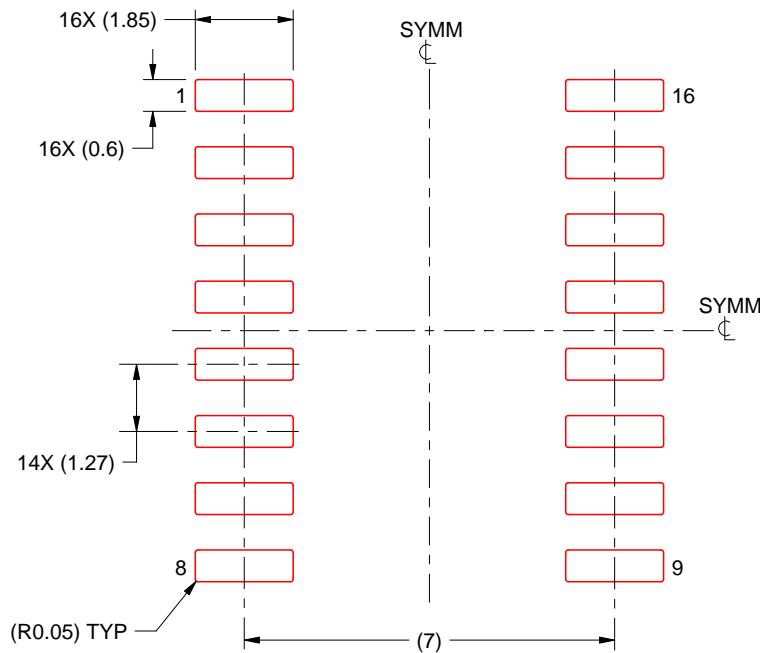
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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