

TASK-4

INTRODUCTION

Objective:

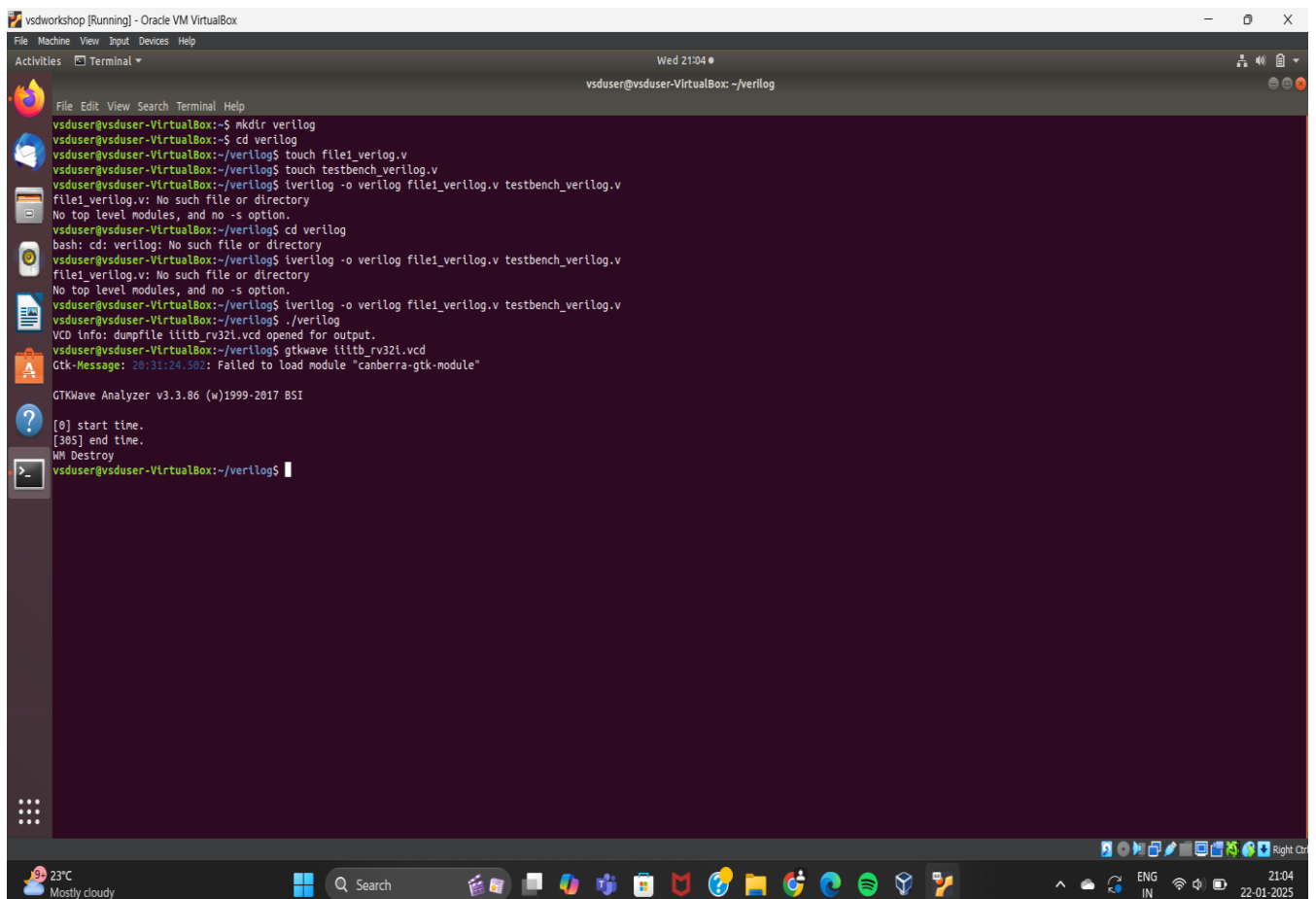
To perform a functional simulation of a RISC-V Core using the provided Verilog netlist and testbench.

Steps to Complete the Task:

1.create a directory:

By using `mkdir file_name` create a file.

Then by using `touch netlist_file.v` command create a verilog file to download the given verilog netlist. Similarly create a testbench file to download the test bench code.



```
vdsuser@vdsuser-VirtualBox:~$ mkdir verilog
vdsuser@vdsuser-VirtualBox:~$ cd verilog
vdsuser@vdsuser-VirtualBox:~/verilog$ touch file1_verilog.v
vdsuser@vdsuser-VirtualBox:~/verilog$ touch testbench_verilog.v
vdsuser@vdsuser-VirtualBox:~/verilog$ iverilog -o verilog file1_verilog.v testbench_verilog.v
file1_verilog.v: No such file or directory
No top level modules, and no -s option.
vdsuser@vdsuser-VirtualBox:~/verilog$ cd verilog
bash: cd: verilog: No such file or directory
vdsuser@vdsuser-VirtualBox:~/verilog$ iverilog -o verilog file1_verilog.v testbench_verilog.v
file1_verilog.v: No such file or directory
No top level modules, and no -s option.
vdsuser@vdsuser-VirtualBox:~/verilog$ iverilog -o verilog file1_verilog.v testbench_verilog.v
vdsuser@vdsuser-VirtualBox:~/verilog$ ./verilog
VCD info: dumpfile iitb_rv32i.vcd opened for output.
vdsuser@vdsuser-VirtualBox:~/verilog$ gtkwave iitb_rv32i.vcd
Gtk-Messsage: 20:31:24.502: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.86 (w)1999-2017 BSI

[0] start time.
[305] end time.
WM Destroy
vdsuser@vdsuser-VirtualBox:~/verilog$
```

2.Download Files:

Obtain the Verilog netlist from the given resource (RISC-V Core Verilog Netlist).

Download the testbench from the specified resource (Testbench for RISC-V Core).

3.Set Up Simulation Environment:

Ensure you have a simulation tool installed, such as iverilog (for simulation) and gtkwave (for waveform visualization).

Load the Verilog netlist and testbench into the chosen simulation tool.

```
vsduser@vsduser-VirtualBox:~$ sudo apt install iverilog gtkwave
Reading package lists... Done
Building dependency tree
Reading state information... Done
gtkwave is already the newest version (3.3.86-1).
iverilog is already the newest version (10.1-0.1build1).
0 upgraded, 0 newly installed, 0 to remove and 78 not upgraded.
vsduser@vsduser-VirtualBox:~$ gtkwave --version
Gtk-Message: 23:17:45.982: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.86 (w)1999-2017 BSI

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warranty; not even for MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE.
vsduser@vsduser-VirtualBox:~$ iverilog -v
Icarus Verilog version 10.3 (stable) (v10_3-42-gb98854309-dirty)

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with this program; if not, write to the Free Software Foundation, Inc.,
51 Franklin Street, Fifth Floor, Boston, MA 02110-1301, USA.

iverilog: no source files.

Usage: iverilog [-ESvV] [-B base] [-c cmdfile|-f cmdfile]
             [-g1995|-g2001|-g2005|-g2005-sv|-g2009|-g2012] [-g<feature>]
             [-D macro[=defn]] [-I includedir]
             [-M [mode=]depfile] [-m module]
             [-N file] [-o filename] [-p flag=value]
             [-s topmodule] [-t target] [-T min|typ|max]
             [-W class] [-y dir] [-Y suf] [-l file] source_file(s)

See the man page for details.
vsduser@vsduser-VirtualBox:~$
```



4.Run Functional Simulation:

Simulate the RISC-V Core using the testbench.

Observe and verify the core's output signals for functional correctness.

5.Capture Waveforms:

Generate waveform files for the simulated design (e.g., .vcd files).

Use tools like gtkwave to capture and save waveform snapshots corresponding to the executed instructions or signals.

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