SENSORS AND AUTOMATION

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SY Comp Div-2, S5 Batch

Practical-8: Timer and Counter

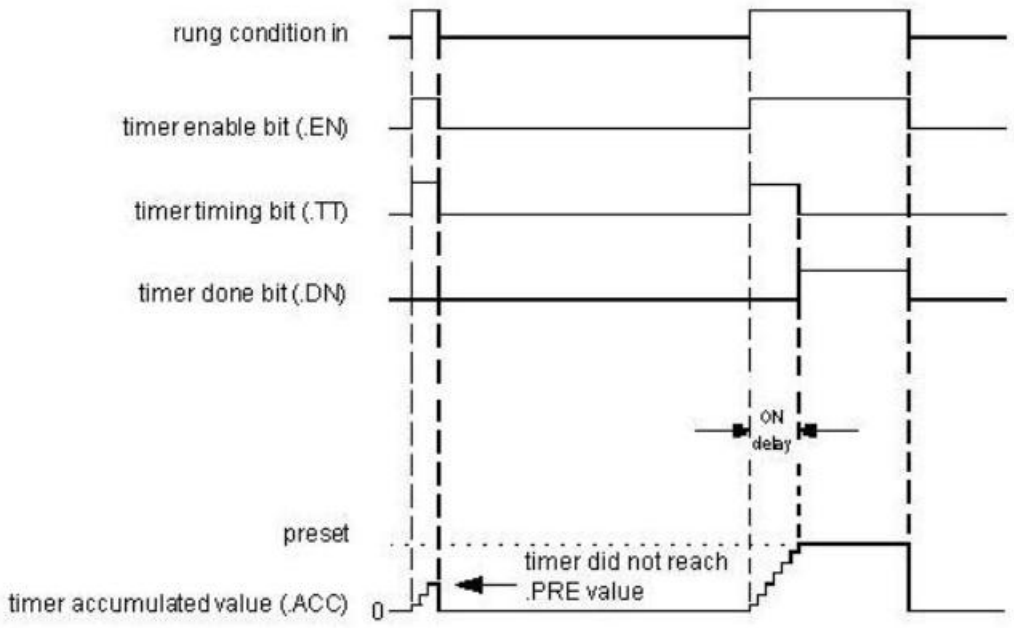
Aim:

1. Study the timing diagram of On Delay Timer
2. Study the timing diagram of OFF Delay Timer
3. Study Counter timing diagram

Theory:

On-Delay Timer (TON) It is used when an action is to begin a specified time after the input becomes true. Consider an example wherein a certain step in the manufacturing process is to begin 30 seconds after a signal is received from a limit switch. The 30 seconds delay is the ON-delay timer's preset value. The figure below shows a symbolic representation of the timer.

The instruction mainly includes three status bits namely EN, TT, DN. Their significance is as follows: Enable (EN) Bit: - The enable bit indicates the TON instruction is enabled Timer-Timing (TT) Bit: - The timing bit indicates that a timing operation is in process. Done (DN) Bit: - The done bit changes state whenever the accumulated value reaches the preset value. Accumulator (ACC) Bit: - The accumulated value specifies the number of milliseconds that have elapsed since the TON instruction was enabled. Preset (PRE) Bit: - The preset value specifies the value (1msec units) which the accumulated value must reach before the instruction sets the .DN bit. The figure shows the timing diagram which illustrates the functioning of all the bits in sequence.



OFF-Delay Timer: Consider an example where the contents of a storage tank are to transfer to further process. When the low level is detected by level switch the outlet valve is to be closed. To allow entire contents to drain out, some time delay is needed as the level switch is installed slightly above the tank bottom level. This can be achieved by using off delay timer. Consider an example that, there is a Low level switch to a tank, and we have to close the drain valve of the tank after 5 second delay when low level is reached. In this case this 5 seconds delay can be given using off delay timer as we have to close the drain valve after delay. The figure below shows a symbolic representation of the off delay timer.

The instruction mainly includes three status bits namely EN, TT, DN. Their significance is as follows:

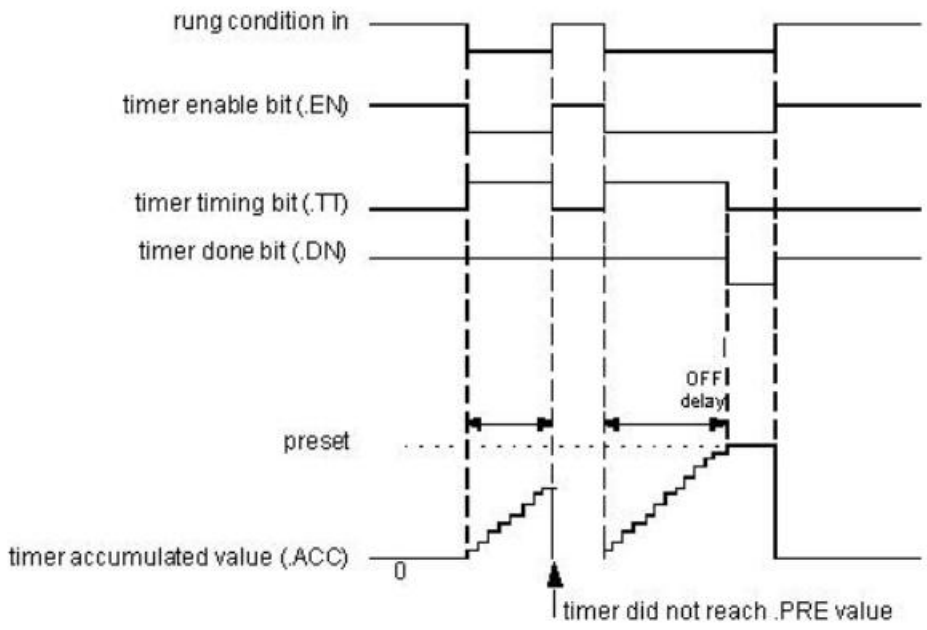
EN-Enable Bit: - The enable bit indicates the TOF instruction is enabled.
TT-Timer-Timing Bit: - The timing bit indicates the timing operation is in process.
DN- Done Bit: - The done bit changes state whenever the accumulated value reaches the preset value.

ACC- Accumulator Bit: - The accumulated value specifies the number of milliseconds that have elapsed since the TOF instruction was enabled.

Pre-Preset Bit: - The preset value specifies the value (1msec units) which the accumulated value must reach before the instruction clears the DN bit.

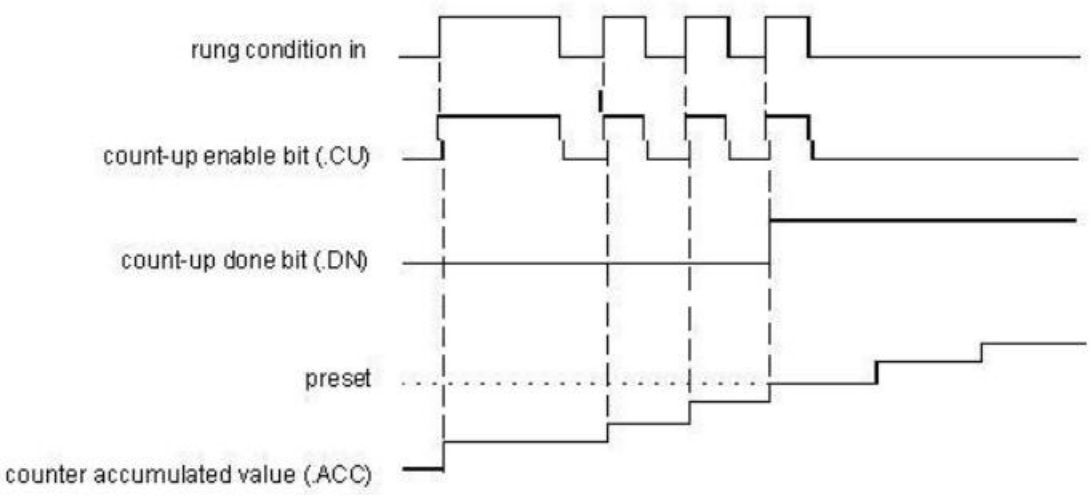
The figure shows the timing diagram which illustrates the functioning of all the bits in sequence.

The timing diagram illustrates the functioning of all the bits in sequence.

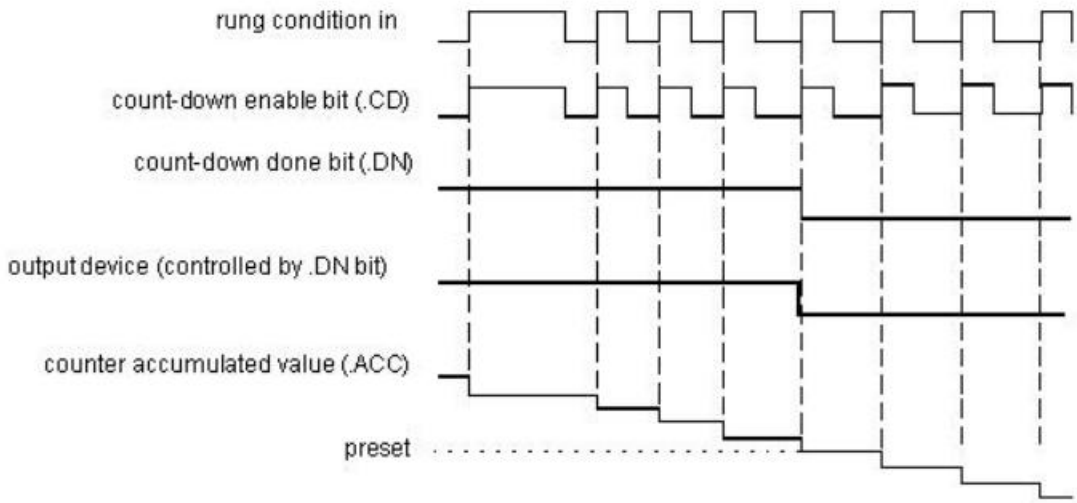


Counters are used to count number of objects or to count cycles of a typical process. Consider an example of bottle filling plant, in that counter is used to count number of bottles filled in a particular batch. In counter instruction the accumulated value will increase only when it completes the transition from open to close or vice versa. It doesn't check how long contact stay closed, it only looks for the transition. There are two basic types of counter

1. Up-Counter (CTU)
2. Down-Counter (CTD)



Timing Diagram for Up Counter

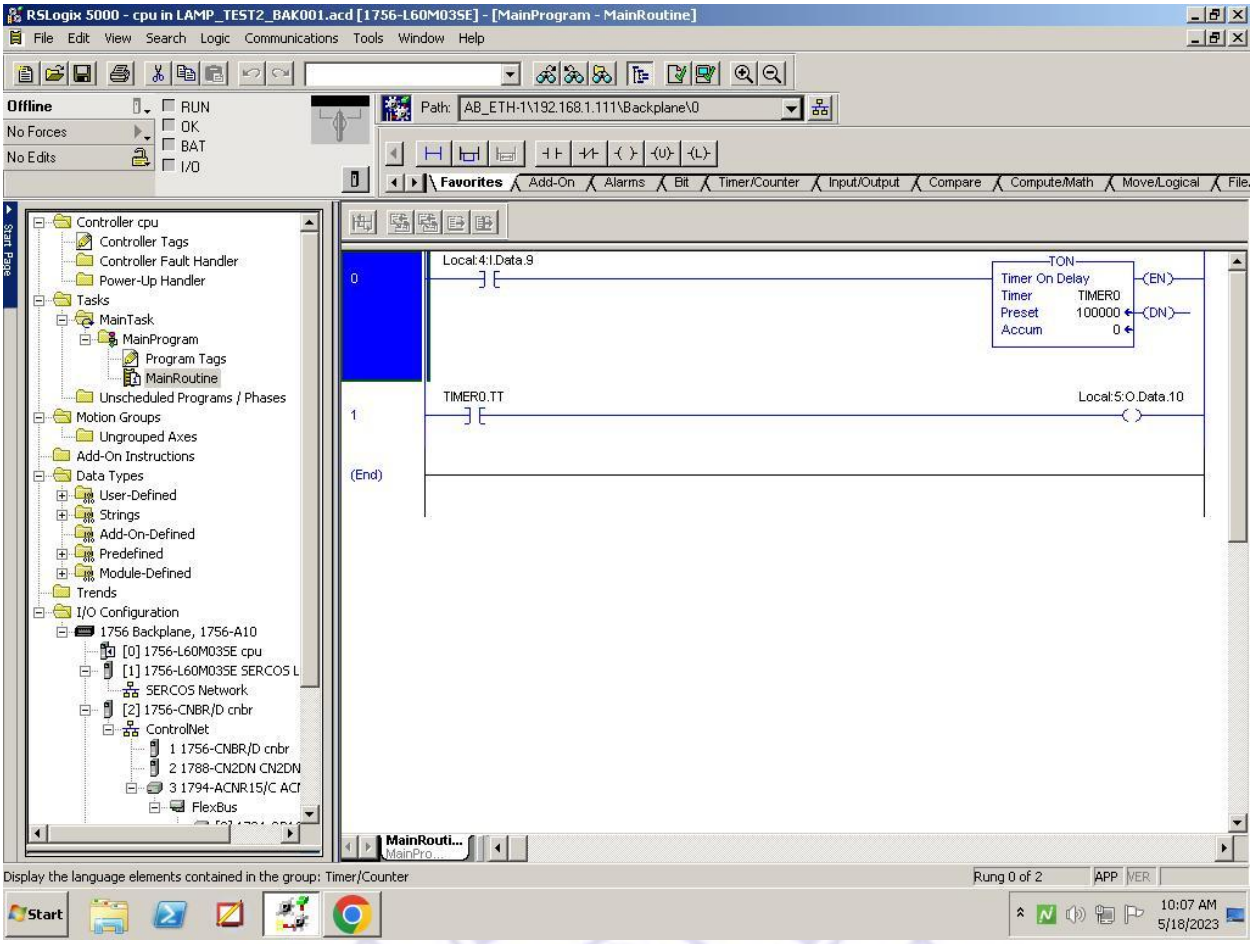


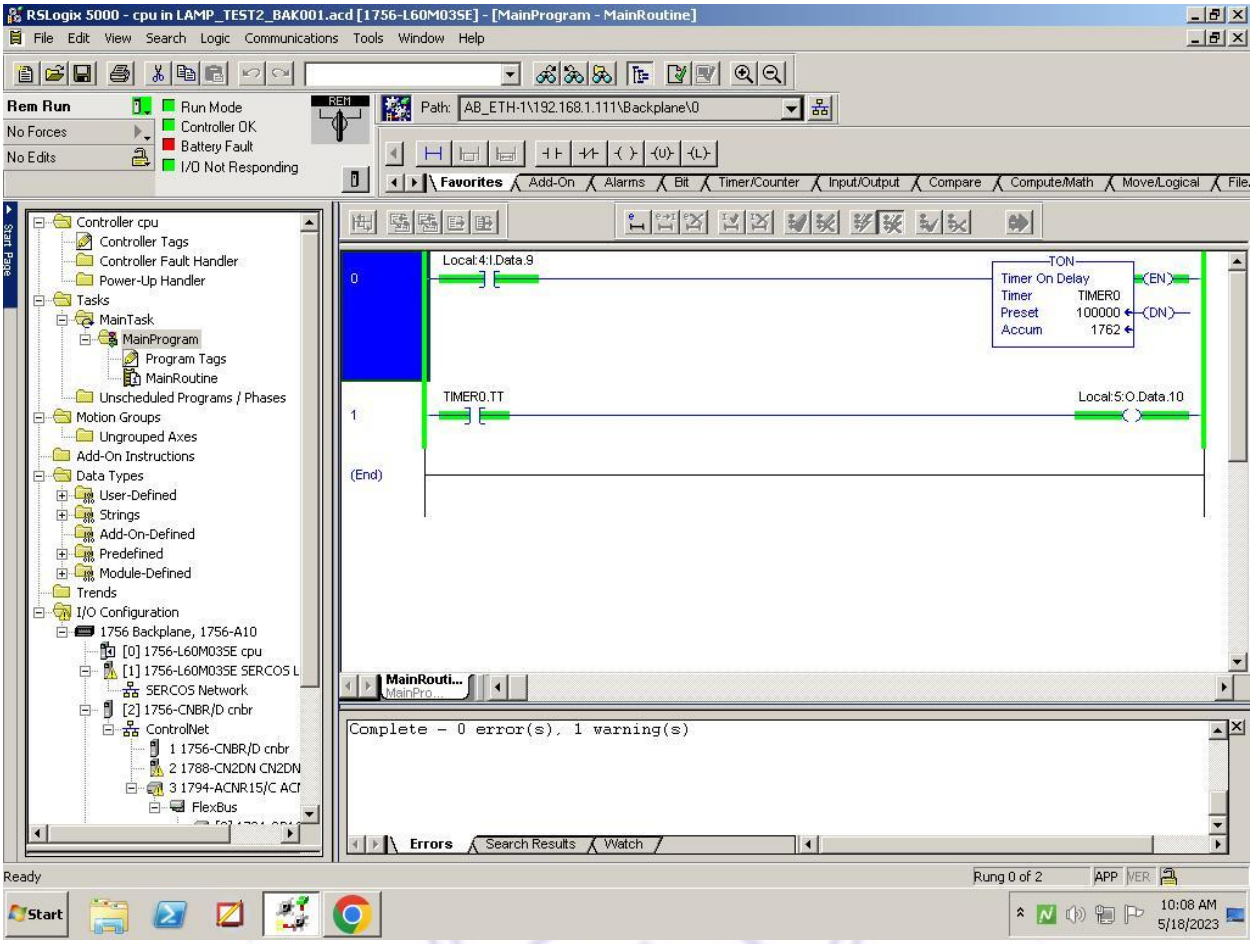
Timing Diagram for Down Counter

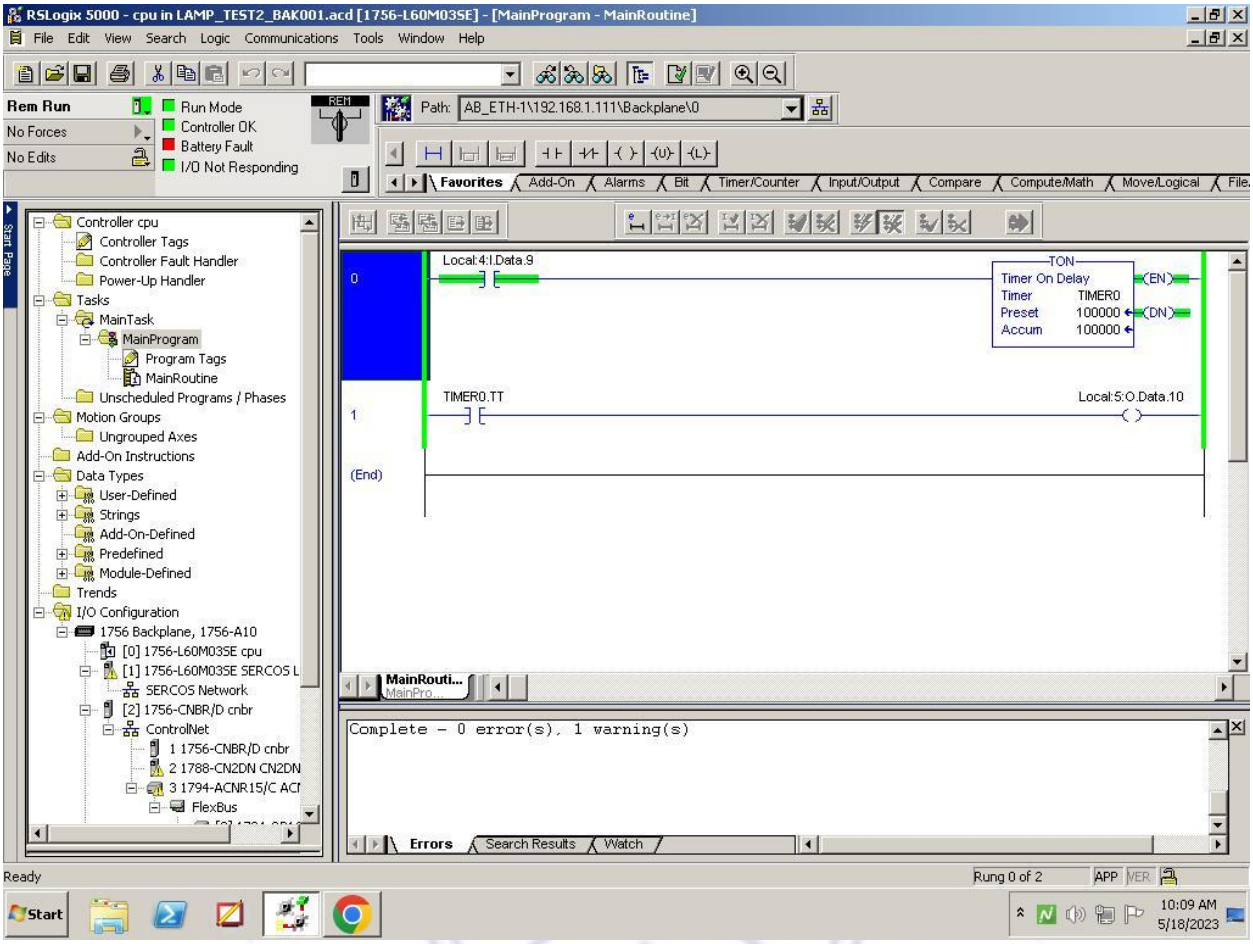
Procedure:

• In this experiment the on delay timer will be tested for its functionalities using Simulator. Following bits of the timer are to be observed.
• Initializing bit "ON" in this case.
• Enable bit "T_en"
• Done bit "T_dn"
• Timer timing bit "T_tt"
• Preset value needs to be entered by the user.
• While configuring the timer the default time is 1 ms. Select appropriate preset value as per the need of the application. The screen shot of the configured timer will appear like this.
• To test the EN, DN, and TT bits;configure the timer by right clicking anywhere on the timer block. Submit tag and preset value.
• Add new rung to test the timer status or to energies the output. You can also test the cascading of the timer using these bits.
• Observe the tag name for timer DN bit.

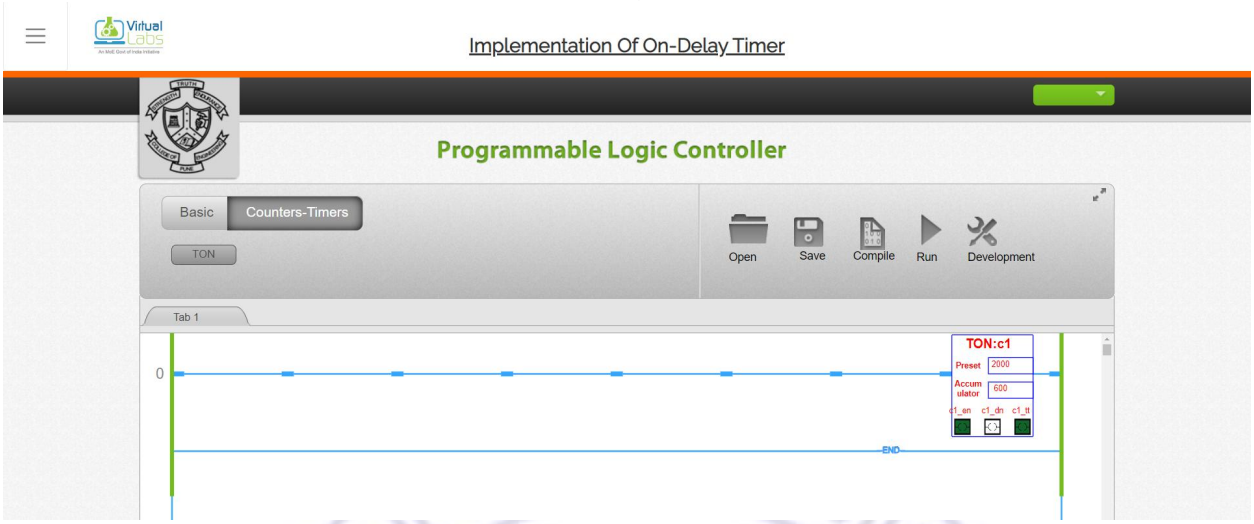
Experiment:

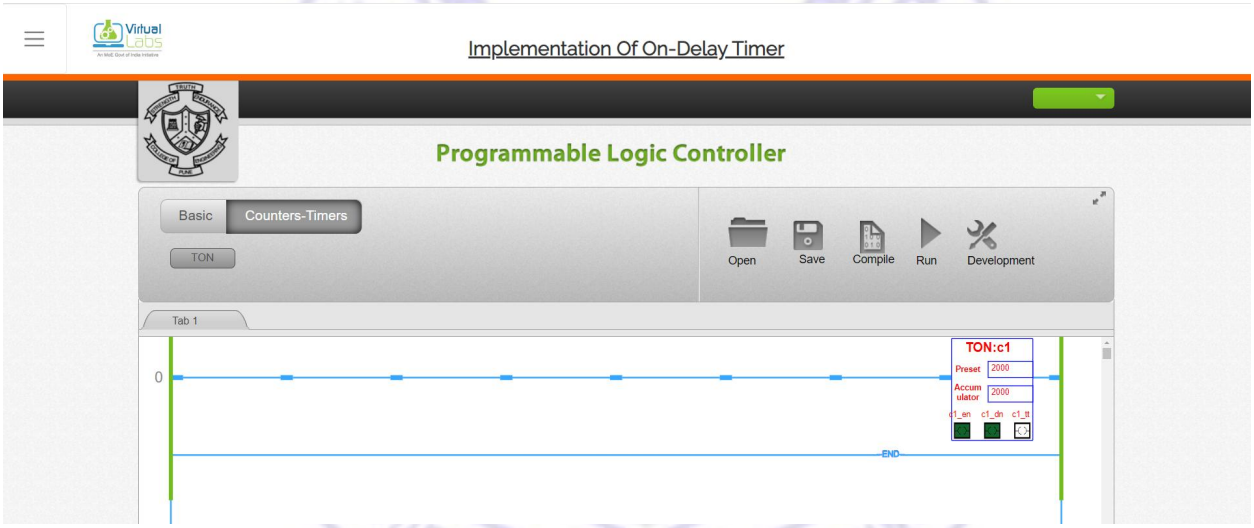




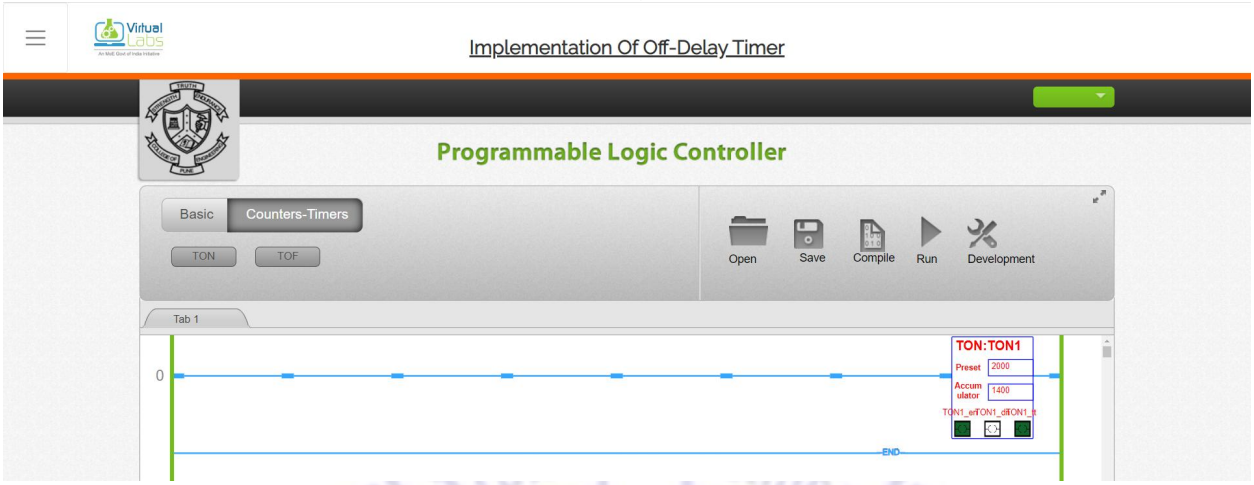


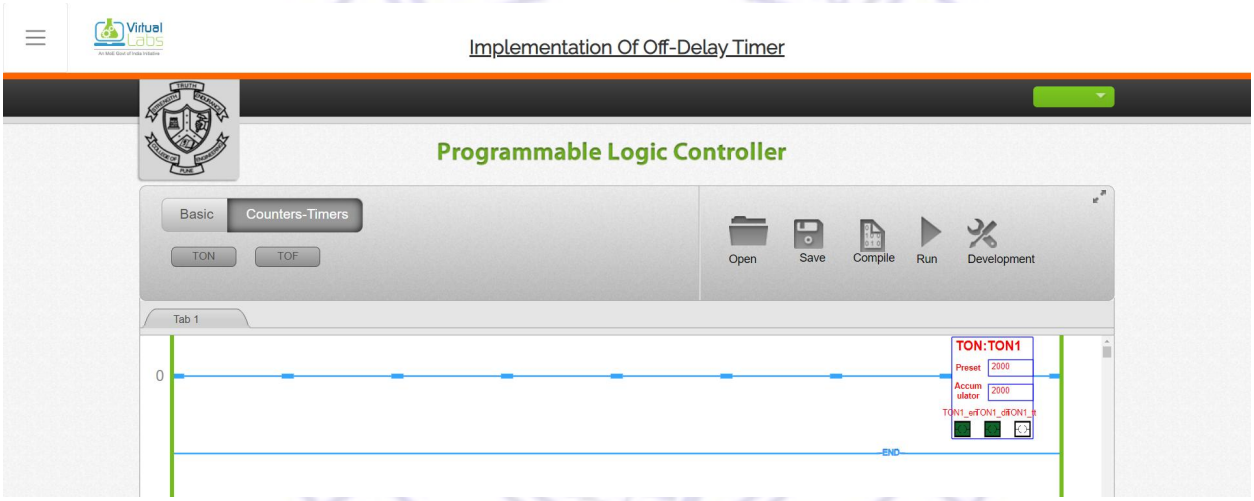
On-Delay Timer



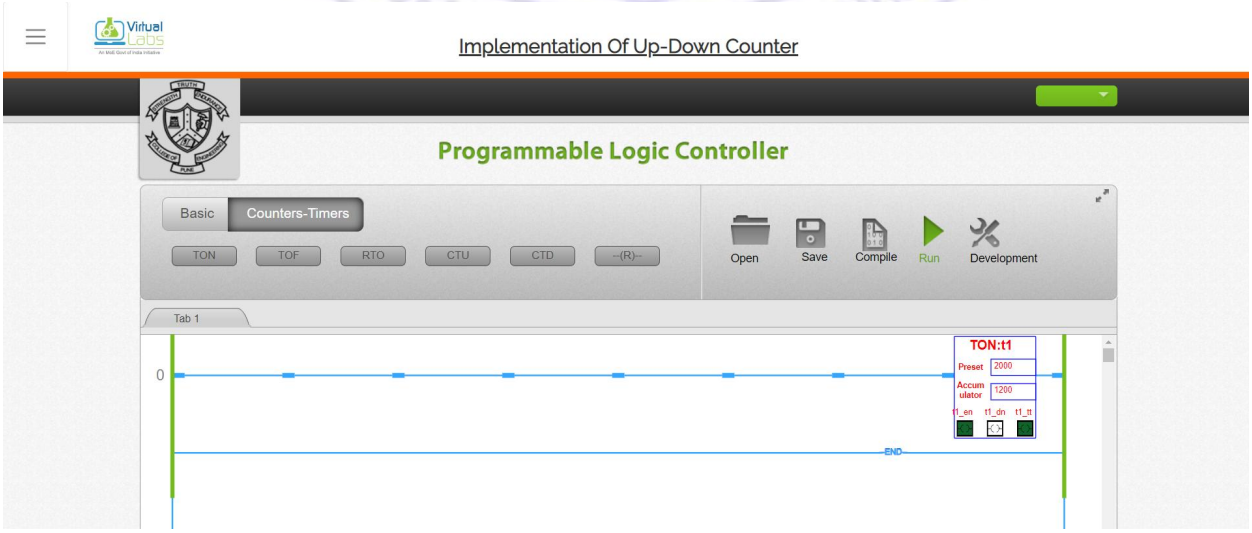


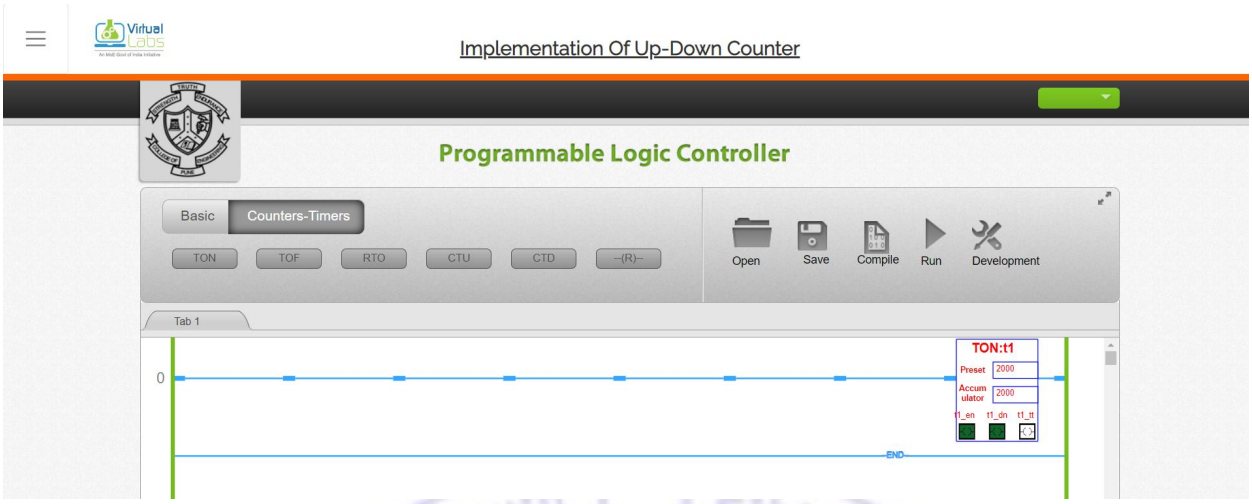
Off-Delay Timer

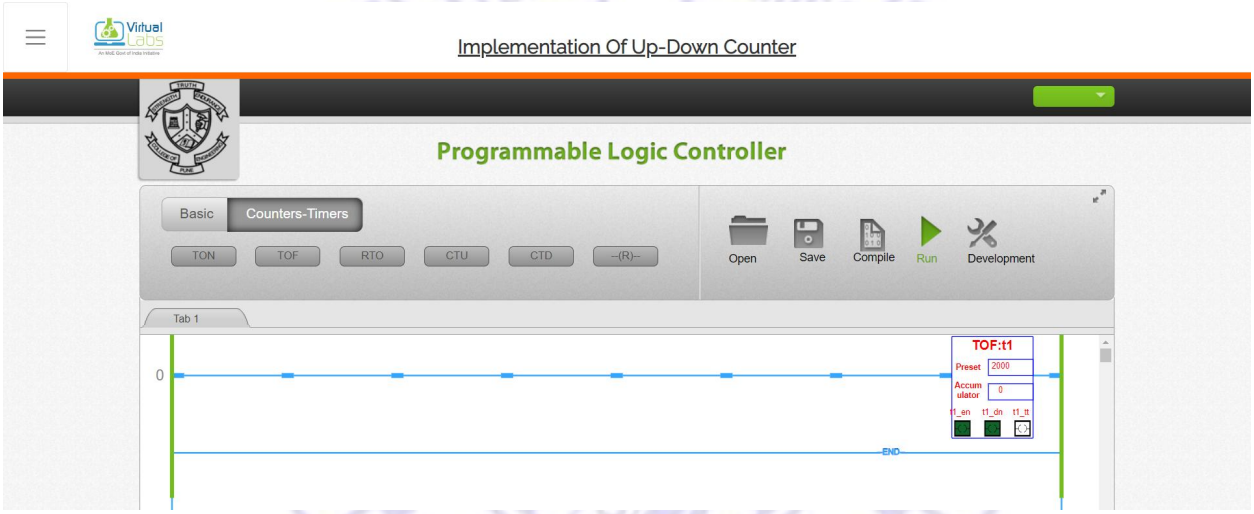




Up-Down Counter







Conclusion:

The experiment focused on studying the timing diagrams of three important components in programmable logic controllers (PLCs): the On Delay Timer, the Off Delay Timer, and the Counter. By analyzing the timing diagrams, participants were able to understand the behavior and operation of these components. The study of the On Delay Timer provided insights into how it initiates an output after a specified delay when the input signal is activated. Similarly, the Off Delay Timer demonstrated how it maintains an output after the input signal is deactivated for a specified delay. Lastly, the study of the Counter timing diagram helped participants understand how a counter component keeps track of the number of input pulses and triggers an output when a specific count is reached. By comprehending these timing diagrams, participants gained a comprehensive understanding of the timing functions and capabilities of these important PLC components.