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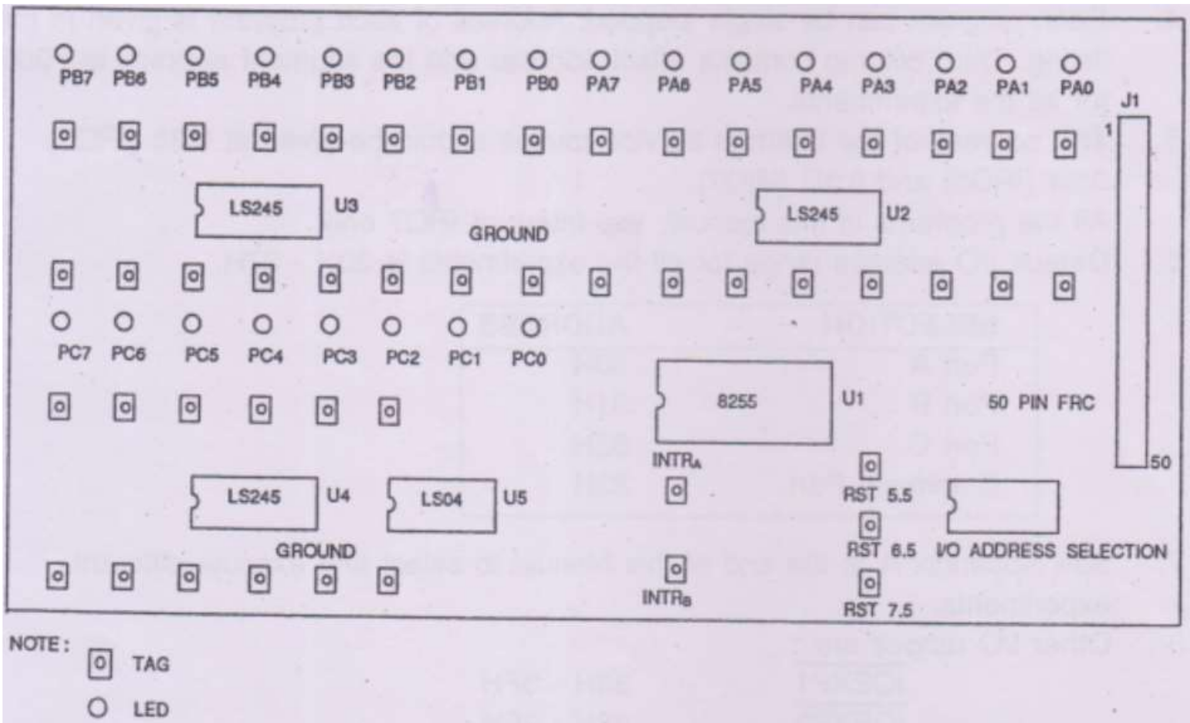
DYNA - PIO/2, STUDY OF 8255

ABOUT DYNA - PIO/ 2, STUDY OF 8255

1. This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
2. It consists of one 8255 with tags for all I/O ports buffers to drive LEDs, VCC and GND tags.

DYNA - PIO/2 STUDY OF 8255 COMPONENT PLACEMENT:



ABOUT 8255:
The Programmable Peripheral Interface chip 8255 has three 8-bit Input! Output ports.

APPLICATION:
8255 is a very powerful tool for interlacing peripheral equipment to the microcomputer system. It is flexible enough to interface with any I/O device without the need of external logic.

Each peripheral device in a microcomputer system usually has a 'service routine' associated with it, which manages software interface between device and CPU. Various applications are Printer Interface, Keyboard & Display Interface, Analog to Digital & Digital to Analog Interface, CRT Controller Interface and Floppy Disk Interface etc.

GENERAL PROCEDURE:

1. Keep the DYNA-PIO/2 card to the left side of DYNA-86LU kit.
2. Connect DYNA-PIO/2 to DYNA-86LU kit using the 50 pin FRC cable.
3. Do not connect/ remove DYNA-PIO/2 to/ from DYNA-86LU while the power is on.

4. Each program can be single stepped. Address of each program is given in the listing, Third column contains offset address and the segment address is F000H for all the experiments.
5. The address of the interrupt service routine should be given at 0:38 (11R06) 0:34 (1RQ5) and 0:3C (ER07).
   All the programs in this manual, use interrupt IRQ7 only.

6. Default I/O address range for all the experiments is 30H - 37H.

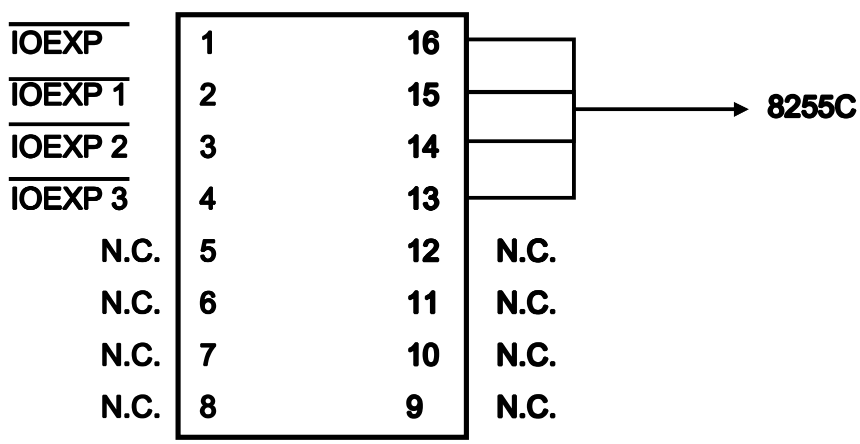
SELECTION	ADDRESS
Port A	30H
Port B	31H
Port C	32H
Command Port	33H

7. See Appendix A at the end of this Manual to select and execute different experiments.

8. Other I/O ranges are:

$\overline{IOEXP1}$	38H - 3FH
$\overline{IOEXP2}$	28H - 2FH
$\overline{IOEXP3}$	20H - 27H

9. I/O address can be selected through a DIP switch.



EXPERIMENT 1:

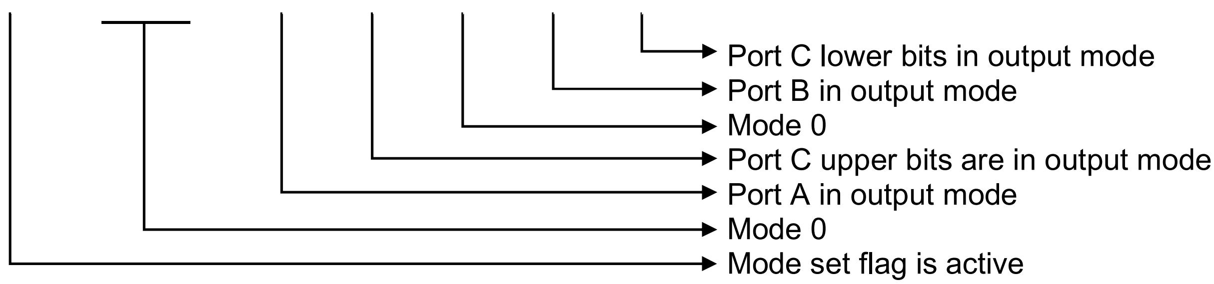
AIM: 8255 is configured in mode 0, i.e. simple Input/ Output mode. Ports A, B, C are in mode 0. All the ports are in output mode and data is transmitted to the respective ports.

CONDUCTING EXPERIMENT:

			P_8255_1
0000:C000	B0 80	MOV AL,80H	Mode 0, All ports in o/p mode
0000:C002	E6 33	OUT CMD_PORT 55,AL	
0000:C004	B0 55	MOV AL,55H	Data for port A
0000:C006	E6 30	OUT PORTA 55,AL	
0000:C008	B0 AA	MOV AL,0AAH	Data for port B
0000:C00A	E6 31	OUT PORTB 55,AL	
0000:C00C	B0 0F	MOV AL,0FH	Data far port C
0000:C00E	E6 32	OUT PORTC 55,AL	
0000:C010	CC	INT 3	

STEP 1: "80H" is the control word for 8255. It is set in simple VO mode and all the ports are in output mode O.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



STEP 2: The LEDs connected to the pins of port A glow according to the data transmitted on port A.

STEP 3: The LEDs connected to the pins of port B glows according to the data transmitted on port B.

STEP 4: The LEDs connected to the pins of port C glows according to the data transmitted on port C.

EXERCISE:

Write a program to set ports A, B and C in mode 0 with port A in output mode, ports B and C in input mode.

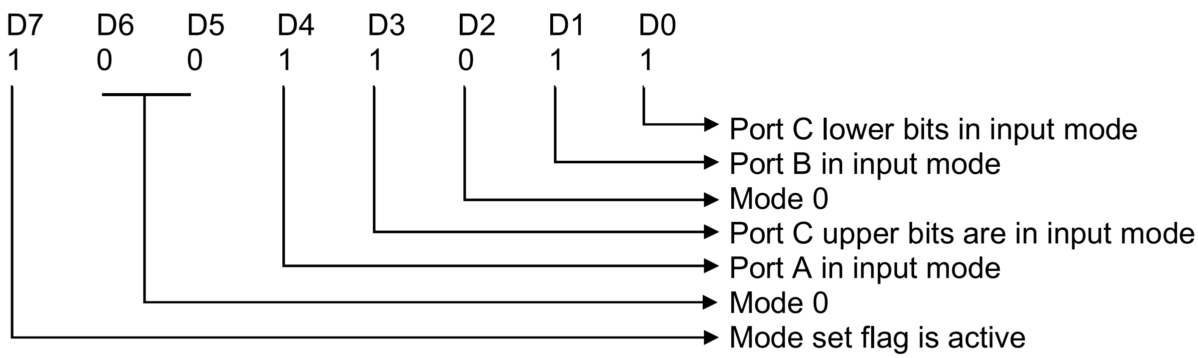
EXPERIMENT 2

AIM: 8255 is configured in mode 0, i.e. simple Input/ Output mode. Ports A, B, C are in input mode. Data from all the 3 ports are read and then stored in different registers.

CONDUCTING EXPERIMENT:

			P_8255_2
0000:C020	B0 9B	MOV AL,9BH	Mode 0, All ports in i/p mode
0000:C022	ES 33	OUT CMD_PORT 55,AL	
0000:C024	E4 30	IN AL,PORTA_55	
0000:C026	8A D0	MOV DL,AL	
0000:C028	E4 31	IN AL, PORT8_55	
0000:C02A	8A D8	MOV BL,AL	
0000:C02C	E4 32	IN AL,PORTC-55	
0000:C02E	8A C8	MOV CL,AL	
0000:C030	CC	INT 3	

STEP 1: 9BH is the control word for 8255, it is in simple I/O. All the ports are in input mode 0.



STEP 2: Connect the pins of ports A, B, C to GND and VCC according to the data to be given to the ports A, B, C respectively.

STEP 3: Data from port A will be stored in reg DL. The data in reg DL should match the data shown by the glowing LEDs of port A.

STEP 4: Data from port B will be stored in reg BL. The data in reg BL should match the data shown by the glowing LEDs of port B.

STEP 5: Data from port C will be stored in reg CL. The data in reg CL should match the data shown by the glowing LEDs of port C.

EXERCISE:

Write a program to set ports A, B, C in mode 0 with port A in input mode and ports B and C in output mode.

EXPERIMENT 3:

AIM: 8255 is configured in the BIT SET/ RESET mode.
To SET or RESET the bits of Port C, it is defined in the OUTPUT MODE and after setting Port C in BSR mode, individual bits of Port C are set. A delay is given and after completion of the delay, the bits are RESET. This routine is given in a loop so that the LEDs glow when the bits are set and go off when the bits are reset.

CONDUCTING EXPERIMENT:

			P_8255_3
0000:C040	B0 80	MOV AL, 80H	Port C in O/p mode
0000:C042	E6 33	OUT CMD-PORT-55,AL	
0000:C044	B0 0F	**LL1:** MOV AL,OFH	BSR mode bit 7 of port C is set.
0000:C046	E6 33	OUT CMD_PORT_55,AL	
0000:C048	OE E8 BFAD	CALL FAR DELAY	DELAY(4000H)
0000:C04B	B0 0E	MOV AL,0EH	
0000:C04D	E6 33	OUT CMD-PORT-55,AL	
0000:C04F	0E ES BFA5	CALL FAR DELAY	DELAY(4000H)
0000:C052	EB EE	JMP LL1	

STEP 1: "80H" is the control word for 8255, it is in simple I/O mode. All the ports are in output mode.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0

→ Port C lower bits in output mode
→ Port B in output mode
→ Mode 0
→ Port C upper bits are in output mode
→ Port A in output mode
→ Mode 0
→ Mode set flag is active

STEP 2: "OFH" is the control word for 8255, it is in BSR mode. Bit 7 of port C is set.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	1	1

→ 7th bit is set
→ Port C. 7th bit is selected
→ Don't care
→ Bit set / reset flag is active

STEP 3: Some delay is given.

STEP 4: "OEH" is the control word for 8255, it is in BSR mode. Bit 7 of port C is reset.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	1	0

7th bit is reset
Port C. 7th bit is selected
Don’t care
Bit set / reset flag is active

EXERCISE:

Write programs to set and reset different bits of port C.

EXPERIMENT 4:

This experiment demonstrates the operation of 8255 in mode 1, i.e. strobed input /output mode. This functional configuration provides the means for transferring I/O data to or from a specified port in conjunction with "HANDSHAKE" signals.

AIM: 8255 is in mode 1, i.e. strobed input / Output made.
Ports A, B are in mode 1. Port A is in output mode, so the data is transmitted to the port. Port B is in input mode, so data is read from the port. Port C is used for control signals. Port C is used in BSR mode to set the interrupts of ports A, B.

CONDUCTING EXPERIMENT:

			P_8255_4
0000:C060	B0 7F	MOV AL,07FH	UNMASK IRQ7
0000:C062	E6 02	OUT OCW1, AL	SEND OCW1
0000:C064	FB	STI	Enable Interrupts
0000:C065	BO A6	MOV AL,0A6H	PORT A O/P MODE 1 PORT B I/P MODE 1 PORT C for control signal
0000:C067	E6 33	OUT CMD_PORT 55,AL	
0000:C069	B0 5A	MOV AL,5AH	
0000:C06B	E6 30	OUT PORTA 55,AL	
0000:C06D	B0 05	MOV AL,05H	INTE-B bit 2 of port C set
0000:C06F	E6 33	OUT CMD_PORT 55,AL	
0000:C071	B0 0D	MOV AL,ODH	INTE-A bit 6 of port C set
0000:C073	E6 33	OUT CMD_PORT 55,AL	
0000:C075	CC	INT 3	

STEP 1: “7FH” is command word given to unmask IRQ7.

STEP 2: "A6H" is the control word for 8255, it is in strobed I/O mode. Ports A, B are in mode 1. Port A is in output mode and port B is in input mode. Port C pins are used for control signals.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	1	1	0

D0 → Port C lower bits in output mode
D1 → Port B in input mode
D2 → Mode 1
D3 → Port C upper bits are in output mode
D4 → Port A in output mode
D6 D5 → Mode 1
D7 → Mode set flag is active

STEP 3: Rest of the program is self-explanatory.

This program uses Port A in output mode 1 and Port B in input mode 1 operation.

STEP 4: First observe the output operation of Port A in mode 1.

1) Execute the program.
2) See data 5AH at Port A.
3) See PC7 i.e. $\overline{OBF}$ is low (i.e. buffer full)
4) Now make PC6 ($\overline{ACKA}$) low by tag. Falling edge of ACK makes PC7 high and rising edge of $\overline{ACKA}$ makes PC3 (i.e. INTRA) high.

STEP 5: To observe input mode1 operation of Port B.

1) Execute program.
2) See PC2 (i.e. $\overline{STB_B}$) is high.
3) Connect pins of Port B to VCC and GND according to data to be transmitted.
4) Make PC2 ($\overline{STB_B}$) low. Falling edge of PC2 makes PC1 (i.e IBF_B) high and rising edge of PC2 makes PCO high (i.e. $INTR_B$).

If these interrupt pins are connected to RST 7.5 (i.e. IRQ7), then "IR07” is displayed in the display when interrupt comes.

EXERCISE:

Write a program to set ports A and B in mode 1 as input.

EXPERIMENT 5:

AIM: 8255 is in strobed Input/ Output mode.
Port B is in output mode, mode 0 and the data is transmitted to the port. Port A is in input mode, mode 1 and the data is received from the port and stored in a reg. Port C higher bit pins are used for control signals.
Port C is used in BSR mode to set the interrupt of port A.

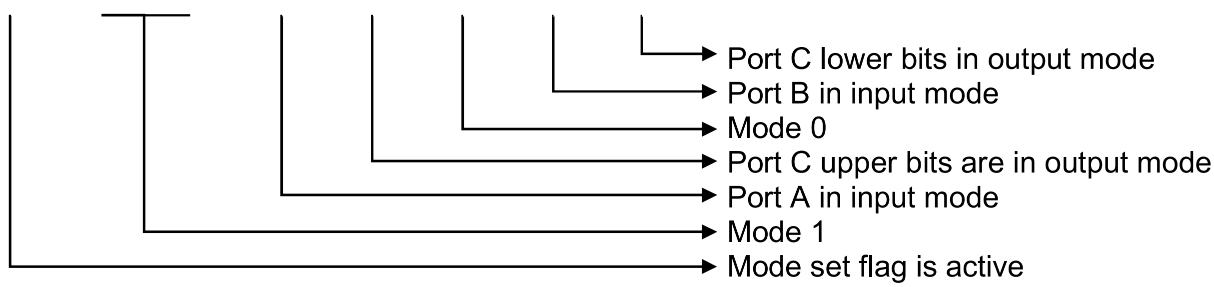
CONDUCTING EXPERIMENT:

			P_8255_5
0000:C080	B0 7F	MOV AL,07FH	Unmask IRQ 7
0000:C082	E6 02	OUT OCW1, AL	Send OCW1
0000:C084	FB	STI	Enable interrupts
0000:C085	B0 B0	MOV AL,0B0H	Port A Mode 1 input Port B Mode 0 output Port C control signal
0000:C087	E6 33	OUT CMD_PORT_55,AL	
0000:C089	B0 6B	MOV AL,6BH	Data for Port B
0000:C08B	E6 31	OUT PORTB_55,AL	
0000:C08D	B0 09	MOV AL,09H	Set PC4 to Enable INTE-A I/P
0000:C08F	E6 33	OUT CMD_PORT_55,A	
0000:C091	CC	INT 3	

STEP 1: "7FH" is the command word given to unmask IRQ7.

STEP 2: "B0H" is the control word for 8255, it is in I/O mode. Port A is in input mode 1 and port B is in output mode.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0



STEP 3: 1) Execute program.
2) See data on Port B is 6BH.
3) See PC4 (i.e. $\overline{STB_A}$) is high.
4) Connect Port A pins to VCC and GND according to the data to be transmitted.
5) Make PC4 low. Falling edge of PC4 makes PC5 (i.e. IBFA) high and rising edge of PC4 makes PC3 (i.e. INTRA) high.

If this INTRA is connected to RST 7.5 (i.e. IRQ7), then "IR 07 is displayed in display.

EXERCISE:
Write a program to set port A in mode 0 and port B in mode   1. Ports A and B are in input mode.

EXPERIMENT 6:

In mode 2 port A is used as a bidirectional port. Port B can be in either in mode 0 or 1. Port C is used for control signals.

AIM: 8255 is in mode 2, i.e. strobed input / Output mode.
Port A is in input mode, mode 2, port B is in output mode, mode 0. Lower bits of port C are in output mode and higher bits are used for control signals.
Port C is used in BSR mode to set the interrupt of port A.

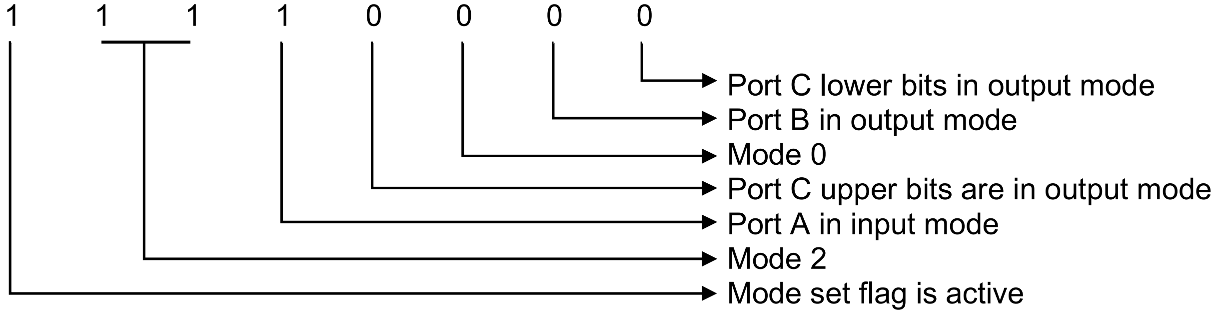
CONDUCTING EXPERIMENT:

			P_8255_6
0000:C0A0	B0 7F	MOV AL,07FH	UNMASK IRQ7
0000:C0A2	E6 02	OUT OCW1,AL	SEND OCW1
0000:C0A4	FB	STI	Enable Interrupts
0000:C0A5	B0 F0	MOV AL,0F0H	PORT A MODE 2 PORT B in MODE 0 O/p PORT C upper 5 bits for control signal & lower 3 bits for in O/p mode.
0000:C0A7	E6 33	OUT CMD_PORT_55,AL	
0000:C0A9	B0 6B	MOV AL,6BH	Data For Port B
0000:C0AB	E6 31	OUT PORTB_55,AL	
0000:C0AD	B0 0D	MOV AL,0DH	PC6 is set i.e. INTE 1 for O/P mode operation of Port A
0000:C0AF	E6 33	OUT CMD_PORT_55,AL	
0000:C0B1	B0 7A	MOV AL,7AH	Data For Port A
0000:C0B3	E6 30	OUT PORT A-55,AL	
0000:C0B5	B0 09	MOV AL,09H	PC4 is set i.e INTE2 for i/p mode operation of PORT A
0000:C0B7	E6 33	OUT CMD PORT_55,AL	
0000:C0B9	CC	INT 3	

STEP 1: “7FH" is the command word given to unmask IRQ7.

STEP 2: "F0H" is the control word for 8255, it is in simple I/O mode. Port A is in mode 2, port B is output in mode 0. Port C lower bits are in output mode and higher bits are used for control signals.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	0	0



STEP 3: Port A is programmed for mode 2 i.e. bidirectional operation mode.
A) To see the output mode of operation of Port A.

1) Execute program.
2) See data 6BH out at Port B.
3) Observe that PC7 (i.e. $\overline{OBF_A}$) is low.
4) Make PC6 (i.e. $\overline{ACK_A}$) low. Falling edge of PC6 makes PC7 high and rising edge of PC6 makes PC3 (i.e. INTRA) high.

B) To see the input mode of operation of Port A
1) Execute program.
2) See data 6BH on Port B.
2) Connect Port A pins to VCC and GND according to the data to be transmitted.
3) Make PC4 (i.e. $\overline{STB_A}$) low. Falling edge of PC4 makes PC5 (i.e. IBFA) high and rising edge of PC4 makes PC3 (i.e. INTRA) high.
4) If this INTRA is connected to RST 7.5 (i.e. IRQ7), then "Ir 07" is displayed.

EXERCISE:

Write a program to set port A in mode 2 and port B in mode 0, Port B and port C lower bits are in input mode.

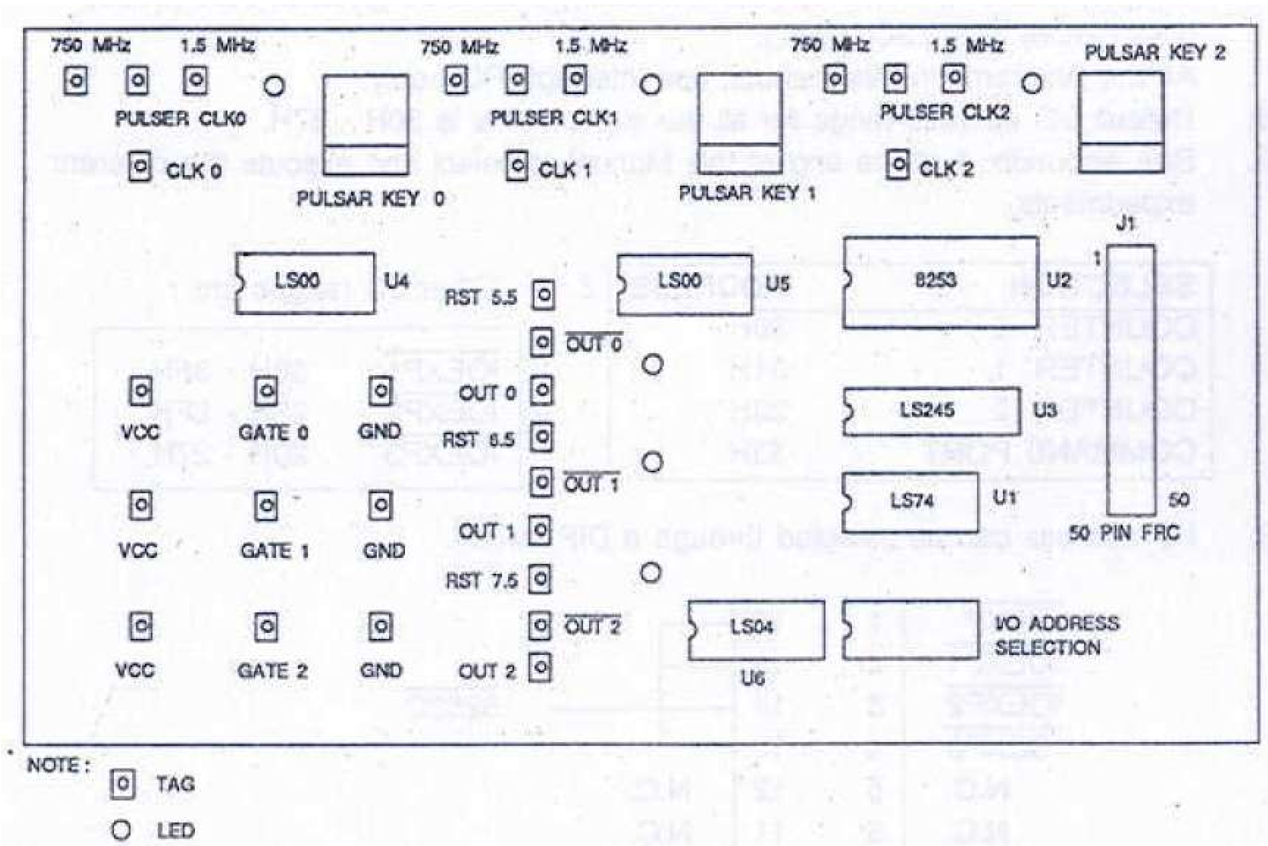
DYNA – TIMER, STUDY OF 8253

ABOUT DYNA – TIMER, STUDY OF 8253

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU.
- It consists of buffers, one 8253 with tags for all the counters, VCC and GND tags, LEDs.

DYNA-TIMER, STUDY OF 8253

COMPONENT PLACEMENT



ABOUT 8253:

The Programmable Interval Timer chip 8253 has three independent built-in 16-bit down counters which supports both binary and decimal counts.

APPLICATIONS:

It is used for Delayed-time setting, pulse counting & rate generation in microcomputers.

GENERAL PROCEDURE:

1. Keep the card to the left side of the DYNA-86LU kit.
2. Connect DYNA-TIMER to DYNA-86LU kit using the 50 pin FRC cable.

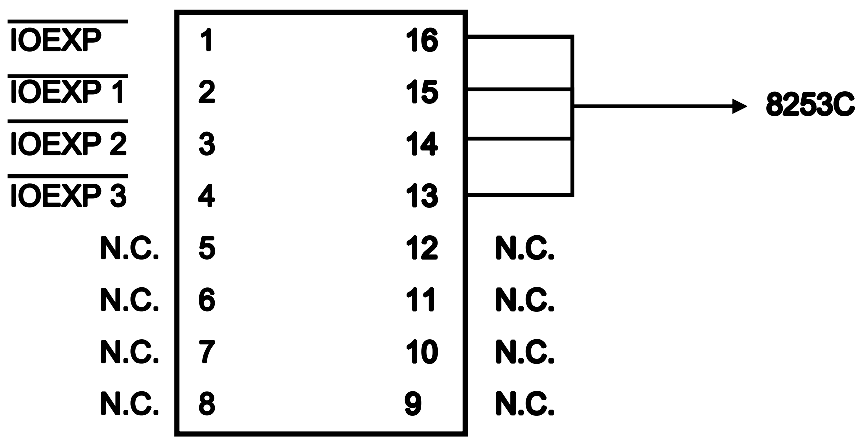
3. Do not connect / remove DYNA-TINIER to / from DYNA-86LU while power is on.
4. Each program can be single stepped. Address of each program is given in the listing. Third column contains offset address and the segment address is F000H for all the experiments.
5. The address of the interrupt service routine should be given at 0:38 (IRQ6) 0:34 (IRQ5) and 0:3C (IRQ7).
   All the programs in this manual, use interrupt IRQ7 only.
6. Default I/O address range for all the experiments is 30H - 37H.
7. See Appendix A at the end of this Manual to select and execute the different experiments.

SELECTION	ADDRESS
Counter 0	30H
Counter 1	31H
Counter 2	32H
Command Port	33H

8. Other I/O ranges are:

$\overline{\text{IOEXP1}}$	38H - 3FH
$\overline{\text{IOEXP2}}$	28H - 2FH
$\overline{\text{IOEXP3}}$	20H - 27H

9. I/O address can be selected through a DIP switch.



EXPERIMENT 1:

There are 3 counters in 8253 and 6 different modes for all the 3 counters.
Mode 0 is also called as an interrupt on terminal count. In mode 0 any one of the counters can be selected. It can be, a binary or BCD counter. The count to be loaded can be either 16-bit or 8-bit.
The function of the gate can be defined as follows:-
Low or low going edge of the pulse disables counting.
Rising edge of the pulse has no effect.
High edge of the pulse enables counting.
The 750 KHz or 1.5 MHz clock can be connected to the CLK pin of the counter or an external CLK can be given through the pulser key. The waveforms can be observed at the Out pin of the counter.

AIM: The counter is in mode 0, i.e. interrupt on terminal count.
Binary counter 0 is selected. Read / Load lower 8-bits and then higher 8-bits.

CONDUCTING EXPERIMENT:

			P_8253_1
0000:C000	B0 7F	MOV AL, 07FH	Unmask IRQ7
0000:C002	E6 02	OUT OCW1, AL	Send OCW1
0000:C004	FB	STI	Enable interrupts
0000:C005	B0 30	MOV AL,30H	Binary counter 0 selected, mode 0 Read/Load LSB first and then MSB
0000:C007	E6 33	OUT CMD PORT-55,AL	
0000:C009	B0 05	MOV AL,05H	
0000:C00B	E6 30	OUT COUNTER_0,AL	Counter 0 LSB
0000:C00D	B0 00	MOV AL,00H	
0000:C00F	E6 30	OUT COUNTER_0,AL	Counter_0 MSB
0000:C011	DB C0	**B1:** MOV AL,00H	Binary Counter_0, mode 0, counter latch
0000:C013	E6 33	OUT CMD PORT 53,AL	
0000:C015	E4 30	IN AL,COUNTER_0	Read LSB
0000:C017	8A D0	MOV DL,AL	
0000:C019	E4 30	IN AL,COUNTER-0	Read MSB
0000:C01B	8A F0	MOV DH,AL	
0000:C01D	EB F2	JMP B1	
0000:C01F	CC	INT 3	

Note: Connect pulsar clock to dock. Gate to VCC. Connect IRQ7 to OUTO after executing the program and then press the pulsar key.

STEP 1: "7FH" is the command used to unmask 1RQ7.

STEP 2: "30H" is the control word for 8253. Binary counter 0 is selected. Timer mode is 0. Lower 8-bit count should be loaded first and then higher 8-bit count should be loaded.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0

→ Binary counter, 16 bits
→ Mode 0
→ Read / Load MSB followed by MSB
→ Select Counter 0

STEP 3: 0005H is the 16-bit count that is loaded into the counter. First the LSB count should be loaded followed by the MSB count.

STEP 4: "00H" is the control word for 8253 to latch the count. If 4th and 5th bits of the control word are 0 then the count can be latched. MSB and LSB count can be stored in a reg, pair so that it can be read.

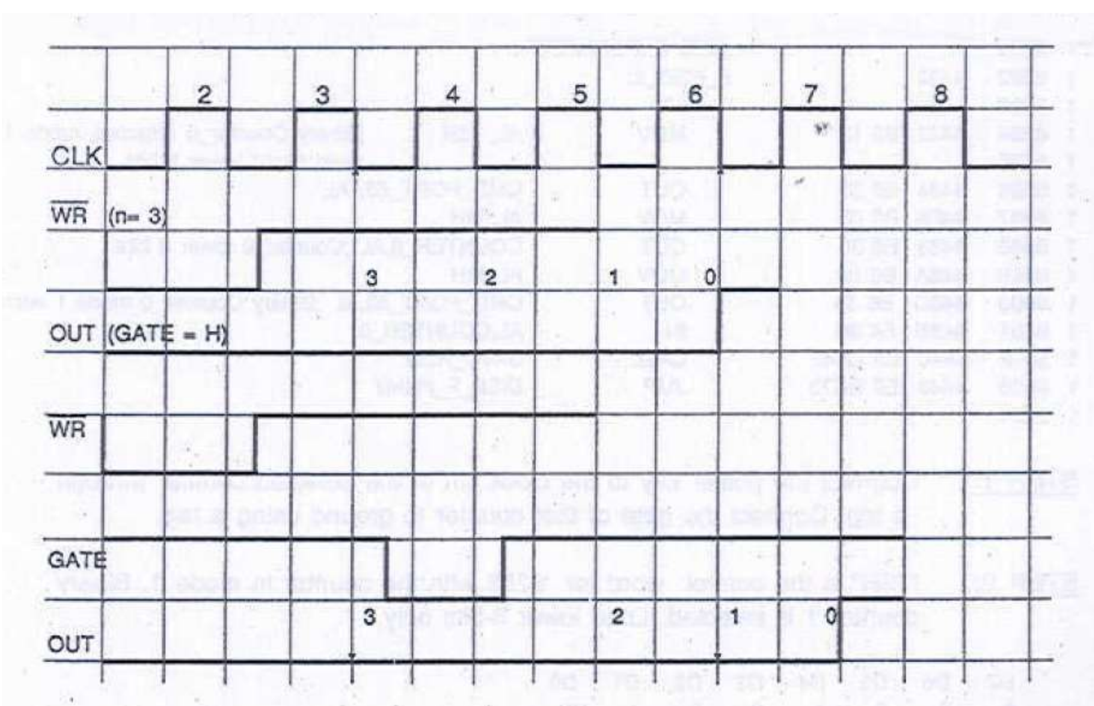
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

→ Binary counter, 16 bits
→ Mode 0
→ Counter latching operation
→ Select Counter 0

STEP 5: A pulse can be given to the pulsar clock and the waveforms can be observed at the OUT0 pin as shown below in Fig 1.1.

STEP 6: After 5 pulses OUT0 goes high generating IRQ7 and "Ir 07" is displayed.

MODE 0 Timing Diagram: Fig 1.1



EXPERIMENT 2:

Mode 1 is also called as programmable one shot. In mode 1 any of the counters can be selected. It can be a binary or BCD counter. The count can be 16-bit or 8-bit. The function of the gate can be defined as follows:-
Low or low going edge of the pulse has no effect on the counter.
Rising edge of the pulse inhibits counting and then resets the output after the next clock.
High edge has no effect on the counter.
A 750 KHz or 1.5 MHz clock can be connected to the CLK pin of the counter or an external CLK can be connected through a pulser key. The waveforms can be observed at OUT pin of the counter selected.

AIM: The counter is in mode 1, i.e. programmable one shot.
Binary counter 1 is selected, Read / Load lower 8-bits only.

CONDUCTING EXPERIMENT:

			P_8253_EXP-2
0000:C020	B0 12	MOV AL,12H	Binary counter 0 selected, mode 1 Read / Load lower 8 bits.
0000:C022	E6 33	OUT CMD-PORT-53,AL	
0000:C024	B0 05	MOV AL,05H	
0000:C026	E6 30	OUT COUNTER 0,AL	Counter 0 lower 8-bits
0000:C028	B0 02	MOV AL,02H	
0000:C02A	E6 33	OUT CMD-PORT-53,AL	Binary counter 0 mode 1 latch
0000:C02C	E4 30	IN AL,COUNTER-0	
0000:C02E	CC	INT 3	

STEP 1: Connect the pulser key to the clock pin of the selected counter through a tag. Connect the gate of that counter to ground using a tag.

STEP 2: "12H" is the control word for 8253 with the counter in mode 1. Binary counter 1 is selected. Load lower 8-bits only.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0

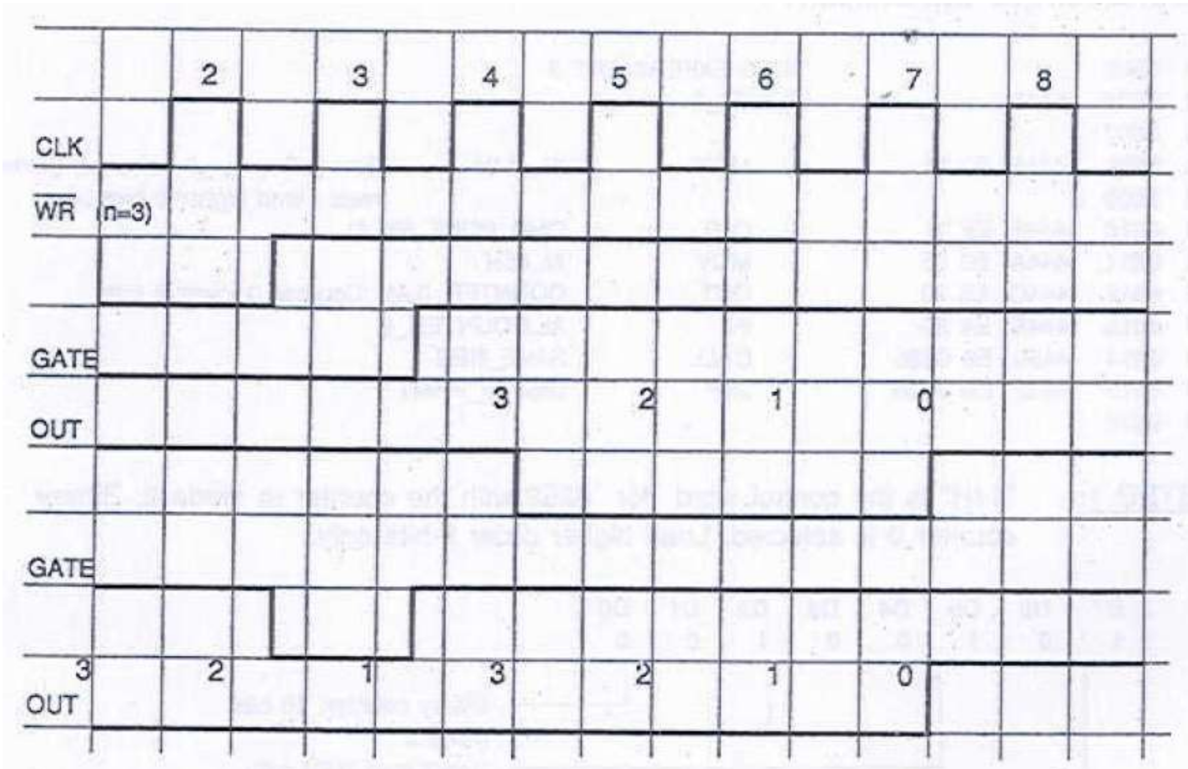
D0 → Binary counter, 16 bits
D3 D2 D1 → Mode 1
D5 D4 → Read / Load LSB only
D7 D6 → Select Counter 1

STEP 3: "0BH" is the lower 8-bit count.

STEP 4: "02H" is the control word for 8253 with the counter in mode 1. It latches the count and then stores it in a reg. so that it can be read.

STEP 5: Execute the program.
Connect the gate to VCC through a tag and start giving the pulse. When the pulse is given, the LED turns off at the falling edge of the pulse and glows on the rising edge of the pulse. The count is 05H. So the output of that counter will go low for 5 counts and the LED at that pin remains off and then it begins to glow again.

MODE 1 Timing Diagram Fig 1.2



EXPERIMENT 3:

Mode 2 is also known as a rate generator. In mode 2 any one of the counters can be selected out of three counters. The counter can be either binary or BCD. The count can be 16-bit or 8-bit. The function of the gate can be defined as follows:-
Low or low going edge of the pulse disables counting and sets the output immediately high.
Rising edge of the pulse initiates counting. High edge of the pulse enables counting.
The clock of the counter can be connected to 750 KHz or 1.5 MHz CLK or an external CLK can be given through a pulser key.
The waveforms can be observed on the OUT pin of the counter selected.

AIM: The counter is in mode 2, i.e. rate generator.
Binary counter 2 is selected, only higher order 8-bits can be loaded.

CONDUCTING EXPERIMENT:

			P_8253_EXP-3
0000:C040	B0 14	MOV AL,14H	Binary counter 0 is selected, mode 2 Read/Load higher 8 bits only
0000:C042	E6 33	OUT CMD PORT -53,AL	
0000:C044	B0 05	MOV AL,05H	
0000:C046	E6 30	OUT COUNTER 0,AL	Counter 0, lower 8-bits
0000:C048	E4 30	IN AL,COUNTER 0	
0000:C04A	CC	INT 3	

STEP 1: "14H" is the control word for 8253 with the counter in mode 2. Binary counter 0 is selected. Load higher order 8-bits only.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	1	0	0

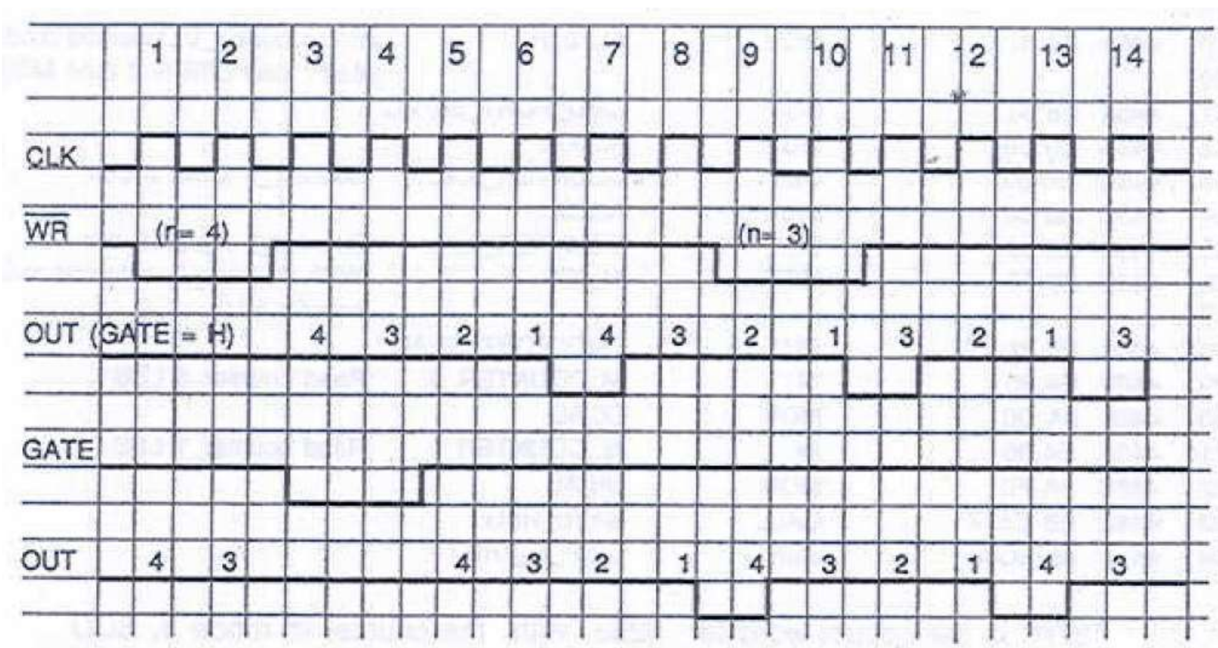
- D0 → Binary counter, 16 bits
- D3 D2 D1 → Mode 2
- D5 D4 → Read / Load LSB only
- D7 D6 → Select Counter 2

STEP 2: 05H is the high order 8-bit count.

STEP 3: The count is stored in reg. A.

STEP 4: Give pulses through pulser key. Observe that OUT0 LED blinks after every five pulses. If clock is connected to 750 KHz or 1.5 MHz observe the waveform on OUT0 pin.

MODE 2 Timing Diagram Fig 1.3



EXPERIMENT 4:

Mode 3 is also known as the square rate generator. In mode 3 any one of the counters can be selected. The counter can be binary or BCD. The count can be either 16-bit or 8-bit.
The function of the gate can be defined as follows:-
Low or low going edge of the pulse disables counting and sets output immediately high.
Rising edge of the pulse initiates counting, High edge of the pulse enables counting.
The clock pin of the counter can be connected to either 750 KHz or 1.5 MHz CLK or an external CLK can be given through the pulser key. The waveforms can be seen at OUT pin of the counter.

AIM: The counter is in mode 3, i.e. square rate generator.
BCD counter 0 is selected, load lower 8-bit count first followed by higher 8-bit count.

CONDUCTING EXPERIMENT:

			P_8253_EXP-4
0000:C060	B0 37	MOV AL,37H	BCD counter -0 selected mode 3 Read /Load LSB first and Then MSB
0000:C062	E6 33	OUT CMD-PORT-53,AL	
0000:C064	B0 06	MOV AL,06H	
0000:C066	E6 30	OUT COUNTER 0,AL	COUNTER-0 lower 8-bits
0000:C068	B0 00	MOV AL,00H	
0000:C06A	E6 30	OUT COUNTER 0,AL	Counter-0 higher 8-bits
0000:C06C	B0 07	MOV AL,07H	BCD Counter-0,Selected Mode 3, Counter Latch
0000:C06E	E6 33	OUT CMD-PORT-53,AL	
0000:C070	E4 30	IN AL,COUNTER 0	Read Counter 0 LSB
0000:C072	8A D0	MOV DL,AL	
0000:C074	E4 30	IN AL,COUNTER 0	Read Counter1 LSB
0000:C076	8A F0	MOV DH,AL	
0000:C078	CC	INT 3	

STEP 1: "37H" is the control word for 8253 with the counter in mode 3. BCD counter 0 is selected. Load low order 8-bits and then high order 8-bits.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	1	1	1

- D0 → BCD Counter 4 decades
- D3 D2 D1 → Mode 3
- D5 D4 → Read / Load LSB followed by MSB
- D7 D6 → Select Counter 2

STEP 2: "06H" is the low order 8-bit count, loaded in counter 0.

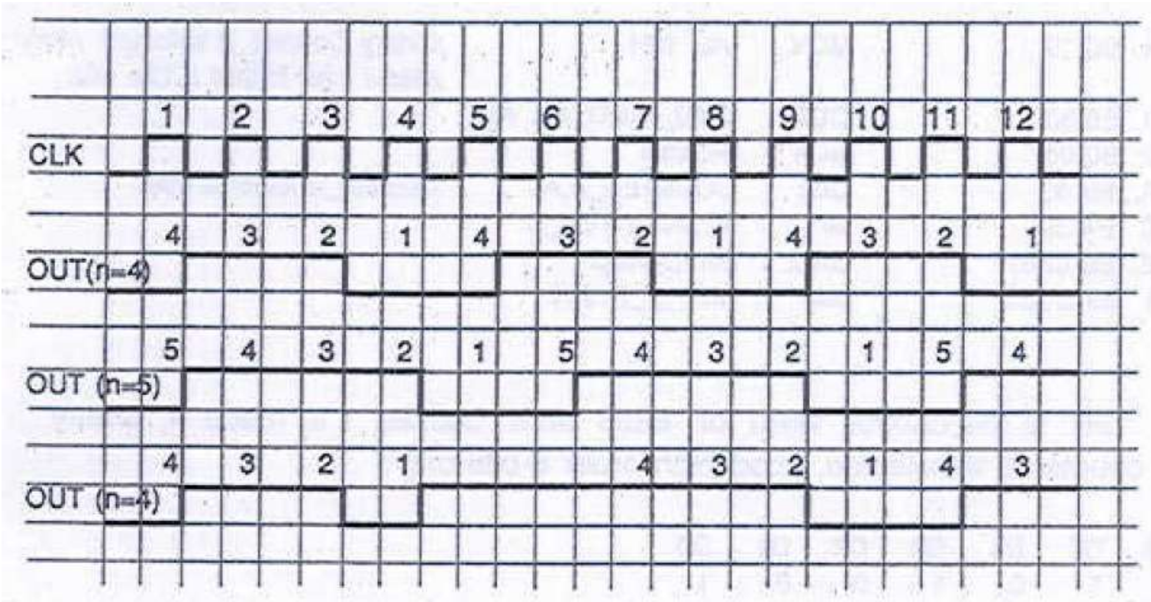
STEP 3: "00H" is the high order 8-bit count, loaded in counter 0.

STEP 4: “87H" is the control word for 8253 with the counter in mode 3. The count is latched and stored in the reg. DX.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	1	1

- D0 → BCD Counter 4 decades
- D3 D2 D1 → Mode 3
- D5 D4 → Counter latching operation
- D7 D6 → Select Counter 2

MODE 3 Timing Diagram: Fig 1.4



NOTE: Programs having high frequency output cannot be seen on the LEDs, only results with the pulser key can be seen on LEDs.

EXPERIMENT 5:

Mode 4 is also known as software triggered strobe. In mode 4 any one of the counters can be selected. It can either be a binary or a BCD counter. The count can be either 16-bit or 8-bit.
The function of the gate can be defined as follows:-
Low or low going edge of the pulse disables counting.
Rising edge of the pulse has no effect on the counter. High edge of the pulse enables counting.
The CLK pin of the counter can be connected to 750 KHz or 1.5 MHz CLK or an external CLK can be given through the pulser key.
The waveforms can be seen on the OUT pin of the counter selected.

AIM: The counter is in mode 4, i.e. software triggered strobe. BCD counter 1 is selected, load high order 8-bits only.

CONDUCTING EXPERIMENT:

			P_8253_EXP-5
0000:C080	B0 19	MOV AL,19H	Binary Counter 0 selected mode 4, Read/Load higher 8-bits only.
0000:C082	E6 33	OUT CMD-PORT-53,AL	
0000:C084	B0 05	MOV AL,05AH	
0000:C086	E6 30	OUT COUNTER 0,AL	Counter-0 Lower 8bit
0000:C088	E4 30	IN AL,COUNTER-0	
0000:C08A	CC	INT 3	

STEP 1: "19H" is the control word for 8253 with counter 1 in mode 4. Binary counter 1 is selected. Load high order 8-bits only.

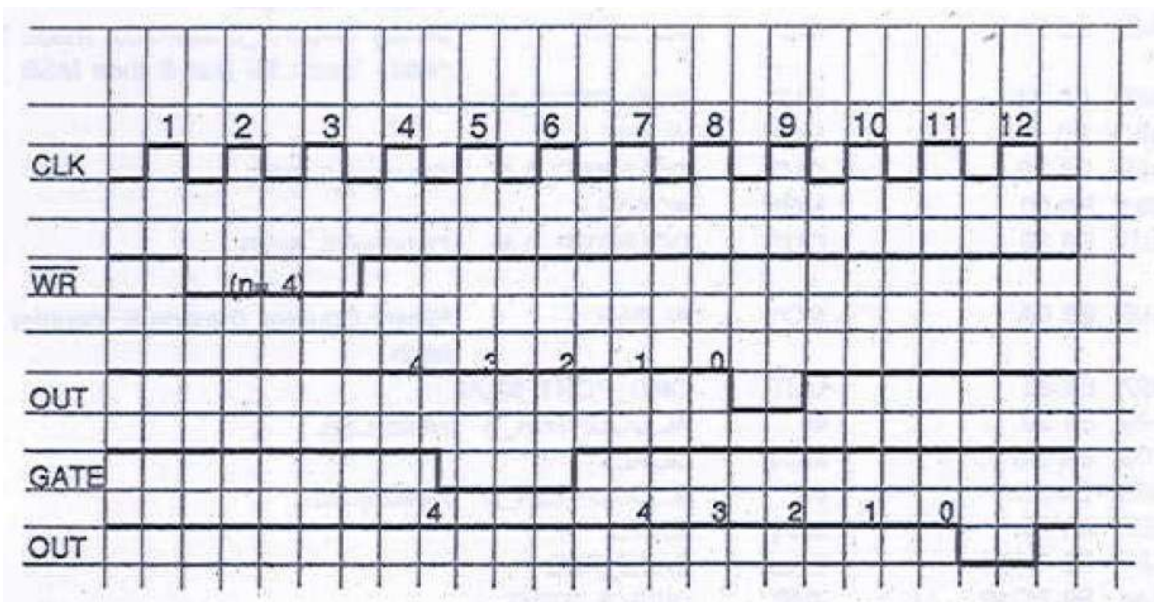
D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	0	1

→ BCD Counter 4 decades
→ Mode 4
→ Read / Load LSB only
→ Select Counter 1

STEP 2: "05H" is the high order 8-bit count for counter 1.

STEP 3: The count is read from the counter and stored in reg A.
Execute the program and give pulses through pulser key. OUT0 goes low after 7 pulses.

MODE 4 Tinting Diagram: Fig 1.5



EXPERIMENT 6:

Mode 5 is also known as hardware triggered strobe. In mode 5 any one of the counters can be selected. It can either be a binary or a BCD counter. The count can be either 16-bit or 8-bit.
The function of the gate can be defined as follows:-
Low or low going edge of the pulse has no effect on the counter. Rising edge of the pulse initiates counting.
High edge of the pulse has no effect on the counter.
The CLK of the counter can be connected to 750 KHz or 1.5 MHz CLK or an external CLK can be given through the pulser key.
The waveforms can be seen at the out pin of the selected counter.

AIM: The counter is in mode 5 i.e. hardware triggered strobe.
Binary counter 0 is selected, load low order 8-bit count and then high order 8-bit count.

CONDUCTING EXPERIMENT:

			P_8253_EXP-6
0000:C0A0	B0 BF	MOV AL,0BFH	Unmask IRQ6
0000:C0A2	E6 02	OUT OCW1,AL	Send OCW1
0000:C0A4	FB	STI	Enable interrupts
0000:C0A5	30 3A	MOV AL,3AH	Binary counter 0 selected, Mode 5, Read/Load LSB first and then MSB
0000:C0A7	E6 33	OUT CMD-PORT-53,AL	
0000:C0A9	B0 05	MOV AL,05H	
0000:C0AB	E6 30	OUT COUNTER 0,AL	Counter 0 LSB
0000:C0AD	B0 00	MOV AL,00H	
0000:C0AF	E6 30	OUT COUNTER 0,AL	Counter 0 MSB
0000:C0B1	B0 0A	MOV AL,0AH	Binary Counter 0 mode 5,Counter Latch
0000:C0B3	E6 33	OUT CMD-PORT-53,AL	
0000:C0B5	E4 30	IN AL,COUNTER-0	Read LSB
0000:C0B7	8A 30	MOV DL,AL	
0000:C0B9	E4 30	IN AL,COUNTER 0	Read MSB
0000:C0BB	8A F0	MOV DH,AL	
0000:C0BD	CC	INT 3	

STEP 1: Connect the gate pin of the selected counter to GND through a tag.

STEP 2: "3AH" is the control word for 8253 with counter 0 in mode 5. Binary counter 0 is selected. Load low order 8-bit count and then high order 8-bit count.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	0

BCD Counter 16-bits
Mode 5
Read / Load LSB followed by MSB
Select Counter 0

STEP 3: "0005H" is the 16-bit count that is loaded in counter 0 simultaneously.

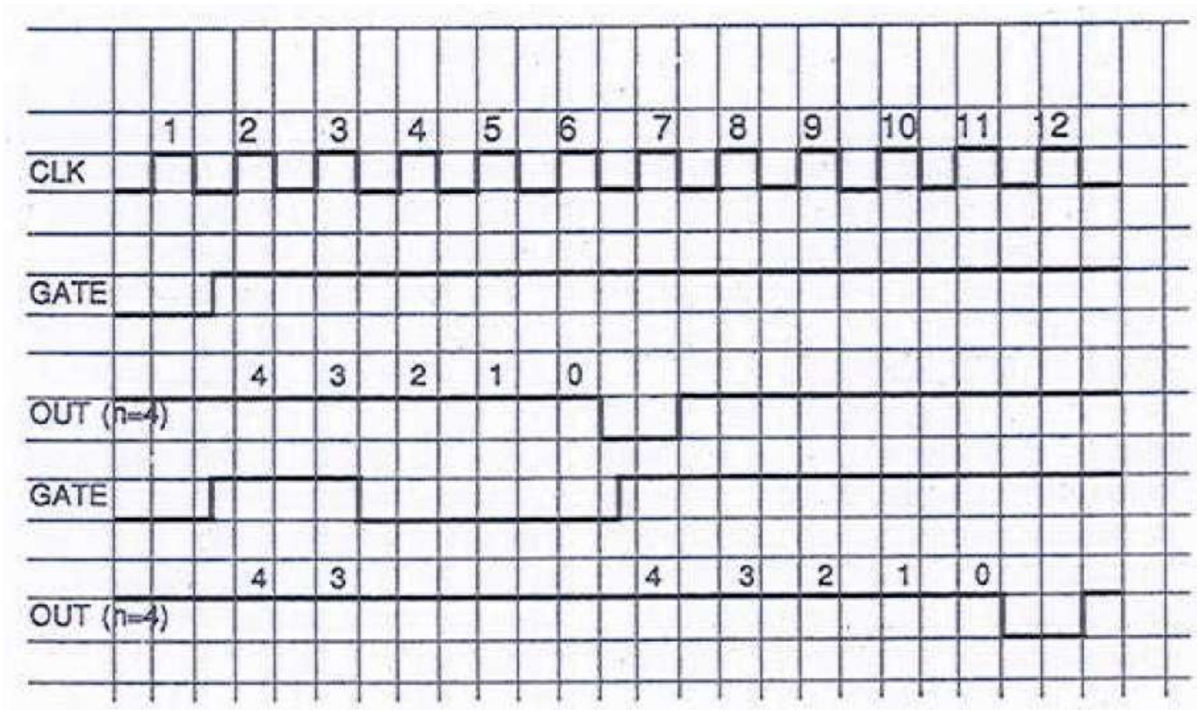
STEP 4: “0AH" is the control word for 8253 with the counter in mode 5. The count is latched and then stored in a reg pair DE.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	0

BCD Counter 16-bits
Mode 5
Counter latching operation
Select Counter 0

STEP 5: Connect the gate pin to VCC through a tag so that at the rising edge of the pulse the counter counts down.

MODE 5 Timing Diagram: Fig 1.6



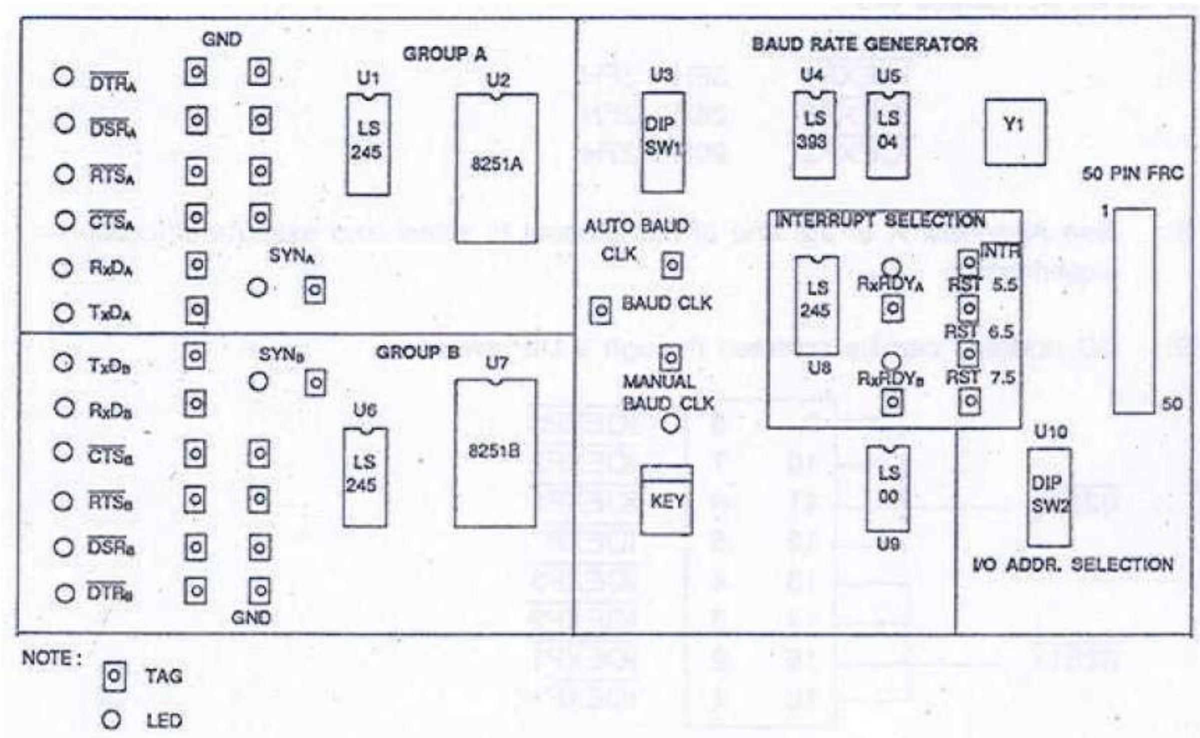
DYNA – SERIAL, STUDY OF 8251

ABOUT DYNA – SERIAL, STUDY OF 8251

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
- It consists of two USARTs (Universal Synchronous Asynchronous Receiver Transmitter) buffers to drive LEDs, interrupt and GND tags.
- This card can help the user explore the various modes of 8251.

DYNA-SERIAL, STUDY OF 8251

COMPONENT PLACEMENT



GENERAL PROCEDURE:

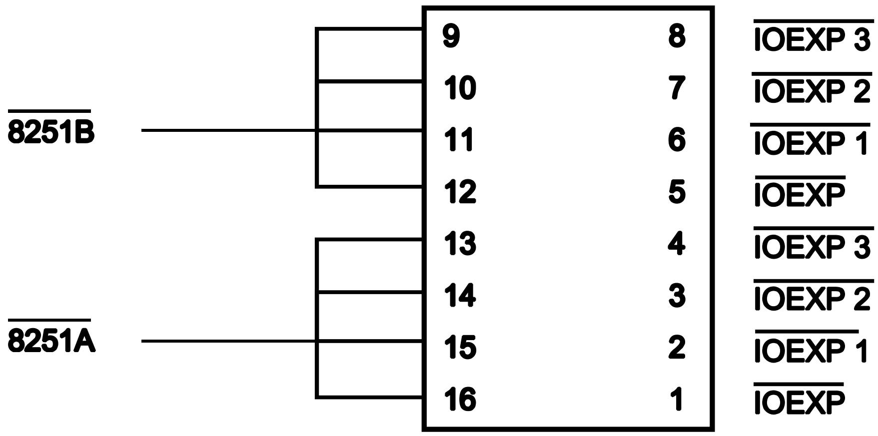
1. Keep the card to the left hand side of the DYNA-86LU kit.
2. Connect DYNA-SER1AL card to the DYNA-86LU kit using the 50 pin FRC cable.
3. Do not connect / remove DYNA-SERIAL to / from DYNA-86LU while the power is on.
4. Each program can be single stepped. Address of each program is given in the listing. Third column contains offset address and the segment address is F000H for all the experiments.
5. The address of the interrupt service routine should be given at 0:38 (IRQ6) 0:34 (IRQ5) and 0:3C (IRQ7).
   All the programs in this manual, use interrupt IRQ7 only.
6. Default I/0 address range for all the experiments is 30H - 37H.

SELECTION	ADDRESS
Data Port	30H
Command Port	31H

7. Other I/O ranges are:

$\overline{\text{IOEXP1}}$	38H - 3FH
$\overline{\text{IOEXP2}}$	28H - 2FH
$\overline{\text{IOEXP3}}$	20H - 27H

8. See Appendix A at the end of this Manual to select & execute and execute different.
9. I/O address can be selected through a DIP switch.



BAUD RATE GENERATION LOGIC:

To select the proper baud rate for serial communication, a DIP switch (SW1) at the top of the card is provided. All the experiments stated, make use of the /16 mode.

/ 64 mode	/ 16 mode
19.2 K	
9600	
4800	19.2 K
2400	9600
1200	4800
600	2400
300	1200

Connect the BAUD CLK to Auto BAUD CLK through a tag or a pulser key is provided to give the BAUD CLK to 8251. The pulser key can be connected to BAUD CLK through a tag. In case of asynchronous and synchronous mode, it is used to observe the data transfer. When a key is pressed once, one clock pulse is transmitted. The LED glows during transmission of each clock pulse.

EXPERIMENT 1:

AIM: Study 8251 in Asynchronous Transmitter mode. Use 8251 of Group A.

Mode command**:**
It is in asynchronous mode. Baud rate factor is selected i.e. 16, character length is 8 bits, parity check is odd, stop bit is 1.

Command word**:**
It is in transmitter mode, $\overline{\text{DTR}}$ is 1 indicates data terminal is ready, $\overline{\text{RTS}}$ is 1 indicates carrier dispatch.

CONDUCTING EXPERIMENT:

			P_8251_EXP-1
0000:C020	B0 5E	MOV AL,5EH	;In asynchronous mode ;Baud rate factor /16 ;Character Length 8-Bit ;Parity Enable, odd Parity ;Stop Bit=1
0000:C022	E6 31	OUT CMD-PORTA,AL	
0000:C024	B0 23	MOV AL,23H	;In transmitter mode ;DTR* is 1,RTS* is 1
0000:C026	E6 31	OUT CMD-PORTA,AL	
0000:C028	B0 55	MOV AL,55H	;Data to be transmitted
0000:C02A	E6 30	OUT DATA -PORTA, AL	
0000:C02C	CC	INT 3	

STEP 1: Connect $\overline{\text{CTS}}$ and $\overline{\text{DSR}}$ to GND with a tag. Unless Clear to Send ($\overline{\text{CTS}}$) and Data Set Receive ($\overline{\text{DSR}}$) is received USART will not transmit the data.

STEP 2: "5EH" is the mode command to initialize 8251 in asynchronous mode. It initializes USART as -

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	0

D1 D0 → Baud rate factor 16
D3 D2 → Character length 8-bits
D5 D4 → Parity check odd, parity enable
D7 D6 → 1.5 stop bits

STEP 3: "23H" is the control word for 8251. It sets 8251 in transmitter mode.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	0

- D0 → Transmission enable
- D1 → Data terminal ready
- D2 → Receiver disable
- D3 → No break characters, so TXD is high
- D4 → Disable error reset
- D5 → Transmission carrier control ON
- D6 → Disable internal reset
- D7 → Disable search for Sync. Char.

The LED for $\overline{RTS}$ will go off.

STEP 4: "55H" Is transmitted as data.

STEP 5: Observe the blinking of the LED at TxD of selected 8251. The LED glows when high bit is transmitted. (Give baud clock manually).

EXERCISE:

Write a program to transmit data continuously and observe the transmitted data on the CRO. Observe the data w.r.t BAUD CLK. Use 8251 of Group B.

EXPERIMENT 2:

AIM: Study 8251 in synchronous transmitter mode. Use 8251 of Group A

Mode command**:**
It is configured in synchronous mode. Character length 5 bits. Parity disable. Sync detection internal. Sync character single.

Command word**:**
It is configured in transmitter mode. $\overline{DTR}$ is 1 indicates data terminal is ready and $\overline{RTS}$ is 1 indicates transmission carrier control ON.
EH is 1 for sync character detection.

CONDUCTING EXPERIMENT:

			P_8251_EXP-3
0000:C060	B0 8C	MOV AL,8CH	;In synchronous mode ;Character length 8 bit ;parity disable ;SYNCH detection internal ;SYNCH character
0000:C062	E6 31	OUT CMD-PORT-A,AL	
0000:C064	B0 0F	MOV AL,0FH	;SYNCH character is programmed
0000:C066	E6 31	OUT CMD-PORTA,AL	
0000:C068	B0 23	MOV AL,23H	;Transmission enable

			;Data terminal ready ;RTS=1
0000:C06A	E6 31	OUT CMD-PORTA,AL	
0000:C06C	B0 45 BACK3:	MOV AL,45H	;Character to be transmitted
0000:C06E	E6 30	OUT DATA-PORTA,AL	
0000:C070	EB FA	JMP BACK 3	

STEP 1: "8CH" is the mode command for 8251. It initializes USART to work in synchronous mode.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	0

- D1 D0 → Synchronous mode
- D3 D2 → Character Length 8 bits
- D5 D4 → Parity disable
- D6 → Internal sync detection
- D7 → Single sync character

STEP 2: "0FH" is the data programmed as a sync character. When transmitter data buffer is empty, this character is sent out till any data is written in the TxD buffer.

STEP 3: "23H' is the command word for 8251, sets it in transmitter mode.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	1

- D0 → Transmission enable
- D1 → Data terminal ready
- D2 → Receiver disable
- D3 → No break characters, so TXD is high
- D4 → Disable error reset
- D5 → Transmission carrier control ON
- D6 → Disable internal reset
- D7 → Disable search for Sync. Char.

STEP 4: "45H" is the data to be transmitted.

STEP 5: Observe the blinking of LED at TxD pin of the selected 8251. LED will glow when high bit is transmitted.

STEP 6: Observe the data on the CRO/DSO. You will find continuous flow of data i.e. data without sync character.

EXERCISE:

Change the value of data and synch characters and observe the waveform.

NOTE: In steps 5 & 6 observe the waveforms w.r.t the BAUD CLK.

EXPERIMENT 3:

AIM: Study 8251 in synchronous receiver mode. Use 8251 of Group A.

Mode command**:**
It is configured in synchronous mode. Character length is 8 bits. Parity enable, parity check even. Sync detection internal, Sync character double.

Command word**:**
It is configured in receiver mode. EH is 1 means enable search for sync character. Receiver enable, data terminal is ready.

CONDUCTING EXPERIMENT:

			P_8251_EXP-4
0000:C050	B0 3C	MOV AL,3CH	;In synchronous mode ;Double sync character ;Character length is 8 bit ;Parity enable, even parity ;Sync detection internal
0000:C052	E6 31	OUT CMD-PORTA,AL	
0000:C054	B0 0F	MOV AL,0FH	;First Sync character
0000:C056	E6 31	OUT CMD-PORTA,AL	
0000:C058	B0 50	MOV AL,50H	;Second Sync Character
0000:C05A	E6 31	OUT CMD-PORTA,AL	
0000:C05C	B0 A7	MOV AL,0A7H	;Enable transmitter and ;Receiver, hunt mode
0000:C05E	E6 31	OUT CMD-PORTA,AL	
0000:C060	B0 55	MOV AL,55AH	;Data to be transmitted
0000:C062	E6 30	OUT DATA PORTA,AL	
0000:C064	E4 31 BACK 4:	IN AL,CMD-PORTA	;Check status word
0000:C066	D0 D8	RCR AL,1	
0000:C068	D0 D8	RCR AL,1	
0000:C06A	73 F8	JNC BACK 4	
0000:C06C	E4 30	IN AL,DATA-PORTA	
0000:C06E	8A D0	MOV DL,AL	
0000:C070	CC	INT 3	

STEP 1: Make $\overline{\text{DSR}}$ & $\overline{\text{CTS}}$ low (SW 2 AND 5 ON)

STEP 2: Short TxD and RXD.

STEP 3: Execute program.

STEP 4: Observe that synA becomes 1 indicating that syncB character is received and RXRDY becomes 1 indicating that it has received a character.

EXERCISE:
Write a program to receive data in synchronous mode of USART using interrupt. Use 8251 of Group B.

EXPERIMENT 4:

AIM: Study 8251A as a transmitter and 8251B as receiver in Synchronous mode.

Mode Command for 8251A**:**
In synchronous mode, character length is 8 bits, parity disable, sync detection internal, sync character single.

Command Word for 8251A**:**
In transmitter mode. $\overline{DTR}$ is 1 means data terminal ready, $\overline{RTS}$ is 1 means carrier dispatch.

Mode Command for 8251B**:**
In synchronous mode, character length is 8 bits, parity disable, sync detection internal, sync character single.

Command Word for 8251B**:**
In receiver mode, $\overline{DTR}$ is 1, means data terminal is ready. $\overline{RTS}$ is 1, means carrier dispatch.

CONDUCTING EXPERIMENT:

			P_8251_EXP-5
0000:C090	B0 8C	MOV AL,8CH	;Synchronous mode ;single sync character ;character length 8 bit ;parity disable ,even parity ;Sync detection internal
0000:C092	E6 31	OUT CMD-PORT A,AL	
0000:C094	90	NOP	
0000:C095	E6 39	OUT CMD-PORTB,AL	
0000:C097	B0 0F	MOV AL,0FH	;Sync character
0000:C099	E6 31	OUT CMD PORT-A,AL	
0000:C09B	90	NOP	
0000:C09C	E6 39	OUT CMD PORTB,AL	
0000:C09E	B0 17	MOV AL,23H	;Transmitter Enable 8255A
0000:C0A0	E6 31	OUT CMD-PORTA,AL	
0000:C0A2	B0 B6	MOV AL,0B6H	;Enable receiver 8255B
0000:C0A4	E6 39	OUT CMD-PORTB,AL	
0000:C0A6	B0 55	MOV AL,55H	;Data to be transmitted
0000:C0A8	E6 30	OUT DATA-PORTA,AL	
0000:C0AA	E4 39 BACK 5:	IN AL, CMD –PORTB	;Check status word 8255B
0000:C0B0	D0 D8	RCR AL,1	
0000:C0B2	D0 D8	RCR AL,1	
0000:C0B4	73 F8	JNC BACK 5	
0000:C0B6	E4 38	IN AL, DATA PORTB	
0000:C0B8	8A D0	MOV DL,AL	
0000:C0BA	CC	INT 3	

STEP 1: 1) Connect TXDA to RXDB.
2) Make SW6 on.
3) Connect SYNA and SYNB tags using links.

STEP 2: "8CH" is the mode command for 8251A and 8251B.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	0

Synchronous mode
Character Length 8 bits
Parity disable
Don't care
Internal sync detection
Single sync character

STEP 3: "0FH" is the sync character for 8251A and 8251B.

STEP 4: "23H" is the command word for 8251A.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	1

Transmission enable
Data terminal ready
Receiver disable
No break characters
Disable error reset
Transmission carrier control ON
Disable internal reset
Disable search for Sync. Character

STEP 5: "B6H" is the command word for 8251B.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	1	1	0

Transmission enable
Data terminal ready
Receiver disable
No break characters
Disable error reset
Transmission carrier control ON
Disable internal reset
Disable search for Sync. Character

STEP 6: “55H” is the data to be transmitted.

STEP 7: Read the status of 8251B and rotate right twice through carry and check if receiver is ready, if ready, in data or else read the status again.

PROCEDURE:
1) Execute the program.
2) Observe RXRDYB glows indicating that it has received a character.

EXERCISE:

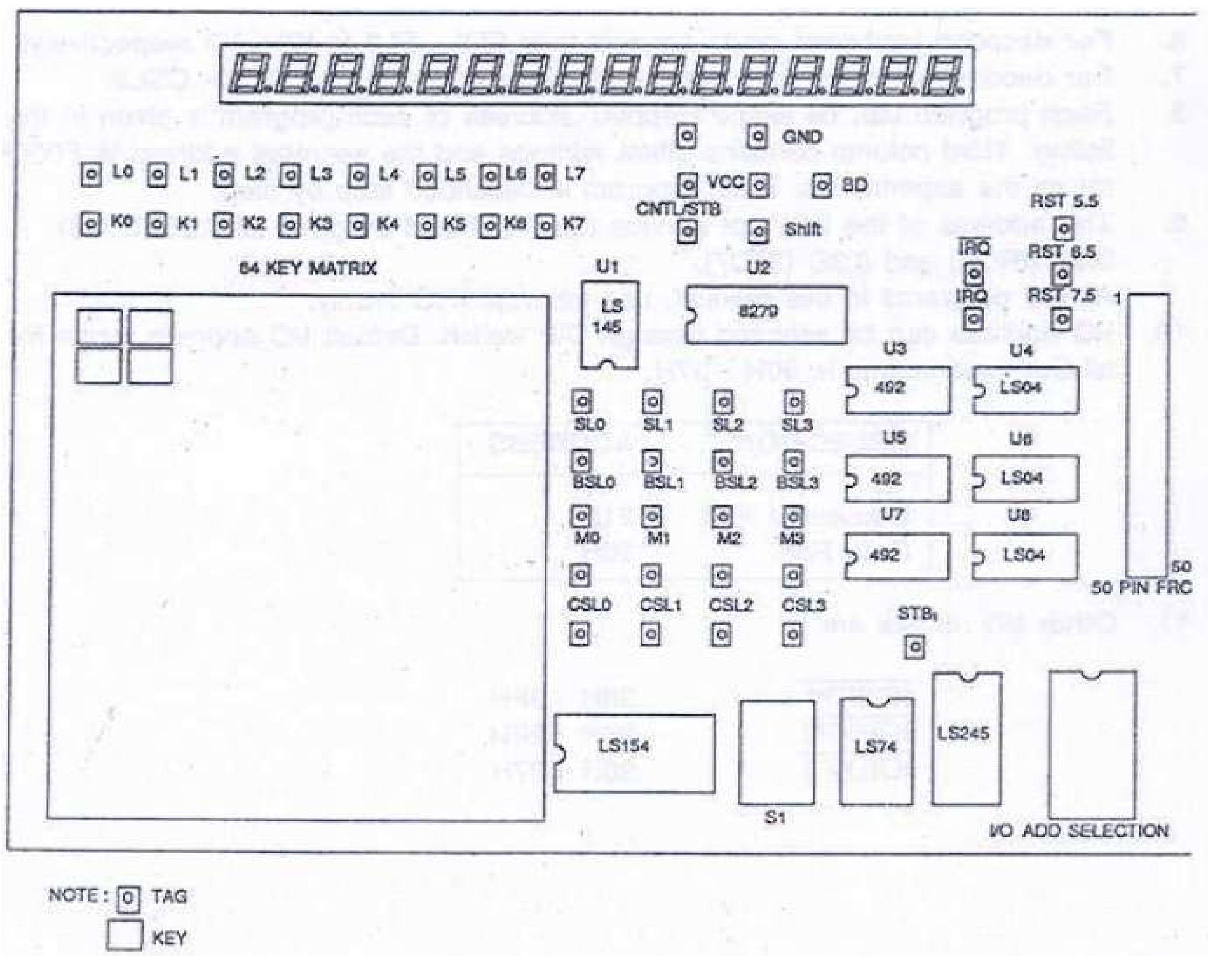
1) Write a program for synchronous mode of USART, so that 8251A will receive data from 8251B.
2) Change sync character for receiver USART and observe the effect.

DYNA – KBDISP, STUDY OF 8279

ABOUT DYNA – KBDISP, STUDY OF 8279

- This interface card is connected through a 50 pin FRC cable to DYNA-86LU kit.
- It consists of buffers, one 8279, VCC, GND tags and LEDs.

DYNA-KBDISP, STUDY OF 8279 COMPONENT PLACEMENT



APPLICATIONS:

Microcomputer I/O device, 64 contact key input device for such items as electronic cash registers, dual 8 or single 16 alphanumeric display.

GENERAL PROCEDURE:

1. Keep the card to the left side of the DYNA-86LU kit.
2. Connect DYNA-KBDISP to DYNA-86LU kit using the 50 pin FRC cable.
3. Do not connect / remove DYNA-KBDISP card to from DYNA-86LU when the power is on.
4. For encoded keyboard mode connect tags K0-K7 to L0-L7 respectively.

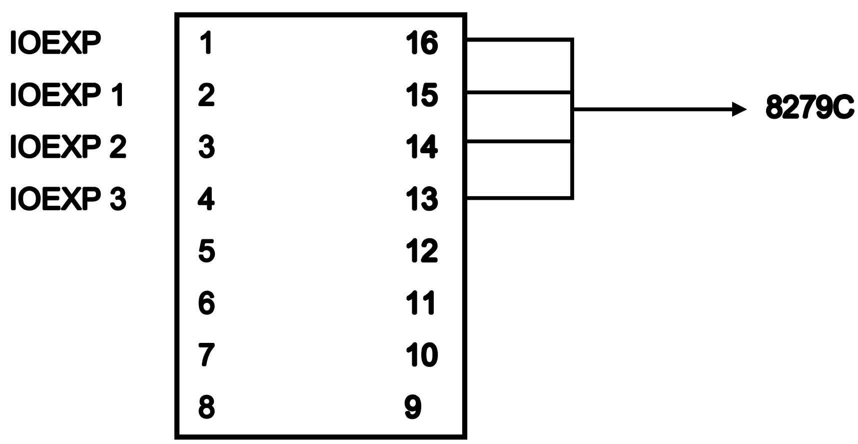
5. For encoded display mode connect the tags SL0-SL3 to BSL0-BSL3 and M0-M3 to CSL0-CSL3.
6. For decoded keyboard mode connect tags SL0-SL3 to K0-K3 respectively.
7. For decoded display mode connect the tags SL0-SL3 to CSL0-CSL3.
8. Each program can be single stepped. Address of each program is given in the listing. Third column contains offset address and the segment address is F000H for all the experiments. Each program is described step by step.
9. The address of the interrupt service routine should be given at 0:38 (IRQ6) 0:34 (IRQ5) and 0:3C (IRQ7).
   All the programs in this manual, use interrupt IRQ 7 only.
10. I/O address can be selected through DIP switch. Default I/O address range for all the experiments is 30H - 37H.

SELECTION	ADDRESS
Data Port	30H
Command Port	31H

11. Other I/O ranges are:

$\overline{\text{IOEXP1}}$	38H - 3FH
$\overline{\text{IOEXP2}}$	28H - 2FH
$\overline{\text{IOEXP3}}$	20H - 27H

12. I/O address can be selected through a DIP switch:



13. See Appendix A at the end of this Manual to select and execute different experiments:

INTRODUCTION TO VARIOUS MODES:

In encoded (8 x 8 key) mode, the counter provides binary count that must be externally decoded to provide scan lines for keyboard and display. Scan lines are active high outputs in this mode.

In decoded (4 x 8 key) mode, the scan counter decodes the least significant two bits and provides decoded 1 of 4 scan so no external decoder is required. Only first four characters in the display RAM are displayed.
In the decoded mode the scan lines are active low outputs.

In 2 key lockout mode, when 2 keys are pressed together both the data are locked and if 2 keys are pressed simultaneously then the code of the key that is pressed last is stored in FIFO.

In N key rollover mode, when N number of keys are pressed together all the codes of the pressed keys are stored in the FIFO simultaneously. The code of the key that is pressed last is stored in the FIFO.

EXPERIMENT 1:

AIM: Keyboard is in encoded scan – 2 key lockout mode.

CONDUCTING EXPERIMENT:

			P_8279_Exp-1
0000:C000	B0 00	MOV AL,00H	;Encoded scan keyboard ;Two key lockout
0000:C002	E6 31	OUT CMD-PORT-79,AL	
0000:C004	E4 31 DD1:	IN AL,CMD-PORT-79	
0000:C006	24 07	AND AL,07H	;The status word is anded ;with 07H to check if any data is entered in FIFO.
0000:C008	74 FA	JZ DD1	
0000:C00A	E4 30	IN AL,DATA PORT-79	
0000:C00C	BB 0002	MOV BX,02H	;2 Digits in data field
0000:C00E	0E E8 BB7E	CALL FAR F000:0D5E	;Display contents of AL
0000:C010	EB EF	JMP DD1	

STEP 1: Make connections as mentioned below: L0-L7 to K0-K7.

STEP 2: "00H" is the mode set command for 8279. Keyboard is in encoded display keyboard mode – 2 key lookout.

STEP 3: Status of 8279 is read to check if any key is pressed. If no key is pressed, then jump to read the status or else read the data and store that in reg AL. The data format of the scanned keyboard is as follows-

CNTL	SHIFT		SCAN			RETURN	

STEP 4: A routine is called to display the data from reg. AL

EXPLANATION: When a key is pressed the corresponding data is displayed in the data field. For e.g. If the first key is pressed then "C1H" is displayed. The data format can be explained as below-

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	1

Encoded return input
Scan timing signals (S_2, S_1 & S_0)
Shift
CNTL

If two keys are pressed together then there is no data displayed in the data field.

EXPERIMENT 2:

AIM: Keyboard is in encoded scan – n key rollover mode.

CONDUCTING EXPERIMENT:

			P_8279_Exp-2
0000:C020	B0 02	MOV AL,02H	;Encoded scan keyboard ;n key rollover mode
0000:C022	E6 31	OUT CMD_PORT_79,AL	
0000:C024	E4 31 DD2:	IN AL,CMD_PORT_79	
0000:C026	24 07	AND AL,07H	;The status word is anded; with 07h to check if the; data is entered in FIFO.
0000:C028	74 FA	JZ DD2	
0000:C02A	E4 30	IN AL,DATA-PORT_79	
0000:C02C	BB 0002	MOV BX,02H	;2 digits in data field
0000:C02F	0E E8 BBC9	CALL FAR F000:0D5E	;Display contents of AL
0000:C034	EB EF	JMP DD2	

STEP 1: Make the connections as mentioned below:
L0 - L3 to K0 - K7.

STEP 2: "02H" is the mode set command for 8279. Keyboard is in encoded display keyboard mode - N key rollover.

STEP 3: Status of 8279 is read to check if any key is pressed. If no key is pressed, then jump to read the status again or else read the data and store it in reg AL.

STEP 4: A routine is called to display the data from reg. AL

EXPLANATION: When a key is pressed the corresponding data is displayed in the data field. For e.g. If the first key is pressed then "C1H" is displayed. The data format can be explained as below-

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	1

→ Encoded return input
→ Scan timing signals (S_2, S_1 & S_0)
→ Shift
→ CNTL

If N keys are pressed together then the respective data will be displayed simultaneously, but finally the data of the last key pressed remains in the data field.

EXPERIMENT 3:

AIM: Keyboard is in decoded scan – 2 key lockout mode.

CONDUCTING EXPERIMENT:

			P_8279_Exp-3
0000:C060	B0 01	MOV AL,01H	;Decoded scan keyboard ;2-key lockout mode
0000:C062	E6 31	OUT CMD_PORT79,AL	
0000:C064	E4 31 DD3:	IN AL,CMD_PORT79	
0000:C066	24 07	AND AL,07H	;The status word is anded with 07H to check if any data is entered in FIFO
0000:C068	74 FA	JZ DD3	
0000:C06A	E4 30	IN AL,DATA PORT_79	
0000:C06C	BB 0002	MOV BX,02H	;2 digits in data field
0000:C06F	0E E8 BB54	CALL FAR F000:0D5E	;Display contents of AL ;Data Field
0000:C074	EB EF	JMP DD3	

STEP 1: Make the connections as mentioned below:
K0 - K3 to SL0 - SL3.

STEP 2: "01H" is the mode set command for 8279. Keyboard is in decoded display keyboard mode – 2 key lockout.

STEP 3: The status of 8279 is read to check if any key is pressed. If no key is pressed then jump to read the status or else read the data and store it in reg A.

EXPLANATION: Same as in experiment no.1

EXPERIMENT 4:

AIM: Keyboard is in decoded scan n – key rollover mode.

CONDUCTING EXPERIMENT:

			P_8279_Exp-4
0000:C090	B0 03	MOV AL,03H	;Decoded scan keyboard ;N key rollover mode
0000:C092	E6 31	OUT CMD_PORT_79,AL	
0000:C094	E4 31 DD4:	IN AL,CMD_PORT_79	
0000:C096	24 07	AND AL,07H	;The status word is anded ;with 07H to check if any data is entered in FIFO.
0000:C098	74 FA	JZ DD4	
0000:C09A	E4 30	IN AL,DATA_PORT_79	

0000:C09C	BB 0002	MOV BX,02H	;2 Digits in data field
0000:C09F	0E E8 BB3F	CALL FAR F000:0D5E	;Display contents of AL
0000:C0A4	EB EF	JMP DD4	

STEP 1: Make the connection as mentioned below:
K0 - K3 to SL0 - SL3.

STEP 2: "03H" is the mode set command for 8279. Keyboard is in decoded display keyboard mode - N key rollover.

STEP 3: The status of 8279 is read to check if any key is pressed. If no key is pressed then jump to read the status or else read the data and store it in reg AL.

STEP 4: A routine is called to display the data from register AL.

EXPLANATION: Same as in experiment no.2

EXPERIMENT 5:

AIM: Keyboard is in encoded scan sensor matrix mode.
In sensor matrix mode there is no debounce logic. In this mode the data on the return lines is entered directly to the row of the sensor RAM that corresponds to the row in the matrix being scanned. There-fore, each switch position maps directly to the sensor RAM position. SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279. There is a command to select the row of the matrix to be read and that is known as read FIFO command.

CONDUCTING EXPERIMENT:

			P_8279_Exp-5
0000:6000	B0 04	MOV AL,04H	;Encoded scan keyboard ;Sensor matrix mode
0000:6002	E6 31	OUT CMD_PORT_79,AL	
0000:6004	E4 31 DD5:	IN AL,CMD _PORT_79	
0000:6006	24 07	AND AL,07H	;The status word is anded with 07H to check if any data is entered in FIFO.
0000:6008	74 FA	JZ DD5	
0000:600A	B0 41	MOV AL,41H	;First row of keyboard is to be read
0000:600C	E6 31	OUT CMD_PORT_79,AL	
0000:600E	E4 30	IN AL,DATA_PORT_79	
0000:6010	BB 0002	MOV BX,02H	;2 Digits in data fields
0000:6013	0E E8 BB26	CALL FAR F000:0D5E	Display contents of AL.
0000:6018	EB EB	JMP DD5	

STEP 1: Make the connections as mentioned below:
L0 - L7 to K0 - K7

STEP 2: "04H" is the mode set command for 8279. Keyboard is in encoded display sensor mode.

STEP 3: The status of 8279 is read to check if any key is pressed. If no key is pressed then jump to read the status or else give read FIFO command to specify the address of the row, read the data and store in reg AL.

The sensor matrix keyboard data format is as follows:

RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

CNTL and SHIFT inputs are ignored.

STEP 4: “41H” is the read FIFO command.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	1

Encoded return input
Scan timing signals (S_2, S_1 & S_0)
Shift
CNTL

STEP 5: A routine is called to display the data from register AL.

EXPLANATION: After executing the program 00 is displayed in the data field. Now when a key is pressed the corresponding data is displayed in the data field. If the program is in loop then the data will be displayed in the data field every time when a key is pressed. For e.g. If the first key is pressed then 01 is displayed in the data field. If the next key is pressed then the corresponding data is displayed.
The data will be displayed according to the data format shown in step 3.

EXPERIMENT 6:

AIM: Keyboard is in decoded scan sensor matrix mode.

CONDUCTING EXPERIMENT:

			P_8279_Exp-6
0000:6020	B0 05	MOV AL,05H	;Decoded scan key board ;Sensor matrix keyboard
0000:6022	E6 31	OUT CMD_PORT_79,AL	
0000:6024	E4 31DD6:	IN AL,CMD_PORT_79	
0000:6026	24 07	AND AL,07H	;The status word is added ;with 07H to check if any ;data is entered In FIFO.
0000:6028	74 FA	JZ DD6	
0000:602A	B0 41	MOV AL,41H	;First row of keyboard ;is to be read
0000:602C	E6 31	OUT CMD_PORT_79,AL	
0000:602E	E4 30	IN AL.,DATA_PORT_79	

0000:6030	BB 0002	MOV BX,02H	;2 Digits in data field
0000:6033	0E E8 BB0D	CALL FAR F000:0D5E	;Display contents of AL
0000:6038	EB EB	JMP DD6	

STEP 1: Make the connections as mentioned below:
K0 - K3 to SL0 - SL3.

STEP 2: "05H" is the mode set command for 8279. Keyboard is in decoded display, sensor mode.

STEP 3: The status of 8279 is read to check if any key is pressed. If no key is pressed then jump to read the status or else read the data.

STEP 4: "41H" is the read FIFO command.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	1

First row of the matrix is selected
Don't care
Disable auto-Increment mode
Defines for read FIFO command

EXPERIMENT 7:

AIM: Keyboard is in strobed input, decoded display scan mode. Give the strobe pulse (rising edge) through key S1.
In strobed input mode, data is entered to the FIFO from the return lines. Data is entered by the rising edge of a CNTUSTB line pulse. Data can come from another end coded keyboard or simple switch matrix.
Return lines can also be used as a general purpose stored input, When a key is pressed and the strobe pulse is given, (the pulse is not in synchronization with the scan line pulses, so the pulses are given continuously through the key S1) Data is entered to FIFO from return lines.

CONDUCTING EXPERIMENT:

			P_8279_Exp-7
0000:6040	B0 07	MOV AL,07H	;Decoded display scan mode
0000:6042	E6 31	OUT CMD_PORT_79,AL	
0000:6044	E4 31 D7:	IN AL,CMD_PORT_79	
0000:6046	24 07	AND AL,07H	;the status word added ;with 07H to check if ;data is entered in FIFO
0000:6048	74 FA	JZ D7	
0000:604A	E4 30	IN AL, DATA_PORT_79	
0000:604C	BB 0002	MOV BX,02H	;2 Digits in data field
0000:604F	0E E8 BAF8	CALL FAR F000:0D5E	;Display contents of AL
0000:6054	46AE EB EF	JMP D7	

STEP 2: "07H" is the control word for 8279 keyboard in strobed input decoded display scan mode.

STEP 3: Read status word, to check if any key is pressed. If any key is pressed then read the data or else jump to read the status word again.

STEP 4: A routine is called to display the data from register AL.

EXPERIMENT 8:

AIM: Display is in 8-8 bit character display, left entry decoded mode.
In this mode the codes of the characters to be displayed are stored from memory location DATA_79 in the listing given below. The data displayed is "DYNA". In left entry the first character is displayed on the left most position, the next character is displayed in the next position and so on. In this program the display is steady.

CONDUCTING EXPERIMENT:

			P_8279_Exp-8
0000:C000	BC 0700	MOV SP,700H	
0000:C003	B1 40	MOV CL,04H	
0000:C005	B0 01	MOV AL,01H	;8*8 BIT CHARACTER LEFT ;ENTRY DECODED MODE
0000:C007	E6 31	OUT CMD_PORT_79,AL	
0000:C009	8C C8	MOV AX,CS	
0000:C00B	8E D8	MOV DS,AX	;DATA SEG INTIALISED
0000:C00D	2E 8B 1E 46B0r	MOV BX,WORD PTR DATA_79	;BX POINTER DATA TO BE DISPLAYED
0000:C010	8A 07 E2:	MOV AL,[BX]	
0000:C012	E6 30	OUT DATA_PORT_79,AL	
0000:C014	0E E8 BC59	CALL FAR DELAY	;DELAY
0000:C017	43	INC BX	
0000:C018	FE C9	DEC CL	
0000:C01A	75 F3	JNZ E2	
0000:C01C	CC	INT 3	

DISPLAY SUBROUTINE:

DATA TO DISPLAY "DYNA"

0000:C0A0	E6
0000:C0A1	EC
0000:C0A2	46
0000:C0A3	7E
0000:C0A4	00
0000:C0A5	00
0000:C0A6	00
0000:C0A7	00

DELAY SUBROUTINE:

0000:4000	PUSH CX
0000:4001	PUSH BX
0000:4002	MOV BX,00F0H
0000:4005	MOV CX,00FFH
0000:4008	LOOP 4008
0000:400A	DEC BX
0000:400B	JNZ 4005
0000:400D	POP BX
0000:400E	POP CX
0000:400F	RET

STEP 1: Make the connections as mentioned below:
SL0 – SL3 to CSL0 - CSL3.

STEP 2: "01H" is the mode set command for 8279. The display is in 8-8 bit character left entry mode.

STEP 3: The data stored from memory location DATA_79 in the listing is read and displayed.

EXERCISE: Write a program for 8279 display in 8-8 bit character display left entry encoded mode.

EXPERIMENT 9:

AIM: 8279 display is in 8-8 bit character display, right entry decoded mode.
In this mode the codes of the characters to be displayed are stored from memory location DATA_79 in the listing given below. The data displayed is "DYNALAB" in right entry the first character is displayed in the right most position. When the next character comes, the first is shifted to its left and the second character is displayed in the right most position and so on, thus it keeps on shifting. This program is for flashing display. In the following program, the characters are displayed once followed by blanking of display.

CONDUCTING EXPERIMENT:

			P_8279_Exp-9
0000:C090	BC 0700	MOV SP,700H	
0000:C093	B0 11	M0V AL,11H	;8*8 Bit character right ;Entry decoded mode
0000:C095	E6 31	OUT CMD_PORT_79,AL	
0000:C097	B0 90E5:	MOV AL,90H	;Write disp RAM first location
0000:C099	E6 31	OUT CMD_PORT_79,AL	
0000:C09B	B1 04	MOV CL,04H	
0000:C09D	8C C8	MOV AX,CS	
0000:C09F	8E D8	MOV DS,AX	;Data seg initialized
0000:C0A1	2E 8B 1E 46B0r	MOV BX, WORD_PTR DATA_79	;BX pointer data ;to be displayed
0000:C0A4	8A 07 E3:	MOV AL,[BX]	
0000:C0A6	E6 31	OUT DATA_PORT_79,AL	
0000:C0A8	43	INC BX	
0000:C0A9	FE C9	DEC CL	
0000:C0AB	75 F7	JNZ E3	
0000:C0AD	0E E8 BC2B	CALL FAR DELAY	;Delay
0000:C0B0	B0 90	MOV AL,90H	;write disp RAM first location
0000:C0B2	E6 31	OUT CMD_PORT_79,AL	
0000:C0B4	B1 04	MOV CL,04H	
0000:C0B6	8A 07 E4:	MOV AL,[BX]	

0000:C0B8	E6 30	OUT DATA_PORT_79,AL	
0000:C0BA	43	INC BX	
0000:C0BB	FE C9	DEC CL	
0000:C0BD	75 F7	JNZ E4	
0000:C0BF	0E E8 BC18	CALL FAR DELAY	;Delay
0000:C0C2	EB CF	JMP E5	
0000:C0C4	CC	INT 3	

DISPLAY SUBROUTINE:

DATA TO DISPLAY "DYNA"

0000:C0A0	E6
0000:C0A1	EC
0000:C0A2	46
0000:C0A3	7E
0000:C0A4	00
0000:C0A5	00
0000:C0A6	00
0000:C0A7	00

DELAY SUBROUTINE:

0000:4000	PUSH CX
0000:4001	PUSH BX
0000:4002	MOV BX,00F0H
0000:4005	MOV CX,00FFH
0000:4008	LOOP 4008
0000:400A	DEC BX
0000:400B	JNZ 4005
0000:400D	POP BX
0000:400E	POP CX
0000:400F	RET

STEP 1: Make the connections as mentioned below:
SL0 - SL3 to CSL0 - CSL3.

STEP 2: "11H" is the mode set command for 8279. The display is in 8-8 bit character display, left entry mode.

STEP 3: The data stored from memory location DATA_79 in the listing is read and displayed.

EXERCISE: Write a program for 8279 display in 8-8 bit character display, right entry encoded mode.

EXPERIMENT 10:

AIM: 8279 display is in 16-8 bit characters display, right entry encoaded mode.
In this mode the code of the characters to be displayed are stored from memory location DATA_79_NUM in the listing given below. In right entry the first character is displayed in the rightmost position. When the next character comes the first is shifted to its left and the second character is displayed in the right most position and thus it keeps on shifting. This program is for rolling display.

CONDUCTING EXPERIMENT:

			P_8279_Exp-10
0000:6000	BC 0700	MOV SP,700H	
0000:6003	B0 18	MOV AL,18H	
0000:6005	E6 31	OUT CMD_PORT_79,AL	
0000:6007	8C C8	MOV AX,CS	

0000:6009	8E D8	MOV DS,AX	
0000:600b	2E 8B 1E 4715r E6:	MOV BX,WORD_PTR DATA_79,AL	
0000:600E	B1 10	MOV CL,10H	
0000:6010	8A 0 E7:	MOV AL,[BX]	
0000:6012	E6 30	OUT DATA_PORT_79,AL	
0000:6014	0E E8 BBEC	CALL FAR DELAY	
0000:6017	43	INC BX	
0000:6018	FE C9	DEC CL	
0000:601A	75 F3	JNZ E7	
0000:601C	EB EA	JMP E6	

DISPLAY SUBROUTINE:

DATA TO DISPLAY "DYNA"

0000:C020	0A
0000:C021	B6
0000:C022	F4
0000:C023	6C
0000:C024	DC
0000:C025	DE
0000:C026	70
0000:C027	FE
0000:C028	0A
0000:C029	B6
0000:C02A	F4
0000:C02B	6C
0000:C02C	DC
0000:C02D	DE
0000:C02E	70
0000:C02F	FE
0000:C030	00

DELAY SUBROUTINE:

0000:4000	PUSH CX
0000:4001	PUSH BX
0000:4002	MOV BX,00F0H
0000:4005	MOV CX,00FFH
0000:4008	LOOP 4008
0000:400A	DEC BX
0000:400B	JNZ 4005
0000:400D	POP BX
0000:400E	POP CX
0000:400F	RET

STEP 1: Make the connections as mentioned below**:**
SL0 - SL3 to BSL0 - BSL3 & M0 - M3 to CSL0 - CSL3.

STEP 2: "18H" is the mode set command for 8279. The display is in 8-8 bit character display, right entry mode.

STEP 3: The data from memory location DATA_79_NUM is read and displayed.

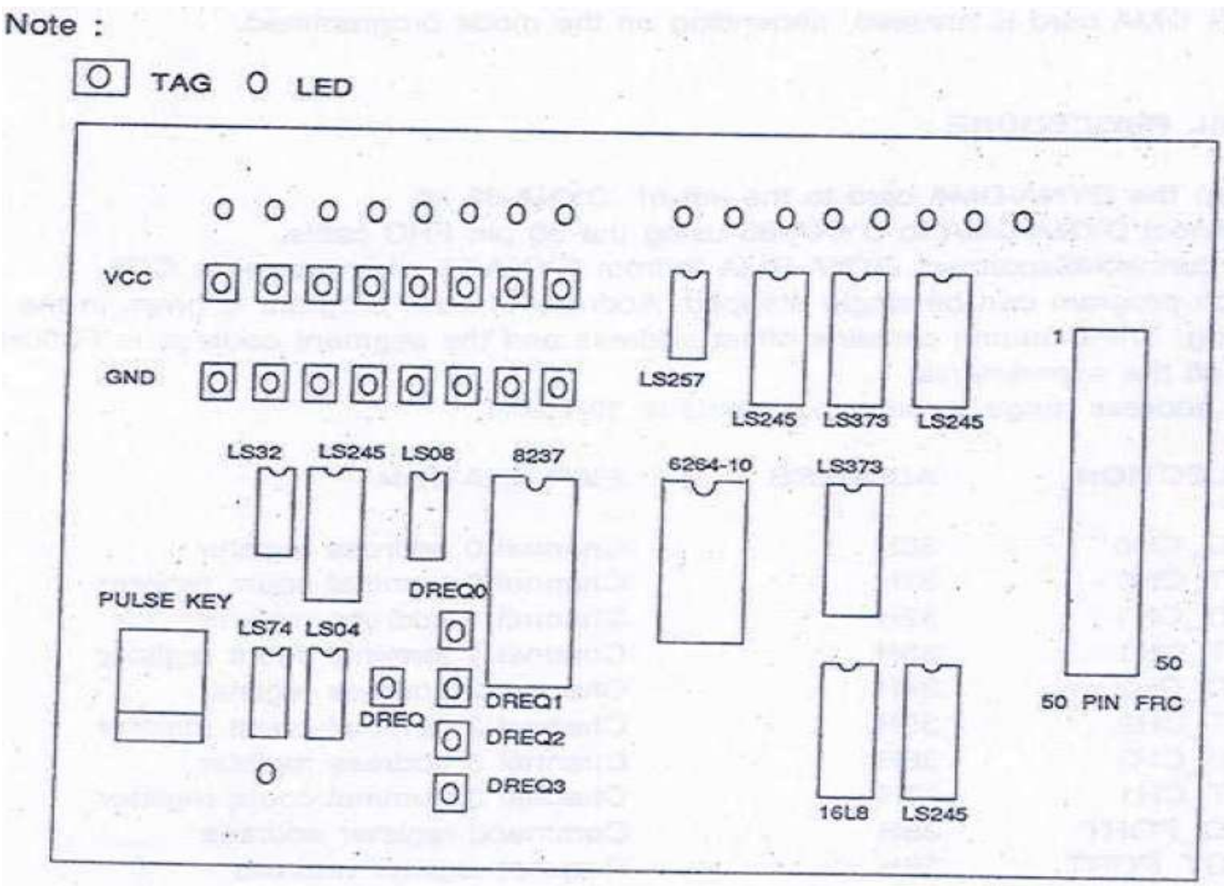
EXERCISE: Write a program to set 8279 display in 16-8 bit character display in left entry decoded mode.

DYNA – DMA, STUDY OF 8237

ABOUT DYNA – DMA, STUDY OF 8237

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
- It consists of 8237-A, RAM, buffers to drive LEDs, VCC and GND tags, LEDs.

DYNA-DMA, STUDY OF 8237 COMPONENT PLACEMENT:



ABOUT 8237:

The 8237 multimode direct memory access (DMA) controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory to memory transfer capability is also provided.

APPLICATIONS:

8237 is used as DMA controller with floppy disk controller, high speed communication controller, etc.

The DYNA-DMA 8237 Study-card demonstrates the use of 8237- High performance DMA CONTROLLER to transfer data in blocks or 1 byte at a time, when the key provided on DYNA-DMA 8237 study-card is pressed, depending on the mode programmed.

GENERAL PROCEDURE:

1. Keep the DYNA-DMA 8237 study-card to the left of DYNA-86LU kit.
2. Connect DYNA-DMA to DYNA-86LU using the 50 pin FRC cable.
3. Do connect/disconnect DYNA-DMA to/from DYNA-86LU only when power is OFF.
4. Each program can be single stepped. Address of each program is given in the listing. Third column contains offset address and the segment address is F000H for all the experiments.
5. I/O address range for all the experiments is 30H - 37H.

SELECTION	ADDRESS	EXPLANATION
ADD_CH0	30H	Channel 0 address register
CNT CH0	31H	Channel 0 terminal count register
ADD_CH1	32H	Channel 1 address register
CNT_CH1	33H	Channel 1 terminal count register
ADD_CH2	34H	Channel 2 address register
CNT CH2	35H	Channel 2 terminal count register
ADD_CH3	36H	Channel 3 address register
CNT_ CH1	37H	Channel 3 terminal count register
CMD_PORT	38H	Command register address
RQST PORT	39H	Request register address
MODE_PORT	3BH	Mode register address
F_F RST	3CH	FIRST/LAST FLIP-FLOP clear address
MSR_CLR	3DH	Master dear address
CLR_MSK	3EH	Clear mask register address
MASK_PORT	3FH	Mask register address

Enter the programs at the specified addresses…

6. See Appendix A at the end of this Manual to select and execute the different experiments.

EXPERIMENT 1:

AIM: To study-8237 in DMA read mode (memory to I/O) - Single transfer mode.

PROCEDURE:

STEP 1: Connect DREQ2to DREQ using a link.

STEP 2: Connect DACK to DACK2 using a shorting link

STEP 3: Store data in memory locations 4000:4C60H TO 4000:4C6AH to be transferred to I/O.

STEP 4: Execute the program.

STEP 5: Generate DMA request using pulser key on the DYNA DMA kit. The data stored at memory locations 4000:4C60H to 4000:4C6AH will be transferred to I/O and port LEDs will glow as per the data transferred.

CONTROL BYTES USED:

1. Master Clear: Data transferred to the 8237 is immaterial in this case. Master Clear command clears command, status, request, temporary registers and internal First/ Last Flip/Flop. The mask register is set.

2. Command Byte:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Memory to memory disable
Channel 0 addr. hold disable
Controller enable
Normal timing
Fixed priority
Late write selection
DREQ sense active high
DACK sense active low

3. Mode Byte:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

Channel 2 select
Read transfer
Auto initialization enable
Address Increment select
Single mode select

4. Mask Byte: Clear masks on all DMA request by outputting on 3EH data transferred is immaterial.

5. Reset First/Last Flip/Flop: Reset First/Last Flip/Flop by outputting a 3CH data transferred is immaterial.

PROGRAM:

			P_8237_Exp-1
0000:C000	B0 00	MOV AL,00H	
0000:C002	E6 3D	OUT MSR_CLR,AL	
0000:C004	E6 3D	OUT MSR_CLR,AL	
0000:C006	E6 3D	OUT MSR_CLR,AL	
0000:C008	E6 3D	OUT MSR_CLR,AL	
0000:C00A	B0 00	MOV AL,00H	
0000:C00C	E6 38	OUT CMD_PORT,AL	;Memory-memory disabled
0000:C00E	B0 5A	MOV AL,5AH	
0000:C00F	E6 3B	OUT MODE_PORT,AL	
0000:C010	B0 0F	MOV AL,0FH	
0000:C012	E6 3F	OUT MASK_PORT,AL	
0000:C014	B0 04	MOV AL,04H	
0000:C016	E6 3A	OUT MASK_SET_RST,AL	;Mask channel 0
0000:C018	B0 05	MOV AL,05H	

0000:C01A	E6 3A	OUT MASK_SET_RST,AL	;Mask channel 1
0000:C01C	B0 02	MOV AL,02H	
0000:C01E	E6 3A	OUT MASK_SET_RST,AL	;Unmask channel 2
0000:C020	B0 07	MOV AL,07H	;Mask channel3
0000:C022	E6 3A	OUT MASK_SET_RST,AL	
0000:C024	B0 00	MOV AL,00H	
0000:C026	E6 3C	OUT F_F_RST,AL	;Clear byte pointer flip flop
0000:C028	B0 60	MOV AL,60H	
0000:C02A	E6 34	OUT ADD_CH2,AL	
0000:C02C	B0 4C	MOV AL,4CH	
0000:C02E	E6 34	OUT ADD_CH2,AL	;Start of address
0000:C030	B0 0A	MOV AL,0AH	
0000:C032	E6 35	OUT CNT_CH2,AL	
0000:C034	B0 00	MOV AL,00H	
0000:C036	E6 35	OUT CNT CH2,AL	;No of bytes count 000AH
0000:C038	E6 30	OUT ADD_CH0,AL	;clear unused channels address &
0000:C03A	E6 30	OUT ADD_CH0,AL	;Count register
0000:C03C	E6 31	OUT CNT_CH0,AL	
0000:C03E	E6 31	OUT CNT_CHO,AL	
0000:C040	E6 32	OUT ADD_CH1,AL	
0000:C042	E6 32	OUT ADD_CH1,AL	
0000:C044	E6 33	OUT CNT_CH1,AL	
0000:C046	E6 33	OUT CNT_CH1,AL	
0000:C048	E6 36	OUT ADD_CH3,AL	
0000:C04A	E6 36	OUT ADD_CH3,AL	
0000:C04C	E6 37	OUT CNT_CH3,AL	
0000:C04E	E6 37	OUT CNT_CH3,AL	
0000:C050	CC	INT 3	

EXPERIMENT 2:

AIM: To study-8237 in DMA write mode (I/O to memory) - Block transfer mode.

PROCEDURE:

STEP 1: Connect DREQ2 to DREQ using a link.
Connect DREQ0, DREQ1 & DREQ3 to GND.

STEP 2: Connect DACK to DACK2 using a shorting link.

STEP 3: Short the input port data lines using links to set the data to be transferred to Logic 0 and keep it open for logic 1.

STEP 4: Execute the program.

STEP 5: Generate DMA request using pulser key. The data at the input port will be transferred to the memory locations 4000:4C00H to 4000:4C0AH.

CONTROL BYTES USED:

1. Master Clear: Data transferred to the 8237 is immaterial in this case. Master Clear command clears command, status, request, temporary registers and internal First/ Last Flip/Flop. The mask register is set.

2. Command Byte:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

- D0 → Memory to memory disable
- D1 → Channel 0 addr. hold disable
- D2 → Controller enable
- D3 → Normal timing
- D4 → Fixed priority
- D5 → Late write selection
- D6 → DREQ sense active high
- D7 → DACK sense active low

3. Mode Byte:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	1	0

- D1 D0 → Channel 3 select
- D3 D2 → Write transfer
- D4 → Auto initialization enable
- D5 → Address Increment select
- D7 D6 → Block mode select

4. Mask Byte: Clear masks on all DMA request by outputting on 3EH data transferred is immaterial.

5. Reset First/Last Flip/Flop: Reset First/Last Flip/Flop by outputting a 3CH data transferred is immaterial.

PROGRAM:

			P_8237_Exp-2
0000:C052	B0 00	MOV AL,00H	
0000:C054	E6 3D	OUT MSR_CLR,AL	
0000:C056	E6 3D	OUT MSR_CLR,AL	
0000:C058	E6 3D	OUT MSR_CLR,AL	
0000:C05A	E6 3D	OUT MSR_CLR,AL	
0000:C05C	B0 00	MOV AL,00H	
0000:C05E	E6 38	OUT CMD_PORT,AL	;Memory-memory disabled
0000:C060	B0 86	MOV AL,86H	;Block transfer mode
0000:C062	E6 3B	OUT MODE_PORT,AL	
0000:C064	B0 0F	MOV AL,0FH	

0000:C066	E6 3F	OUT MASK_PORT,AL	
0000:C068	B0 04	MOV AL,04H	
0000:C06A	E6 3A	OUT MASK_SET_RST,AL	;Mask channel 0
0000:C06C	B0 05	MOV AL,05H	
0000:C06E	E6 3A	OUT MASK_SET_RST,AL	;Mask channel 1
0000:C070	B0 02	MOV AL,02H	
0000:C072	E6 3A	OUT MASK_SET_RST,AL	;Unmask channel 2
0000:C074	B0 07	MOV AL,07H	;Mask channel3
0000:C076	E6 3A	OUT MASK_SET_RST,AL	
0000:C078	B0 00	MOV AL,00H	
0000:C080	E6 3C	OUT F_F_RST,AL	;Clear byte pointer flip flop
0000:C082	B0 00	MOV AL,00H	
0000:C084	E6 34	OUT ADD_CH2,AL	
0000:C086	B0 4C	MOV AL,4CH	
0000:C088	E6 34	OUT ADD_CH2,AL	;Start of address
0000:C08A	B0 0A	MOV AL,0AH	
0000:C08C	E6 35	OUT CNT_CH2,AL	
0000:C08E	B0 00	MOV AL,00H	
0000:C090	E6 35	OUT CNT_CH2,AL	;No of bytes count 000AH
0000:C092	E6 30	OUT ADD_CH0,AL	;clear unused channels address &
0000:C094	E6 30	OUT ADD _CH0,AL	;Count register
0000:C096	E6 31	OUT CNT_CH0,AL	
0000:C098	E6 31	OUT CNT_CHO,AL	
0000:C09A	E6 32	OUT ADD_CH1,AL	
0000:C09C	E6 32	OUT ADD_CH1,AL	
0000:C09E	E6 33	OUT CNT_CH1,AL	
0000:C100	E6 33	OUT CNT_CH1,AL	
0000:C102	E6 36	OUT ADD_CH3,AL	
0000:C104	E6 36	OUT ADD _CH3,AL	
0000:C106	E6 37	OUT CNT_CH3,AL	
0000:C108	E6 37	OUT CNT_CH3,AL	
0000:C10A	CC	INT 3	

EXPERIMENT 3:

AIM: To study memory to memory transfer by 8237. In this mode data stored at 4000:4050H to 4000:405AH in DYNA-DMA memory is transferred to DMA memory at 4000:4150H to 4000:415AH.

PROCEDURE:

STEP 1: Store data in the memory locations 4000:4050H to 4000:405AH. This data will be transferred to 4000:4150H to 4000:415AH.

STEP 2: Execute the program.

CONTROL BYTES USED:

1. Master Clear: Data transferred to the 8237 is immaterial in this case. Master Clear command clears command, status, request, temporary registers and internal First/ Last Flip/Flop. The mask register is set.

2. Command Byte:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

→ Memory to memory disable
→ Channel 0 addr. hold disable
→ Controller enable
→ Normal timing
→ Fixed priority
→ Late write selection
→ DREQ sense active high
→ DACK sense active low

3. Mode Byte:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	1

→ Channel 1 select
→ Write transfer
→ Auto initialization enable
→ Address Increment select
→ Block mode select

4. Mask Byte: Clear masks on all DMA request by outputting on 3EH data transferred is immaterial.

5. Reset register byte:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0

→ Select channel 0
→ Set request bit
→ Don't care

PROGRAM:

			P_8237_Exp-3
0000:6020	B0 00	MOV AL,00H	
0000:6022	E6 3D	OUT MSR_CLR,AL	
0000:6024	E6 3D	OUT MSR_CLR,AL	
0000:6026	E6 3D	OUT MSR_CLR,AL	
0000:6028	E6 3D	OUT MSR_CLR,AL	
0000:602A	B0 50	MOV AL,50H	
0000:602C	E6 30	OUT ADD_CH0,AL	
0000:602E	B0 40	MOV AL,40H	
0000:6030	E6 30	OUT ADD_CH0,AL	Start of address (4000:)4050H
0000:6032	B0 0A	MOV AL,0AH	

0000:6034	E6 31	OUT CNT_CH0,AL	
0000:6036	B0 00	MOV AL,00H	
0000:6038	E6 31	OUT CNT_CH0,AL	No. of bytes 000AH
0000:603A	B0 50	MOV AL,50H	
0000:603C	E6 32	OUT ADD_CH0,AL	
0000:603E	B0 41	MOV AL,41H	
0000:6040	E6 32	OUT CNT_CH0,AL	Start of Address(4000:)4150H
0000:6042	B0 0A	MOV AL,00H	
0000:6044	E6 33	OUT CNT_CH1,AL	No. of bytes count 000AH
0000:6046	B0 00	MOV AL,00H	;Clear unused channels add & ;Count register
0000:6048	E6 33	OUT ADD_CH2,AL	
0000:604A	B0 00	OUT ADD_CH2,AL	
0000:604C	E6 34	OUT CNT_CH2,AL	
0000:604E	E6 34	OUT CNT_CH2,AL	
0000:6050	E6 35	OUT ADD_CH2,AL	
0000:6052	E6 35	OUT ADD_CH2,AL	
0000:6054	E6 36	OUT CNT_CH2,AL	
0000:6056	E6 36	OUT CNT _CH2,AL	
0000:6058	E6 37	MOV AL,01H	
0000:605A	E6 37	OUT CMD_PORT,AL	Memory-memory enable
0000:605C	B0 01	MOV AL,85H	Block transfer mode
0000:605E	E6 38	OUT MODE_PORT,AL	Channel 1 for read
0000:6060	B0 85	MOV AL,88H	Block transfer mode
0000:6062	E6 3B	OUT MODE_PORT,AL	Channel 0 for read
0000:6064	B0 88	MOV AL,0FH	
0000:6066	E6 3B	OUT MASK_PORT,AL	
0000:6068	B0 0F	MOV AL,0FH	
0000:606A	E6 3F	OUT MASK_SET_RST,AL	
0000:606C	B0 00	MOV AL,00H	
0000:606E	E6 3A	OUT MASK SET/RST,AL	Unmask channel 0
0000:6070	B0 01	MOV AL,01H	
0000:6072	E6 3A	OUT MASK_SET_RST,AL	Unmask channel 1
0000:6074	B0 06	MOV AL,06H	
0000:6076	E6 3A	OUT MASK_SET_RST,AL	Mask channel 2
0000:6078	B0 07	MOV AL,07H	
0000:607A	E6 3A	OUT MASK_SET_RST,AL	;Mask channel 3
0000:607C	B0 04	MOV AL,04H	
0000:607E	E6 39	OUT RQST_PORT,AL	;Request register byte.
0000:6080	CC	INT 3	

EXERCISE:

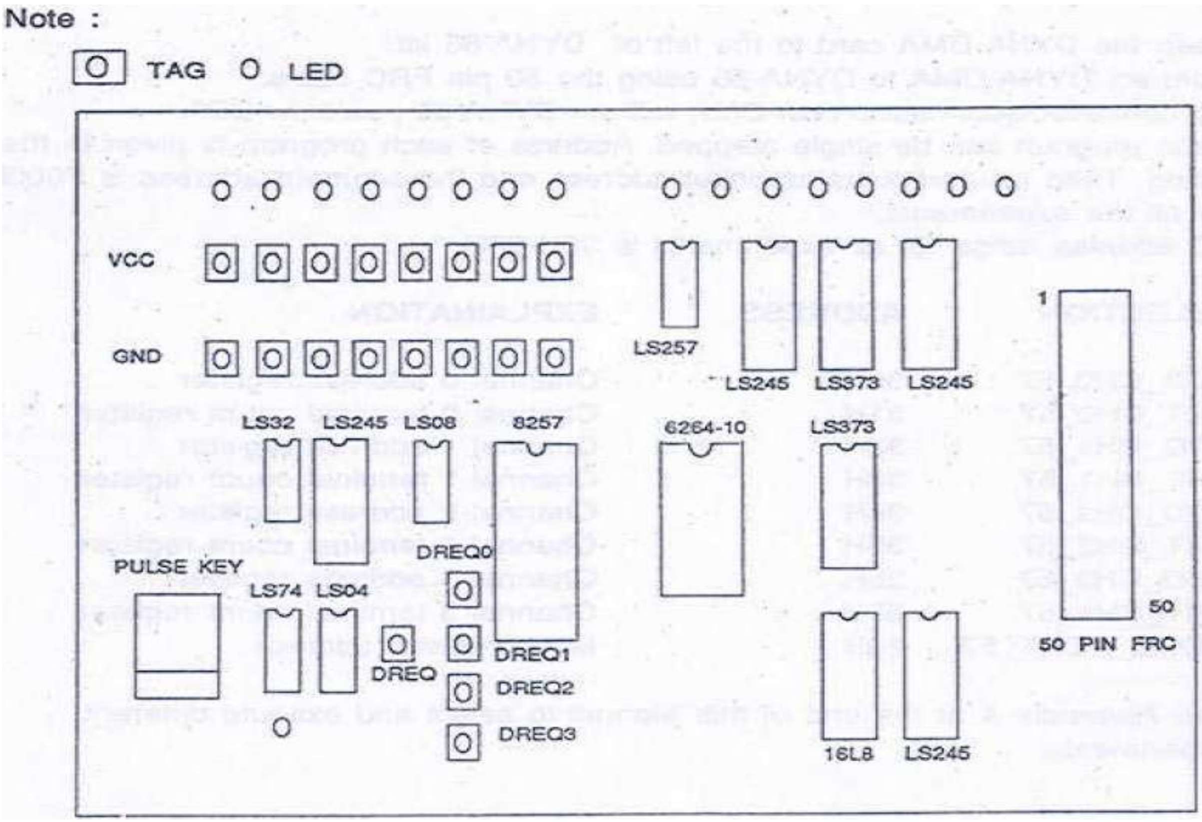
Perform this experiment for address decrement mode by changing the Mode.

DYNA – DMA, STUDY OF 8257

ABOUT DYNA – DMA, STUDY OF 8257

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
- It consists of 8257-A, RAM, buffers to drive LEDs, VCC and GND tags, LEDs.

DYNA-DMA, STUDY OF 8257 COMPONENT PLACEMENT:



ABOUT 8257:

The 8257 multimode direct memory access (DMA) controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory.

APPLICATIONS:

8257 is used as DMA controller with floppy disk controller, high speed communication controller, etc.

GENERAL PROCEDURE:

1. Keep the DYNA-DMA 8257 study-card to the left of DYNA-86LU kit.
2. Connect DYNA-DMA to DYNA-86LU using the 50 pin FRC cable.

3. Do connect/disconnect DYNA-DMA to/from DYNA-86LU only when power is OFF.
4. Each program can be single stepped. Address of each program is given in the listing. Third column contains offset address and the segment address is F000H for all the experiments.
5. I/O address range for all the experiments is 30H - 37H.

SELECTION	ADDRESS	EXPLANATION
ADD_CH0_57	30H	Channel 0 address register
ADD_CH0_57	31H	Channel 0 terminal count register
ADD_CH1_57	32H	Channel 1 address register
CNT_CH1_57	33H	Channel 1 terminal count register
ADD_CH2_57	34H	Channel 2 address register
CNT CH2_57	35H	Channel 2 terminal count register
ADD_ CH3_57	36H	Channel 3 address register
CNT_CH1_57	37H	Channel 3 terminal count register
MODE_PORT_57	38H	Mode register address

Enter the programs at the specified addresses…

6. See Appendix A at the end of this Manual to select and execute the different experiments.

EXPERIMENT 1:

AIM: To study-8257 in DMA read mode (memory to I/O).

PROCEDURE:

STEP 1: Connect DREQ2 to DREQ using a link.

STEP 2: Connect DACK to DACK2 using a shorting link.

STEP 3: Store data in memory locations 4000:4000H to 4000:400AH to be transferred to I/O.

STEP 4: Execute the program.

STEP 5: Generate DMA request using pulser key on the DYNA DMA kit. The data stored at memory locations 4000:4000H to 4000:400AH will be transferred to I/O and port LEDs will glow as per the data transferred.

CONTROL BYTES USED:

1. Mode Byte:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	0

- D0 → Disables DMA ch.0
- D1 → Disables DMA ch.1
- D2 → Enables DMA ch.2
- D3 → Disables DMA ch.3
- D4 → Disables Rotating Priority
- D5 → Disables Extended Write
- D6 → Disables TC STOP
- D7 → Enables AUTOLOAD

2. Channel – 3 Terminal Count MSB:

RD	WR	C13	C12	C10	C9	C8
1	0	0	0	0	0	0

- RD, WR → DMA Read Cycle

PROGRAM:

			P_8257_Exp-1
0000:C020	B0 84	MOV AL,84H	
0000:C022	E6 38	OUT MODE_PORT_57,AL	
0000:C024	B0 00	MOV AL,00H	
0000:C026	E6 34	OUT ADD_CH2_57,AL	
0000:C028	B0 40	MOV AL,40H	
0000:C02A	E6 34	OUT ADD_CH2_57,AL	
0000:C02C	B0 0A	MOV AL,0AH	
0000:C02E	E6 35	OUT CNT_CH2_57,AL	
0000:C030	B0 80	MOV AL,80H	
0000:C032	E6 35	OUT CNT_CH2_57,AL	
0000:C034	CC	INT 3	

EXPERIMENT 2:

AIM: To study-8257 in DMA write mode (I/O to memory).

PROCEDURE:

STEP 1: Connect DREQ3 to DREQ using a link.

STEP 2: Connect DACK to DACK3 (J5) using a shorting link.

STEP 3: Connect the input port data lines to VCC and GND using links to set the data to be transferred.

STEP 4: Execute the program.

STEP 5: Generate DMA request using pulser key on the DYNA DMA kit. The data at the input port will be transferred to the memory locations 4000:4000H to 4000:400AH.

CONTROL BYTES USED:

1. Mode Byte:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	0

Disables DMA ch.0
Disables DMA ch.1
Enables DMA ch.2
Disables DMA ch.3
Disables Rotating Priority
Disables Extended Write
Disables TC STOP
Enables AUTOLOAD

2. Channel – 2 Terminal Count MSB:

RD	WR	C13	C12	C10	C9	C8
0	1	0	0	0	0	0

DMA Write Cycle

PROGRAM:

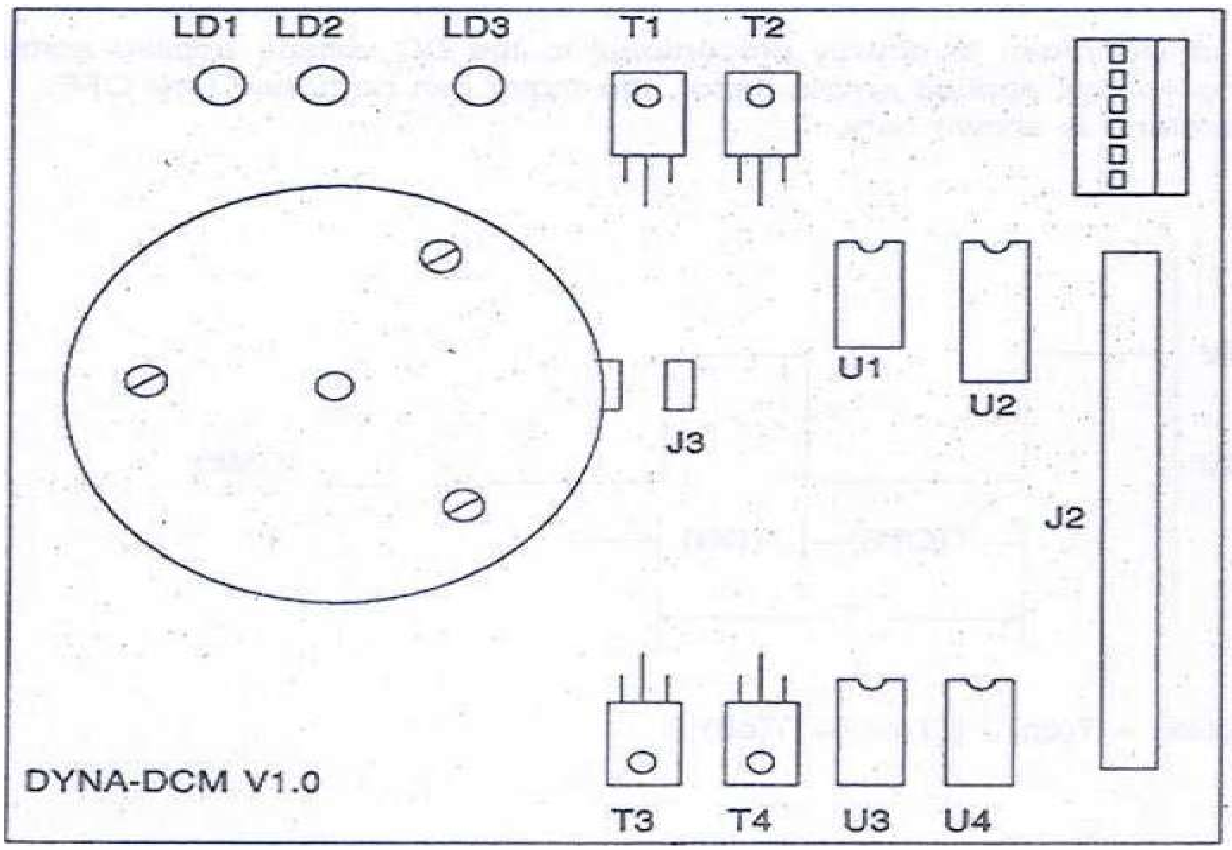
			P_8257_Exp-1
0000:C040	B0 48	MOV AL,48H	
0000:C042	E6 38	OUT MODE_PORT_57,AL	
0000:C044	B0 00	MOV AL,00H	
0000:C046	E6 36	OUT ADD_CH3_57,AL	
0000:C048	B0 40	MOV AL,40H	
0000:C04A	E6 36	OUT ADD_CH3_57,AL	
0000:C04C	B0 0A	MOV AL,0AH	
0000:C04E	E6 37	OUT CNT_CH3_57,AL	
0000:C050	B0 40	MOV AL,40H	
0000:C052	E6 37	OUT CNT_CH3_57,AL	
0000:C054	CC	INT 3	

DYNA – DCM, STUDY OF DC MOTOR

ABOUT DYNA – DCM, STUDY OF DC MOTOR

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
- It consists of Latch, DC MOTOR, LEDs, etc.

DYNA-DCM, STUDY OF DC MOTOR COMPONENT PLACEMENT:



APPLICATIONS:

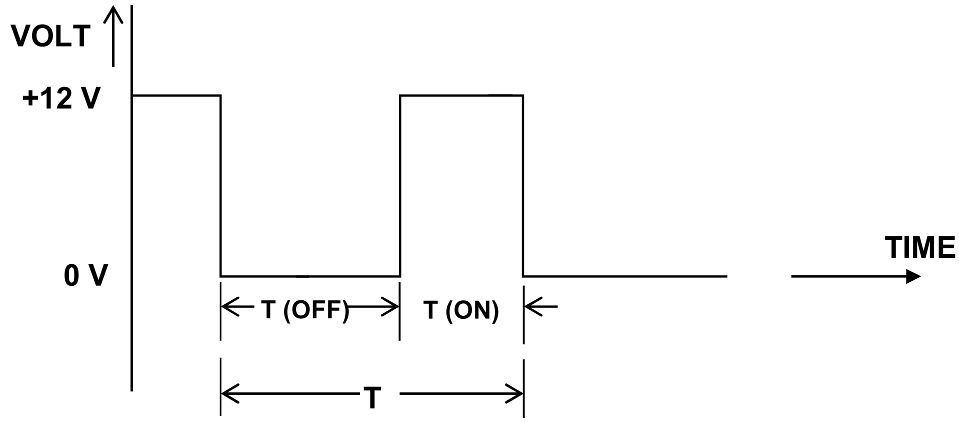
The DC MOTOR is used in tape recorders, VCRs. It is also used in grinders, mixers, ships, aeroplanes, locomotives etc. with increased rating and related changes in contactor, diver circuitry.

DC MOTOR & ITS SPEED CONTROL USING PWM:

The DC MOTOR used in this card is a 12V, 300mA motor with maximum speed limit of 2400 revolutions per minute (RPM).

Speed of DC motor is directly proportional to the DC voltage applied across it. By switching voltage applied across motor, the motor can be turned ON/OFF.

The waveform is shown here.



Duty Cycle = T(ON) / { T(ON) + T(OFF) }

The DC motor will rotate during ON TIME & will remain idle during OFF TIME. But that is an ideal case. Practically, due to mechanical inertia & other inherent electrical, mechanical properties the DC motor cannot follow fast switching of rectangular voltage waveform.

The DC motor treats rectangular waveform as a constant DC voltage whose magnitude is equal to the average value of rectangular voltage applied.

Consider the rectangular waveform shown in the diagram. Average value of this waveform can be found by integrating the waveform over time period T and dividing this number by T as follows:

V(avg) = Constant 1 * T(on)
= Constant * duty cycle

As can be seen from the above equation, V(avg) is directly proportional to the duty cycle or T(ON) or Pulse Width of applied waveform.

Thus, by varying Pulse Width of the rectangular waveform we can vary the speed of the DC motor. To change direction of rotation, it is only necessary to reverse the polarity of the applied voltage waveform. This technique of DC motor speed control is widely known as **Pulse Width Modulation (PWM)** technique.

PROCEDURE:

1. Keep DYNA-DCM V1.0 on left side of the DYNA-86LU kit. Connect them using 50 pin FRC cable.
2. Connect power supply cables to both DYNA-86LU & DYNA-DCM V1.0.
3. DO NOT CONNECT/ DISCONNECT DYNA-DCM V1.0 WHEN POWER IS ON.

4. Enter the given program & execute.

PROGRAM:

FOR CLOCKWISE DIRECTION:

			P_DCM_Exp-CW
0000:C000		MOV AL,8FH	
0000:C002		OUT 30,AL	
0000:C004		CALL DELAY	
0000:C006		MOV AL,8BH	
0000:C009		OUT 30,AL	
0000:C00B		CALL DELAY	
0000:C00C		JMP C000	

FOR CLOCKWISE DIRECTION:

			P_DCM_Exp-ACW
0000:C020		MOV AL,57H	
0000:C022		OUT 30,AL	
0000:C024		CALL DELAY	
0000:C027		MOV AL,53H	
0000:C029		OUT 30,AL	
0000:C02B		CALL DELAY	
0000:C02E		JMP C020	

FOR DELAY SUBROUTINE:

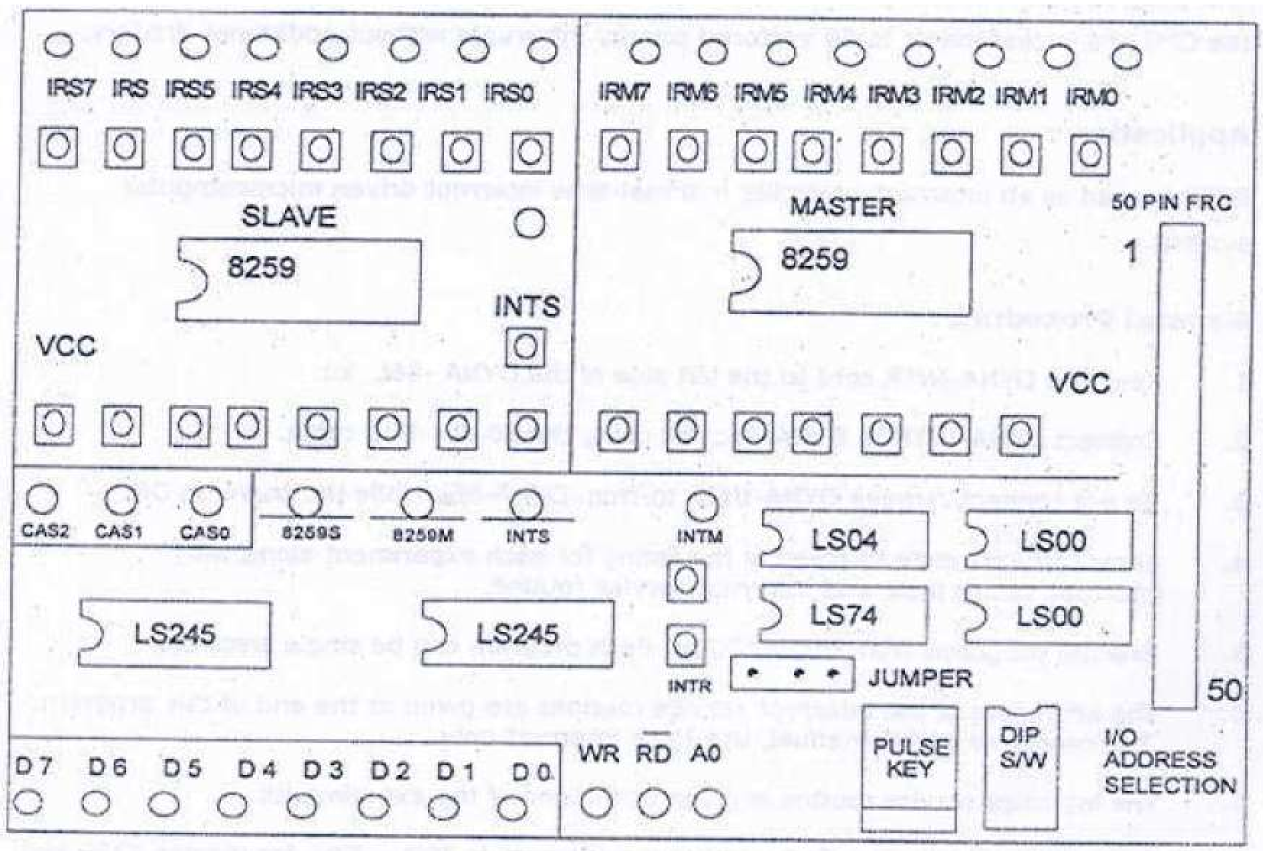
			P_DCM_Exp-Delay
0000:4000		PUSH CX	
0000:4001		PUSH BX	
0000:4002		MOV BX,00F0H	
0000:4005		MOV CX,00FFH	
0000:4008		LOOP 4008	
0000:400A		DEC BX	
0000:400B		JNZ 4005	
0000:400D		POP BX	
0000:400E		POP CX	
0000:400F		RET	

DYNA-INTR: STUDY Of 8259

ABOUT DYNA – INTR, STUDY OF 8259

- This study card is interfaced through a 50 pin FRC cable to the DYNA-86LU kit.
- It consists of 8259, buffers to drive LEDs, VCC and GND tags, LEDs, etc.

DYNA-INTR, STUDY OF 8259 COMPONENT PLACEMENT:



ABOUT 8259:

The programmable Interrupt Controller 8259 can handle 8 vectored priority Interrupts for the CPU and is cascadable to 64 vectored priority interrupts without additional circuitry.

APPLICATION:

8259 is used as an interrupt controller in a real-time interrupt driven microcomputer system.

GENERAL PROCEDURE:

1. Keep the DYNA-INTR 8259 card to the left side of the DYNA -86LU kit.
2. Connect DYNA-INTR to DYNA-86LU kit using the 50 pin FRC cable.
3. Do not connect / remove DYNA-INTR to / from DYNA-86LU while the power is ON.

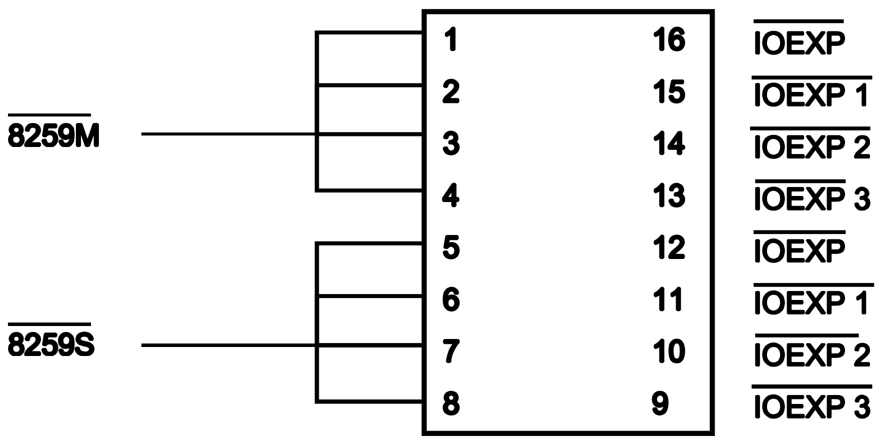
4. Enter software code as given in the listing for each experiment along with interrupt vector table and interrupt service routine.
5. Execute programs from 0000:1000H. Each program can be single stepped.
6. The addresses of the interrupt service routines are given at the end of this program. The programs in this manual, use INTR interrupt only.
7. The interrupt service routine is given at the end of the experiments.
8. Default I/O address range for all the experiments is 30H - 37H for master 8259 and 20H - 27H for slave 8259.

SELECTION	ADDRESS
ICW1, OCW2, OCW3	30H, 20H
ICW2, OCW1, ICW3, ICW4	31H, 21H

9. Other I/O ranges are:

$\overline{\text{IOEXP1}}$	38H - 3FH
$\overline{\text{IOEXP2}}$	28H - 2FH
$\overline{\text{IOEXP3}}$	20H - 27H

10. I/O address can be selected through a DIP switch:



INTRODUCTION:

In 8259 there are 4 Initialization command word (ICW1 - ICW4) and 3 operation command word (OCW1-OCW3).

ICW1 specifies the vectored address bits A0-A7, whether it is level triggered or edge triggered, call address Interval, single or cascade mode and whether ICW4 is needed or not.

ICW2 specifies the T7-T3 of interrupt vector address.

ICW3 (for master) specifies whether it has a slave or not. ICW3 (for slave) specifies the address. If the D1 bit of ICW1 is 1 then ICW3 is not needed.

ICW4 specifies the type of CPU used (8080, 8085, 8086 or 8088), whether nested mode, buffered mode master/slave, auto EOI.

OCW1 specifies the IRQ that is masked.

OCW2 specifies IR level to be acted upon. It also indicates if it is EOI mode or specific EOI mode or automatic EOI mode. It also indicates whether to set priority command for rotation or it is in automatic rotation mode.

OCW3 specifies whether interrupt request register is read or Interrupt service register. It indicates if poll command is used and whether special mask mode is set or reset.

EXPERIMENT 1:

AIM: To study of master 8259 in stand-alone mode and not as a master.

CONDUCTING EXPERIMENT:

			P_8259_Exp-1
0000:1000	B0 1F	MOV AL,1F	; ICW4 NEEDED ; INTERVAL OF 4 ; LEVEL TRIGGER SINGLE
0000:1002	E6 30	OUT ICW1M,AL	
0000:1004	B0 80	MOV AL,80	; ICW2 VECTOR AT 0:200
0000:1006	E6 31	OUT ICW2M	
0000:1008	B0 01	MOV AL,01H	; 8086 MODE NORMAL EDI
0000:100A	E6 31	OUT ICW4,AL	
0000:100C	B0 00	MOV AL,00H	; ALL IR MASK RST
0000:100E	E6 31	OUT 31,AL	
0000:1010	FB	STI	; ENABLE INTERRUPTS
0000:1011	EB FE WAIT:	LOOP WAIT	; WAIT FOR INTERRUPTS

STEP1: Keep the strap on DYNA-INTR on the left. Connect all IRM inputs to GND by using the connecting link chain provided. Connect INTM to INTR using link. **Make address selection switch 1 & 8 ON.** Enter the addresses of the interrupt service routine at vectored along with data at **0000:0200**. Run the program at address 0000:1000 and connect IRM to VCC. Press the pulsar key.

STEP 2: 1000H to 1003H
"1F" is ICW1M for 8259. The meaning of bits of ICW1 is explained in the figure below along with the functions.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1

D0 → ICW4 NEEDED.

D1 → Single 8259

D2 → Call address interval of 4

D3 → Level triggered mode

STEP 3: 1004 to 1007

"80H" is ICW2M for 8259. It contains T7-T3 of interrupt vector address.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0

→ T1-T3 of interrupt vector address.

STEP 4: 1008H to 100BH

“01H” is ICW4M for 8259. It contains 8086 mode, normal EDI, non-Buffered.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

D0 → 86 Mode.

D1 → Normal EDI.

D3 D2 → Non Buffer

D4 → Non not special Nested Mode.

STEP 5: 1000 to 100F

"00H" is ICW1M for 8259. Each bit off IMR can be independently changed (Set or Reset) by OCW1.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

→ Interrupt mask reset.

STEP 6: Press the pulser key. Interrupt controller will interrupt the CPU. The CPU sends the interrupt acknowledge signal and the interrupt service routine is executed displaying the message 'INT' and display the respective interrupt number.

INTERRUPT SERVICE ROUTINE:

			P_8259_Exp_ICR
0000:2000		CLI	
0000:2001		LEA SI, [3000]	
0000:2005		CALL FAR F000:0D3B	; to display ‘INT'
0000:200A		LEA SI, [3010]	
0000:200E		CALL FAR F000:0D3B	; to display '0'
0000:2013		JMP 2013	
0000:2015		CLI	
0000:2016		LEA SI, [3000]	
0000:201A		CALL FAR F000:0D3B	; to display ‘INT'
0000:201F		LEA SI, [3012]	
0000:2023		CALL FAR F000:OD3B	; to display '1'
0000:2028		JMP 2028	
0000:202A		CLI	
0000:2028		LEA SI,[3000]	
0000:202F		CALL FAR F000:003B	; to display ‘INT'
0000:2034		LEA SI, [3014]	
0000:2038		CALL FAR F000:0D3B	; to display '2'
0000:2030		JMP 2030	
0000:203F		CLI	
0000:2040		LEA SI, [3000]	
0000:2044		CALL FAR F000:0D3B	; to display ‘INT'
0000:2049		LEA SI,[3016]	
0000:204D		CALL FAR F000:0D3B	; to display '3'
0000:2052		JMP 2052	
0000:2054		CLI	
0000:2055		LEA SI, [3000]	
0000:2059		CALL FAR F000:003B	; to display ‘INT'
0000:205E		LEA SI, [3018]	
0000:2062		CALL FAR F000:0D3B	; to display '4'
0000:2067		JMP 2067	
0000:2069		CLI	
0000:206A		LEA SI,[3000]	
0000:206E		CALL FAR F000:003B	; to display ‘INT'
0000:2073		LEA SI, [301A]	
0000:2077		CALL FAR F000:0D3B	; to display '5'
0000:207C		JMP 207C	
0000:207E		CLI	
0000:207F		LEA SI, [3000]	
0000:2083		CALL FAR F000:OD3B	; to display ‘INT'
0000:2288		LEA SI,[301C]	
0000:208C		CALL FAR F000:0D3B	; to display '6'

0000:2091		JMP 2091	
0000:2093		CLI	
0000:2094		LEA SI, [3000]	
0000:2098		CALL FAR F000:0D3B	; to display ‘INT'
0000:209D		LEA SI,[301E]	
0000:20A1		CALL FAR F000:0D3B	; to display '7'
0000:20A6		JMP 20A6	

HEX CODE TO DISPLAY INT:

0000:3000	0D 0A 49 4E 54 00

HEX CODE TO DISPLAY '0 to F:

0000:3010	30 00 31 00 32 00 33 00 34 00 35 00 36 00 37 00

VECTOR TABLE: (HEX CODE)

0000:0200	00 20 00 00	; VECTOR ADDR FOR IRM0 (0000:2000)
0000:0204	15 20 00 00	; VECTOR ADDR FOR IRM1 (0000:2015)
0000:0208	2A 20 00 00	; VECTOR ADDR FOR IRM2 (0000:202A)
0000:020C	3F 20 00 00	; VECTOR ADDR FOR /RM3 (0000:203F)
0000:0210	54 20 00 00	; VECTOR ADDR FOR IRM4 (0000:2054)
0000:0214	69 20 00 00	; VECTOR ADDR FOR IRM5 (0000:2069)
0000:0218	7E 20 00 00	; VECTOR ADDR FOR IRM6 (0000:207E)
0000:021C	93 20 00 00	; VECTOR ADDR FOR IRM7 (0000:2093)

EXPERIMENT 2:

AIM: To study of 8259 in cascaded mode i.e.one 8259 as a master and the other as a slave.

CONDUCTING EXPERIMENT:

			P_8259_Exp-1
0000:1000	B0 1D	MOV AL,1D	; ICW4 NEEDED ; INTERVAL OF 4 ; LEVEL TRIGGER CASCADE
0000:1002	E6 30	OUT ICW1M,AL	
0000:1004	B0 80	MOV AL,80	; ICW2 Master Vector at 0:200H
0000:1006	E6 31	OUT ICW2M,AL	
0000:1008	B0 20	MOV AL,20	
0000:100A	E6 31	OUT ICW3M,AL	; IRM5 has a Slave
0000:100C	B0 01	MOV AL,01	; 8086 MODE NORMAL EDI
0000:100E	E6 31	OUT ICW4M,AL	
0000:1010	B0 1D	MOV AL,1D	; ICW4 needed, interval of 4
0000:1012	E6 20	OUT ICW1S,AL	; Level Trigger Cascade
0000:1014	B0 88	MOV AL,88	; ICW2 Slave Vector at 0:220H
0000:1016	E6 21	OUT ICW2S,AL	
0000:1018	B0 05	MOV AL,5	
0000:101A	E6 21	OUT ICW3S,AL	; Slave ID = 5
0000:101C	B0 01	MOV AL,01	
0000:101E	E6 21	OUT ICW4S,AL	; 86 Mode, normal EDI
0000:1020	B0 00	MOV AL,0	
0000:1022	E6 21	OUT 21,AL	; All Interrupt Mask Reset
0000:1024	FB	STI	; Set Interrupt
0000:1025	EB FE		; Wait for IR

STEP 1: Place the strap on the left. Keep all IRS and IRM Inputs grounded using links provided. Enter the addresses of the interrupt service routine at vectored interrupt addresses from 2000-21F. Connect INTM to INTR using link. Make address selection **switch 1 & 8 ON**.

STEP 2: Use the key provided on the board to execute the program from address 1000H. It will execute the program step by step. The contents of data bus will be displayed on the LEDs. Similarly control signals will also be displayed on respective LEDs.

STEP 3: Connect any IRS to VCC & INTS to IRM5 using the link.

STEP 4: 1000H to 1003H
"1DH" is ICW1M for 8259. The meaning of bits of ICW1 is explained in the figure below along with the functions.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1

ICW4 NEEDED.

Cascaded mode.

Interval of 4.

Level triggered mode

STEP 5: 1004 to 1007

"80H" is ICW2M for 8259. It contains the T7-T3 of interrupt vector address.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0

T1-T3 of interrupt vector address.

STEP 6: 1008H to 100BH

“20H” is ICW3M for 8259M. When SNGL = 0, ICW3 is valid and indicates cascade connections with other 8259 devices. In other master mode a "1" is set for each slave.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0

IMR5 IR input slave.

STEP 7: 1000 to 100F

"01H" is ICW4M for 8259. It contains 8086 mode, normal EDI, non-buffered.

STEP 8: 1010 to 1013

"0DH" is ICW1S for 8259S. The meaning of bits of ICW1 is explained in the figure below along with the functions.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	1

ICW4 needed.

Cascaded mode.

Interval of 4.

Level triggered mode.

STEP 9: 1014 to 1017

"C3H" is ICW2S for 8259S. It contains vectored address bits A15-A8.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0

T1-T3 of Interrupt vector address to slave

STEP 10: 1018 to 101B
"C5H" is ICW3S for 8259S. When SGNL = 0, ICW3 is valid and indicates cascade connections with other 8259 devices.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1

Slave ID 101

STEP 11: 101C to 101F
"00H" is ICW4S for 8259S. Only when ICW4 = 1 in ICW1 is ICW4 valid. Otherwise all bits are set it zero.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

86 Mode.

Normal EDI.

Non Buffered mode.

Not special fully nested mode defines ICW4.

STEP 12: 1020 to 1023
"00H" is ICW4S for 8259S. Each bit off IMR can be independently changed (Set or Reset) by OCW1.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Interrupt mask reset.

STEP 13: Connect **INTM to INTR** using the links. Connect **INTS to IRM5** using links.

Connect IR to VCC & other IR Inputs to ground. Execute the program from 1000H. Use pulser key to step. Interrupt controller will Interrupt CPU. The CPU sends interrupt acknowledge & interrupt service routine is executed displaying message “**INT**” & display the respective interrupts number. Int number 0 to 7 for master IRMs & B to F for slave IR-S.

INTERRUPT SERVICE ROUTINE:

			P_8259_Exp_ICR
0000:2000		CLI	
0000:2001		LEA SI, [3000]	
0000:2005		CALL FAR F000:0D3B	; to display ‘INT'
0000:200A		LEA SI, [3010]	
0000:200E		CALL FAR F000:0D3B	; to display '0'
0000:2013		JMP 2013	
0000:2015		CLI	
0000:2016		LEA SI, [3000]	
0000:201A		CALL FAR F000:0D3B	; to display ‘INT'
0000:201F		LEA SI, [3012]	
0000:2023		CALL FAR F000:OD3B	; to display '1'
0000:2028		JMP 2028	
0000:202A		CLI	
0000:2028		LEA SI,[3000]	
0000:202F		CALL FAR F000:003B	; to display ‘INT'
0000:2034		LEA SI, [3014]	
0000:2038		CALL FAR F000:0D3B	; to display '2'
0000:203D		JMP 2030	
0000:203F		CLI	
0000:2040		LEA SI, [3000]	
0000:2044		CALL FAR F000:0D3B	; to display ‘INT'
0000:2049		LEA SI,[3016]	
0000:204D		CALL FAR F000:0D3B	; to display '3'
0000:2052		JMP 2052	
0000:2054		CLI	
0000:2055		LEA SI, [3000]	
0000:2059		CALL FAR F000:003B	; to display ‘INT'
0000:205E		LEA SI, [3018]	
0000:2062		CALL FAR F000:0D3B	; to display '4'
0000:2067		JMP 2067	
0000:2069		CLI	
0000:206A		LEA SI,[3000]	
0000:206E		CALL FAR F000:003B	; to display ‘INT'
0000:2073		LEA SI, [301A]	
0000:2077		CALL FAR F000:0D3B	; to display '5'
0000:207C		JMP 207C	
0000:207E		CLI	
0000:207F		LEA SI, [3000]	
0000:2083		CALL FAR F000:OD3B	; to display ‘INT'
0000:2288		LEA SI,[301C]	
0000:208C		CALL FAR F000:0D3B	; to display '6'

0000:2091		JMP 2091	
0000:2093		CLI	
0000:2094		LEA SI, [3000]	
0000:2098		CALL FAR F000:0D3B	; to display ‘INT'
0000:209D		LEA SI,[301E]	
0000:20A1		CALL FAR F000:0D3B	; to display '7'
0000:20A6		JMP 20A6	
0000:20A8		CLI	
0000:20A9		LEA SI, [3000]	
0000:20AD		CALL FAR F000:0D3B	; to display ‘INT'
0000:20B2		LEA SI, [3020]	
0000:20B6		CALL FAR F000:0D3B	; to display '8'
0000:20BB		JMP 20BB	
0000:20BD		CLI	
0000:20BE		LEA SI, [3000]	
0000:20C2		CALL FAR F000:0D3B	; to display ‘INT'
0000:20C7		LEA SI, [3022]	
0000:20CB		CALL FAR F000:OD3B	; to display '9'
0000:20D0		JMP 20D0	
0000:20D2		CLI	
0000:20D3		LEA SI,[3000]	
0000:20D7		CALL FAR F000:003B	; to display ‘INT'
0000:20DC		LEA SI, [3024]	
0000:20E0		CALL FAR F000:0D3B	; to display 'A'
0000:20E5		JMP 20E5	
0000:20E7		CLI	
0000:20E8		LEA SI, [3000]	
0000:20EC		CALL FAR F000:0D3B	; to display ‘INT'
0000:20F1		LEA SI,[3026]	
0000:20F5		CALL FAR F000:0D3B	; to display 'B'
0000:20FA		JMP 20FA	
0000:20FC		CLI	
0000:20FD		LEA SI, [3000]	
0000:2101		CALL FAR F000:003B	; to display ‘INT'
0000:2106		LEA SI, [3028]	
0000:210A		CALL FAR F000:0D3B	; to display 'C'
0000:210F		JMP 210F	
0000:2111		CLI	
0000:2112		LEA SI,[3000]	
0000:2116		CALL FAR F000:003B	; to display ‘INT'
0000:211B		LEA SI, [302A]	
0000:201F		CALL FAR F000:0D3B	; to display 'D'
0000:2124		JMP 2124	
0000:2126		CLI	

0000:2127		LEA SI, [3000]	
0000:212B		CALL FAR F000:OD3B	; to display ‘INT'
0000:2130		LEA SI,[302C]	
0000:2134		CALL FAR F000:0D3B	; to display 'E'
0000:2139		JMP 2139	
0000:213B		CLI	
0000:213C		LEA SI, [3000]	
0000:2140		CALL FAR F000:0D3B	; to display ‘INT'
0000:2145		LEA SI,[302E]	
0000:2149		CALL FAR F000:0D3B	; to display 'F'
0000:214E		JMP 214E	

HEX CODE TO DISPLAY INT:

0000:3000	0D 0A 49 4E 54 00

HEX CODE TO DISPLAY '0 to F:

0000:3010	30 00 31 00 32 00 33 00 34 00 35 00 36 00 37 00
0000:3010	38 00 39 00 41 00 42 00 43 00 44 00 45 00 46 00

VECTOR TABLE: (HEX CODE)

0000:0200	00 20 00 00	; VECTOR ADDR FOR IRM0 (0000:2000)
0000:0204	15 20 00 00	; VECTOR ADDR FOR IRM1 (0000:2015)
0000:0208	2A 20 00 00	; VECTOR ADDR FOR IRM2 (0000:202A)
0000:020C	3F 20 00 00	; VECTOR ADDR FOR /RM3 (0000:203F)
0000:0210	54 20 00 00	; VECTOR ADDR FOR IRM4 (0000:2054)
0000:0214	69 20 00 00	; VECTOR ADDR FOR IRM5 (0000:2069)
0000:0218	7E 20 00 00	; VECTOR ADDR FOR IRM6 (0000:207E)
0000:021C	93 20 00 00	; VECTOR ADDR FOR IRM7 (0000:2093)
0000:0220	A8 20 00 00	; VECTOR ADDR FOR IRM0 (0000:20A8)
0000:0224	BD 20 00 00	; VECTOR ADDR FOR IRM1 (0000:20BD)
0000:0228	D2 20 00 00	; VECTOR ADDR FOR IRM2 (0000:20D2)
0000:022C	E7 20 00 00	; VECTOR ADDR FOR IRM3 (0000:20E7)
0000:0230	FC 20 00 00	; VECTOR ADDR FOR IRM4 (0000:20FC)
0000:0234	11 21 00 00	; VECTOR ADDR FOR IRM5 (0000:2111)
0000:0238	26 21 00 00	; VECTOR ADDR FOR IRM6 (0000:2126)
0000:023C	3B 21 00 00	; VECTOR ADDR FOR IRM7 (0000:2135)