COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)

END Semester Examination

Programme: B.Tech / M.Tech | **Semester: III**

Course Code: CT-16005 | **Course Name: Digital Logic Design**

Branch: Computer Engineering | **Academic Year: 2019-20**

Duration: 3 Hr | **Max Marks: 60**

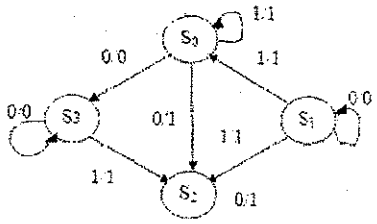
Student PRN No.

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of stationery, calculator etc. not allowed.
5. Write your PRN Number on Question Paper.

			Marks	CO	PO
Q 1	a	Find a cost-effective implementation of $Y(A, B, C) = (A+B)\ (A+B+C)\ (A+C)$ Using K-Map. Draw the logic diagrams using basic gates.	3	1,2	1,3
	b	A digital circuit is to have a single output and four input: A, B, C and D. The output is 1 whenever the decimal equivalent of $(ABCD)_2$ is divisible by either 3 or 5. Design the logic circuit.	5	2	1,3, 4
	c	Convert the numbers with the indicated bases. i. $(4310)_5 = (\ ?\ )_{10}$ ii. $(A9F)_{16} = (\ ?\ )_8$	2	1	1
Q 2	a	Realize $Y(A,B,C) = A'B'+B'C'+ABC$ using an 8x1 MUX. Can it be realized with a 4x1 MUX? If yes then realize.	6	2	4
		OR			
		Generate the following Boolean functions with a PAL. Y_3=A'BC'D+A'BCD'+A'BCD+ABCD' Y_2=A'BCD'+A'BCD+ABCD Y_1=A'BC'+A'BC+AB'C+ABC' Y_0=ABCD			
	b	Using only single-bit half adders, obtain a logic circuit that can add four single-bit numbers.	4	2	1,3, 4
Q 3	a	For synchronous sequence counter with sequence 2 -> 6 -> 5 -> 3 -> 1 -> 0 -> 2. i. Draw state diagram. ii. Give present state/next state state table using D flip flop. iii. Simplify and realize the circuit.	6	2,3	4,6

	b	Implement JK flip-flip using D flip flop by deriving the Characteristics equation of both JK flip flop and D flip flop using Characteristics table and further simplification by using K-map.	4	3	4,7
Q 4	a	A sequential circuit with two D Flip-Flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations: $A(t+1) = x'y + xA$ $B(t+1) = x'B + xA$ $z = B$ i. Draw the logic diagram of the circuit. ii. List the state table for the sequential circuit. iii. Draw the corresponding state diagram.	6	2,3	4,7
	b	Draw the logic diagram of four-bit Serial-In Parallel-Out left shift register. (Consider the circuit you drawn and answer following question) The binary number 1011 is serially left shifted into an above mentioned shift register that has an initial content of 1010. Draw waveforms at Q_0, Q_1, Q_2, Q_3 and table showing data movement through a shift register after each clock pulse and answer the following questions. i. What are the Q outputs after one clock pulses? ii. What are the Q outputs after two clock pulses? iii. What are the Q outputs after four clock pulses?	4	3	4.7
Q 5	a	What is ASM chart? List components involved in ASM chart. Draw ASM chart for given state diagram.	6	2,3, 4	7,8
	b	Draw and explain Johnson counter with initial state 110. Explain all possible states (from initial state) with the help of waveforms.	4	2,3	4,6
Q 6	a	A sequential ring counter with present state '1001'. The circuit also have an input 'X'. If X = 0, circuit shows next output (right shift) else X = 1, it shows same state. i. Draw the state diagram of circuit ii. Give the state table of circuit. iii. Draw the circuit using D Flip-flops.	6	2,3, 4	7,8
	b	Write short note on Random Access Memory.	4	4	6,8



OR

Write VHDL (entity-architecture) declaration of 2-bit NAND and OR gate.

----------*******----------