Department of Computer Engineering and Information Technology

Second Year B. Tech. (Computer Science and Engineering)

TEST I

Sub: Digital Logic Design

Max. Marks 20

1. Simplify following Boolean expressions **(06 marks)** (ANY TWO)
   a) (A+ B)' (A' + B')'
   b) xyz + x'y + xyz'
   c) ABC + A'B + ABC'

   Draw logic diagram of the circuits that implement the original and simplified expressions of ~~above~~ above

2. Obtain truth tables of following, and express each function in sum of minterms and product of maxterms form **(04 marks)**
   a) (b + cd) (c + bd)
   b) (c' + d) (b + c')

3. Express following function to its both canonical forms without using the truth table: **(02 Marks)**

   F = B'D + A'D + BD

4. Convert hexadecimal number 64CD to binary and then to octal, then convert it from binary to decimal **(02 mark)**

5. Obtain 1's and 2's compliment of following binary number **(4 marks)**

   a. 00010000
   b. 00000000
   c. 11111111
   d. 11011010

6. Convert following numbers in the decimal **(2 marks)**

   a. (10110.0101) which is a binary number
   b. (DADA.B) which is a hexadecimal number

COEP Technological University, Pune

Department of Computer Engineering and IT

Mid Semester Examination S. Y. B.Tech. (Computer Engineering) 2022-23

Subject: Digital Logic Design (III Semester)

Re-Test 1

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Duration: One hour **Maximum Marks: 20**

Q.1 Minimise following Boolean expressions using K map. Draw the logic diagram of minimized Boolean function **09**

a) F(A,B,C,D) = A'B'C' + B'CD' + A'BCD' + AB'C'

b) F(w,x,y,z) = ∑ (1,3,7,11,15)

c) F (A,B, C, D) = ∑ (0,1,2,4,5,6,8,9,12,13,14)

Q.2 Simplify Booleans expressions to minimum number of literals using Boolean identities and draw logic diagram of circuits that implement original and simplified expressions **06**

a) ABC + A'B + ABC'

c) (BC' + A'D) (AB' + CD')

Q.3 Convert following decimal numbers to binary **02**

a) 81.14

b) 2817

Q.4 Perform subtraction of following binary numbers using 2's compliment of subtrahend. If the result is negative take the 2's compliment of the number and affix the minus sign to it. Prove your answer by appropriate conversions in decimal equivalents **03**

a) 1001 - 110101

b) 101000 - 10101

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TEST 2 (Date:

Duration: One hour **Max Marks: 20**

Q. 1. Three bits x, y and z constitute the binary message and are input to the digital circuit. The parity bit ***P*** is the output. For even parity, the bit ***P*** must be generated to make the total number of 1's (including ***P***) even. Design an even parity generator using K map. Draw the logic diagram. **03**

Q.2. Design a Binary Coded Decimal (BCD) to Excess-3 Code Converter for the decimal digits. **04**

Q.3. Design a full adder. Convert the Booleans expression of the full adder to implement the full adder with two half adders and an OR gate. Draw logic diagram. **03**

Q.4. Design a carry look-ahead generator for the four bit binary addition. Redraw the logic diagram of full adder designed in Q.3 above and mark intermediate variables ***P*** and ***G***. **03**

Q.5. Draw logic diagram of a four bit binary adder/subtractor using full adders as building block. Explain the operation of **v** (Overflow) flag. **02**

Q.6. Design a 4:2 bit priority encoder. The priority function should be designed such that if more than one inputs are equal to 1 the input having highest priority will take precedence. Design a third output as valid **v** bit which is 1 when one or more inputs are 1, 0 otherwise. Draw the logic diagram. **03**

Q.7. Draw function table and logic diagram of positive edge triggered D type of flipflop. Add asynchronous Reset input to it. **02**

College of Engineering, Pune
Department of Computer Science and IT
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End Semester Examination 2022-23

Duration: Three Hours **Sub: Digital Logic Design** **Max Marks: 60**

(All questions are Compulsory) *Marks*

Q.1 Convert the following decimal numbers in to binary **04**
a) 561.125 b) 6531

Q.2 Minimize following Boolean expressions to minimum number of literals using Boolean identities. **04**
a) $xy + x(wz + wz')$ b) $ABC + A'B + ABC'$

Q.3 Derive the circuits from truth table and K-map minimization for a three bit parity generator and four bit parity checker using an even parity bit **08**

Q.4 Design a full adder from the truth table and K map minimization. Implement the full adder using two half adders and an OR gate. **06**

Q.5 Design a combinational circuit that converts a four bit binary to a BCD using K-maps. Draw the logic diagram. **08**

Q.6 Draw the function table, graphic symbol, characteristic table & excitation table for positive edge triggered JK flipflop. Design JK flipflop using a D flipflop and gates. **06**

Q.7 Draw the diagram & explain the operation of Basic Cell of memory using a SR latch. Design a 4x4 bit memory using Basic Cells & a 2 to 4 decoder for address generation. **06**

Q.8 Draw four bit updown binary synchronous counter using positive edge triggered T type Flipflops. Draw the waveforms of outputs in response to the clock. **04**

Q.9 Consider the sequential circuit with two D flipflops whose output Q is named as A and B respectively and one input x and one output y. The Following are the state equations:
$A(t+1) = Ax + Bx$, $B(t+1) = A'x$ $y = Ax' + Bx'$
a) Find the state table for the above defined sequential circuit with JK flipflops
b) Draw the logic diagram and the state diagram of the circuit **08**

Q.10 Write short notes on: (ANY TWO) **06**
a) Algorithmic State Machine
b) Register Transfer Level (RTL) notation
c) Memory cycle timing waveforms