COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)

END Semester Examination

Programme: B.Tech | **Semester: III**

Course Code: CT 16005 | **Course Name: Digital Logic Design**

Branch: Computer Engineering & IT | **Academic Year:2018-19**

Duration: 3 Hr | **Max Marks: 60**

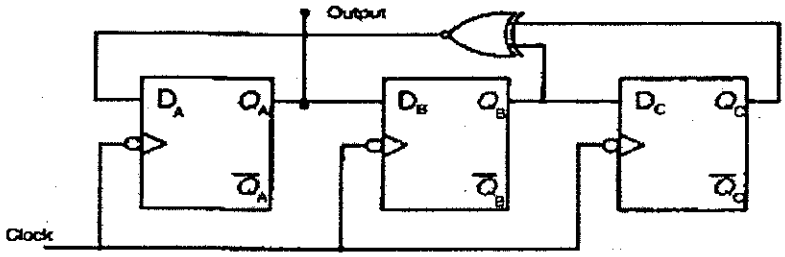
Student PRN No.

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of stationery, calculator etc. not allowed.
5. Write your PRN Number on Question Paper.

			Mark	CO	PO
Q 1	a	i. If $101_3 = X_2$, then X is _____ (show step wise calculation) ii. Simplify the following expression into sum of products using Karnaugh map: $F(A, B, C, D) = \Sigma(1, 3, 4, 5, 6, 7, 9, 12, 13)$	3	1	1
	b	Simplify the following Boolean function by using a Quine Mc Cluskey method. $F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$ also list out all PI and EPI.	7	1,2	1,3
Q 2	a	Input to combinational circuit is 4-bit binary number. Design the circuit with minimum hardware for the following i. Output P=1 if the number is prime. ii. Output Q=1 if number is divisible by 3.	6	2	1,3, 4
	b	Implement the given Boolean function with 8x1 multiplexer with A, B and D connected to select lines S_2, S_1 and S_0 respectively. $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$	4	2	4
Q 3	a	Design Mod 13 asynchronous down counter. What is glitch problem? How to avoid glitch?	7	2,3	4,6
	b	Realize F (A,B,C) = A'B'+B'C'+ABC using suitable DeMUX.	3	1,2	3,4
Q 4	a	Design a synchronous counter for the random count sequence as 4->6->7->3->4. Use JK flip-flop for design.	6	2,3	4,6

	b	How many flip-flops are required to build a binary counter circuit to count from 0 to 2048. What is the frequency of the output of last flip-flop for an input clock frequency of 6MHz?	2	3	4,7
	c	Assume that all flip-flops are in reset condition initially. What is the count sequence (for first seven clock input signals) observed at Q_A in the given circuit.	2	3	4,7



Q 5	a	A clocked sequential circuit has three states, A,B and C and one input X. As long as the input X is '0', the circuit alternates between the states A and B. If the input becomes '1' (either in state A or state B), the circuit goes to state C and remain in state C as long as X continues to become '1'. The circuit returns to state A if the input becomes '0' once again and from then repeats its behaviour. Assume that state assignments are A=00, B=01, C=10. a. Draw the state diagram of circuit b. Give the state table of circuit. c. Draw the circuit using D Flip-flops.	6	2,3, 4	7,8
	b	Write VHDL (entity-architecture) declaration of 2-bit NOR and AND gate.	4	4	6,8
Q 6	a	Draw State table, State diagram and ASM chart for 3-Bit octal number UP/DOWN counter with control input M such that if M=1 counter counts in UP direction and if M=0 counter counts in DOWN direction. OR A two bit UP counter with output 'Q_1Q_0' and enable signal 'X' is to be designed. If 'X' = 1, counter changes the state as '00-01-10-11-00'. If 'X'=0, counter should remain in same state. Design your circuit using D flip flops and suitable MUXs.	6	2,3, 4	4,7
	b	Write short note on Random Access Memory.	4	4	8

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