Unit-1

CPU Architecture: Instruction format, control signals in CPU, micro program control unit
and hardwired control unit, ALU & sequencer, look ahead carry generator, MIPS ISA

Unit 1

Sr. No.	Reference	Reading sequence
1.	Performance and Numericals	Chapter 1: Hennessy Patterson (COAD)
2.	Instruction Format, General Discussion	Chapter 2: Hamacher Zaky (CO)
3.	Instruction Cycle, Subcycle	Chapter 14: William Stallings
4.	Data path and related concepts and Control Signal; Hardwired, Mircroprogrammed Control	Chapter 5: Hamachar Zaky (CO)
5.	Control unit operations	Chapter 20 & 21: William Stallings
6.	Data path and control signal for RISC-V instructions ADD, LOAD etc.	Chapter 4.1 to 4.4: Hennessy Patterson (COAD)