

```

MOV AX, 8000
MOV DS, AX
MOV AL, [0000H]

```

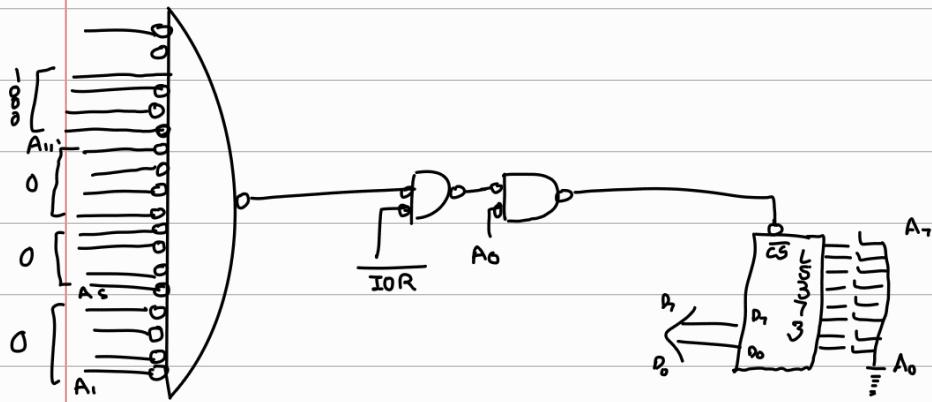
When I<sub>7</sub>, I<sub>6</sub> is selected,  
we have  
00111111 ⇒ BF  
goes on data line

### I/O Mapped I/O

- IN
- OUT
- IN AL, 80H

- In processors with segmentation, I/O Mapped I/O must be discouraged as it makes program less readable.
- In case of 'I/O mapped I/O' there is no segment reference
- when using 8 bit address, address represented on address bus is repeated address the other four address lines A<sub>19</sub> to A<sub>16</sub> are don't care lines.
- e.g. 80H → presented as 8080H.

Q.  $\text{MOV DX, } \underline{\underline{1000H}}$   $\rightarrow$  1000000000000000  
 $\text{IN AX, DX}$



Port is a data trafficking device.

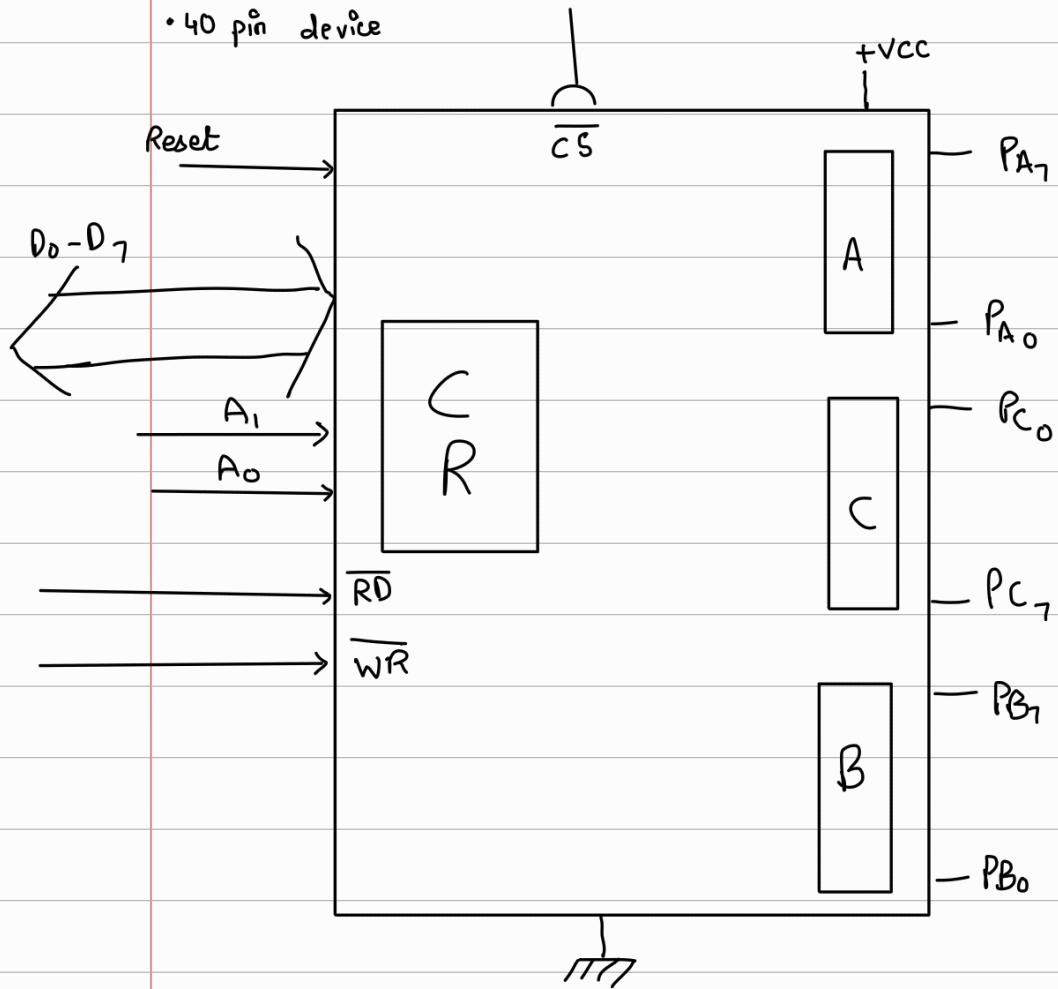
for Processor '74LS343' can be a port.

Most of the time  $\rightarrow$  processor fetches program from memory and executes it.

# 8255 PPI

- 8255 Programmable Peripheral Interface

- 40 pin device



$A, B, C$  — Named Registers.

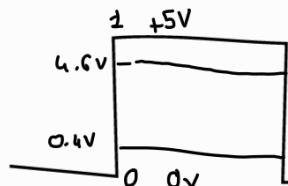
$CR$  — Control Register

Reset → Resets data in device.

4 locations ( $A, B, C, CR$ ) →

Bus Contention → When two devices conflict on data bus we get error. It is one of the most dangerous. Catastrophic in nature as it is irreversible.

Computation world based on



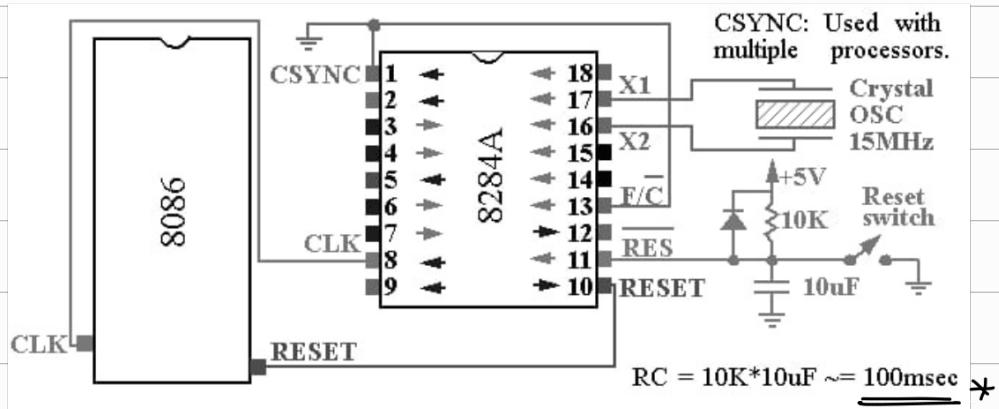
Noise upto 0.4 Volt is rounded up/down. As its allowed.

$4.6V \rightarrow 5V$  considered

as

- 8086 → pin 21 → Reset pin.

- 8284 clock generator gives CLK as well as reset signal to 8086.



When 8284's Reset out connected to 8086's Reset in, 8086 is reset.

\* during reset, all buses of 8086 are tri-stated.

\* -u- CPU almost dead other than clock signals reaching 8086 clock from 8284 clock.

\* The moment CPU gains power,

————— CPU gains consciousness and starts running a bus cycle.

\* After reset contents of all registers of CPU are reset to 0, except CS, CS=FFF-F.

After processor resets, it gets synchronised to 1st rising edge of next T-state to begin bus cycle.

i.e. next T-state becomes [considered as] first bus cycle of the bus's first T-state.

• Upon reset CPU synchronised to clock's rising edge, CPU knows this being the OP Code fetch cycle (as some first instruction should be given at start).

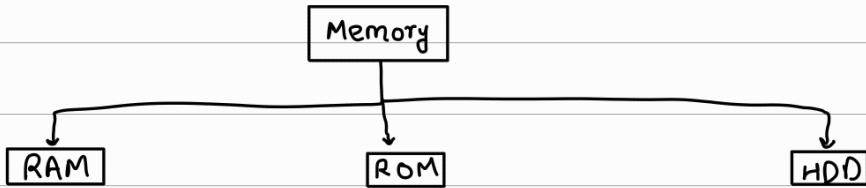
CS : IP  
ffff 0000 → physical  
ffff 0

• This location should be on ROM.

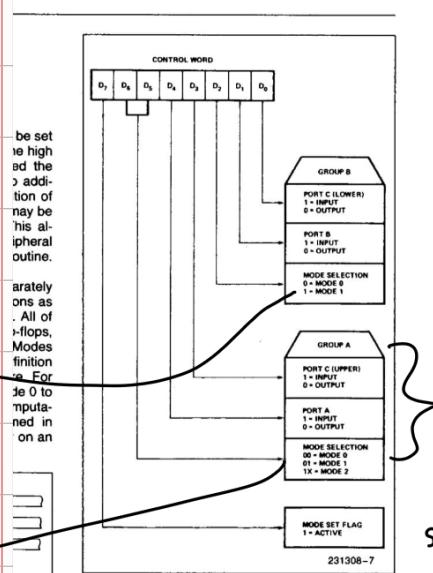
\* Designing a bootstrap program!

- Make sure of this {
1. Make sure ffff0 is available in ROM
  2. Write a 'long jump' instruction to a safe location with more memory available.

Bootstrap loader → loads imp. parts of OS from ROM.



8255A/8255A-5



The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

$D_2 = 0, MODE = 0$   
Simple I/O Mode

$D_0 = 0, MODE = 0$   
Simple I/O

$D_1 = 1$  → handshake

Port A and Port C upper form together Group A,

in simple I/O mode when no handshake signal are required both can act as any i/p or o/p port.

If  $D_4 = 0$ , port A is o/p port

If  $D_4 = 1$ , port A is i/p port.

A] WAP to initialize 8255 in mode 0 with port A and C as output ports and port B as an input port.

Base address for 8255 is 80H

B] If PB<sub>0</sub> line is 0,  
OFH.

-11- is 1,  
FOH.

| o/p port A with

| o/p port C as

$\frac{10000010}{8} \frac{2}{2} H$

⇒

If starting port is 80H,

MOV AL, 82H

Port A → 80H

OUT 86H, AL

B → 82H

B]

IN AL, 82H

(Control register format)  
A address of Port B

AND AL, 01H

C → 84H

Configure Port A and C as o/p,

Port B as i/p port.

CMP AL, 01H

? necessary

JZ NEXT

IN AL, 82H  
CMP AL, 02H,

MOV AL, OFH

OUT 80H, AL

RET

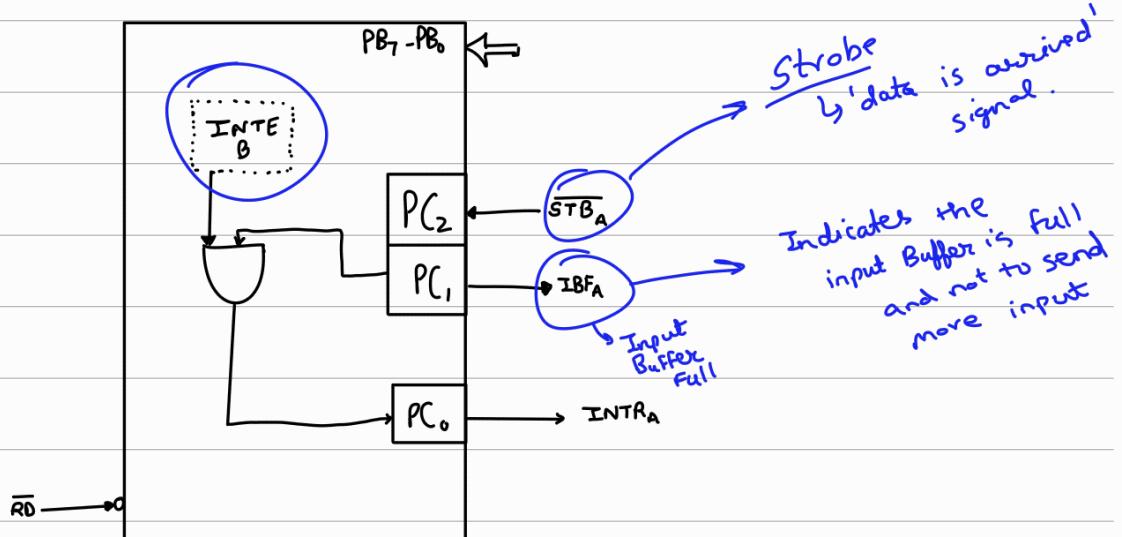
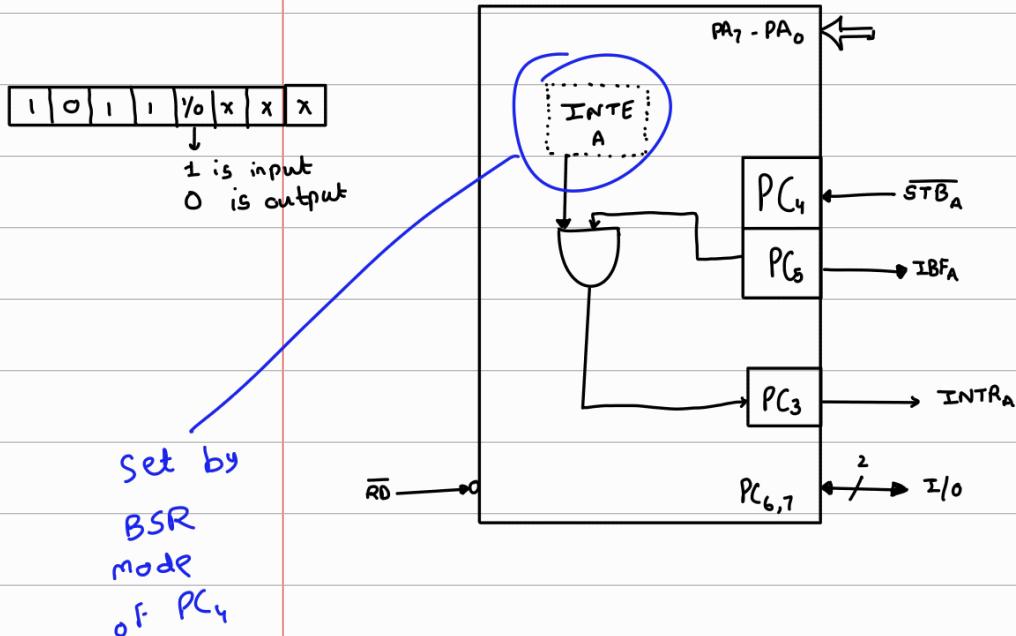
NEXT:

MOV AL, FOH  
OUT 84H, AL  
RET

When processor checks status of I/O devices this is Polling. (Processor waste time)

Q. Configure Port A , Port B as input ports in mode 1

A  
 $\frac{10110110}{B \quad 6}$



\* Program Driven Data Transfer .

aka [Polled I/O Mode] ?

WAP for setting INTEA flag [for port f in o/p port in mode 1]

BACK :

```
IN AL,30H  
CMP AL,FFH  
JZ BACK
```

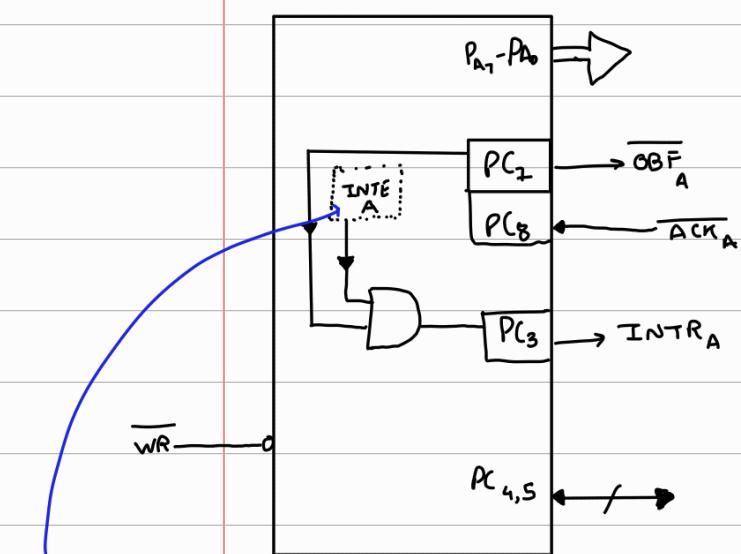
} 'Polled I/O Mode?' driven data transfer  
[loop till input given by user]

Interrupt Driven data transfer :

```
MOV AL, B0H  
OUT 36H, AL  
MOV AL, 09H  
OUT 36H, AL
```

NMISBB:

```
IN AL,30H  
MOV [BX], AL  
IRET
```



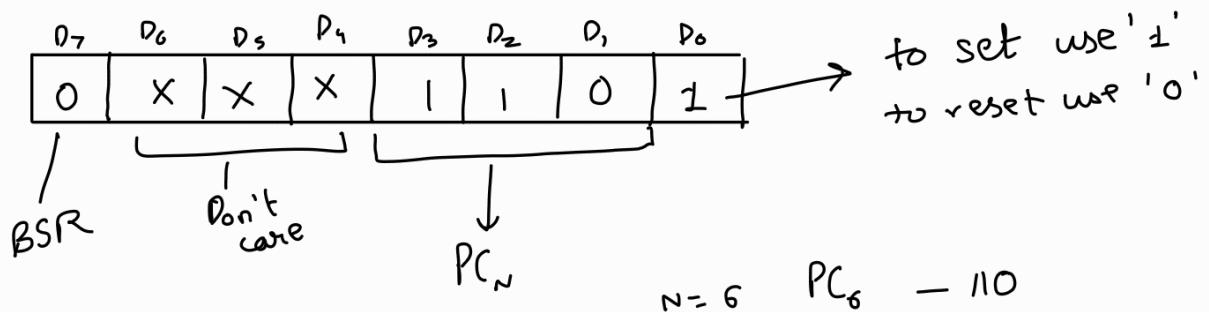
Controlled by  
BSR of  $PC_C$   
↓  
bit  
set/reset!

- Status word of 8255 can be read by reading Port C.

```

MOV BX, 3000
MOV AL, [BX]
OUT 30, AL

```



(Configure 8255 in mode 1 output (port A) : assume base address 80H.

1010 0100  
A      4

MOV AL, A4H

OUT 86H, AL

1010 0000  
A      0

MOV AL, A0H

OUT 86H, AL

MOV BX, 3000H

MOV AL, [BX]

d. Configure 8255 in mode 1 op:

OUT 80, AL

1011 0100

e. WAP for setting INTEA for port A in output mode 1 of 8255

MOV AL, A0H

this came from  
data sheet.

OUT 86H, AL

XXX   

MOV AL, 0DH

OUT 86H, AL

MOV BX, 3000H

NMI SUBB:

MOV AL, [BX]

OUT 80H, AL

INC BX

IRET

Q. Interface 4 digit, 7 segment LED display to 8086 through 8255.

A) Configure Port A as o/p port in mode 0 for segments of the LED. Configure Port C lower as o/p port- in mode 0 for digit port of the displays,

K - common cathode type of displays.

B)  $\frac{1}{1} \cdot E \frac{1}{1} \cdot \frac{1}{1}$ , as flashing display.

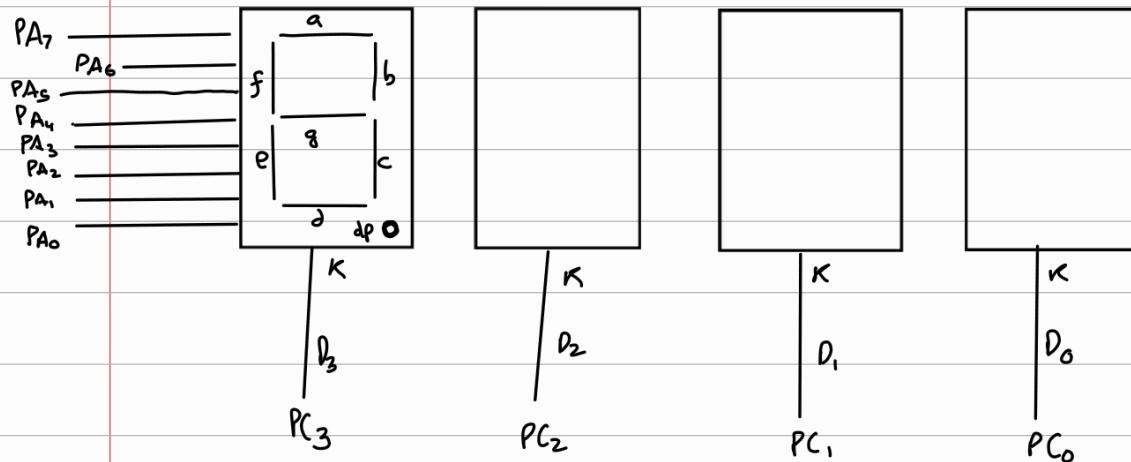
Assuming Port connected at 80H.

$\frac{1000}{8} \frac{x}{0} \frac{x}{H}$

MOV AL, 80H

OUT 86H, AL

A	80H
B	82H
C	84H
CR	86H



dp - decimal point.

A) MOV AL, 80H  
OUT 86H, AL

a  
F | g | b  
e | | c  
d | o  
f | a |  
e | | j

MOV AL, 76H  
OUT 80, AL

MOV AL, 07H

OUT 84, AL

CALL DELAY

; FOR E

MOV AL, 79H

OUT 80H, AL

MOV AL, 0BH

OUT 84H, AL

CALL DELAY

; FOR L

MOV AL, 38H

OUT 80H, AL

MOV AL, 0DH



OUT 84H, 0DH ; 86?  
CALL DELAY

; For O

MOV AL, 3FH  
OUT 80H, AL  
MOV AL, 0EH  
OUT 84H, AL  
CALL DELAY

PA<sub>7</sub> - . . . . . PA<sub>0</sub>

dp g f e d c b a  
0 1 1 1 0 1 1 0  
7 6

0 1 1 1 0 0 1  
7 9

a  
f | — | b  
e | — | c  
d | — |  
0 1 0 1 1 1 1  
7

/ /

---

;

; For blank

MOV AL, 00H

OUT 80H, AL

MOV AL, 00H

OUT 84H, AL

CALL DELAY

JMP BACK.

---

Q. Interface scanned keyboard.