`timescale 1ns / 1ps

// Author: Ghulam Sarwar

//2\_Bit\_comparator

module Task\_\_01(Eq,L\_th,G\_th,A0,A1,B0,B1);// initialize all inputs and outputs

input A0,A1,B0,B1; // set the Inputs

output Eq, L\_th, G\_th;// set the outputs

wire a0,a1,b0,BB1,an1,an2,an4,an5,an6,xnr1,xnr2; //dclare the wires that we use in our hardware programming

not Not1(a0,A0); //By use Not gate, we will get inverse of all the inputs that will we use later

not Not2(a1,A0);

not Not3(b0,B0);

not Not4(BB1,B1);

//2\_Bit number 'Greater\_than' comparator Logic (A>B=(A0 B1' B0')+(A1 B1')+(A1 A0 B0'))

and and1(an1,A0,BB1,b0);

and and2(an2,A1,BB1);

and and3(an3,A1,A0,b0);

or or1(G\_th,an1,an2,an3);

//2\_Bit number 'Equal' comparator Logic ((A0 Ex-Nor B0)(A1 Ex-Nor B1))

xnor xnor1(xnr1,A0,B0);

xnor xnor2(xnr2,A1,B1);

and and4(Eq,xnr1,xnr2);

//2\_Bit number 'Less\_than' comparator Logic ((A1' A0' B0)+(A0' B1 B0)+(A1' B1))

and and5(an4,a1,a0,B0);

and and6(an5,a0,B1,B0);

and and7(an6,a1,B1);

or or2(L\_th,an4,an5,an6);

endmodule