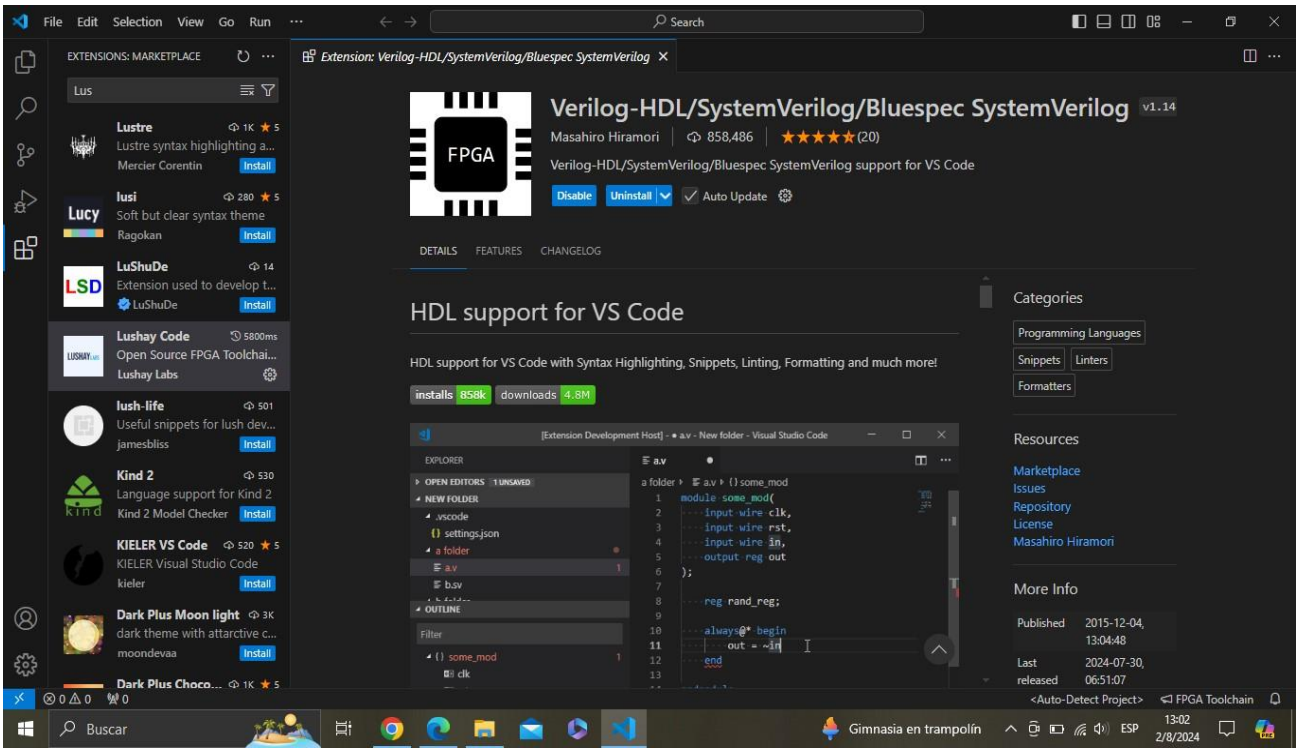
Tutorial Diseño Lógico

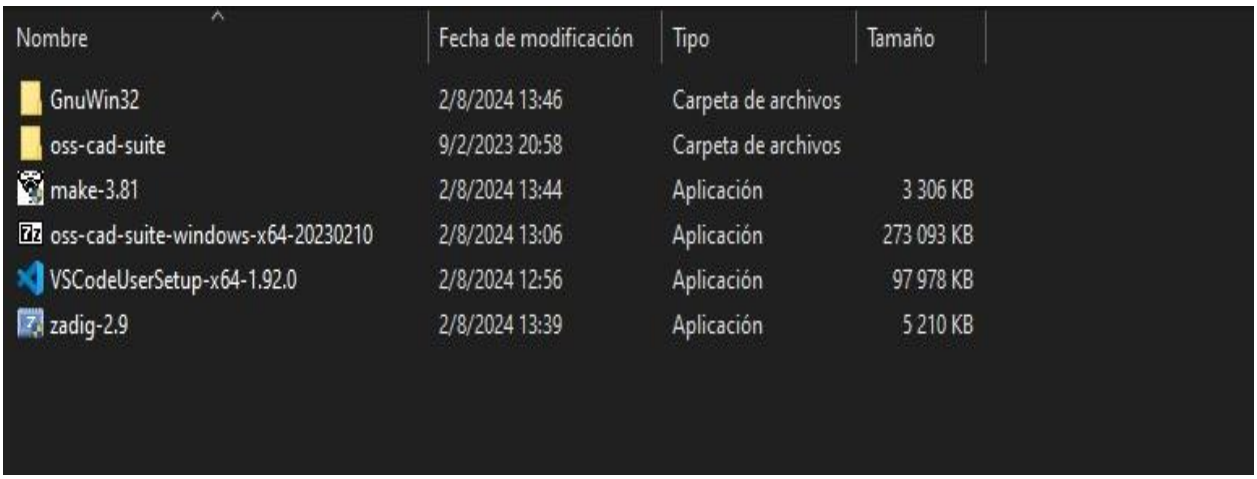
Estudiante: Sary Vargas Zamora (2022129491)

Evidencias Parte 1:

Instalación de la extensión Lushay Code

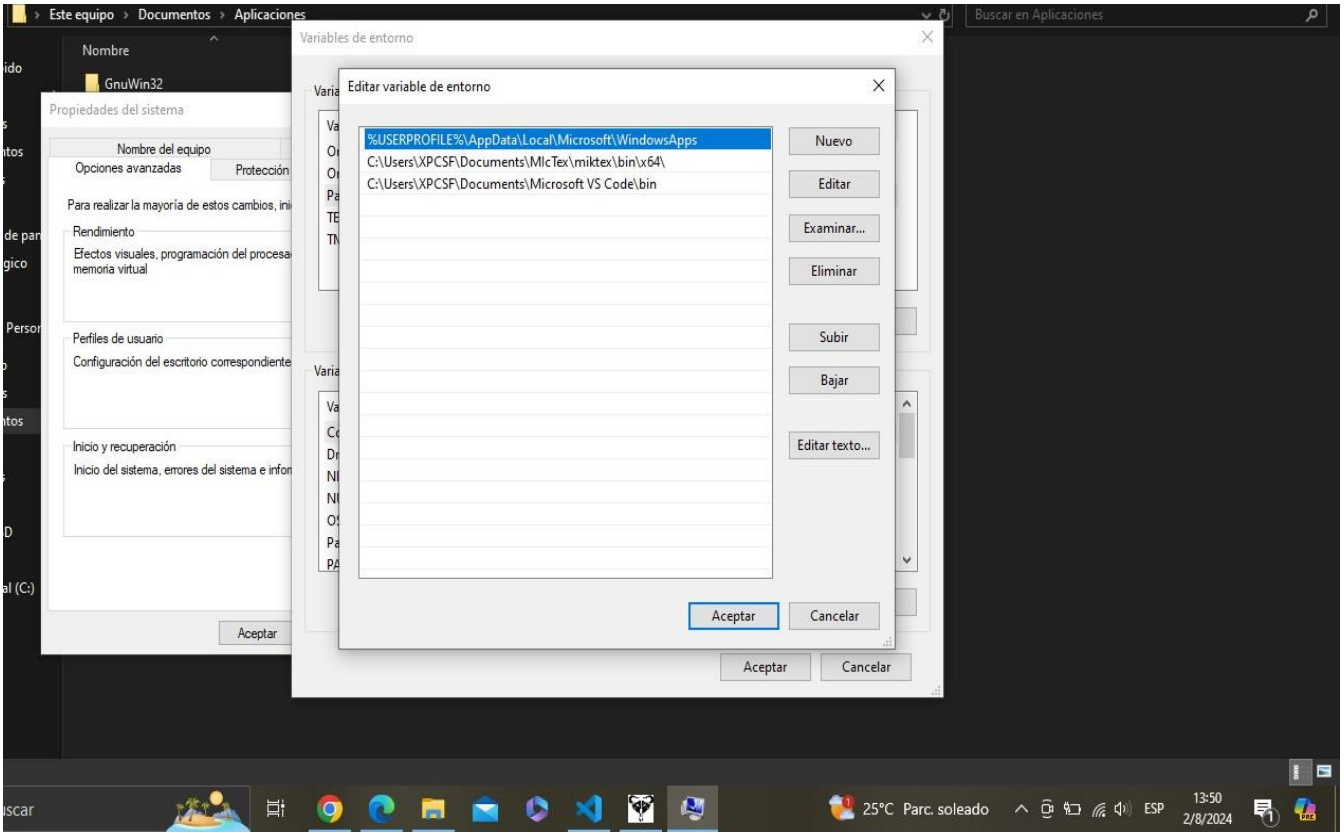


Instalación del OSS-Cad-Suite de YosysHQ e Instalación de GNU-Make



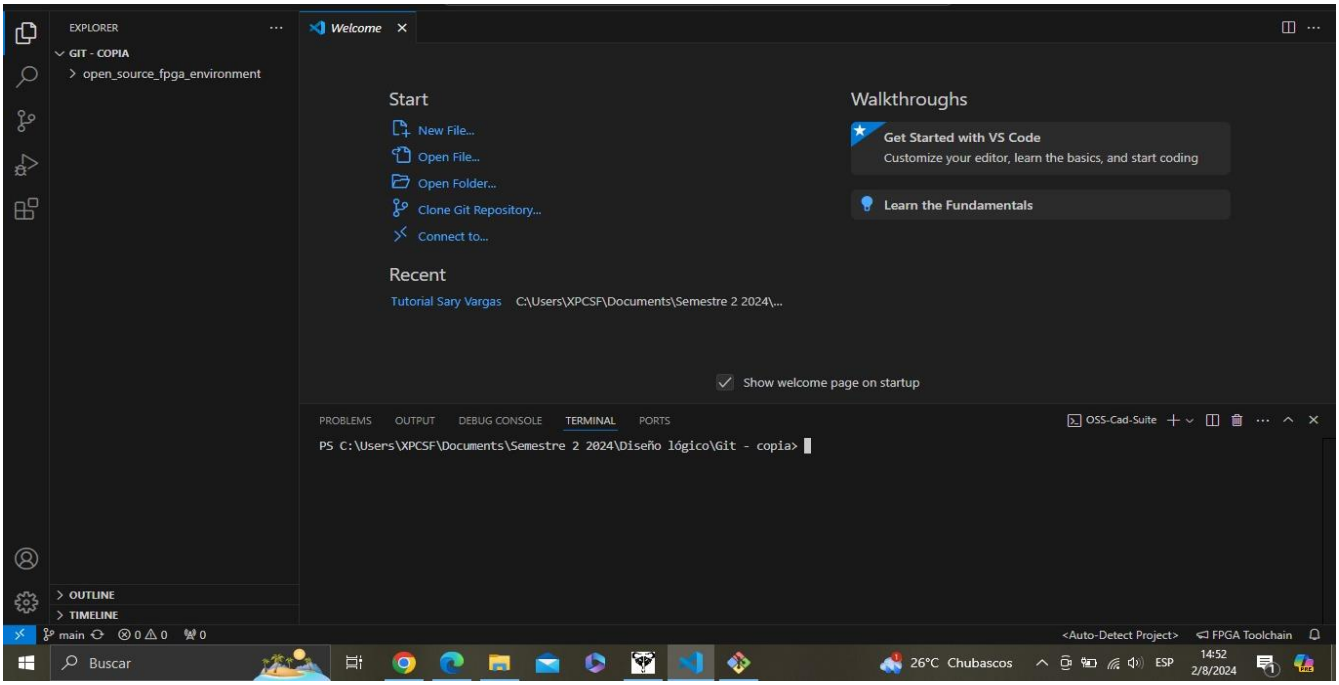
Nombre	Fecha de modificación	Tipo	Tamaño
GnuWin32	2/8/2024 13:46	Carpeta de archivos	
oss-cad-suite	9/2/2023 20:58	Carpeta de archivos	
make-3.81	2/8/2024 13:44	Aplicación	3 306 KB
oss-cad-suite-windows-x64-20230210	2/8/2024 13:06	Aplicación	273 093 KB
VSCodeUserSetup-x64-1.92.0	2/8/2024 12:56	Aplicación	97 978 KB
zadig-2.9	2/8/2024 13:39	Aplicación	5 210 KB

Agregar Make al Path

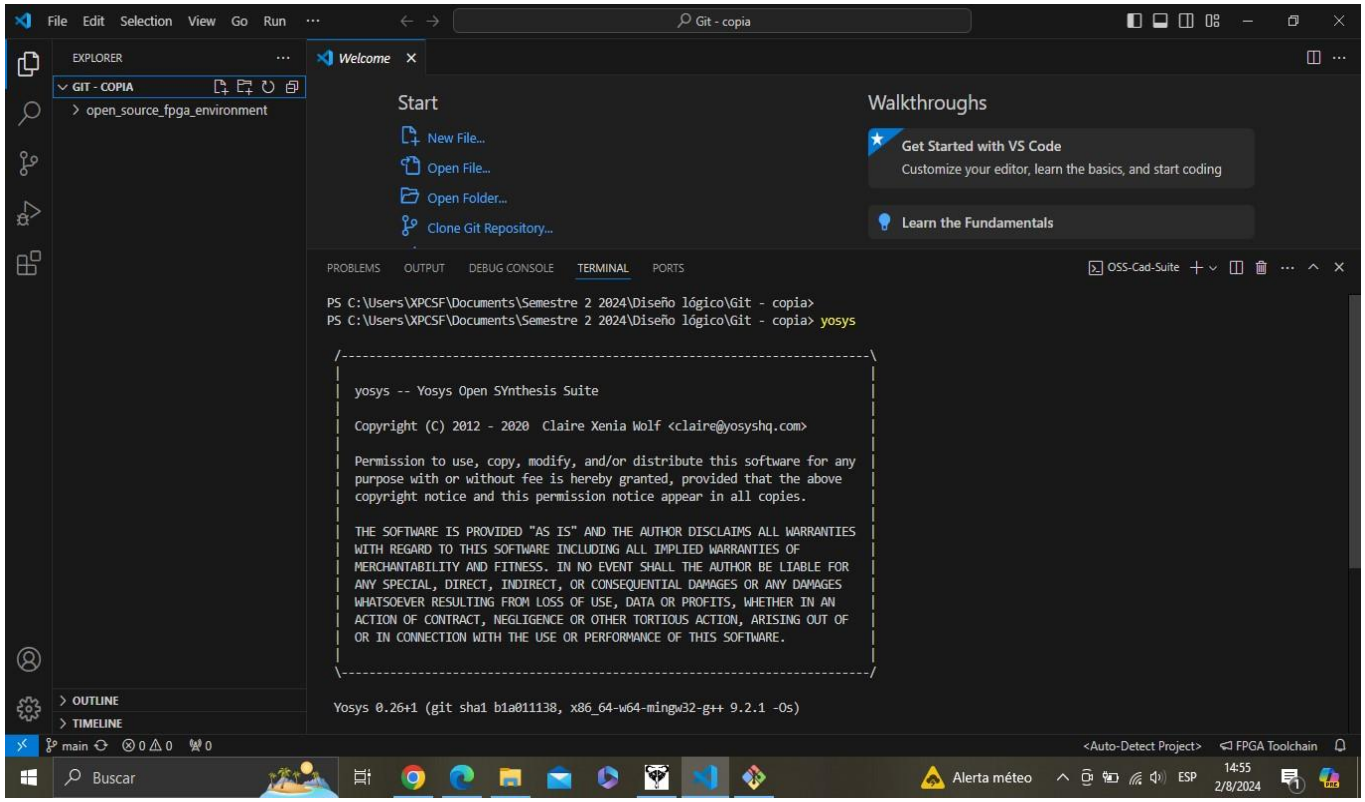


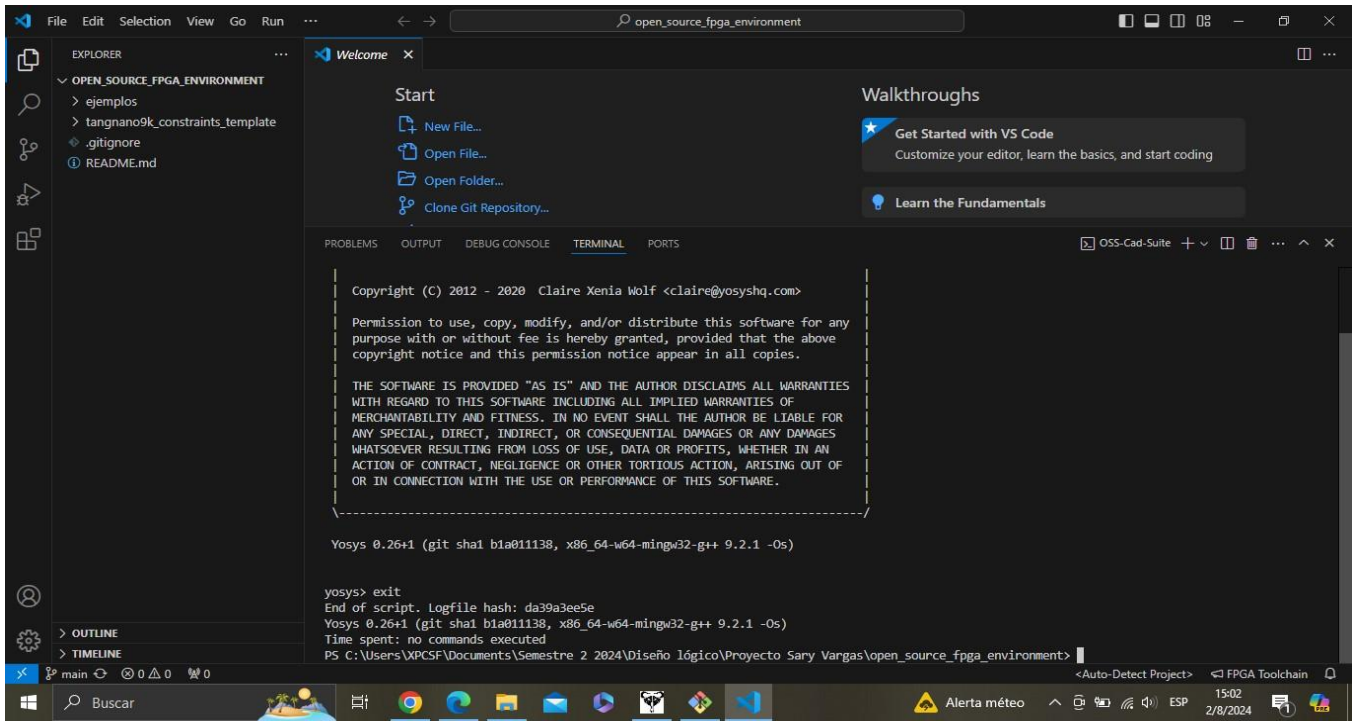
Evidencias Parte 2:

Inicializar la terminal del toolchain:

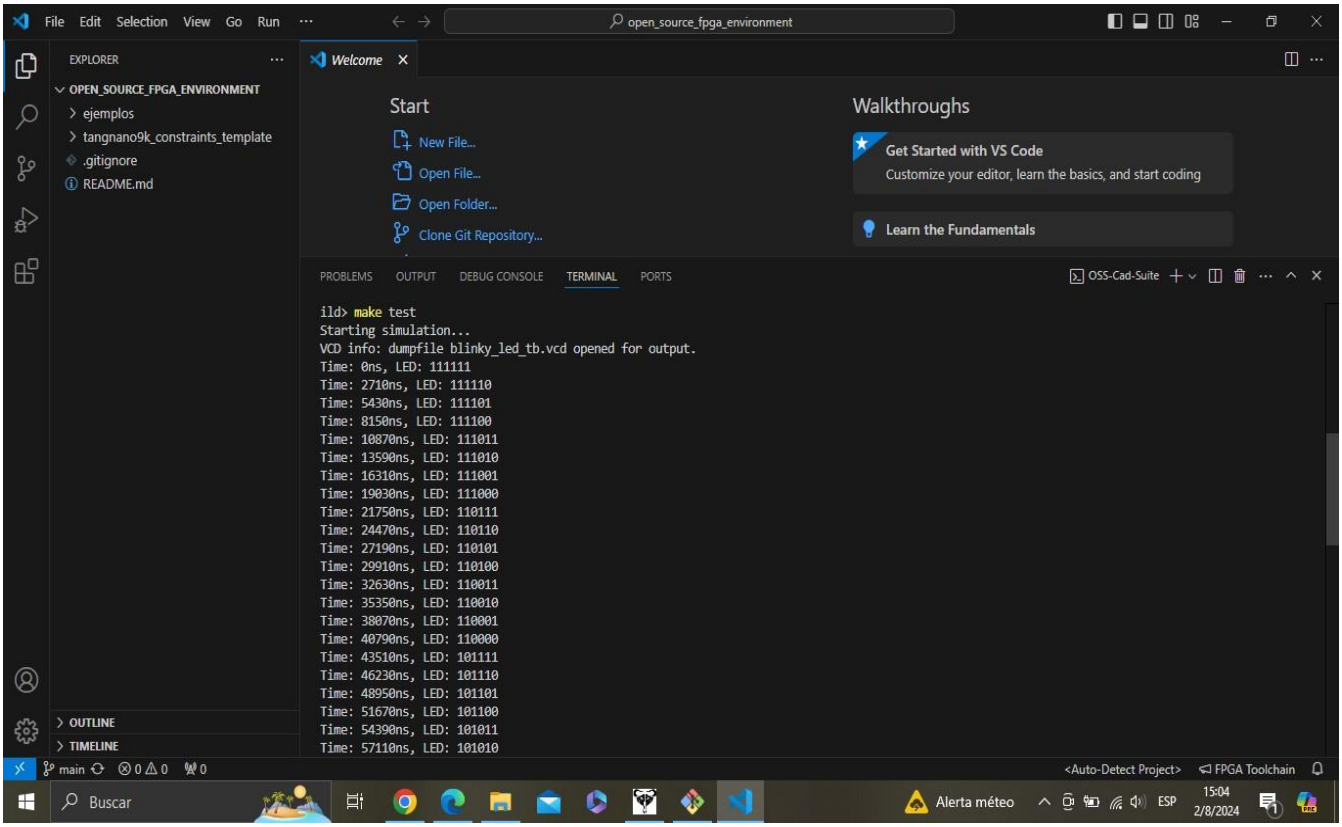


Comando yosys:

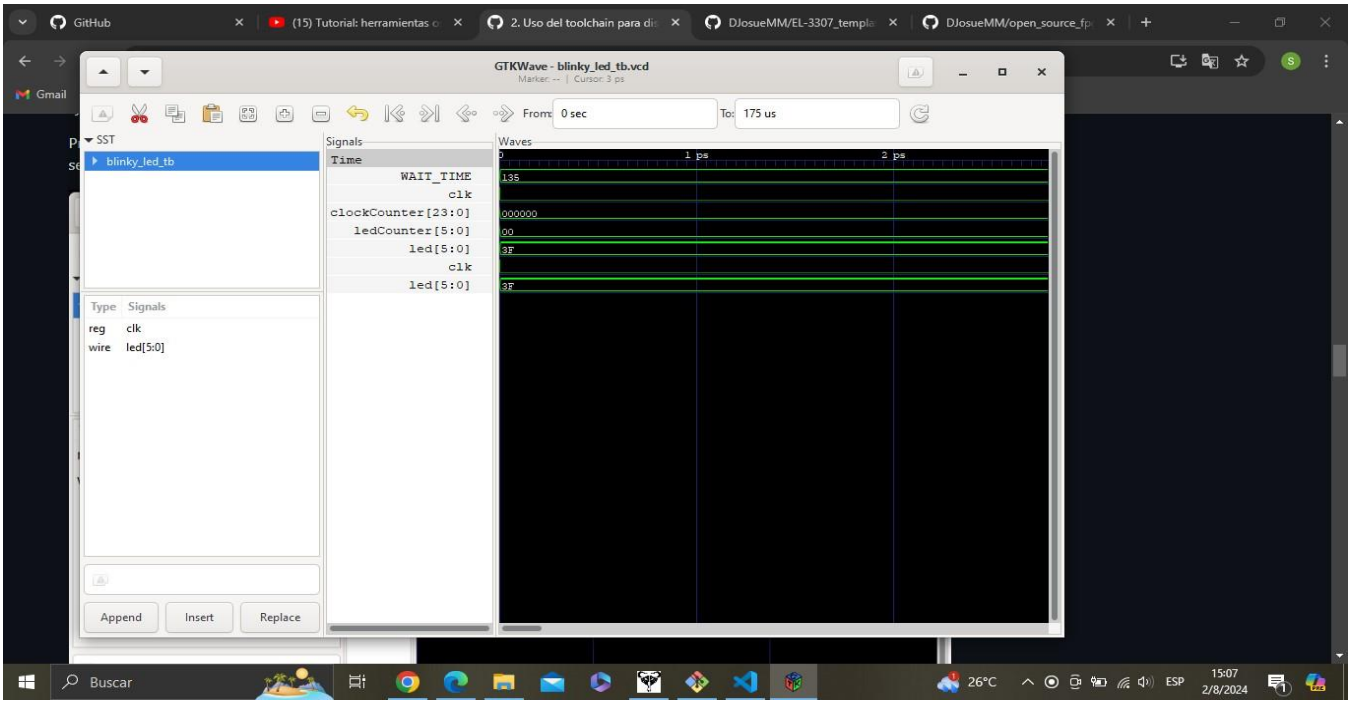




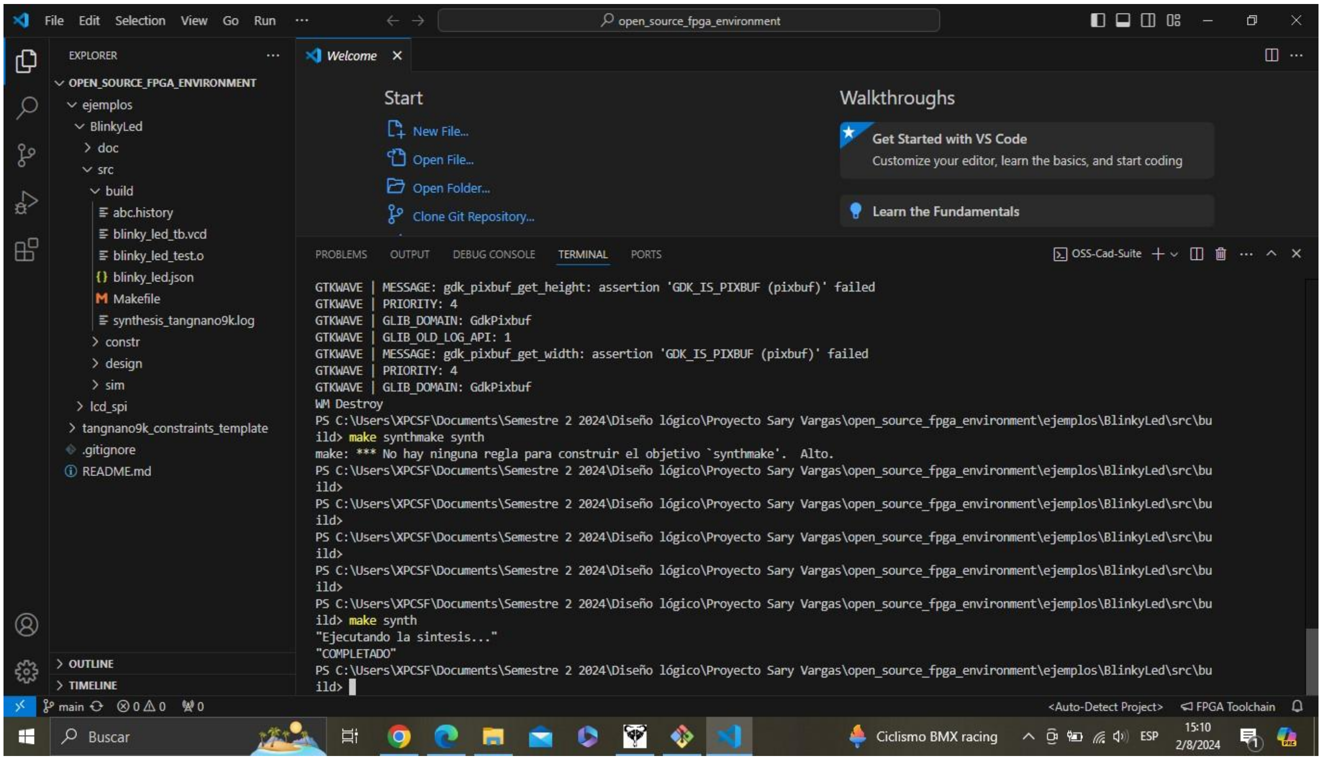
Comando make test:



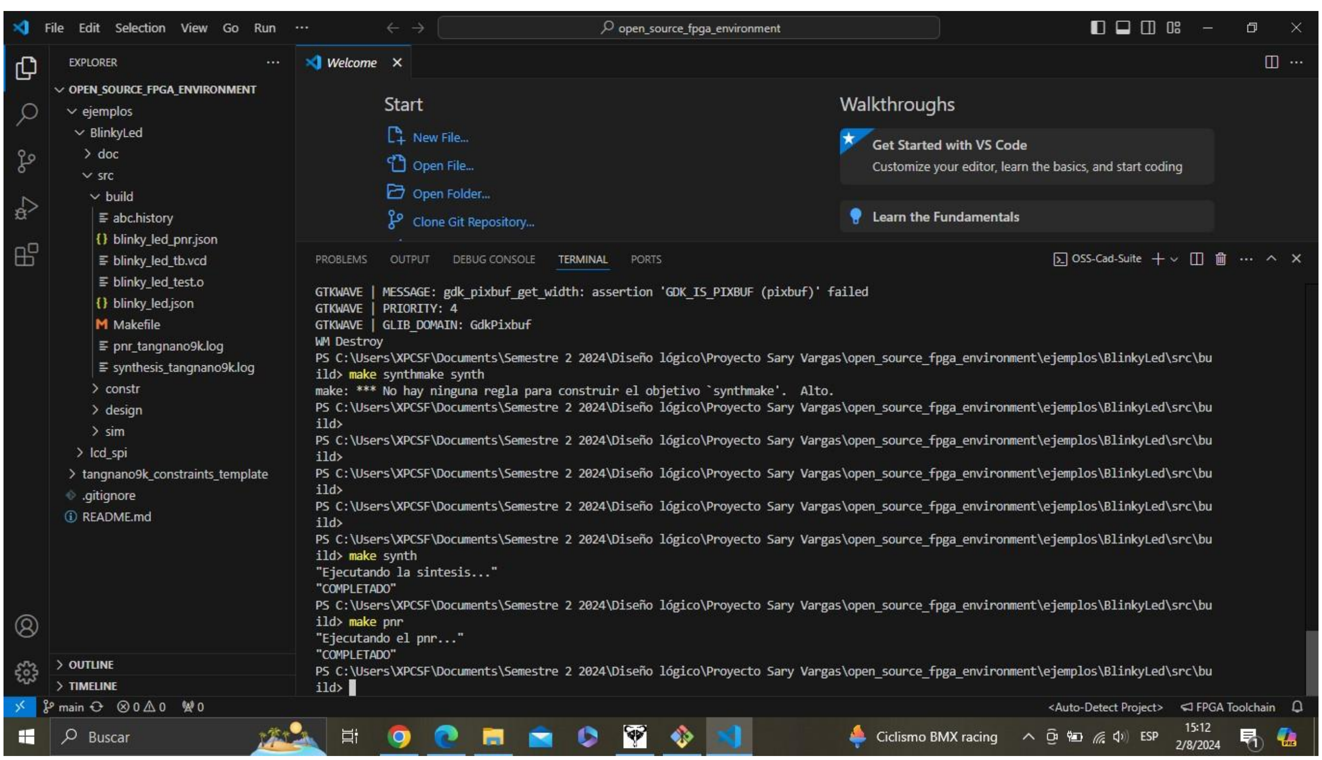
Comando make wv:



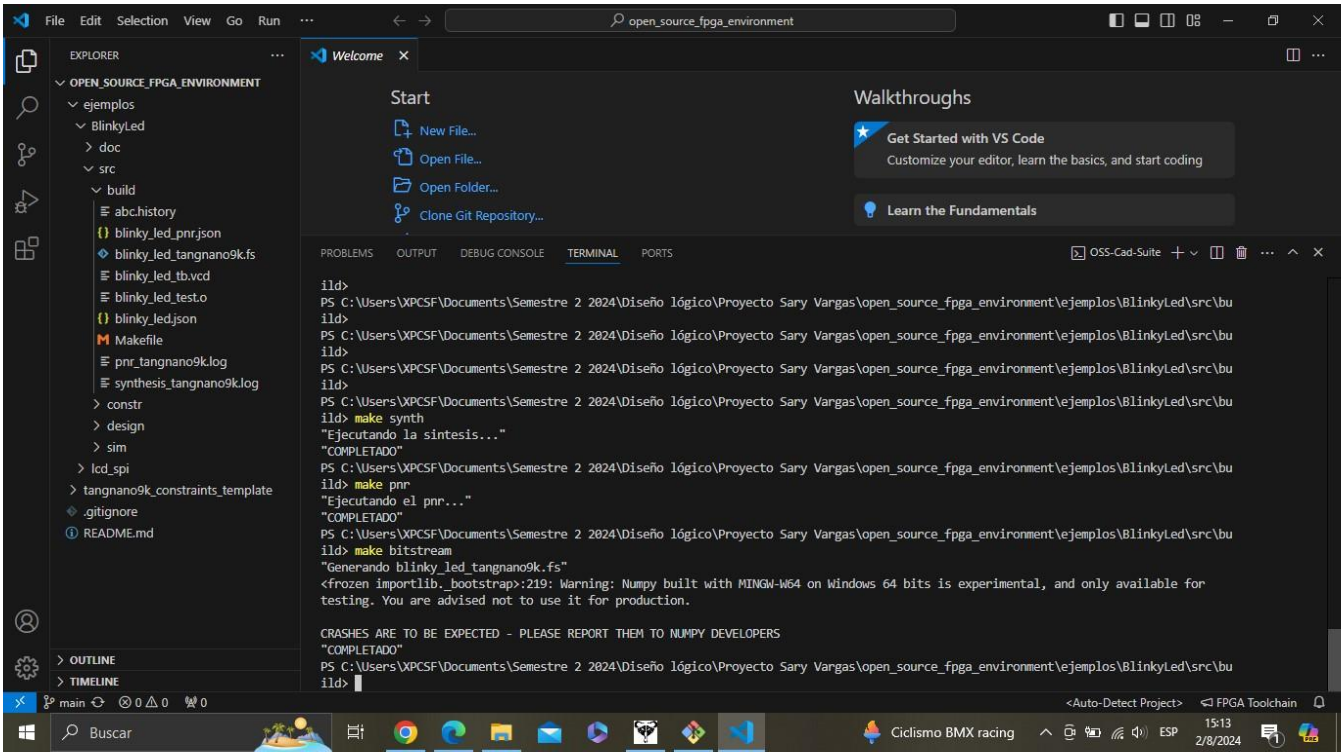
Comando make synth:



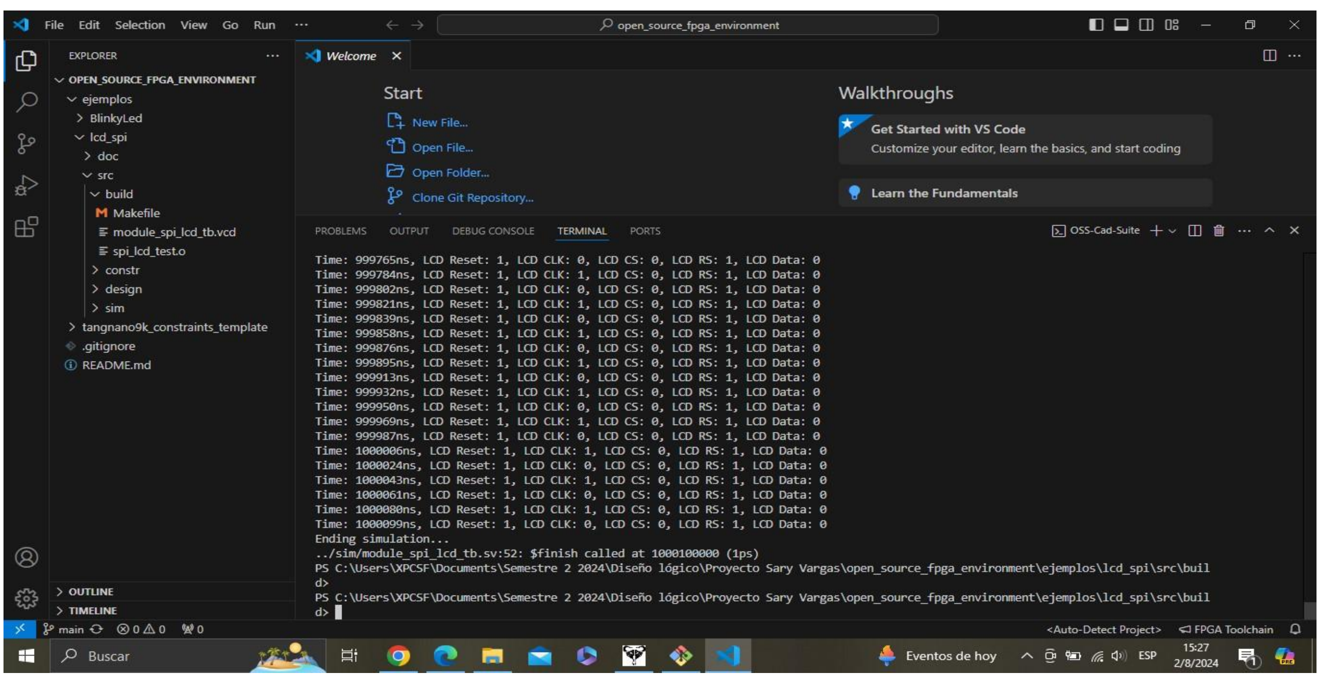
Comando pnr:

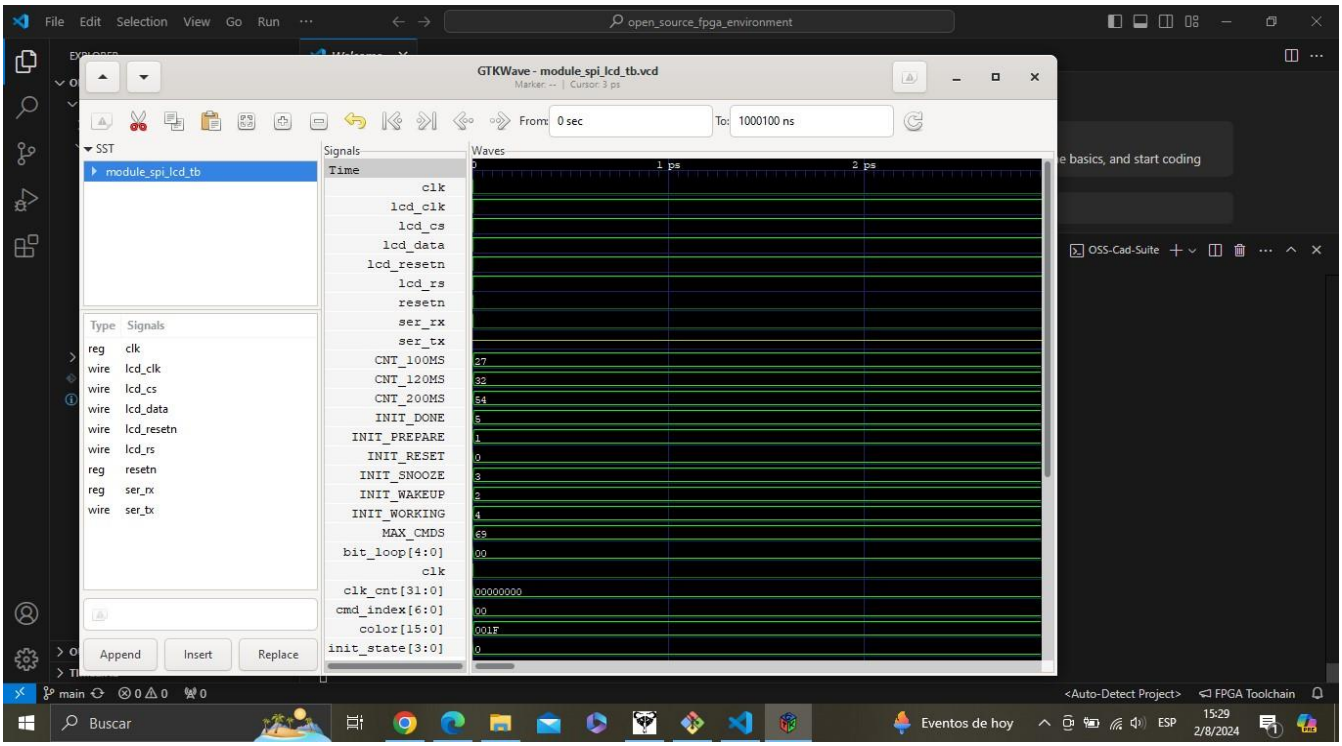


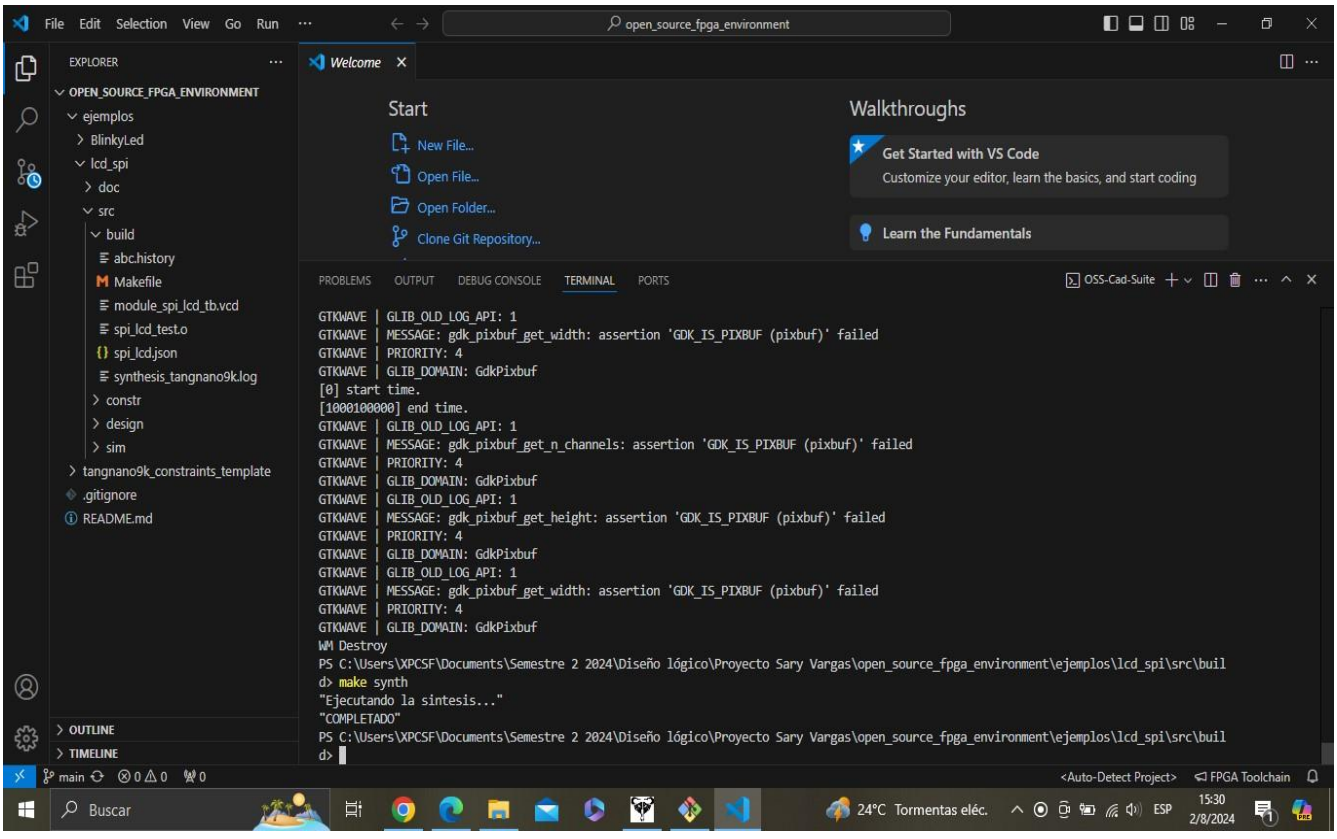
Comando make bitstream:

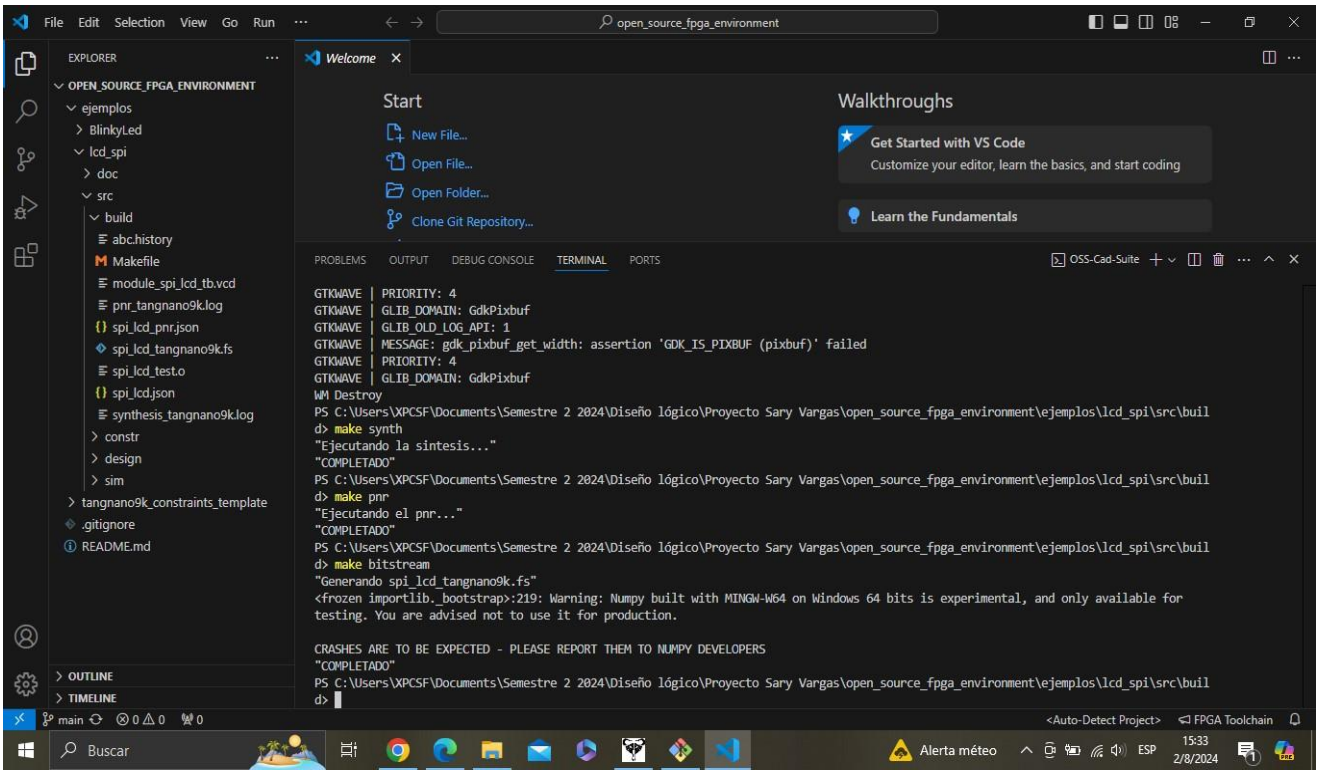


Carpeta carpeta build del ejemplo **lcd_spi:**

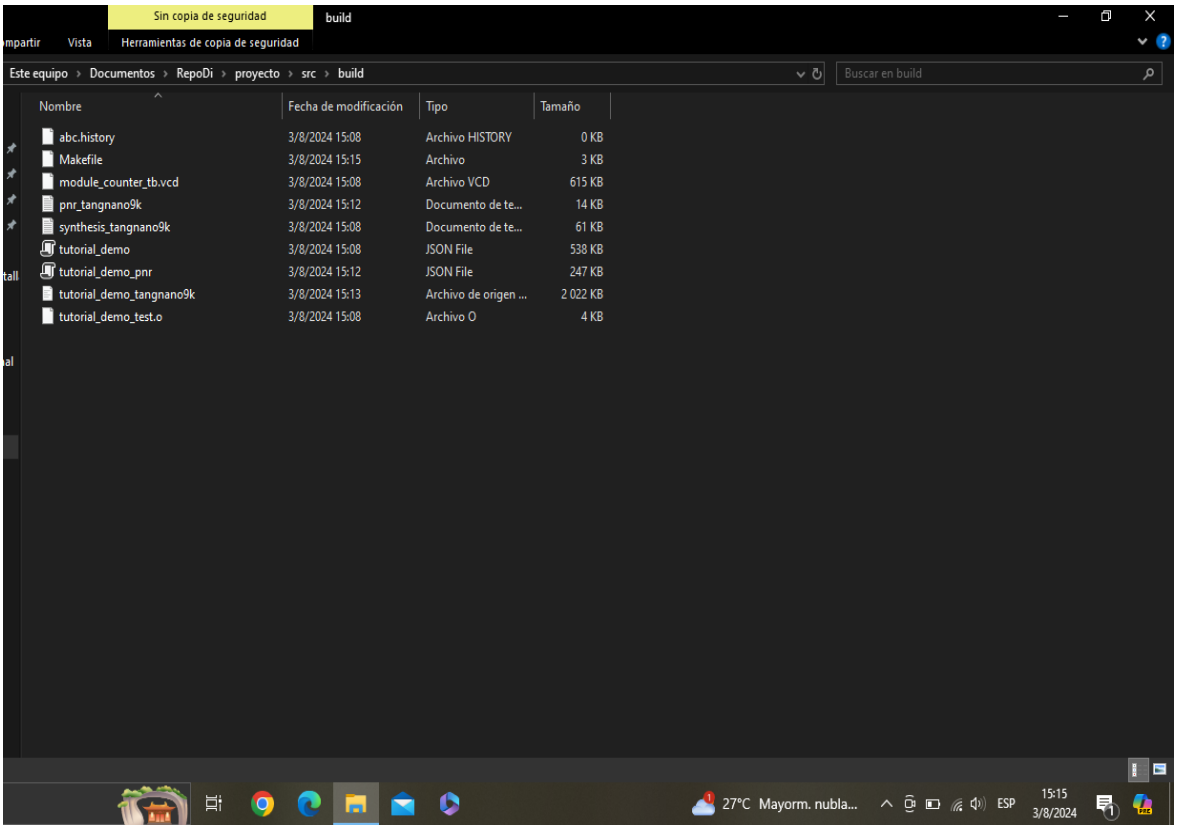


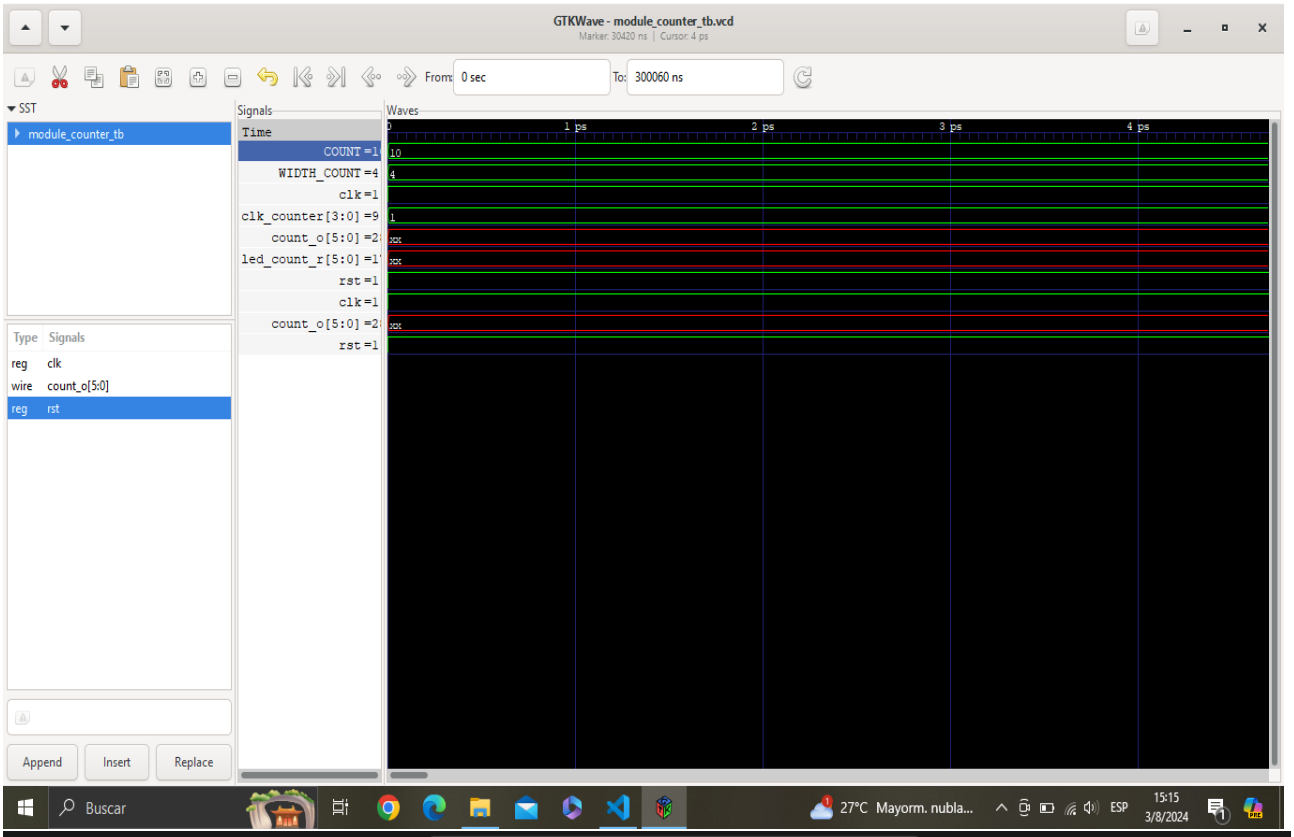

File Edit Selection View Go Run
open_source_fpga_environment
GTKWave - module_spi_lcd_tb.vcd
From: 0 sec
To: 1000100 ns
SST
module_spi_lcd_tb
Signals
Waves
Time
clk
lcd_clk
lcd_cs
lcd_data
lcd_resetn
lcd_rs
resetn
ser_rx
ser_tx
CNT_100MS
CNT_120MS
CNT_200MS
INIT_DONE
INIT_PREPARE
INIT_RESET
INIT_SNOOZE
INIT_WAKEUP
INIT_WORKING
MAX_CMDS
bit_loop[4:0]
clk_cnt[31:0]
cmd_index[6:0]
color[15:0]
init_state[3:0]
Type Signals
reg clk
wire lcd_clk
wire lcd_cs
wire lcd_data
wire lcd_resetn
wire lcd_rs
reg resetn
reg ser_rx
wire ser_tx
Append
Insert
Replace
1 ps
2 ps
OSS-Cad-Suite
<Auto-Detect Project>
FPGA Toolchain
Buscar
Eventos de hoy
ESP
15:29
2/8/2024

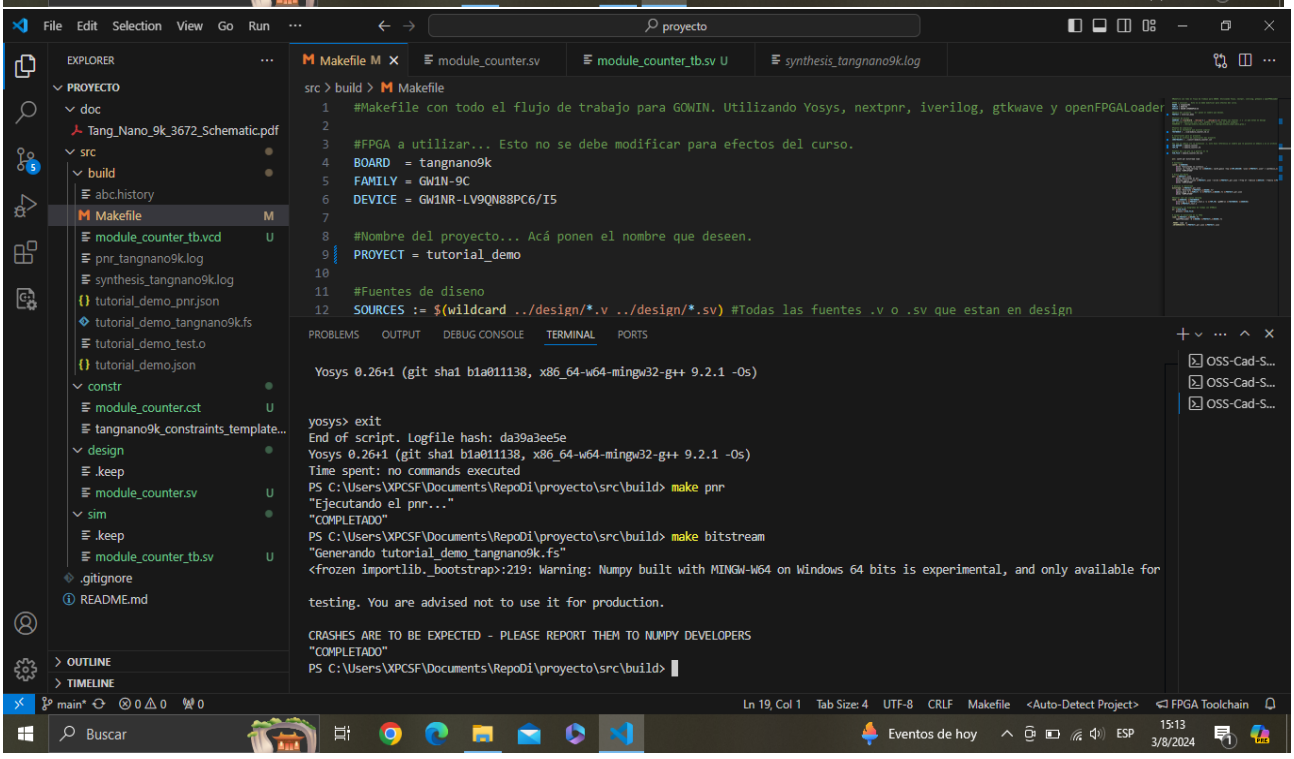

File Edit Selection View Go Run
open_source_fpga_environment
EXPLORER
OPEN_SOURCE_FPGA_ENVIRONMENT
ejemplos
BlinkyLed
lcd_spi
doc
src
build
abc.history
Makefile
module_spi_lcd_tb.vcd
spi_lcd_test.o
spi_lcd.json
synthesis_tangnano9k.log
constr
design
sim
tangnano9k_constraints_template
.gitignore
README.md
OUTLINE
TIMELINE
Welcome
Start
New File...
Open File...
Open Folder...
Clone Git Repository...
Walkthroughs
Get Started with VS Code
Customize your editor, learn the basics, and start coding
Learn the Fundamentals
PROBLEMS
OUTPUT
DEBUG CONSOLE
TERMINAL
PORTS
OSS-Cad-Suite
GTKWAVE | GLIB_OLD_LOG_API: 1
GTKWAVE | MESSAGE: gdk_pixbuf_get_width: assertion 'GDK_IS_PIXBUF (pixbuf)' failed
GTKWAVE | PRIORITY: 4
GTKWAVE | GLIB_DOMAIN: GdkPixbuf
[0] start time.
[1000100000] end time.
GTKWAVE | GLIB_OLD_LOG_API: 1
GTKWAVE | MESSAGE: gdk_pixbuf_get_n_channels: assertion 'GDK_IS_PIXBUF (pixbuf)' failed
GTKWAVE | PRIORITY: 4
GTKWAVE | GLIB_DOMAIN: GdkPixbuf
GTKWAVE | GLIB_OLD_LOG_API: 1
GTKWAVE | MESSAGE: gdk_pixbuf_get_height: assertion 'GDK_IS_PIXBUF (pixbuf)' failed
GTKWAVE | PRIORITY: 4
GTKWAVE | GLIB_DOMAIN: GdkPixbuf
GTKWAVE | GLIB_OLD_LOG_API: 1
GTKWAVE | MESSAGE: gdk_pixbuf_get_width: assertion 'GDK_IS_PIXBUF (pixbuf)' failed
GTKWAVE | PRIORITY: 4
GTKWAVE | GLIB_DOMAIN: GdkPixbuf
WM Destroy
PS C:\Users\XPCSF\Documents\Semestre 2 2024\Diseño lógico\Proyecto Sary Vargas\open_source_fpga_environment\ejemplos\lcd_spi\src\buil
d> make synth
"Ejecutando la sintesis..."
"COMPLETADO"
PS C:\Users\XPCSF\Documents\Semestre 2 2024\Diseño lógico\Proyecto Sary Vargas\open_source_fpga_environment\ejemplos\lcd_spi\src\buil
d>
<Auto-Detect Project>
FPGA Toolchain
Buscar
24°C Tormentas eléc.
ESP
15:30
2/8/2024

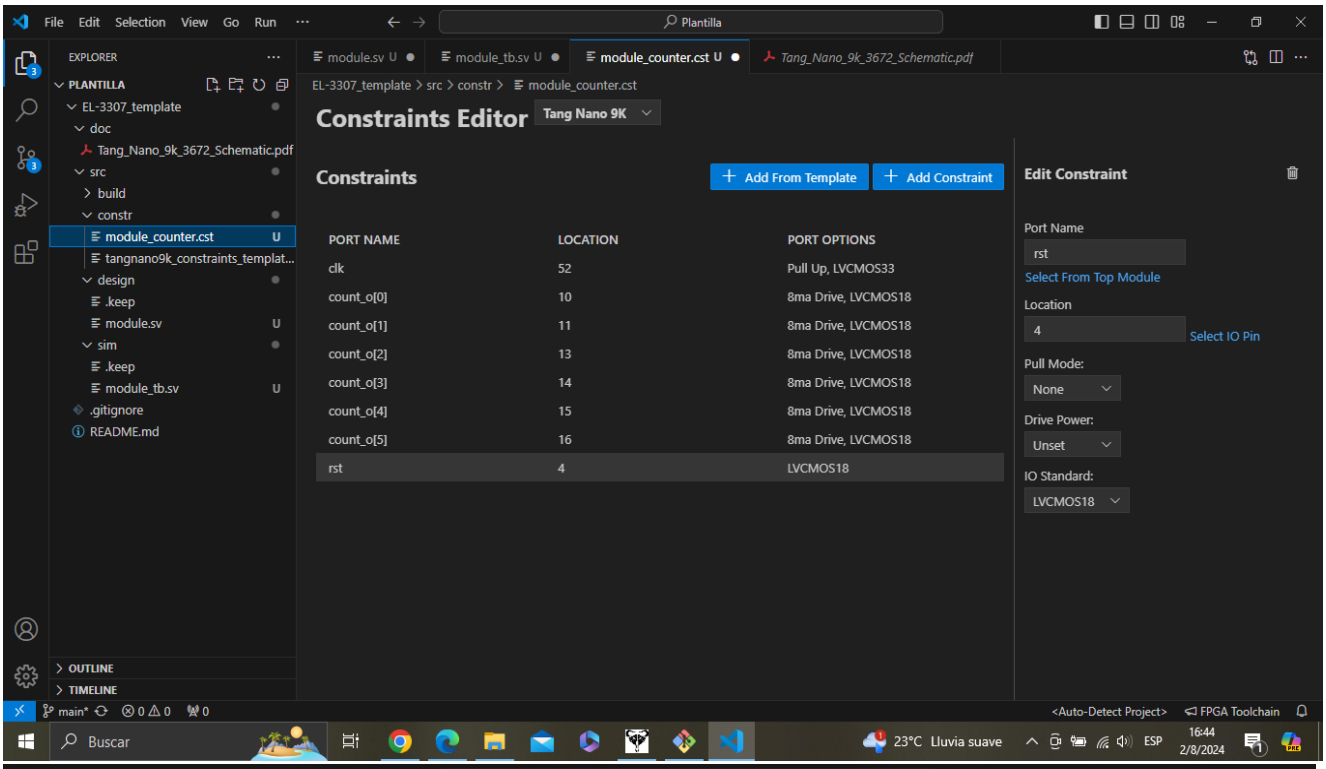


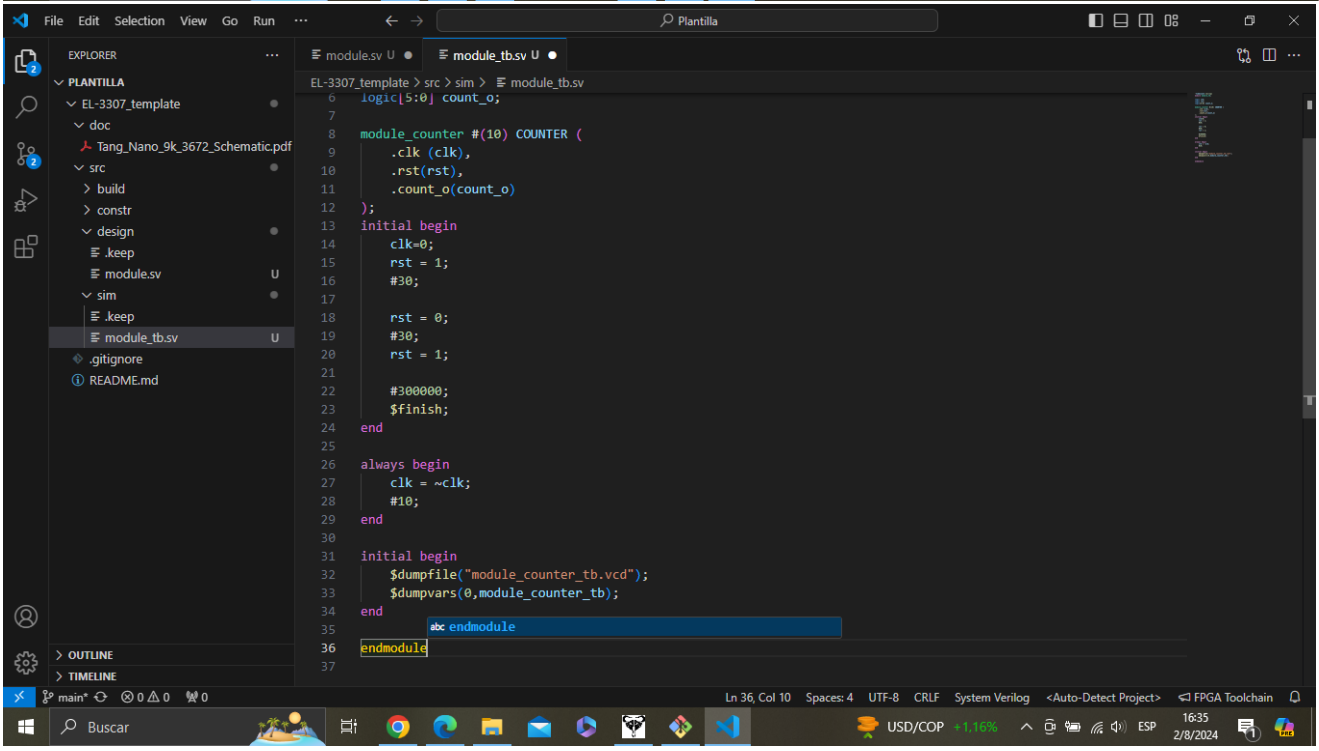
Evidencias Parte 3: Video

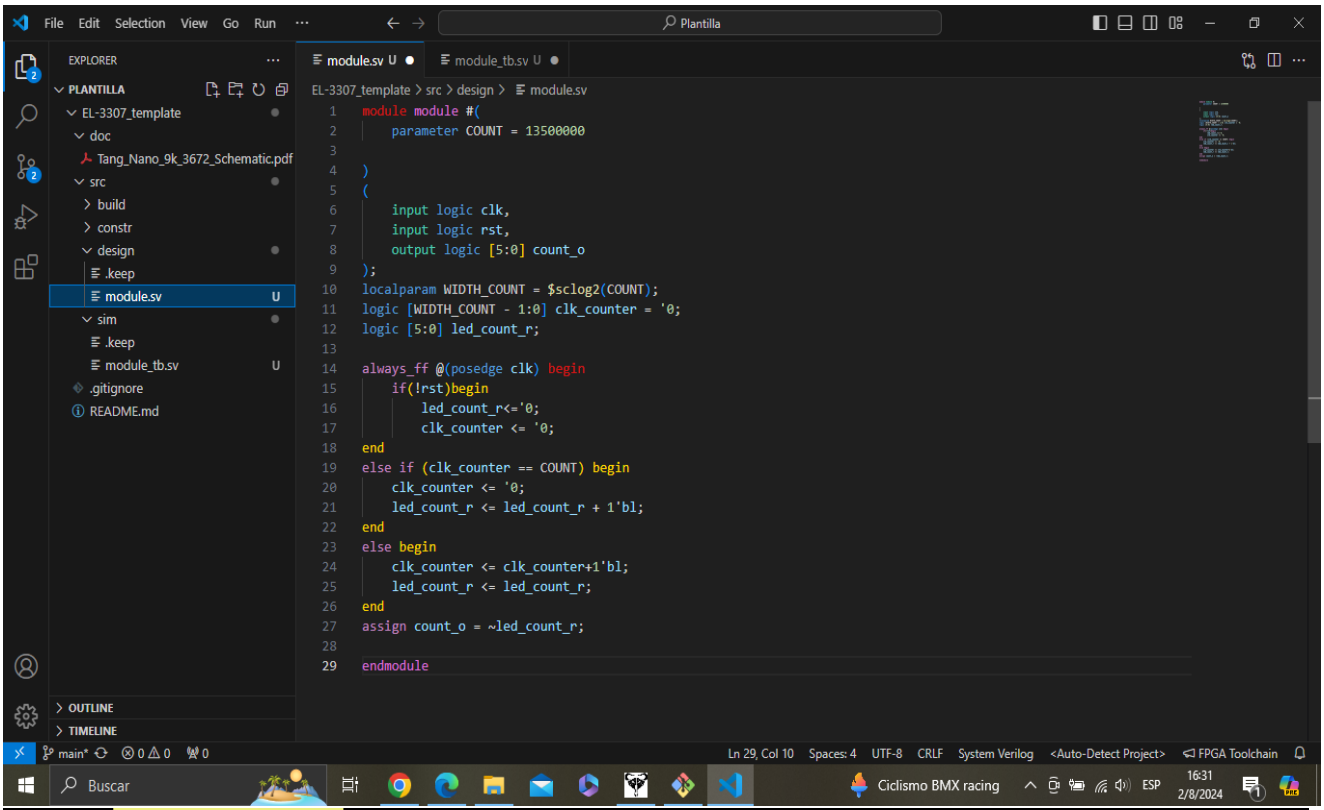


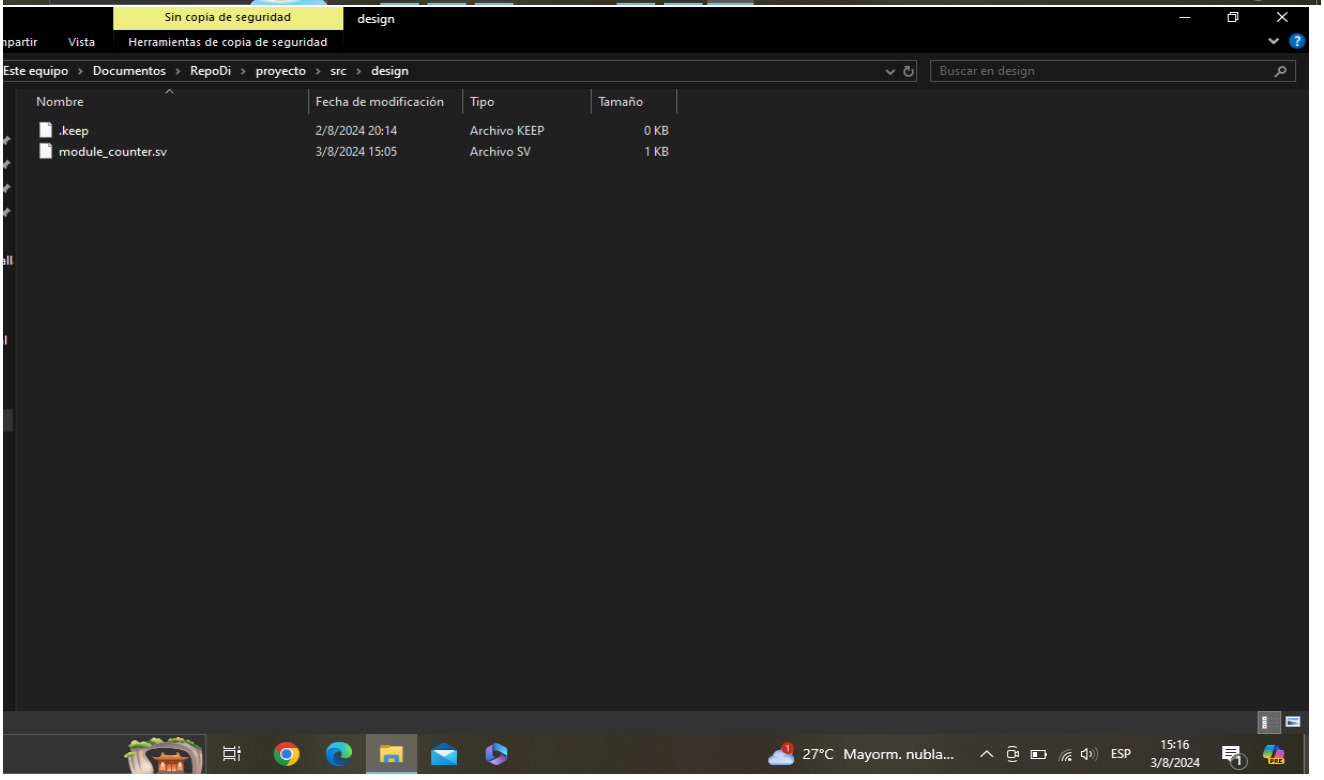

GTKWave - module_counter_tb.vcd
Marker: 30420 ns | Cursor: 4 ps
From: 0 sec
To: 300060 ns
SST
module_counter_tb
Signals
Time
COUNT = 1
WIDTH_COUNT = 4
clk = 1
clk_counter[3:0] = 9
count_o[5:0] = 2
led_count_r[5:0] = 1
rst = 1
clk = 1
count_o[5:0] = 2
rst = 1
Waves
1 ps
2 ps
3 ps
4 ps
Type Signals
reg clk
wire count_o[5:0]
reg rst
Append
Insert
Replace
Buscar
27°C Mayorm. nubla...
ESP
15:15
3/8/2024

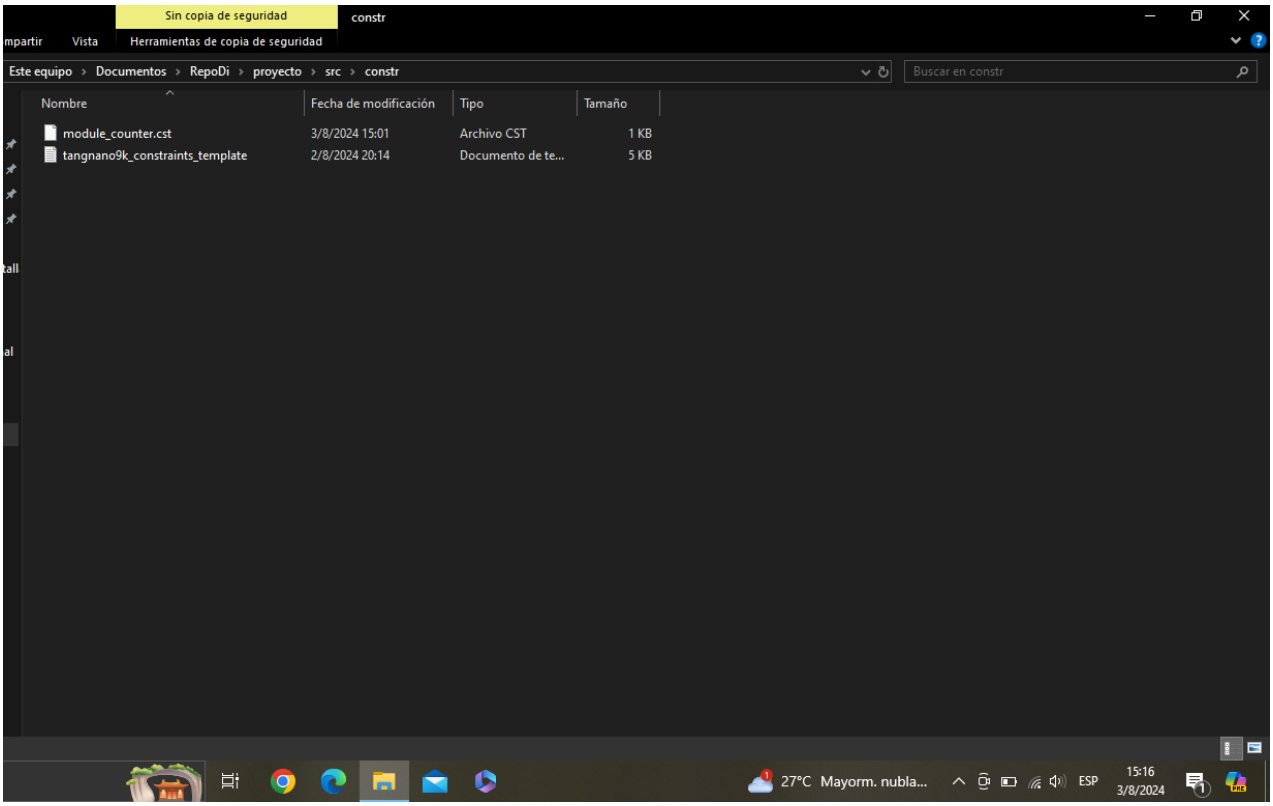

File Edit Selection View Go Run
proyecto
EXPLORER
PROYECTO
doc
Tang_Nano_9k_3672_Schematic.pdf
src
build
abc.history
Makefile M
module_counter_tb.vcd U
pnr_tangnano9k.log
synthesis_tangnano9k.log
tutorial_demo_pnr.json
tutorial_demo_tangnano9k.fs
tutorial_demo_test.o
tutorial_demo.json
constr
module_counter.cst U
tangnano9k_constraints_template...
design
.keep
module_counter.sv U
sim
.keep
module_counter_tb.sv U
.gitignore
README.md
OUTLINE
TIMELINE
Makefile M
module_counter.sv
module_counter_tb.sv U
synthesis_tangnano9k.log
src > build > Makefile
#Makefile con todo el flujo de trabajo para GOWIN. Utilizando Yosys, nextpnr, iverilog, gtkwave y openFPGALoader
#FPGA a utilizar... Esto no se debe modificar para efectos del curso.
BOARD = tangnano9k
FAMILY = GW1N-9C
DEVICE = GW1NR-LV9QN88PC6/I5
#Nombre del proyecto... Acá ponen el nombre que deseen.
PROYECT = tutorial_demo
#Fuentes de diseno
SOURCES := $(wildcard ../design/*.v ../design/*.sv) #Todas las fuentes .v o .sv que estan en design
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL PORTS
Yosys 0.26+1 (git sha1 b1a011138, x86_64-w64-mingw32-g++ 9.2.1 -Os)
yosys> exit
End of script. Logfile hash: da39a3ee5e
Yosys 0.26+1 (git sha1 b1a011138, x86_64-w64-mingw32-g++ 9.2.1 -Os)
Time spent: no commands executed
PS C:\Users\XPCSF\Documents\RepoDi\proyecto\src\build> make pnr
"Ejecutando el pnr..."
"COMPLETADO"
PS C:\Users\XPCSF\Documents\RepoDi\proyecto\src\build> make bitstream
"Generando tutorial_demo_tangnano9k.fs"
<frozen importlib._bootstrap>:219: Warning: Numpy built with MINGW-W64 on Windows 64 bits is experimental, and only available for
testing. You are advised not to use it for production.
CRASHES ARE TO BE EXPECTED - PLEASE REPORT THEM TO NUMPY DEVELOPERS
"COMPLETADO"
PS C:\Users\XPCSF\Documents\RepoDi\proyecto\src\build>
OSS-Cad-S...
OSS-Cad-S...
OSS-Cad-S...
main*
Ln 19, Col 1
Tab Size: 4
UTF-8
CRLF
Makefile
<Auto-Detect Project>
FPGA Toolchain
Buscar
Eventos de hoy
ESP
15:13
3/8/2024


File Edit Selection View Go Run
Plantilla
EXPLORER
PLANTILLA
EL-3307_template
doc
Tang_Nano_9k_3672_Schematic.pdf
src
build
constr
module_counter.cst U
tangnano9k_constraints_templat...
design
.keep
module.sv U
sim
.keep
module_tb.sv U
.gitignore
README.md
module.sv U
module_tb.sv U
module_counter.cst U
Tang_Nano_9k_3672_Schematic.pdf
EL-3307_template > src > constr > module_counter.cst
Constraints Editor
Tang Nano 9K
Constraints
Add From Template
Add Constraint
PORT NAME
LOCATION
PORT OPTIONS
clk 52 Pull Up, LVCMOS33
count_o[0] 10 8ma Drive, LVCMOS18
count_o[1] 11 8ma Drive, LVCMOS18
count_o[2] 13 8ma Drive, LVCMOS18
count_o[3] 14 8ma Drive, LVCMOS18
count_o[4] 15 8ma Drive, LVCMOS18
count_o[5] 16 8ma Drive, LVCMOS18
rst 4 LVCMOS18
Edit Constraint
Port Name
rst
Select From Top Module
Location
4
Select IO Pin
Pull Mode:
None
Drive Power:
Unset
IO Standard:
LVCMOS18
OUTLINE
TIMELINE
main*
<Auto-Detect Project>
FPGA Toolchain
Buscar
23°C Lluvia suave
ESP
16:44
2/8/2024


File Edit Selection View Go Run
Plantilla
EXPLORER
PLANTILLA
EL-3307_template
doc
Tang_Nano_9k_3672_Schematic.pdf
src
build
constr
design
.keep
module.sv U
sim
.keep
module_tb.sv U
.gitignore
README.md
module.sv U
module_tb.sv U
EL-3307_template > src > sim > module_tb.sv
logic[5:0] count_o;
module_counter #(10) COUNTER (
.clk (clk),
.rst(rst),
.count_o(count_o)
);
initial begin
clk=0;
rst = 1;
#30;
rst = 0;
#30;
rst = 1;
#300000;
$finish;
end
always begin
clk = ~clk;
#10;
end
initial begin
$dumpfile("module_counter_tb.vcd");
$dumpvars(0,module_counter_tb);
end
endmodule
OUTLINE
TIMELINE
main*
Ln 36, Col 10
Spaces: 4
UTF-8
CRLF
System Verilog
<Auto-Detect Project>
FPGA Toolchain
Buscar
USD/COP +1,16%
ESP
16:35
2/8/2024


File Edit Selection View Go Run
Plantilla
EXPLORER
module.sv U
module_tb.sv U
PLANTILLA
EL-3307_template
doc
Tang_Nano_9k_3672_Schematic.pdf
src
build
constr
design
.keep
module.sv U
sim
.keep
module_tb.sv U
.gitignore
README.md
EL-3307_template > src > design > module.sv
module module #(
parameter COUNT = 13500000
)
(
input logic clk,
input logic rst,
output logic [5:0] count_o
);
localparam WIDTH_COUNT = $sclog2(COUNT);
logic [WIDTH_COUNT - 1:0] clk_counter = '0;
logic [5:0] led_count_r;
always_ff @(posedge clk) begin
if(!rst)begin
led_count_r<='0;
clk_counter <= '0;
end
else if (clk_counter == COUNT) begin
clk_counter <= '0;
led_count_r <= led_count_r + 1'b1;
end
else begin
clk_counter <= clk_counter+1'b1;
led_count_r <= led_count_r;
end
assign count_o = ~led_count_r;
endmodule
OUTLINE
TIMELINE
main*
Ln 29, Col 10
Spaces: 4
UTF-8
CRLF
System Verilog
<Auto-Detect Project>
FPGA Toolchain
Buscar
Ciclismo BMX racing
ESP
16:31
2/8/2024


Sin copia de seguridad
design
Vista
Herramientas de copia de seguridad
Este equipo › Documentos › RepoDi › proyecto › src › design
Buscar en design
Nombre
Fecha de modificación
Tipo
Tamaño
.keep
2/8/2024 20:14
Archivo KEEP
0 KB
module_counter.sv
3/8/2024 15:05
Archivo SV
1 KB
27°C Mayorm. nubla...
ESP
15:16
3/8/2024


Sin copia de seguridad
constr
mpartir
Vista
Herramientas de copia de seguridad
Este equipo › Documentos › RepoDi › proyecto › src › constr
Buscar en constr
Nombre
Fecha de modificación
Tipo
Tamaño
module_counter.cst
3/8/2024 15:01
Archivo CST
1 KB
tangnano9k_constraints_template
2/8/2024 20:14
Documento de te...
5 KB
27°C Mayorm. nubla...
ESP
15:16
3/8/2024