HT-HC01

WiFi HaLow Module

Document version

Version	Time	Description	Remark
Rev. 1.0	2024-10-16	P-Development version	Richard

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目录

1 Description

1.1 Overview

HT-HC01 is a Wi-Fi HaLow module with excellent RF performance, which operates in 902 - 928MHz, with maximum data rates of 32.5Mbps and up to 1-2km transmission range.

HT-HC01 uses LLC package, small size and rich pin, can be very convenient to integrate in a variety of PCB. It includes ultra-long range PA, high linear LNA, T/R switching, 32 MHz crystal oscillator, and is designed to simplify Wi-Fi HaLow connectivity to external hosts for applications.

HT-HC01 meets IEEE 802.11ah standard, which is specifically designed for battery-operated devices, allowing them to remain in longer sleep and idle states without frequent wake-ups. This significantly reduces power consumption and extends the device's battery life.As a result, HT-HC01 becomes an ideal choice for Internet of Things (IoT) devices and other battery-powered equipment.

1.2 Features

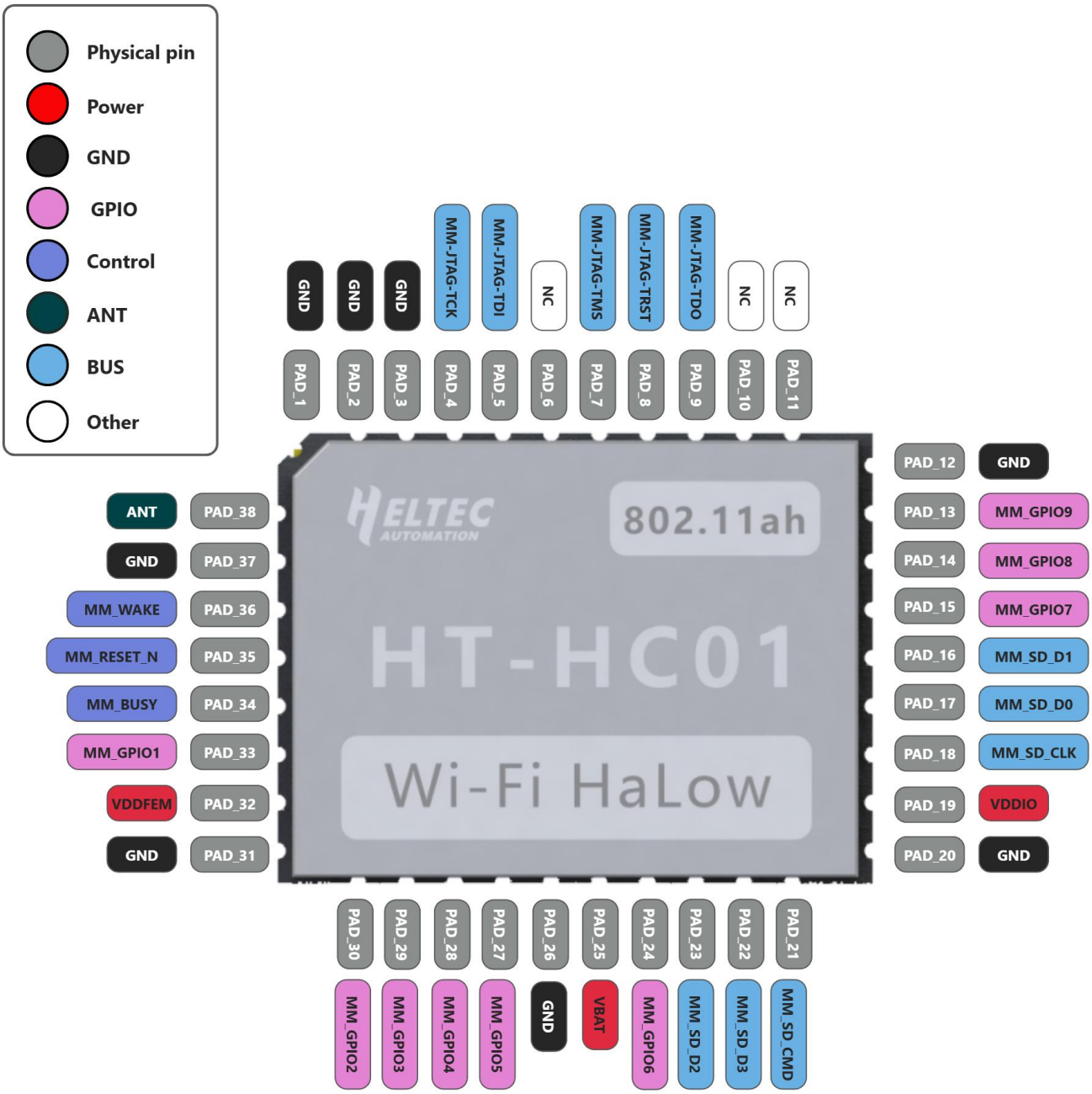
- Long-range transmission, up to 1km or and further within the visual distance.
- Channel bandwidth options of 1/2/4/8 MHz.
- High data rate, single-stream max rate of 32.5 Mbps @ 8 MHz or 15 Mbps @ 4 MHz.
- Support Sub-1 GHz frequency bands, frequency range: 902~928 MHz.
- Max output power:21dBm.
- 802. 11ah OFDM PHY supporting WFA HaLow certification.
- 802. 11ah MAC supporting WFA HaLow certification.
- Support for various interface options, include SDIO 2.0, 2* UART..
- Hibernate mode (internal / external wake).
- Integrated DC-DC converter supporting a voltage supply from 3.0V to 3.6V.
- 1.27mm stamp hole design, easy to integrate.
- Wide spectrum of security features.

1.3 Application

Wi-Fi HaLow can seamlessly integrate with traditional Wi-Fi or Ethernet networks and is suitable for most IoT scenarios, especially those requiring long-range high-speed transmission

- Remote camera monitoring
- Industrial automation control
- Asset management and tracking
- Smart home
- Smart city
- Smart farming
- Construction Site Management
- Wi-Fi/Ethernet/Wi-Fi_HaLow extension and bridging
- WiFi HaLow device development
- Proximity sensors
- Rural internet access
- Autonomous driving
- Mobile phone location
- Environmental monitoring
- Unmanned supermarket
- Commodity management
- Intelligent lighting controls
- Digital transformation of legacy equipment

2 Pin Description



PAD_1	Name	Type	Function	Alternate & Other Function(s)
PAD_1	GND	POWER	Ground	
PAD_2	GND	POWER	Ground	
PAD_3	GND	POWER	Ground	
PAD_4	MM_JTAG_TCK	I	JTAG Clock	

PAD_5	MM_JTAG_TDI	I	JTAG Data In	
PAD_6	NC	NC		
PAD_7	MM_JTAG_TMS	I	JTAG Mode Select	
PAD_8	MM_JTAG_TRST_N	I	JTAG Reset	
PAD_9	MM_JTAG_TDO	O	JTAG Data Out	
PAD_10	NC	I/O		
PAD_11	NC	I/O		
PAD_12	GND	POWER	Ground	
PAD_13	MM_GPIO_9	I/O	General Purpose IO9	
PAD_14	MM_GPIO_8	I/O	General Purpose IO8	
PAD_15	MM_GPIO_7	I/O	General Purpose IO7	UART1_TX[4]
PAD_16	MM_SDIO_D1	I/O	SDIO D1	SPI_INT
PAD_17	MM_SDIO_DO	I/O	SDIO D0	SPI_MISO
PAD_18	MM_SDIO_CLK	I/O	SDIO Clock	SPI_SCK
PAD_19	MM_VDD_IO	POWER	3.3V VBAT Supply	
PAD_20	GND	POWER	Ground	
PAD_21	MM_SDIO_CMD	I/O	SDIO Command	SPI_MOSI
PAD_22	MM_SDIO_D3	I/O	SDIO D3	SPI_CS
PAD_23	MM_SDIO_D2	I/O	SDIO D2	
PAD_24	MM_GPIO_6	I/O	General Purpose IO6	UART1_RX[4]
PAD_25	VBAT	POWER	3.3V VBAT Supply	
PAD_26	GND	POWER	Ground	
PAD_27	MM_GPIO_5	I/O	General Purpose IO5	I2C_SCL[4]

PAD_28	MM_GPIO_4	I/O	General Purpose IO4	I2C_SDA[4]
PAD_29	MM_GPIO_3	I/O	General Purpose IO3	UART0_TX, PWM1_3[4]
PAD_30	MM_GPIO_2	I/O	General Purpose IO2	UART0_RX, PWM1_2[4]
PAD_31	GND	POWER	Ground	
PAD_32	VDD_FEM	POWER	3.3V Frontend Supply	
PAD_33	MM_GPIO_1	I/O	General Purpose IO1	PWM1_1[4]
PAD_34	MM_GPIO_0	O	Wi-Fi BUSY	
PAD_35	RESET_N	I	System Reset	
PAD_36	WAKE	I	Wake	
PAD_37	GND	POWER	Ground	
PAD_38	ANT_1	ANALOG	Antenna	

NOTE:

- JTAG pins should be tied to GND via a 10k pull down resistor
- All unused GPIO should be tied to GND via a 10k pull down resistor
- All SDIO bus pins should be pull up with a 10k-100k resistor as per the the SDIO standard
- Pending software support
- Supplied from VBAT domain. Other digital pins are driven by VDDIO domain.

3 Specifications

3.1 General Specifications

Table 3.1 General specifications

Parameters	Description
Main Chip	MM6108IQ
Power Supply	3.0~3.6V
HaLow Standard	IEEE 802.11ah
Band Width	1/2/4/8MHz
Interface	38 Header Pins
Power consumption	See table 3.4
Operating temperature	-40 ~ 85℃
Operating humidity	10% ~ 90%, no-condensing
Dimensions	18.5*14*26mm
Data Rate	32.5 Mbps @ 8 MHz

3.2 Electrical characteristics

3.2.1 Absolute max ratings

Stress beyond absolute maximum ratings may cause permanent damage to the module. Functional operation is guaranteed for recommended operation conditions only. Operation of the device outside the recommended conditions may result in a reduced lifetime and/or reliability problems (even if the absolute maximum ratings are not exceeded).

Table3.2.1 Absolute max ratings

Parameter	Min	Max	Unit
VBAT voltage	-0.3	4.3	V
VDD_FEM voltage	-0.3	4.3	V
Voltage on digital I/O pin	-0.3	4.3	V
Voltage on analog/RF pin	-0.3	1.2	V
Storage temperature	-40	125	°C
RF input power (CW)	-	6	dBm

3.2.2 Immunity

Table3.2.2 Immunity

Parameter			Min	Max	Unit
Electrostatic discharge(ESD) performance	Human body model (H3M).perANSI/ESDA/JEDEC JS001 Charged device model (CDM).perJESD22-C101	RF Input	-1000	1000	V
		All pins except RF Input	-2000	2000	V
		All pins	-500	500	V

3.2.3 Recommended operating conditions

Table3.2.3 Recommended operating conditions

Parameter	Min	Type	Max	Unit
Ambient temperature	-40	25	85	°C
VBAT	3.0	3.3	3.6	V
VDD_FEM	3.0	3.3	3.6	V
VDDIO	1.62	3.3	3.6	V
Digital I/O voltage	0	3.3	VDDIO	V
RESET / WAKE I/O Voltage	0	3.3	VBAT	V

3.2.4 Power consumption

3.2.4.1 Transmit power consumption

Table3.2.4.1 Transmit power consumption

Mode	Condition: $V_{BAT}/V_{VDDIO}/V_{DD\_FEM}$=3.3V, 102.4ms Beacon Interval	VBAT Current			VDD_FEM			Unit
		Min	TYP	Max	Min	TYP	Max	
Transmit current (MCS0, 21dBm, 100% D.C.)	1 MHz channel	54	57	73	151	152	162	mA
	2 MHz channel	54.5	60	73	150.5	152	159.5	mA
	4 MHz channel	60.5	66	79.5	146.5	151	156	mA
	8 MHz channel	71	78	91.5	142.5	147	153	mA
Transmit current (MCS7,17dBm, 100% D.C.)	1 MHz channel	48	51	62.5	98.5	104	112	mA
	2 MHz channel	51.5	55	66.5	97.5	104	112	mA
	4 MHz channel	57	62	73	93.5	102	108.5	mA
	8 MHz channel	68	72	84	91	99	105.5	mA

3.2.4.2 Receive power consumption

Table3.2.4.2 Receive power consumption

Mode	Condition	VBAT Current			VDD_FEM			Unit
	VBAT/VDDIO/VDD_FEM=3.3V	Min	TYP	Max	Min	TYP	Max	
Listen	1 MHz channel	25	26	35.5				mA
	2 MHz channel	26	28	35				mA
	4 MHz channel	30	32	40				mA
	8 MHz channel	35	37	45.5				mA
Active receive MCS7	1 MHz channel	26.5	26	35.5				mA
	2 MHz channel	30	30	39.5				mA
	4 MHz channel	37.5	40	49				mA
	8 MHz channel	54	53	67				mA
Active receive MCS0	1 MHz channel	28	26	37				mA
	2 MHz channel	29.5	28	38.5				mA
	4 MHz channel	36	36	47	4	4.5	4.7	mA
	8 MHz channel	50	48	62.5				mA

3.2.4.3 Sleep Power

Table3.2.4.3 Sleep power

Mode	Condition VBAT/VDDIO/VDD_FEM =3.3V	VBAT			VFEM			Unit
		Min	TYP	Max	Min	TYP	Max	
Snooze	RC Oscillator on, Memory retained, configurable wake up timer	9.5	27	370	0.001	0.05	0.55	μA
Deep sleep	RC Oscillator on, configurable wake up timer	0.8	1	1.8	0.001	0.05	0.55	μA
Hibernate	Power off, wait for external interrupt	0.03	0.05	1	0.001	0.05	0.55	μA

3.2.4.3 DTIM3 power consumption

Table3.2.4.3 DTIM3 power consumption

Mode	Condition: $V_{BAT}/V_{VDDIO}/V_{DD\_FEM}$=3.3V, 102.4ms Beacon Interval	VBAT			VFEM			Unit
		Min	TYP	Max	Min	TYP	Max	
S1G beacons	1 MHz channel	380	395	420	45	47	55	μA
	2 MHz channel	380	395	420	45	47	55	μA
	4 MHz channel	260	280	320	24	25	30	μA
	8 MHz channel	260	280	320	24	25	30	μA
S1G beacons with proprietary	1 MHz channel	170	190	250	12	13	43	μA
	2 MHz channel	170	190	250	12	13	43	μA

DTIM signaling1	4 MHz channel	155	190	200	8	9	20	µA
	8 MHz channel	155	190	200	8	9	20	µA

3.2.4.4 DTIM10 power consumption

Table3.2.4.4 DTIM10 power consumption

Mode	Condition: $V_{BAT}/V_{VDDIO}/V_{DD\_FEM}$=3.3V, 102.4ms Beacon Interval	VBAT			VFEM			Unit
		Min	TYP	Max	Min	TYP	Max	
S1G beacons	1 MHz channel	140	155	240	14	15	16	µA
	2 MHz channel	140	155	240	14	15	16	µA
	4 MHz channel	100	115	130	8	8	9	µA
	8 MHz channel	100	115	130	8	8	9	µA
S1G beacons with proprietary DTIM signaling2	1 MHz channel	85	95	195	4	5	6	µA
	2 MHz channel	85	95	195	4	5	6	µA
	4 MHz channel	75	90	110	3	5	6	µA
	8 MHz channel	75	90	110	3	5	6	µA

3.3 RF characteristics

3.3.1 Receiver sensitivities

Table3.3.1 Receiver sensitivities

MCS index	Modulation scheme	Coding rate	Phy rate (kbps) per BW				Minimum Receive sensitivity (dBm) per BW			
			1MHz	2MHz	4MHz	8MHz	1MHz	2MHz	4MHz	8MHz
0	BPSK	1/2	333	722	1500	3250	-105	-103	-101	-97
1	QPSK	1/2	667	1444	3000	6500	-102	-100	-97	-93
2	QPSK	3/4	1000	2167	4500	9750	-99	-97	-95	-91
3	16-QAM	1/2	1333	2889	6000	13000	-96	-94	-91	-88
4	16-QAM	3/4	2000	4333	9000	19500	-93	-90	-88	-85
5	64-QAM	2/3	2667	5778	12000	26000	-89	-87	-84	-80
6	64-QAM	3/4	3000	6500	13500	29250	-88	-85	-83	-79
7	64-QAM	5/6	3333	7222	15000	32500	-87	-84	-81	-77
10	BPSK	1/2 x 2	167	N/A			-107	N/A		

3.3.2 Transmission power

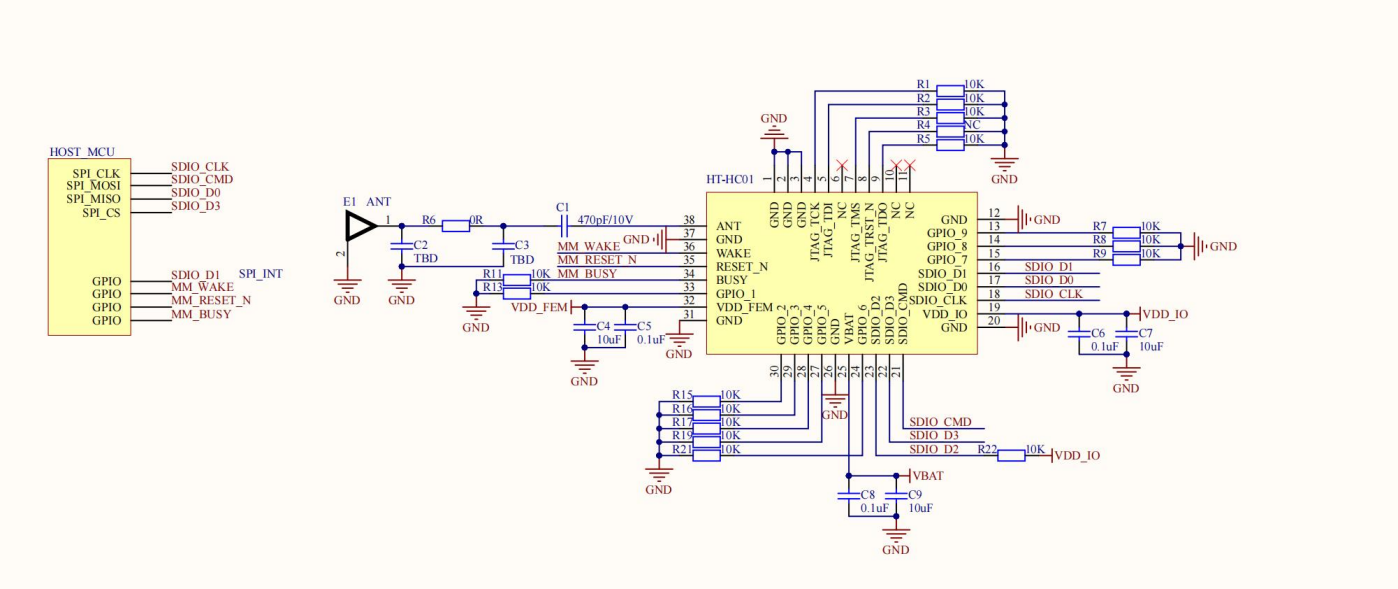
Table3.3.2 Transmission power

Tx output power (1, 2 MHz BW)	Min (dBm)	Typical (dBm)	Max (dBm)
MCS 0	20	21	22
MCS 7	16	17	18.5
Tx output power (4 MHz BW)	**Min (dBm)**	**Typical (dBm)**	**Max (dBm)**
MCS 0	20.5	21	22
MCS 7	16	17	18
Tx output power (4 MHz BW)	**Min (dBm)**	**Typical (dBm)**	**Max (dBm)**
MCS 0	20.5	21	22
MCS 7	16	17	18

4 Reference Design

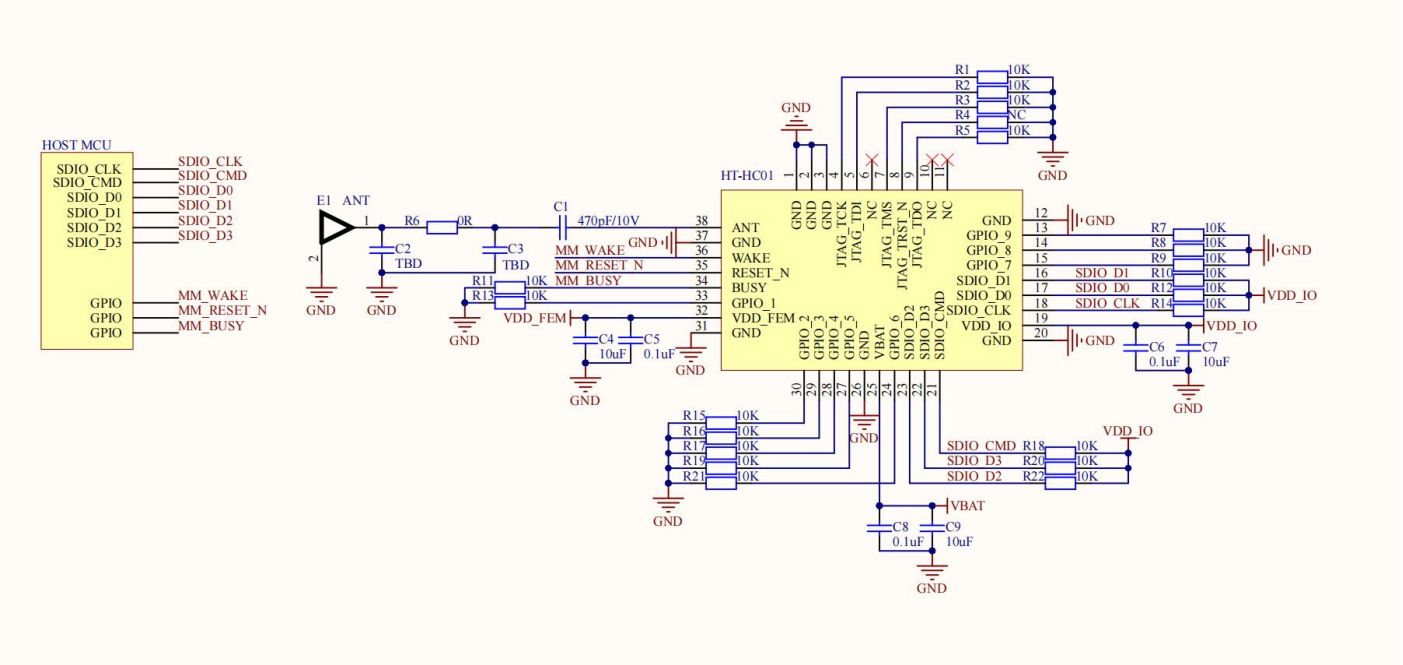
4.1 SPI

https://resource.heltec.cn/download/HT-HC01/Reference_design/SPI.PDF



4.2 SDIO

https://resource.heltec.cn/download/HT-HC01/Reference_design/SDIO.PDF



4.3 Requirements and considerations

4.3.1 SDIO host requirements

- The host should support SDIO v2.0 with SDIO clock speeds of up to 50 MHz. Slower clock speeds will impact the maximum achievable throughput.
- At a minimum, 2 x GPIOs are required as a CMOS output to drive the RESET and WAKE signals. If power save is used, a third GPIO is needed, set as a CMOS input to receive the BUSY signal from the module.
- The SDIO data and command lines should be pulled up with 10k-100k resistors as per the SDIO 2.0 specification.

4.3.2 SPI host requirements

When selecting a CPU host to interface via SPI to the MM6108-MF08551 module, consider the following recommendations to achieve the best throughput::

- The host should support level-triggered interrupts.
- The host should support full-duplex SPI mode.
- The host should support DMA backed transactions on the SPI bus.

Standard SPI can achieve up to 25 Mbps at 50 MHz but this will reduce significantly if there is no DMA support. For example, an SPI interface with an 8-byte buffer per transaction might only achieve 2Mbps throughput on the SPI

bus.

4.3.3 Power management

MM6108-MF08551 module power is derived from a 3.0 to 3.6V supply provided on pins VBAT and VDD_FEM. VBAT powers the internal circuitry of the MM6108 and VDD_FEM powers the on-board ultra-long-range power amplifler.

VDDIO sets the IO voltage of the MM6108 and should be connected to the same power supply as the host MCU.

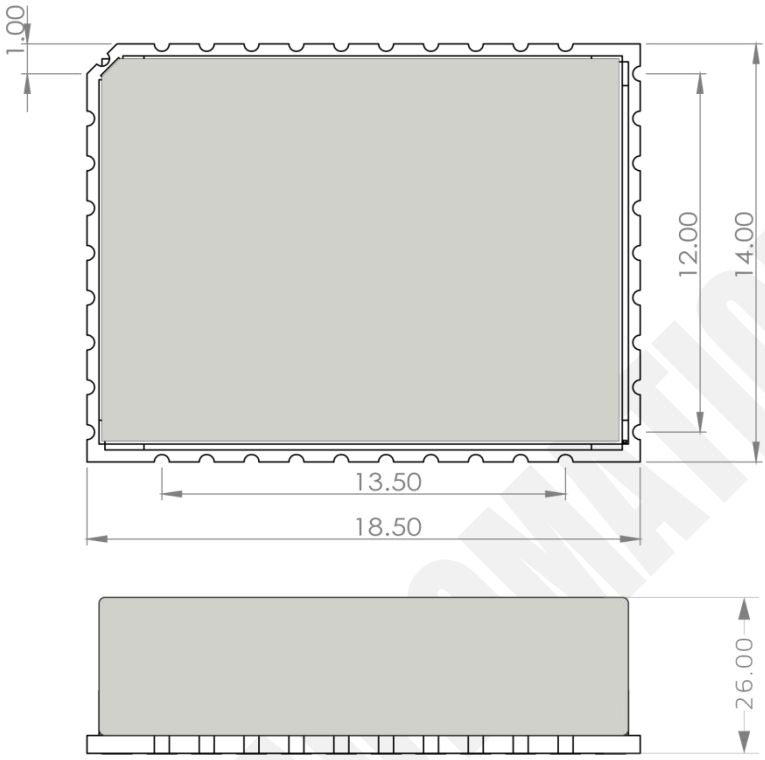
There are no strict power-up sequencing requirements, however the voltage on VDDIO must not exceed VBAT.

4.3.4 Digital interfaces

All unused digital IO pins must be pulled up or down to ensure they do not float. Failure to do so will result in a higher leakage current on the VDDIO supply.

5 Hardware Dimensions

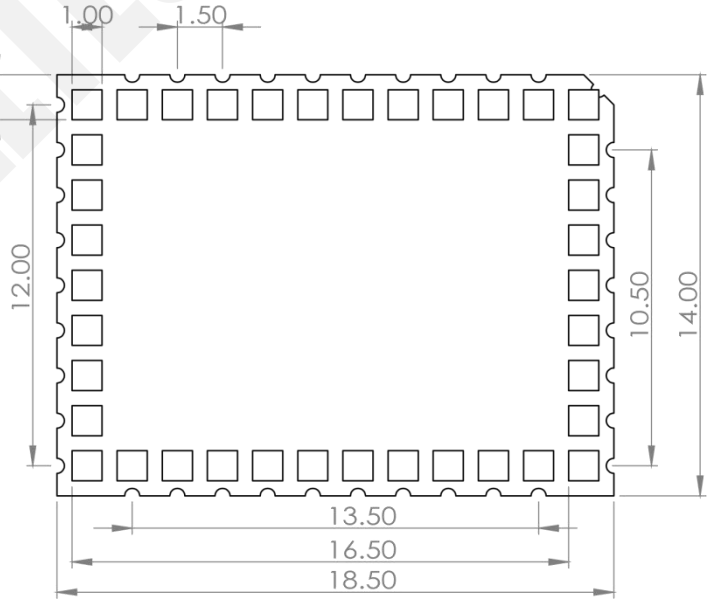
5.1 Dimensions



5.2 PCB footprint

For a detailed PCB Footprint, please refer to the following link:

https://resource.heltec.cn/download/Heltec_Module_Footprint/HT-HC01



6 Resource

6.1Relevant resources

- Documents Page: Heltec Products Operation Documention
- Schematic Diagram: https://resource.heltec.cn/download/HT-HC01/Schematic_diagram
- Reference Design: https://resource.heltec.cn/download/HT-HC01/Reference_design

6.2 Heltec Contact Information

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