DFT ASSIGNMENT-3

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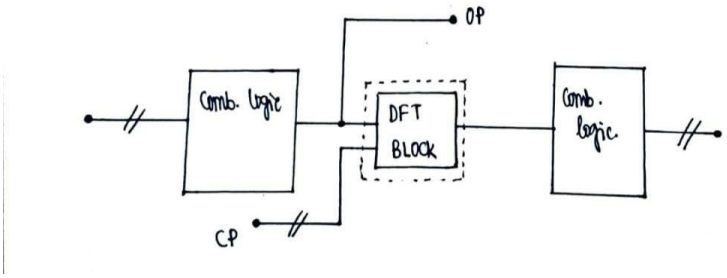
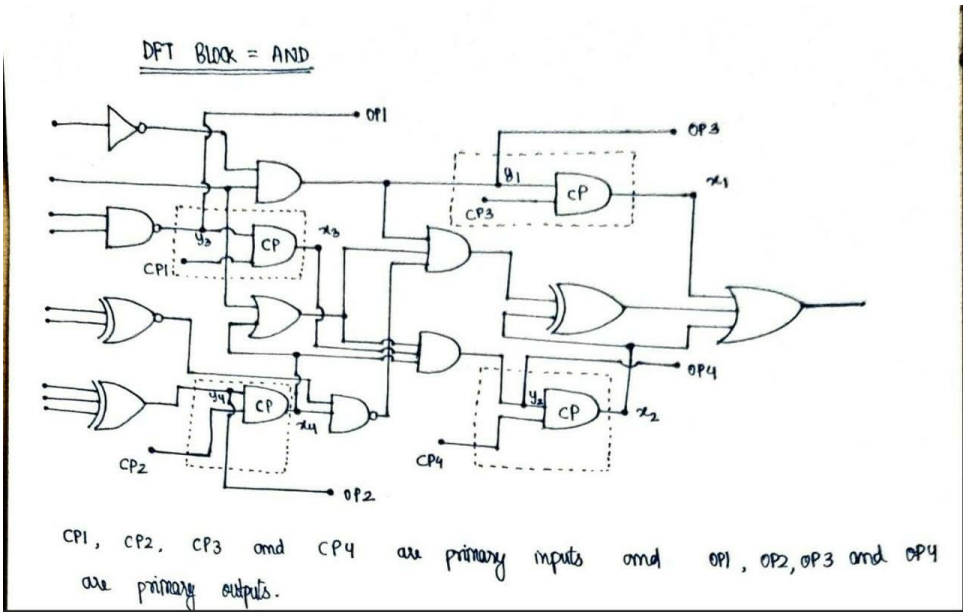
GENERAL DFT BLOCK:



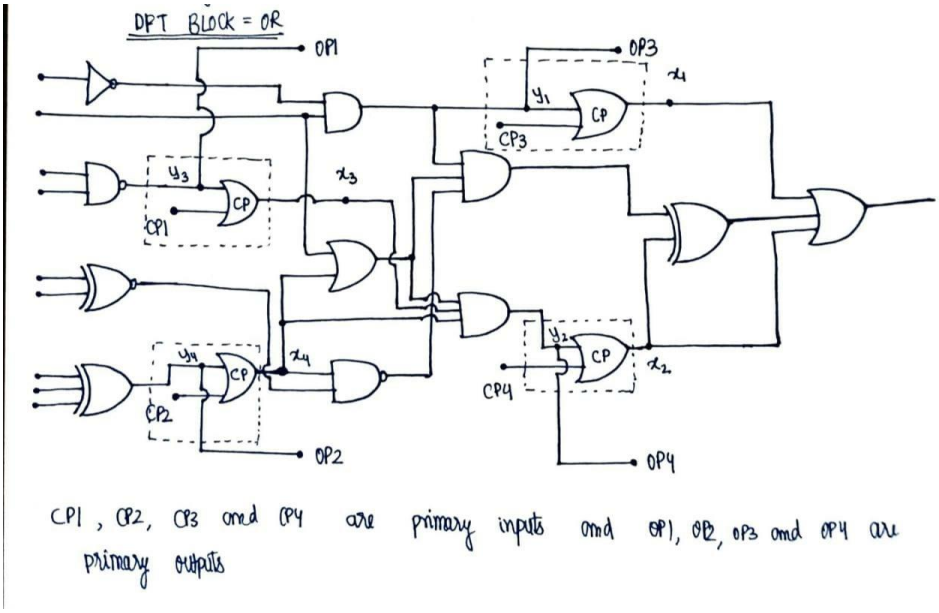
In the above shown figure, if Combinational Logic 1 (left) isn't observable and Combinational Logic 2 (Right) isn't controllable, the DFT Block is inserted them, which adds direct controllability from primary inputs and direct observability using primary outputs. This is not only done to induce controllability/observability, it can also be used to reduce their values (improve them), which is shown in the circuits below, with 4 different DFT Blocks – AND, OR, AND+OR, MUX (2x1).

DFT AND BLOCK:



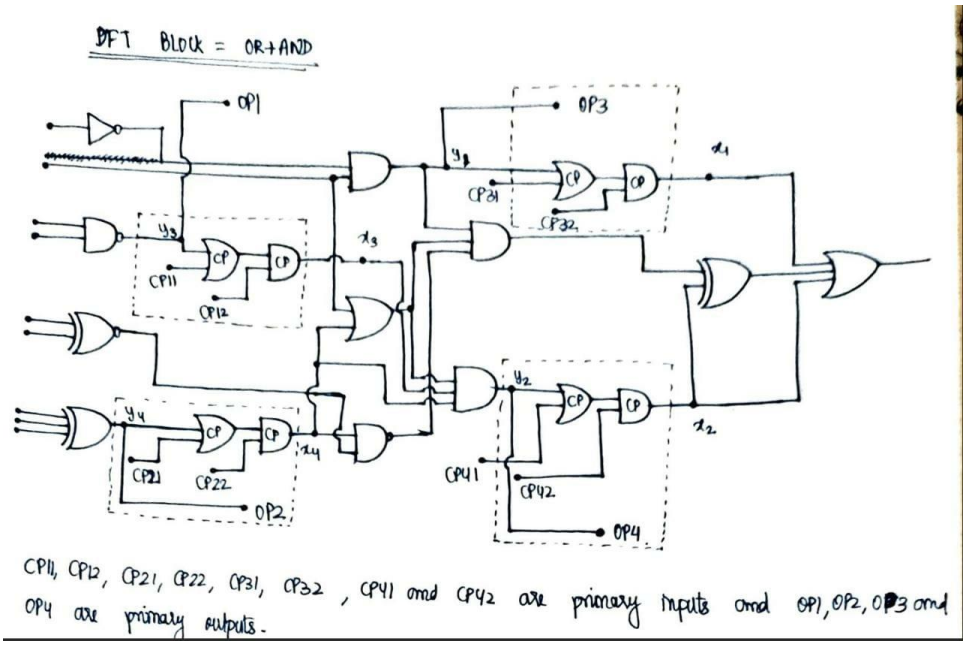
Here, using CP inputs (CP_1 CP_2 CP_3 CP_4), the CC0 values of points (x_1 x_2 x_3 x_4) can be made 2 (as CC values of primary inputs are 1), instead of some big values (>2). The OP outputs (OP_1 OP_2 OP_3 OP_4), the CO values of points (y_1 y_2 y_3 y_4) can be made 0 (as CO of primary outputs is 0), instead of some big values (>0).

DFT OR BLOCK:



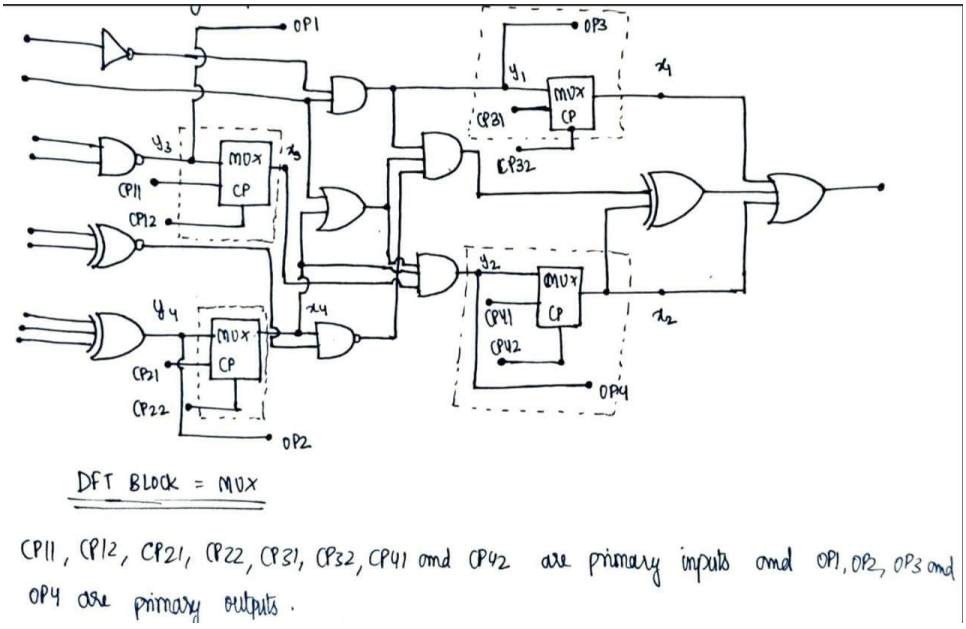
Here, using CP inputs (CP_1 CP_2 CP_3 CP_4), the CC1 values of points (x_1 x_2 x_3 x_4) can be made 2 (as CC values of primary inputs are 1), instead of some big values (>2). The OP outputs (OP_1 OP_2 OP_3 OP_4), the CO values of points (y_1 y_2 y_3 y_4) can be made 0 (as CO of primary outputs is 0), instead of some big values (>0).

DFT OR+AND BLOCK:



Here, using CP inputs (CP_{11} CP_{12} CP_{21} CP_{22} CP_{31} CP_{32} CP_{41} CP_{42}), the CC values of points (x_1 x_2 x_3 x_4) can be made 3 (as CC values of primary inputs are 1), instead of some big values (>2). The OP outputs (OP_1 OP_2 OP_3 OP_4), the CO values of points (y_1 y_2 y_3 y_4) can be made 0 (as CO of primary outputs is 0), instead of some big values (>0).

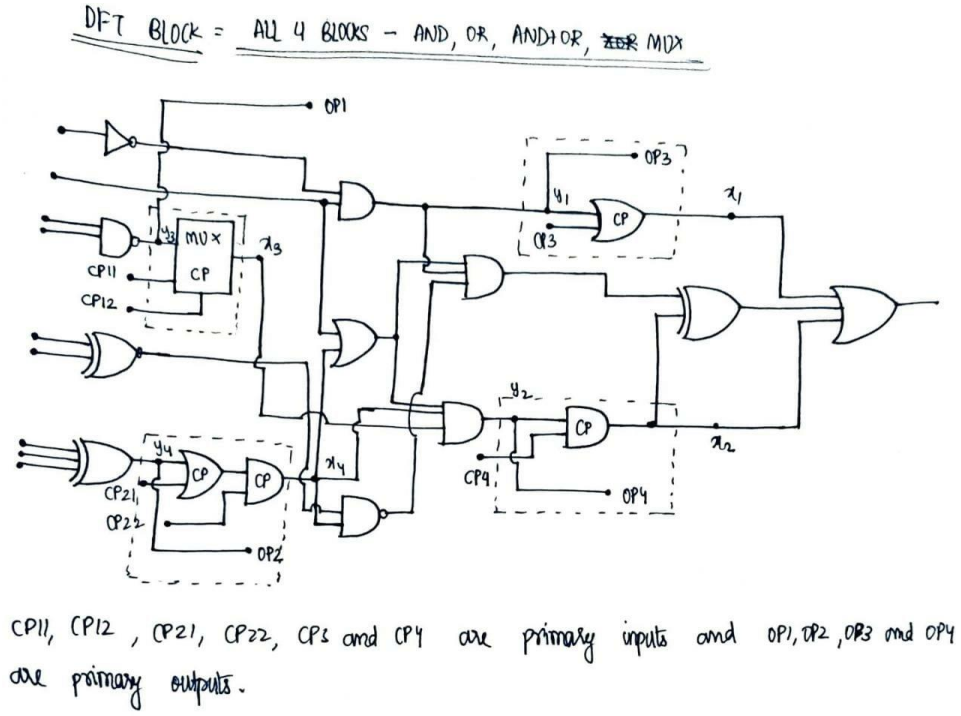
DFT MUX BLOCK:



Here, using CP inputs (CP_{11} CP_{12} CP_{21} CP_{22} CP_{31} CP_{32} CP_{41} CP_{42}), the CC values of points (x_1 x_2 x_3 x_4) can be made 3 (as CC values of primary inputs are 1), instead of some big values (>2). The OP outputs (OP_1 OP_2

OP_3 OP_4), the CO values of points (y_1 y_2 y_3 y_4) can be made 0 (as CO of primary outputs is 0), instead of some big values (>0).

DFT ALL 4 BLOCKS:



CP11, CP12, CP21, CP22, CP3 and CP4 are primary inputs and OP1, OP2, OP3 and OP4 are primary outputs.

The combination of all 4 also does the similar task of improving controllability and observability of the nodes as shown in the above cases.

The only disadvantage of control point insertion is that the complexity of the circuit worsens, taking higher chip area. The primary outputs might be tough to pull out, making big changes in the actual circuit design.

VERILOG CODES FOR ABOVE CIRCUITS ALONG WITH TESTBENCHES AND VCD DUMPFILES:

The Verilog codes, testbenches and vcd dumpfiles for the above circuits have been uploaded on the GitHub repository with the link given below. They have also been zipped in the submitted folder.

https://github.com/Sasanka-GRS/DFT-3