

Main Block

Declaration

- Identifier: `c`
- Size: 1

Declaration

- Identifier: `a`
- Size: 3

Composite Gate

- Identifier: `c_reg_h`
- Map:  
 $\text{control} \mapsto \text{c}$   
 $\text{reg} \mapsto \text{a}$

If Statement

- Guard: `control`

Loop Statement

- Range:  
 $0 \leq i \leq \text{sizeof}(\text{reg}) - 1$

Gate Statement

- Gate: `h`
- Arguments: [  
    `reg[i]`  
]